TEXAS INSTRUMENTS
ADC12D1620QML-SP
JAJSDJ8A – APRIL 2017 – REVISED OCTOBER 2021

ADC12D1620QML-SP 12 ビット、シングルまたはデュアル、3200 または 1600MSPS RF サンプリング A/D コンバータ (ADC)

1 特長

- 総照射線量 (TID) 耐性 = 300krad (Si)
- シングル・イベント機能割り込み (SEFI) テスト済み
- シングル・イベント・ラッチアップ耐性:120MeV-cm^2/mg 超
- コールド・スペア対応
- 広い温度範囲:-55℃～+125℃
- 消費電力 = 3.8W または 2.7W (1600 または 800MHz クロック)
- 3dB 入力帯域幅 = 3GHz
- 低サンプリング・パワー・セービング・モード (LSPSM) により、f_{CLK} ≤ 800 MHz について消費電力を低減し性能を向上
- マルチチップ・システム用の自動同期機能
- タイム・スタンプ機能により外部トリガをキャプチャ
- システム・デバッグ用にテスト・パターンを出力
- 1:1 非デマルチプレクス、または 1:2 もしくは 1:4 の並列デマルチプレクスの LVDS 出力
- 1.9V 単一電源

2 アプリケーション

- 直接 RF ダウン変換
- 広帯域衛星通信
- 合成開口レーダーおよび LIDAR

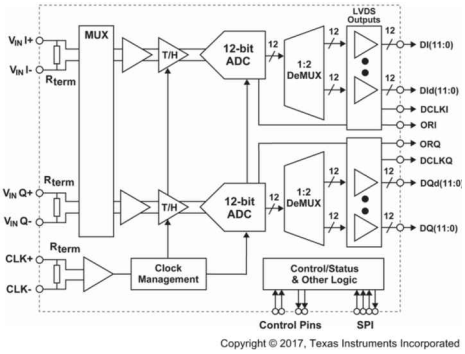
3 概要

ADC12D1620QML は、パッケージの再設計により、ADC12D1600QML と比較して ENOB、SNR、クロストークが改良されています。前世代の製品と同様に、ADC12D1620QML は低消費電力、高性能の CMOS A/D コンバータ (ADC) であり、インターリーブ・モードにおいて最高 3.2GSPS のサンプリング・レートと 12 ビットの分解能で信号をデジタル化します。また、デュアル・チャネル ADC として、最高 1.6GSPS のサンプリング・レートでも使用できます。サンプリング・レートが 800MHz 未満の場合、低サンプリング・パワー・セービング・モード (LSPSM) により、消費電力が 1 チャネルあたり 1.4W 未満 (標準値) に低減されます。この ADC は、最低で 200MSPS の変換レートをサポートできます。

製品情報

部品番号(1)	グレード	パッケージ
5962F1220502VXF	SMD フライト 300 krad(Si)	CCGA (376)
ADC12D1620CCMLS	フライト 300 krad(Si)	CCGA (376)
ADC12D1620CCMPR	プリフライトのエンジニアリング・プロトタイプ	CCGA (376)
ADC10D1000DAISY	デイジー・チェーン、メカニカル・サンプル、ダイなし	CCGA (376)
ADC12D1620LGMLS	フライト 300 krad(Si)	CLGA (256)
ADC12D1620LGMPR	プリフライトのエンジニアリング・プロトタイプ	CLGA (256)
ADC10D1000LDAZ	デイジー・チェーン、メカニカル・サンプル、ダイなし	CLGA (256)

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ注文情報の付録 (POA) を参照してください。



機能ブロック図

Table of Contents

4 Revision History

Changes from Revision * (April 2017) to Revision A (October 2021)	Page
• *旧式の用語を使用している場合、文書全体にわたってプライマリおよびセカンダリに変更*	1
• 「*製品情報*」表に 5962F1220502VXF を追加	1
• Changed VinI+, VinI–, VinQ+, VinQ– voltage MIN value From: −0.15 V To: −0.5 in the *Absolute Maximum Ratings* table	12

5 Pin Configuration and Functions

The center ground pins are for thermal dissipation and must be soldered to a ground plane to ensure rated performance. See *Layout Guidlines* for more information.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	V_A	SDO	TPM	NDM	V_A	GND	V_E	GND_E	DId0+	V_DR	DId3+	GND_DR	DId6+	V_DR	DId9+	GND_DR	DId11+	DId11-	GND_DR	A
B	Vbg	GND	ECEb	SDI	CalRun	V_A	GND	GND_E	V_E	DId0-	DId2+	DId3-	DId5+	DId6-	DId8+	DId9-	DId10+	DI0+	DI1+	DI1-	B
C	Rtrim+	Vcmo	Rext+	SCSb	SCLK	GND	V_A	V_E	GND_E	DId1+	DId2-	DId4+	DId5-	DId7+	DId8-	DId10-	DI0-	V_DR	DI2+	DI2-	C
D	V_A	Rtrim-	Rext-	GND	GND	CAL	Vbiasl	V_A	V_A	DId1-	V_DR	DId4-	GND_DR	DId7-	V_DR	GND_DR	V_DR	DI3+	DI4+	DI4-	D
E	V_A	Tdiode+	RSV1	GND													GND_DR	DI3-	DI5+	DI5-	E
F	V_A	GND_TC	Tdiode-	RSV2	AA		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND_DR	DI6+	DI6-	GND_DR	F
G	V_TC	GND_TC	V_TC	V_TC	AB	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DI7+	DI7-	DI8+	DI8-	G
H	Vinl+	V_TC	GND_TC	V_A	AC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DI9+	DI9-	DI10+	DI10-	H
J	Vinl-	GND_TC	V_TC	Vbiasl	AD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_DR	DI11+	DI11-	V_DR	J
K	GND	Vbiasl	V_TC	GND_TC	AE	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	ORI+	ORI-	DCLKI+	DCLKI-	K
L	GND	VbiasQ	V_TC	GND_TC	AF	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	ORQ+	ORQ-	DCLKQ+	DCLKQ-	L
M	VinQ-	GND_TC	V_TC	VbiasQ	AG	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND_DR	DQ11+	DQ11-	GND_DR	M
N	VinQ+	V_TC	GND_TC	V_A	AH	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DQ9+	DQ9-	DQ10+	DQ10-	N
P	V_TC	GND_TC	V_TC	V_TC	AJ	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DQ7+	DQ7-	DQ8+	DQ8-	P
R	V_A	GND_TC	V_TC	V_TC	AK	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_DR	DQ6+	DQ6-	V_DR	R
T	V_A	GND_TC	GND_TC	GND	AL	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_DR	DQ3-	DQ5+	DQ5-	T
U	GND_TC	CLK+	PDI	GND	GND	RCOut1-	VbiasQ	V_A	V_A	DQd1-	V_DR	DQd4-	GND_DR	DQd7-	V_DR	V_DR	GND_DR	DQ3+	DQ4+	DQ4-	U
V	CLK-	DCLK_RST+	PDQ	LSPSM	DES	RCOut2+	RCOut2-	V_E	GND_E	DQd1+	DQd2-	DQd4+	DQd5-	DQd7+	DQd8-	DQd10-	DQ0-	GND_DR	DQ2+	DQ2-	V
W	DCLK_RST-	GND	RSV	DDRPh	RCLK-	V_A	GND	GND_E	V_E	DQd0-	DQd2+	DQd3-	DQd5+	DQd6-	DQd8+	DQd9-	DQd10+	DQ0+	DQ1+	DQ1-	W
Y	GND	V_A	FSR	RCLK+	RCOut1+	V_A	GND	V_E	GND_E	DQd0+	V_DR	DQd3+	GND_DR	DQd6+	V_DR	DQd9+	GND_DR	DQd11+	DQd11-	GND_DR	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

The center ground pins are for thermal dissipation and must be soldered to a ground plane to ensure rated performance. See *Layout Guidlines* for more information.

図 5-1. NAA Package, 376-Pin CCGA and CLGA, Top View

表 5-1. Pin Functions: Analog Front-End and Clock Pins

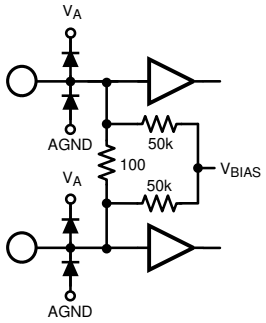
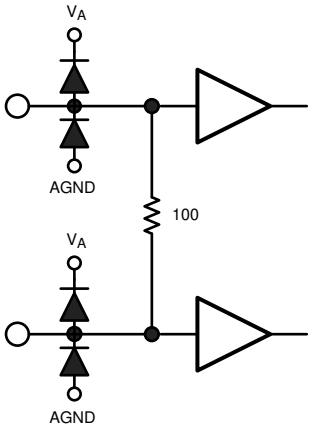
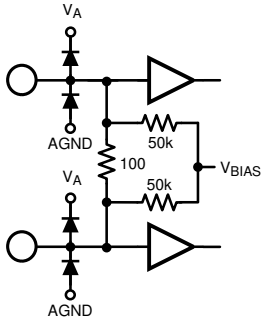
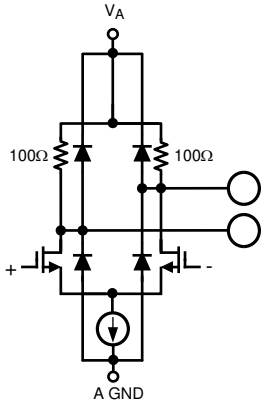
PIN		TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	NO.			
ANALOG FRONT-END AND CLOCK PINS				
CLK+ CLK–	U2/V1	I	Differential converter sampling clock. In the non-DES mode, the analog inputs are sampled on the positive transitions of this clock signal. In the DES mode, the selected input is sampled on both transitions of this clock. This clock must be AC-coupled.	
DCLK_RST+ DCLK_RST–	V2/W1	I	Differential DCLK reset. A positive pulse on this input is used to reset the DCLKI and DCLKQ outputs of two or more ADC12D1620 devices in order to synchronize them with other ADC12D1620 devices in the system. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized. The pulse applied here must meet timing relationships with respect to the CLK input. Although supported, this feature has been superseded by AutoSync.	
RCLK+ RCLK–	Y4/W5	I	Reference clock input. When the AutoSync feature is active, and the ADC12D1620 is in secondary mode, the internal divided clocks are synchronized with respect to this input clock. The delay on this clock may be adjusted when synchronizing multiple ADCs. This feature is available in ECM with the DRC bits of the AutoSync Control Register (Addr: E**h**, Bits: 15:7).	
RCOut1+, RCOut1– RCOut2+, RCOut2–	Y5/U6 V6/V7	O	Reference clock output 1 and 2. These signals, when enabled, provide a reference clock. The RCOut rates for all of the available modes can be found in 表 7-8; the rates displayed in the table are independent of whether the ADC is in primary or secondary mode. RCOut1 and RCOut2 are used to drive the RCLK of ADC12D1620 to enable automatic synchronization for multiple ADCs (AutoSync feature). The impedance of each trace from RCOut1 and RCOut2 to the RCLK of ADC12D1620 should be 100-Ω differential. Having two clock outputs allows the auto-synchronization to propagate as a binary tree. Use the DOC bit of the AutoSync Control Register (Addr: E**h**; Bit: 1) to enable or disable this feature; default is disabled.	

表 5-1. Pin Functions: Analog Front-End and Clock Pins (continued)

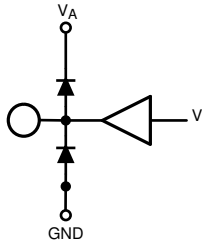
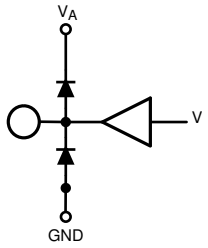
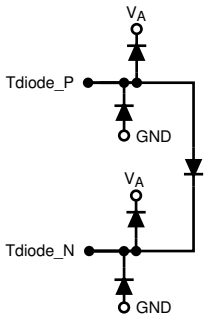
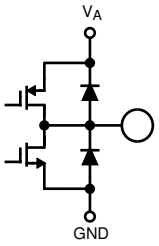
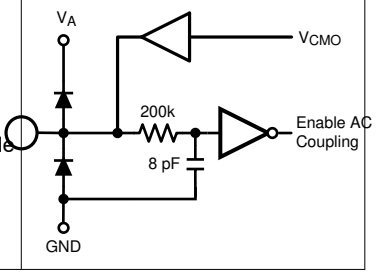
PIN		TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	NO.			
Rext+ Rext–	C3/D3	I/O	External reference resistor terminals. Connect a 3.3-kΩ, ±0.1% resistor between Rext+, Rext–. The Rext resistor is used as a reference to trim internal circuits that affect the linearity of the converter; the value and precision of this resistor must not be compromised.	
Rtrim+ Rtrim–	C1/D2	I/O	Input termination trim resistor terminals. Connect a 3.3-kΩ, ±0.1%resistor between Rtrim+/ Rtrim–. The Rtrim resistor is used to establish the calibrated 100-Ω input impedance of VinI, VinQ, and CLK. These impedances may be fine-tuned by varying the value of the resistor by a corresponding percentage; however, the tuning range and performance is not tested for such an alternative values.	
Tdiode+ Tdiode–	E2/F3	O	Temperature sensor diode positive (anode) and negative (cathode) terminals. This set of pins is used for die temperature measurements. It has not been fully characterized.	
V_{BG}	B1	I/O	Bandgap voltage output or LVDS common-mode voltage select. This pin provides a buffered version of the bandgap output voltage; it is capable of sourcing/sinking 100 µA and driving a load of up to 80 pF. Alternately, this pin may be used to select the LVDS digital output common-mode voltage. If tied to logic-high, the 1.2-V LVDS common-mode voltage is selected; 0.8 V is the default.	
V_{CMO}	C2	I/O	Common-mode voltage. This pin is the common-mode output in DC-coupling mode and also serves as the AC-coupling mode select pin. When DC-coupling is used at the analog inputs, the voltage output at this pin is required to be the common-mode input voltage at VIN+ and VIN−. When AC-coupling is used, this pin must be grounded. This pin is capable of sourcing or sinking 100 µA.	

表 5-1. Pin Functions: Analog Front-End and Clock Pins (continued)

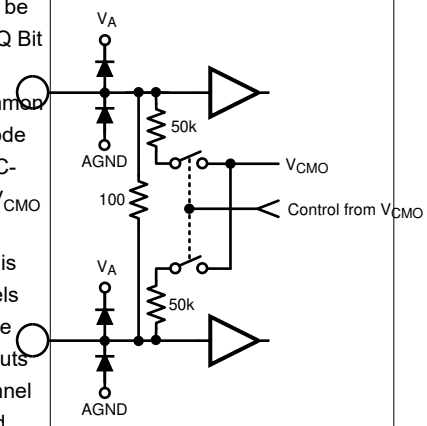
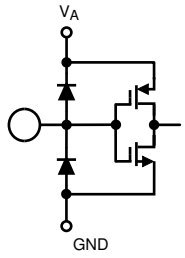
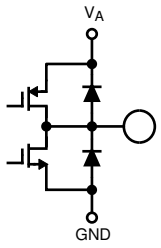
PIN		TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	NO.			
VinI+, VinI– VinQ+, VinQ–	H1/J1 N1/M1	I	Differential signal I and Q inputs. In the non-dual edge sampling (non-DES) mode, each I and Q input is sampled and converted by its respective channel with each positive transition of the CLK input. In non-ECM (non-extended control mode) and DES mode, both channels sample the I input. In Extended Control mode (ECM), the Q input may optionally be selected for conversion in DES mode by the DEQ Bit of the Configuration Register (Addr: 0**h**; Bit: 6). Each I- and Q-channel input has an internal common mode bias that is disabled when DC-coupled mode is selected. Both inputs must be either AC- or DC-coupled. The coupling mode is selected by the V_{CMO} pin. In non-ECM, the full-scale range of these inputs is determined by the FSR pin; both I and Q channels have the same full-scale input range. In ECM, the full-scale input range of the I- and Q-channel inputs may be independently set with the I- and Q-channel Full-Scale Range Adjust Registers (Addr: 3**h** and Addr: B**h**, respectively). The high and low full-scale input range setting in non-ECM corresponds to the mid and minimum full-scale input range in ECM. The input offset may also be adjusted in ECM with the I- and Q-channel Offset Adjust Registers (Addr: 2**h** and Addr: A**h**, respectively).	
CONTROL AND STATUS PINS				
CAL	D6	I	Calibration cycle initiate. The user can command the device to execute a self-calibration cycle by holding this input high for a minimum of t_{CAL_H} after having held it low for a minimum of t_{CAL_L}. This pin is active in both ECM and non-ECM. In ECM, this pin is logically OR'd with the CAL Bit of the Configuration Register (Addr: 0**h**, Bit 15). Therefore, both the pin and bit must be set low and then either can be set high to execute an on-command calibration. TI recommends holding the CAL pin high during normal usage to reduce the chance that an SEU causes a calibration cycle.	
CalRun	B5	O	Calibration running indication. This output is logic-high while the calibration sequence is executing; otherwise, this output is logic-low.	

表 5-1. Pin Functions: Analog Front-End and Clock Pins (continued)

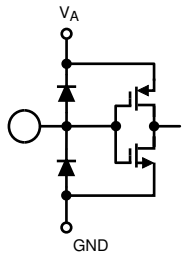
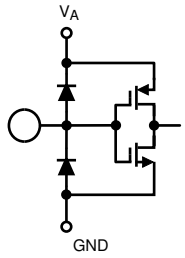
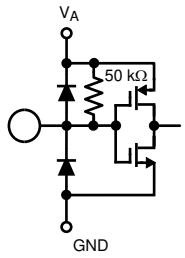
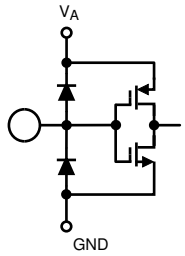
PIN		TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	NO.			
DDRPh	W4	I	DDR phase select. In DDR, when this input is logic-low, it selects the 0° data-to-DCLK phase relationship. When this input is logic-high, it selects the 90° data-to-DCLK phase relationship; that is, the DCLK transition indicates the middle of the valid data outputs. In SDR, when this input is logic-low, the output transitions on the rising edge of DCLK. When this input is logic-high, output transition is on the falling edge of DCLK. This pin only has an effect when the chip is in 1:2 demuxed mode; that is, the NDM pin is set to logic-low. In ECM, this input is ignored and the DDR phase is selected through the Control Register by the DPS bit (Addr: 0**h**, Bit 14); the default is 0° mode.	
DES	V5	I	Dual edge sampling (DES) mode select. In the non-extended control mode (Non-ECM), when this input is set to logic-high, the DES mode of operation is selected; this means that the VinI input is sampled by both channels in a time-interleaved manner and the VinQ input is ignored. When this input is set to logic-low, the device is in non-DES mode; that is, I and Q channels operate independently. In the extended control mode (ECM), this input is ignored and DES mode selection is controlled through the DES bit of the Configuration Register (Addr: 0**h**; Bit: 7); default is non-DES mode operation.	
$\overline{\text{ECE}}$	B3	I	Extended control enable. Extended feature control through the SPI interface is enabled and the device is in ECM when this signal is asserted (logic-low). Please reference 表 7-1 for information on the behavior of the control pins when the extended feature control is enabled. When this signal is de-asserted (logic-high), the SPI interface is disabled, all SPI registers are reset to their default values, and all available settings are controlled with the control pins.	
FSR	Y3	I	Full-scale input range select. In non-ECM, when this input is set to logic-low or logic-high, the full-scale differential input range for both I- and Q-channel inputs is set to the lower or higher FSR value, respectively. In the ECM, this input is ignored and the full-scale range of the I- and Q-channelinputs is independently determined by the setting of the I- and Q-channel Full-Scale Range Adjust Registers (Addr: 3**h** and Addr: B**h**, respectively). Note that the high (lower) FSR value in non-ECM corresponds to the mid (min) available selection in ECM; the FSR range in ECM is greater.	

表 5-1. Pin Functions: Analog Front-End and Clock Pins (continued)

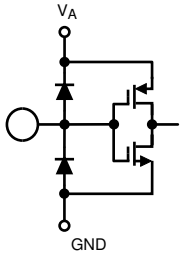
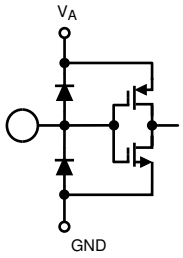
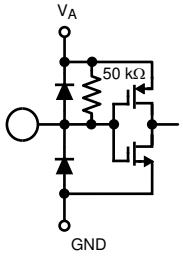
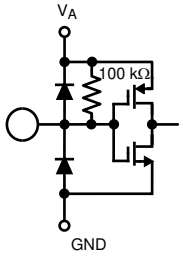
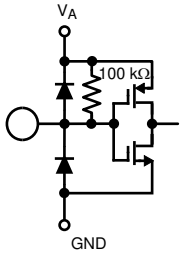
PIN		TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	NO.			
LSPSM	V4	I	Low-sampling power-saving mode (LSPSM) select. In LSPSM, the power consumption is reduced by approximately 20%, and some improvement in performance may be seen. The output is in SDR in 1:2 demux mode and DDR in 1:1 non-demux mode. DDR is not available in 1:2 demux mode in LSPSM. The maximum sampling rate in LSPSM in non-DES mode is 800 MSPS. When this input is logic-high, the device is in LSPSM and when this input is logic-low, the device is in normal mode or non-LSPSM.	
NDM	A5	I	Non-demuxed mode select. Setting this input to logic-high causes the digital output bus to be in the 1:1 non-demuxed mode. Setting this input to logic-low causes the digital output bus to be in the 1:2 demuxed mode. This feature is pin-controlled only and remains active during both ECM and non-ECM.	
PDI PDQ	U3 V3	I	Power down I and Q channels. Setting either input to logic-high powers down the respective I or Q channel. Setting either input to logic-low brings the respective I or Q channel to a operational state after a finite time delay. This pin is active in both ECM and non-ECM. In ECM, each pin is logically OR'd with its respective bit. Therefore, either this pin or the PDI and PDQ bits in the Configuration Register (Addr: 0**h**; Bit: 11 and Bit: 10, respectively) can be used to power down the I and Q channels.	
RSV	W3	—	Reserved. This pin is used for internal purposes and must be connected to GND through a 100-kΩ resistor.	NONE
RSV1	E3	—	Decouple this pin with a 100-nF capacitor with a low resistance, low inductance path to GND.	NONE
RSV2	F4	—	Decouple this pin with a 100-nF capacitor with a low resistance, low inductance path to GND.	NONE
SCLK	C5	I	Serial clock. In ECM, serial data is shifted into and out of the device synchronously to this clock signal. This clock may be disabled and held logic-low, as long as timing specifications are not violated when the clock is enabled or disabled.	
$\overline{SCS}$	C4	I	Serial chip select. In ECM, when this signal is asserted (logic-low), SCLK is used to clock in serial data that is present on SDI and to source serial data on SDO. When this signal is de-asserted (logic-high), SDI is ignored and SDO is tri-state.	

表 5-1. Pin Functions: Analog Front-End and Clock Pins (continued)

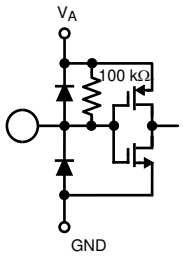
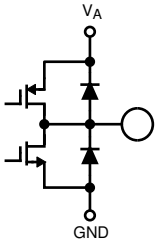
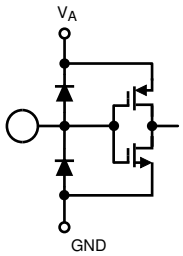
PIN		TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	NO.			
SDI	B4	I	Serial data-in. In ECM, serial data is shifted into the device on this pin while $\overline{SCS}$ signal is asserted (logic-low).	
SDO	A3	O	Serial data-out. In ECM, serial data is shifted out of the device on this pin while $\overline{SCS}$ signal is asserted (logic-low). This output is tri-state when $\overline{SCS}$ is de-asserted (logic-high).	
TPM	A4	I	Test pattern mode select. With this input at logic-high, the device continuously outputs a fixed, repetitive test pattern at the digital outputs. In ECM, this input is ignored, and the test pattern mode can only be activated through the Control Register by the TPM bit (Addr: 0**h**, Bit: 12).	
POWER AND GROUND PINS				
GND	A1, A7, B2, B7, C6, D4, D5, E4, K1, L1, T4, U4, U5, W2, W7, Y1, Y7, AA2:AL11	P	Analog ground return	NONE
GND_{DR}	A13, A17, A20, D13, D16, E17, F17, F20, M17, M20, U13, U17, V18, Y13, Y17, Y20	P	Ground return for the output drivers	NONE
GND_{E}	A9, B8, C9, V9, W8, Y9	P	Ground return for the digital encoder	NONE
GND_{TC}	F2, G2, H3, J2, K4, L4, M2, N3, P2, R2, T2, T3, U1	P	Ground return for the track-and-hold and clock circuitry	NONE
V_A	A2, A6, B6, C7, D1, D8, D9, E1, F1, H4, N4, R1, T1, U8, U9, W6, Y2, Y6	P	Analog power supply. This supply is tied to the ESD ring; therefore, it must be powered up before or with any other supply.	NONE
VbiasI	D7, J4, K2	P	Bias voltage I channel. This is an externally decoupled bias voltage for the I channel. Each pin must individually be decoupled with a 100-nF capacitor through a low resistance, low inductance path to GND.	NONE

表 5-1. Pin Functions: Analog Front-End and Clock Pins (continued)

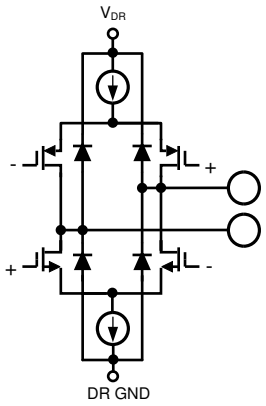
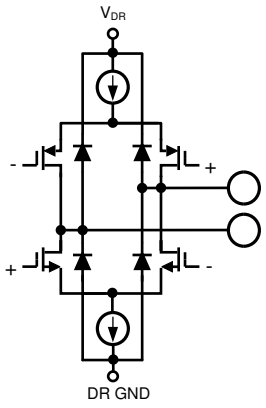
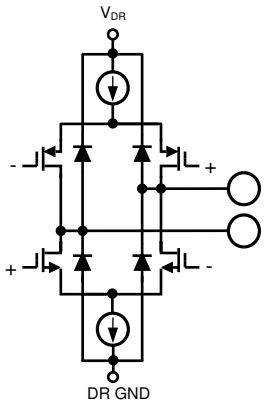
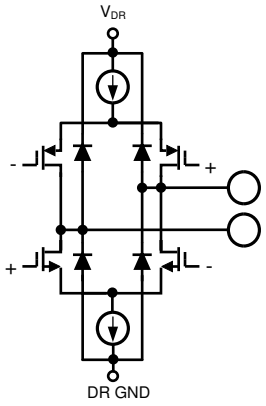
PIN		TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	NO.			
VbiasQ	L2, M4, U7	P	Bias voltage Q channel. This is an externally decoupled bias voltage for the Q channel. Each pin must individually be decoupled with a 100-nF capacitor through a low resistance, low inductance path to GND.	NONE
V_{DR}	A11, A15, C18, D11, D15, D17, J17, J20, R17, R20, T17, U11, U15, U16, Y11, Y15	P	Power supply for the output drivers	NONE
V_E	A8, B9, C8, V8, W9, Y8	P	Power supply for the digital encoder	NONE
V_{TC}	G1, G3, G4, H2, J3, K3, L3, M3, N2, P1, P3, P4, R3, R4	P	Power supply for the track-and-hold and clock circuitry	NONE
HIGH-SPEED DIGITAL OUTPUT PINS				
DCLKI+, DCLKI– DCLKQ+, DCLKQ–	K19/K20 L19/L20	O	Data clock output for the I- and Q-channel data bus. These differential clock outputs are used to latch the output data and, if used, terminate with a 100-Ω differential resistor placed as closely as possible to the differential receiver. Delayed and non-delayed data outputs are supplied synchronously to this signal. The DCLK rates for all of the available modes can be found in 表 7-8. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized.	
DI11+, DI11– DI10+, DI10– DI9+, DI9– DI8+, DI8– DI7+, DI7– DI6+, DI6– DI5+, DI5– DI4+, DI4– DI3+, DI3– DI2+, DI2– DI1+,DI1 – DI0+, DI0– . DQ11+, DQ11– DQ10+, DQ10– DQ9+, DQ9– DQ8+, DQ8– DQ7+, DQ7– DQ6+, DQ6– DQ5+, DQ5– DQ4+, DQ4– DQ3+, DQ3– DQ2+, DQ2– DQ1+, DQ1– DQ0+, DQ0–	J18/J19 H19/H20 H17/H18 G19/G20 G17/G18 F18/F19 E19/E20 D19/D20 D18/E18 C19/C20 B19/B20 B18/C17 . M18/M19 N19/N20 N17/N18 P19/P20 P17/P18 R18/R19 T19/T20 U19/U20 U18/T18 V19/V20 W19/W20 W18/V17	O	I- and Q-channel digital data outputs. In non-demux mode, this LVDS data is transmitted at the sampling clock rate. In demux mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the delayed data; that is, the other ½ of the data which was sampled one clock cycle earlier. Compared with the DId and DQd outputs, these outputs represent the later time samples. If used, terminate each of these outputs with a 100-Ω differential resistor placed as closely as possible to the differential receiver.	

表 5-1. Pin Functions: Analog Front-End and Clock Pins (continued)

PIN		TYPE	DESCRIPTION	EQUIVALENT CIRCUIT
NAME	NO.			
DId11+, DId11– DId10+, DId10– DId9+, DId9– DId8+, DId8– DId7+, DId7– DId6+, DId6– DId5+, DId5– DId4+, DId4– DId3+, DId3– DId2+, DId2– DId1+,DId1 – DId0+, DId0– . DQd11+, DQd11– DQd10+, DQd10– DQd9+, DQd9– DQd8+, DQd8– DQd7+, DQd7– DQd6+, DQd6– DQd5+, DQd5– DQd4+, DQd4– DQd3+, DQd3– DQd2+, DQd2– DQd1+, DQd1– DQd0+, DQd0–	A18/A19 B17/C16 A16/B16 B15/C15 C14/D14 A14/B14 B13/C13 C12/D12 A12/B12 B11/C11 C10/D10 A10/B10 . Y18/Y19 W17/V16 Y16/W16 W15/V15 V14/U14 Y14/W14 W13/V13 V12/U12 Y12/W12 W11/V11 V10/U10 Y10/W10	O	Delayed I- and Q-channel digital data outputs. In non-demux mode, these outputs are tri-state. In demux mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the non-delayed data; that is, the other ½ of the data which was sampled one clock cycle later. Compared with the DI and DQ outputs, these outputs represent the earlier time samples. If used, terminate each of these outputs with a 100-Ω differential resistor placed as closely as possible to the differential receiver.	
ORI+, ORI– ORQ+, ORQ–	K17/K18 L17/L18	O	Out-of-range output for the I and Q channel. This differential output is asserted logic-high while the over- or under-range condition exists; that is, the differential signal at each respective analog input exceeds the full-scale value. Each OR result refers to the current data, with which it is clocked out. If used, terminate each of these outputs with a 100-Ω differential resistor placed as closely as possible to the differential receiver.	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (1) (2)

	MIN	MAX	UNIT
Supply voltage (V_A, V_{TC}, V_{DR}, V_E)		2.2	V
Supply difference – max($V_{A\ /TC\ /DR\ /E}$) – min($V_{A\ /TC\ /DR\ /E}$)	0	100	mV
Voltage on any input pin (except VinI+, VinI–, VinQ+, VinQ–)	−0.15	2.35	V
VinI+, VinI–, VinQ+, VinQ– voltage (maintaining common mode)(3)	−0.5	2.5	V
Input current at VinI+, VinI–, VinQ+, VinQ–(3)		±50	mA
Ground difference – max($GND_{TC\ /DR\ /E}$) – min($GND_{TC\ /DR\ /E}$)	0	100	mV
Input current at any pin(4)		±50	mA
Power dissipation at $T_A \le 125°C$(4)		4.4	W
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = GND_{DR} = GND_E = GND_{TC} = 0 V, unless otherwise specified.
(3) Verified during product qualification high-temperature lifetime testing (HTOL) at T_J = 150°C for 1000 hours continuous operation with V_A = V_D = 2.2 V.
(4) When the input voltage at any pin exceeds the power supply limits, the current at that pin must be limited to 50 mA. In addition, overvoltage at a pin must adhere to maximum voltage limits. Simultaneous overvoltage at multiple pins requires adherence to the maximum package power dissipation limits, which are calculated using the JEDEC JESD51-7 thermal model. Higher dissipation may be possible based on customer-specific thermal situations and specified thermal package resistances from junction to case.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body Model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Case temperature		−55	125	°C
Supply voltage (V_A, V_{TC}, V_E)		1.8	2	V
Voltage on any input pin (except VinI+, VinI–, VinQ+, VinQ–)		−0.15	2.15	V
Driver supply voltage (V_{DR})		1.8	V_A	V
VinI+, VinI–, VinQ+, VinQ– voltage(2)	DC-coupled	–0.4	2.4	V
VinI+, VinI–, VinQ+, VinQ– differential voltage(3)	DC-coupled at 100% duty cycle		1	V
	DC-coupled at 20% duty cycle		2	
	DC-coupled at 10% duty cycle		2.8	
VinI+, VinI–, VinQ+, VinQ– current(2)	AC-coupled	–50	50	mA
VinI+, VinI–, VinQ+, VinQ– power	Maintaining common-mode voltage, AC-coupled		15.3	dBm
	Not maintaining common-mode voltage, AC-coupled		17.1	
Ground difference – max($GND_{TC/DR/E}$) – min($GND_{TC/DR/E}$)			0	V
Input current at any pin except VinI+, VinI–, VinQ+, or VinQ–(4)			±50	mA
CLK+, CLK– voltage		0	V_A	V
Differential CLK amplitude		0.4	2	V_{P-P}
V_{CMI} common-mode input voltage		V_{CMO} – 150	V_{CMO} + 150	mV

(1) All voltages are measured with respect to GND = GND_{DR} = GND_E = GND_{TC} = 0 V, unless otherwise specified.
(2) Proper common mode voltage must be maintained to ensure proper output code, especially during input overdrive.
(3) This rating is intended for DC-coupled applications; the voltages and duty cycles listed may be safely applied to V_{IN}± for the lifetime of the part.
(4) When the input voltage at any pin exceeds the power supply limits, the current at that pin must be limited to 50 mA. In addition, overvoltage at a pin must adhere to maximum voltage limits. Simultaneous overvoltage at multiple pins requires adherence to the maximum package power dissipation limits, which are calculated using the JEDEC JESD51-7 thermal model. Higher dissipation may be possible based on customer-specific thermal situations and specified thermal package resistances from junction to case.

6.4 Thermal Information

THERMAL METRIC(1) (2)		ADC12D1620QML-SP NAA (CCGA) 376 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	13.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.7	°C/W

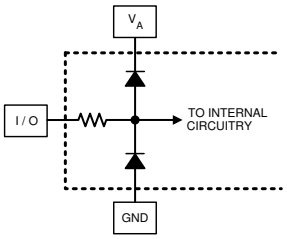
(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*
(2) Solder process specifications in *Board Mounting Recommendation*.

6.5 Converter Electrical Characteristics: Static Converter Characteristics

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10-pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

PARAMETER		TEST CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
INL	Integral non-linearity	DC-coupled, 1 MHz sine wave over-ranged	[1, 2, 3]	–7.5	±2.5	7.5	LSB
DNL	Differential non-linearity	DC-coupled, 1 MHz sine wave over-ranged	[1, 2, 3]	–1.35	±0.5	1.35	LSB
	Resolution with no missing codes		[1, 2, 3]			12	bits
V_{OFF}	Offset error				8		LSB
V_{OFF}_ADJ	Input offset adjustment range	Extended control mode			±45		mV
PFSE	Positive full-scale error	See(4)	[1, 2, 3]	–30		30	mV
NFSE	Negative full-scale error	See(4)	[1, 2, 3]	–30		30	mV
	Out-of-range output code	(V_{IN}+) − (V_{IN}−) > positive full scale	[1, 2, 3]			4095	
		(V_{IN}+) − (V_{IN}−) < negative full scale	[1, 2, 3]	0			

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(2) To ensure accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

(4) Calculation of full-scale error for this device assumes that the actual reference voltage is exactly its nominal value. Full-scale error for this device, therefore, is a combination of full-scale error and reference voltage error. For relationship between gain error and full-scale error, see gain error in *Device Nomenclature*.

6.6 Converter Electrical Characteristics: Dynamic Converter Characteristics

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

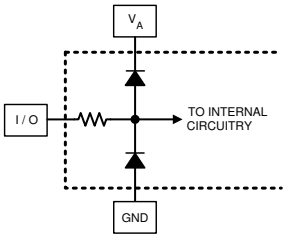
PARAMETER		TEST CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
CER	Code error rate				10^{-18}		Error/ Sample
IMD_3	3rd order intermodulation distortion	f_{IN} = 2070 MHz ± 2.5 MHz at –13 dBFS			–76		dBFS
					–63		dBc
		f_{IN} = 2070 MHz ± 2.5 MHz at –16 dBFS			–80		dBFS
					–64		dBc
		f_{IN} = 2670 MHz ± 2.5 MHz at –13 dBFS			–72		dBFS
					–59		dBc
		f_{IN} = 2670 MHz ± 2.5 MHz at –16 dBFS			–77		dBFS
					–61		dBc
1:2 DEMUX, NON-DES MODE, NON-ECM, NON-LSPSM, f_{CLK} = 1.6 GHz, f_{IN} = 248 MHz, V_{IN} = –0.5 dBFS							
ENOB	Effective number of bits		[4]	8.8	9.1		bits
			[5]	8.7			
			[6]	8.4			
SINAD	Signal-to-noise plus distortion ratio		[4]	54.7	56.5		dBFS
			[5]	54.1			
			[6]	52.3			
SNR	Signal-to-noise ratio		[4]	56	58.4		dBFS
			[5]	54.6			
			[6]	53.5			dBFS
THD	Total harmonic distortion		[4, 5]		–62	–59.2	dBFS
			[6]			–55.5	dBFS
2nd Harm	Second harmonic distortion				–72.2		dBFS
3rd Harm	Third harmonic distortion				–62.1		dBFS
SFDR	Spurious-free dynamic range		[4]	58.9	62.1		dBFS
			[5]	58.1			
			[6]	56			dBFS
1:2 DEMUX, NON-DES MODE, NON-ECM, LSPSM, f_{CLK} = 800 MHz, f_{IN} = 248 MHz, V_{IN} = –0.5 dBFS							
ENOB	Effective number of bits		[4, 5]	9.1	9.5		bits
			[6]	8.6			bits
SINAD	Signal-to-noise plus distortion ratio		[4, 5]	56.5	58.6		dBFS
			[6]	53.5			dBFS
SNR	Signal-to-noise ratio		[4, 5]	57.6	59.8		dBFS
			[6]	56.8			dBFS
THD	Total harmonic distortion		[4, 5]		–67	–62.3	dBFS
			[6]			–57	dBFS
2nd Harm	Second harmonic distortion				–77.7		dBFS
3rd Harm	Third harmonic distortion				–67.5		dBFS

6.6 Converter Electrical Characteristics: Dynamic Converter Characteristics (continued)

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

PARAMETER		TEST CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
SFDR	Spurious-free dynamic range		[4, 5]	62.5	67.4		dBFS
			[6]	57.5			dBFS
NON-DEMUX, NON-DES MODE, ECM, NON-LSPSM, f_{CLK} = 1.6 GHz, f_{IN} = 248 MHz, V_{IN} = –0.5 dBFS							
ENOB	Effective number of bits				9.1		bits
SINAD	Signal-to-noise plus distortion ratio				56.6		dBFS
SNR	Signal-to-noise ratio				58.6		dBFS
THD	Total harmonic distortion				–63.2		dBFS
2nd Harm	Second harmonic distortion				–72		dBFS
3rd Harm	Third harmonic distortion				–63.3		dBFS
SFDR	Spurious-free dynamic range				63.3		dBFS
1:4 DEMUX, DES MODE, NON-LSPSM, f_{CLK} = 1.6 GHz, f_{IN} = 248 MHz, V_{IN} = –0.5 dBFS							
ENOB	Effective number of bits				8.9		bits
SINAD	Signal-to-noise plus distortion ratio				55.5		dB
SNR	Signal-to-noise ratio				56.9		dBFS
THD	Total harmonic distortion				–62.3		dBFS
2nd Harm	Second harmonic distortion				–79.1		dBFS
3rd Harm	Third harmonic distortion				–62.3		dBFS
SFDR	Spurious-free dynamic range				61.7		dBFS

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(2) To ensure accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

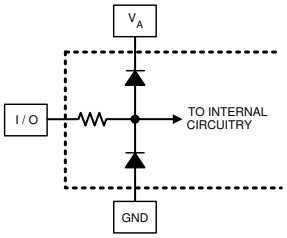
(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

6.7 Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10-pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

PARAMETER		TEST CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
V_{IN_FSR}	Analog differential input full-scale range	FSR pin Y3 Low	[4, 5, 6]		630		mV_{P-P}
		FSR pin Y3 High	[4, 5, 6]	750	820	890	mV_{P-P}
		EXTENDED CONTROL MODE					
		FM(14:0) = 0000**h**			600		mV_{P-P}
		FM(14:0) = 4000**h** (default)			800		mV_{P-P}
		FM(14:0) = 7FFF**h**			1000		mV_{P-P}
C_{IN}	Analog input capacitance, Non-DES mode (4) (5)	Differential			0.02		pF
		Each input pin to ground			1.6		pF
	Analog input capacitance, DES mode (4) (5)	Differential			0.02		pF
		Each input pin to ground			2.2		pF
R_{IN}	Differential input resistance		[1, 2, 3]	99	103	107	Ω
COMMON-MODE OUTPUT							
V_{CMO}	Common-mode output voltage	I_{CMO} = ±100 µA	[1, 2, 3]	1.15	1.25	1.35	V
TC_V_{CMO}	Common-mode output voltage temperature coefficient	I_{CMO} = ±100 µA			38		ppm/°C
V_{CMO_LVL}	V_{CMO} input threshold to set DC-coupling mode				0.63		V
$C_L\_V_{CMO}$	Maximum V_{CMO} load capacitance	See(5)				80	pF
BANDGAP REFERENCE							
V_{BG}	Bandgap reference output voltage	I_{BG} = ±100 µA	[1, 2, 3]	1.15	1.27	1.35	V
TC_V_{BG}	Bandgap reference voltage temperature coefficient	I_{BG} = ±100 µA			50		ppm/°C
C_{LOAD} V_{BG}	Maximum bandgap reference load capacitance				80		pF

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(2) To ensure accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

(4) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.22-pF differential and 1.06-pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

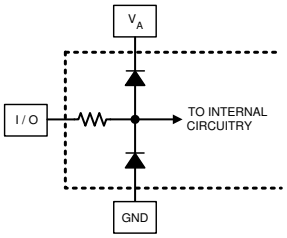
(5) This parameter is specified by design and/or characterization and is not tested in production.

6.8 Converter Electrical Characteristic: Channel-to-Channel Characteristics

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

	PARAMETER	CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
	Phase matching (I, Q)	f_{IN} = 1 GHz			< 1		Degree
X-TALK Q-channel	Crosstalk from I channel (aggressor) to Q channel (victim)	Aggressor = 248 MHz			–72		dBFS
		Aggressor = 498 MHz			–75		dBFS
X-TALK I-channel	Crosstalk from Q channel (aggressor) to I channel (victim)	Aggressor = 248 MHz			–71		dBFS
		Aggressor = 498 MHz			–79		dBFS

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(2) To ensure accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

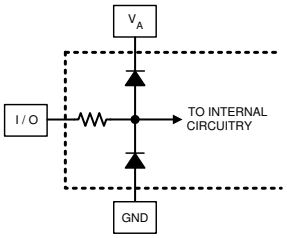
(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

6.9 Converter Electrical Characteristics: LVDS CLK Input Characteristics

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

	PARAMETER	CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
V_{IN_CLK}	Differential clock input level(5)	Sine-wave clock	[1, 2, 3]	0.4		2	V_{P-P}
		Square-wave clock	[1, 2, 3]	0.4		2	
C_{IN_CLK}	Sampling clock input capacitance(5)(4)	Differential			0.1		pF
		Each input to ground			1		
R_{IN_CLK}	Sampling clock input resistance				100		Ω

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(2) To ensure accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

(4) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.22-pF differential and 1.06-pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

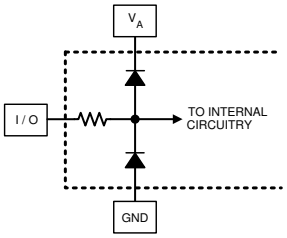
(5) This parameter is specified by design and/or characterization and is not tested in production.

6.10 Electrical Characteristics: AutoSync Feature

The following specifications apply after calibration for for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = High; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on(1) (2)

PARAMETER		TEST CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
V_{IN_RCLK}	Differential RCLK input level	Differential peak-to-peak			360		mV_{p-p}
C_{IN_RCLK}	RCLK input capacitance	Differential			0.1		pF
		Each input to ground			1		
R_{IN_CLK}	RCLK differential input resistance				100		Ω
I_{IH_RCLK}	Input leakage current	V_{IN} = V_A	[1, 2, 3]		20		µA
I_{IL_RCLK}	Input leakage current	V_{IN} = GND	[1, 2, 3]		–32		µA
V_{O_RCOUT}	Differential RCOut output voltage				360		mV_{p-p}

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(2) To ensure accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

6.11 Converter Electrical Characteristics: Digital Control and Output Pin Characteristics

The following specifications apply after calibration for for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = High; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

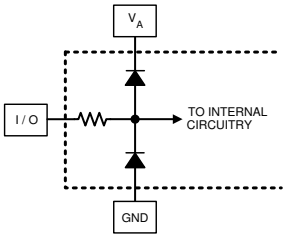
PARAMETER		CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
DIGITAL CONTROL PINS, (DES, LSPSM, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$— unless otherwise specified)							
V_{IH}	Logic high input voltage		[1, 2, 3]	0.7 x V_A			V
V_{IL}	Logic low input voltage		[1, 2, 3]			0.3 x V_A	V
I_{IH}	Input leakage current	V_{IN} = V_A	[1, 2, 3]	–1		1	µA
I_{IL}	Input leakage current (DES, LSPSM, CAL, TPM, NDM, FSR, DDRPh)	V_{IN} = GND	[1, 2, 3]	–1		1	µA
	Input leakage current (SCLK, SDI, $\overline{SCS}$)		[1, 2, 3]	–30			µA
	Input leakage current (PDI, PDQ, $\overline{ECE}$)		[1, 2, 3]	–55			µA
C_{IN_DIG}	Input capacitance (4)	Each input to ground			1.5		pF
DIGITAL OUTPUT PINS (Data, DCLKI, DCLKQ, ORI, ORQ) - see *Device Nomenclature*							

6.11 Converter Electrical Characteristics: Digital Control and Output Pin Characteristics (continued)

The following specifications apply after calibration for for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = High; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

PARAMETER		CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
V_{OD}	LVDS differential output voltage	V_{BG} = floating, OVS = High	[1, 2, 3]	380	600	840	mV_{P-P}
		V_{BG} = floating, OVS = Low	[1, 2, 3]	240	440	650	mV_{P-P}
		V_{BG} = V_A, OVS = high	[1, 2, 3]		670		mV_{P-P}
		V_{BG} = V_A, OVS = low	[1, 2, 3]		500		mV_{P-P}
$\Delta V_{O\ DIFF}$	Change in LVDS output swing between logic levels			-20	1	20	mV
V_{OS}	Output offset voltage	V_{BG} = floating			0.8		V
		V_{BG} = V_A			1.2		V
ΔV_{OS}	Change in output offset voltage between logic levels				±1		mV
I_{OS}	Output short-circuit current	V_{BG} = floating; D+ and D− connected to 0.8 V			±3.8		mA
Z_O	Differential output impedance				100		Ω
DIFFERENTIAL DCLK RESET PINS (DCLK_RST)							
V_{CMI_DRST}	DCLK_RST Common mode Input Voltage				1.25		V
V_{ID_DRST}	Differential DCLK_RST Input Voltage				0.6		V_{P-P}
R_{IN_DRST}	Differential DCLK_RST Input Resistance(5)				100		Ω
DIGITAL OUTPUT PINS (CalRun, SDO)							
V_{OH}	Logic high output level	CalRun, SDO I_{OH} = −400 µA	[1, 2, 3]	1.5	1.7		V
V_{OL}	Logic low output level	CalRun, SDO I_{OH} = 400 µA	[1, 2, 3]		0.14	0.3	V

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(2) To ensure accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).
(4) The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6-pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(5) This parameter is specified by design and/or characterization and is not tested in production.

6.12 Converter Electrical Characteristics: Power Supply Characteristics

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

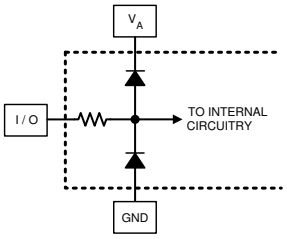
PARAMETER		CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
f_{CLK} = 1.6 GHz, 1:2 DEMUX MODE, NON-LSPSM							
I_A	Analog supply current	PDI = PDQ = Low	[1, 2, 3]		1160		mA
		PDI = Low; PDQ = High			637		mA
		PDI = High; PDQ = Low			635		mA
		PDI = PDQ = High			2		mA
I_{TC}	Track-and-hold and clock supply current	PDI = PDQ = Low	[1, 2, 3]		471		mA
		PDI = Low; PDQ = High			284		mA
		PDI = High; PDQ = Low			284		mA
		PDI = PDQ = High			1		mA
I_{DR}	Output driver supply current	PDI = PDQ = Low	[1, 2, 3]		281		mA
		PDI = Low; PDQ = High			149		mA
		PDI = High; PDQ = Low			143		mA
		PDI = PDQ = High			8		µA
I_E	Digital encoder supply current	PDI = PDQ = Low	[1, 2, 3]		90		mA
		PDI = Low; PDQ = High			54		mA
		PDI = High; PDQ = Low			42		mA
		PDI = PDQ = High			0.04		µA
I_T	Total current	PDI = PDQ = Low	[1, 2, 3]		2020	2280	mA
		PDI = Low; PDQ = High	[1, 2, 3]		1120	1300	mA
		PDI = High; PDQ = Low	[1, 2, 3]		1110	1300	mA
		PDI = PDQ = High			2.7		mA
P_C	Power consumption	PDI = PDQ = Low	[1, 2, 3]		3.8	4.4	W
		PDI = Low; PDQ = High			2.1		W
		PDI = High; PDQ = Low			2.1		W
		PDI = PDQ = High			5.2		mW

6.12 Converter Electrical Characteristics: Power Supply Characteristics (continued)

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

PARAMETER		CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
f_{CLK} = 800 MHz, 1:2 DEMUX MODE, LSPSM							
I_A	Analog supply current	PDI = PDQ = Low	[1, 2, 3]		754		mA
		PDI = Low; PDQ = High			423		mA
		PDI = High; PDQ = Low			423		mA
		PDI = PDQ = High			2		mA
I_{TC}	Track-and-hold and clock supply current	PDI = PDQ = Low	[1, 2, 3]		344		mA
		PDI = Low; PDQ = High			212		mA
		PDI = High; PDQ = Low			212		mA
		PDI = PDQ = High			1		mA
I_{DR}	Output driver supply current	PDI = PDQ = Low	[1, 2, 3]		273		mA
		PDI = Low; PDQ = High			141		mA
		PDI = High; PDQ = Low			141		mA
		PDI = PDQ = High			8		µA
I_E	Digital encoder supply current	PDI = PDQ = Low	[1, 2, 3]		46		mA
		PDI = Low; PDQ = High			24		mA
		PDI = High; PDQ = Low			22		mA
		PDI = PDQ = High			0.03		µA
I_T	Total current	PDI = PDQ = Low	[1, 2, 3]		1417	1620	mA
		PDI = Low; PDQ = High	[1, 2, 3]		801	940	mA
		PDI = High; PDQ = Low	[1, 2, 3]		799	940	mA
		PDI = PDQ = High			2.7		mA
P_C	Power consumption	PDI = PDQ = Low	[1, 2, 3]		2.7	3.1	W
		PDI = Low; PDQ = High			1.5		W
		PDI = High; PDQ = Low			1.5		W
		PDI = PDQ = High			5.2		mW

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(2) To ensure accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

6.13 Converter Electrical Characteristics: AC Electrical Characteristics

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

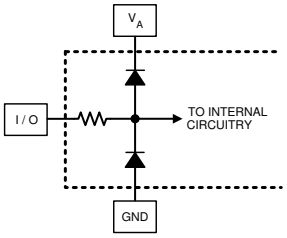
PARAMETER		CONDITIONS		SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
INPUT CLOCK (CLK)								
$f_{CLK\ (max)}$	Maximum input clock frequency	Non-LSPSM		[9, 10, 11]	1.6			GHz
		LSPSM		[9, 10, 11]	800			MHz
$f_{CLK\ (min)}$	Minimum input clock frequency	Non-LSPSM	Non-DES mode; LFS = 1**b**	[9, 10, 11]			200	MHz
			DES mode				250	
		LSPSM	Non-DES mode	[9, 10, 11]			200	MHz
	Input clock duty cycle(4)	$f_{CLK(min)} \le f_{CLK} \le f_{CLK}$ (max)			20%	50%	80%	
t_{CL}	Input clock low time(4)				200	500		ps
t_{CH}	Input clock high time(4)				200	500		ps
DCLK_RST								
t_{SR}	Setup time DCLK_RST±					45		ps
t_{HR}	Hold time DCLK_RST±					45		ps
t_{PWR}	Pulse width DCLK_RST±					5		Input Clock Cycles
DATA CLOCK (DCLKI, DCLKQ)								
	DCLK duty cycle					50%		
t_{SYNC_DLY}	DCLK synchronization delay	90° mode				4		Input Clock Cycles
		0° mode				5		
t_{LHT}	Differential low-to-high transition time	10% to 90%, C_L = 2.5-pF				200		ps
t_{HLT}	Differential high-to-low transition time	10% to 90%, C_L = 2.5-pF				200		ps
t_{SU}	Data-to-DCLK set-up time	DDR mode, 90° DCLK				500		ps
t_H	DCLK-to-data hold time	DDR mode, 90° DCLK				500		ps
t_{OSK}	DCLK-to-data output skew	50% of DCLK transition to 50% of data transition				±50		ps

6.13 Converter Electrical Characteristics: AC Electrical Characteristics (continued)

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1) (2)

PARAMETER		CONDITIONS	SUB-GROUPS	MIN	TYP(3)	MAX	UNIT
DATA INPUT-TO-OUTPUT							
t_{AD}	Sampling (aperture) delay	Input CLK+ rise to acquisition of data			1.3		ns
t_{AJ}	Aperture jitter				0.2		ps (rms)
t_{OD}	Input clock-to data output delay (in addition to t_{LAT})	50% of input clock transition to 50% of data transition			3.2		ns
t_{LAT}	Latency in 1:2 demux non-DES mode(4)	DI, DQ outputs	[4, 5, 6]			34	Input Clock Cycles
		DId, DQd outputs	[4, 5, 6]			35	
	Latency in 1:4 demux DES mode(4)	DI outputs	[4, 5, 6]			34	Input Clock Cycles
		DQ outputs	[4, 5, 6]			34.5	
		DId outputs	[4, 5, 6]			35	
		DQd outputs	[4, 5, 6]			35.5	
	Latency in non-demux non-DES mode(4)	DI outputs	[4, 5, 6]			34	Input Clock Cycles
		DQ outputs	[4, 5, 6]			34	
	Latency in non-demux DES mode(4)	DI outputs	[4, 5, 6]			34	Input Clock Cycles
		DQ outputs	[4, 5, 6]			34.5	
t_{ORR}	Over range recovery time	Differential V_{IN} step from ±1.2 V to 0 V to get accurate conversion			1		Input Clock Cycle
t_{WU}	PD low-to-rated accuracy conversion (wake-up time)	Non-DES mode			500		ns
		DES mode			1		µs

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(2) The maximum clock frequency for non-demux mode is 1 GHz.
(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).
(4) This parameter is specified by design and/or characterization and is not tested in production.

6.14 Electrical Characteristics: Delta Parameters

over operating free-air temperature range (unless otherwise noted)(1) (2) (3) (4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_A	Analog supply current		–6		6	mA
I_{TC}	Track and hold supply current		–4		4	mA
I_{DR}	Output driver supply current		–15		15	mA
I_E	Digital encoder supply current		–30		30	mA

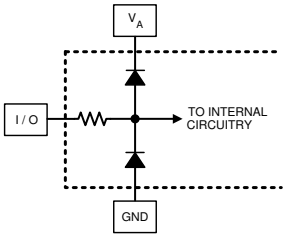
(1) Delta parameters are measured on the automated test equipment (ATE) as part of the ATE program at both pre and post burn-in.
(2) The four delta parameter currents are measured at the beginning of the ATE program. The voltage supply is then pulsed to the absolute max and the remainder of the ATE program is executed. After the ATE program is executed, the four delta parameter currents are measured again. The differences in the measured supply currents at the beginning and end of the ATE program are the delta parameters.
(3) Delta parameters are measured at T_A = 25°C prior to burn-in and at T_A= –55°C, 25°C, and 125°C after burn-in. The differences between supply currents measured before and after burn-in are not included in the delta parameter analysis.
(4) For delta parameters outside of the distribution, the corresponding parts are rejected.

6.15 Timing Requirements: Serial Port Interface

over operating free-air temperature range (unless otherwise noted) The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = High; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1)(2)

PARAMETER		TEST CONDITIONS	SUB-GROUPS	MIN	NOM(2)	MAX	UNIT
$f_{SCLK\ (max)}$	Maximum serial clock frequency	See(3)		15			MHz
$f_{SCLK\ (min)}$	Minimum serial clock frequency	See(3)				0	MHz
	Serial clock low time		[9, 10, 11]	30			ns
	Serial clock high time		[9, 10, 11]	30			ns
t_{SSU}	Serial data to serial clock rising setup time	See(3)		2.5			ns
t_{SH}	Serial data to serial clock rising hold time	See(3)		1			ns
t_{SCS}	$\overline{SCS}$ to serial clock rising setup time				2.5		ns
t_{HCS}	$\overline{SCS}$ to serial clock falling hold time				1.5		ns
t_{BSU}	Bus turnaround time				10		ns

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *セクション 6.1* may damage this device.



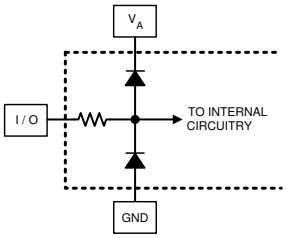
(2) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).
(3) This parameter is specified by design and/or characterization and is not tested in production.

6.16 Timing Requirements: Calibration

over operating free-air temperature range (unless otherwise noted) The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = 1.9 V; I and Q channels AC-coupled, FSR pin = high; C_L = 10 pF; differential AC-coupled sine wave input clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I and Q channels; duty-cycle stabilizer on.(1)(2)

PARAMETER		TEST CONDITIONS	SUB-GROUPS	MIN	NOM(2)	MAX	UNIT
t_{CAL}	Calibration cycle time	Non-ECM			4.1×10^7		Clock Cycles
		ECM; CSS = 0b					
		ECM; CSS = 1b					
t_{CAL_L}	CAL pin low time	See 図 6-8, note (3)	[9, 10, 11]	1280			Clock Cycles
t_{CAL_H}	CAL pin high time	See 図 6-8, note (3)	[9, 10, 11]	1280			Clock Cycles

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(2) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

(3) This parameter is specified by design and/or characterization and is not tested in production.

6.17 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMPERATURE (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Setting time at	+25
13	Setting time at	+125
14	Setting time at	-55

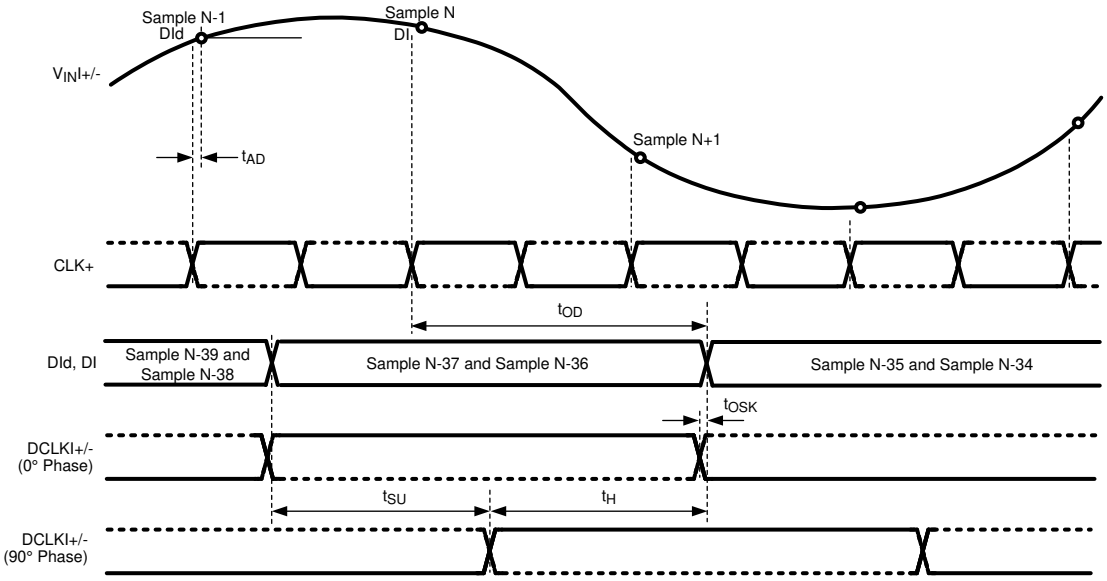


図 6-1. Clocking in Non-LSPSM, 1:2 Demux, Non-DES Mode*

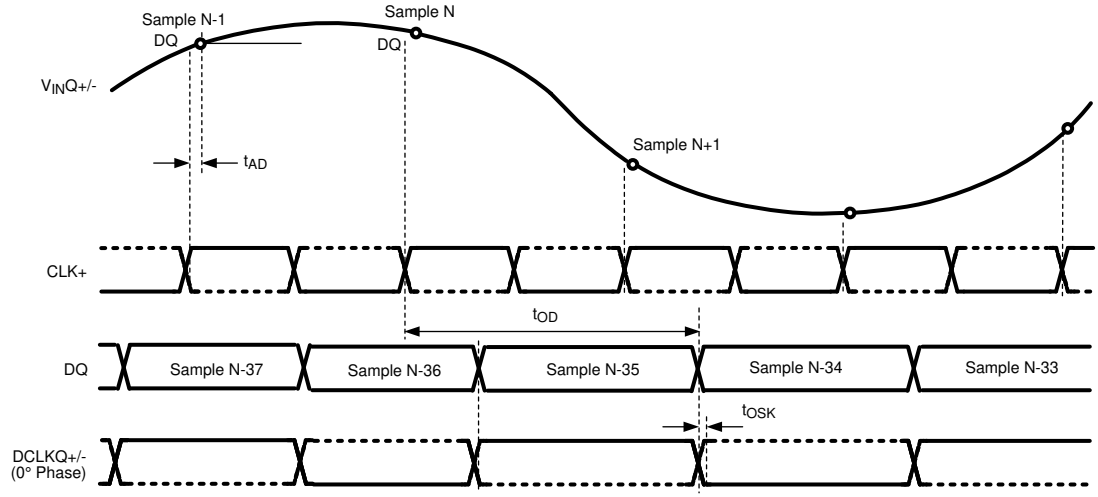


図 6-2. Clocking in Non-LSPSM, Non-Demux, Non-DES Mode*

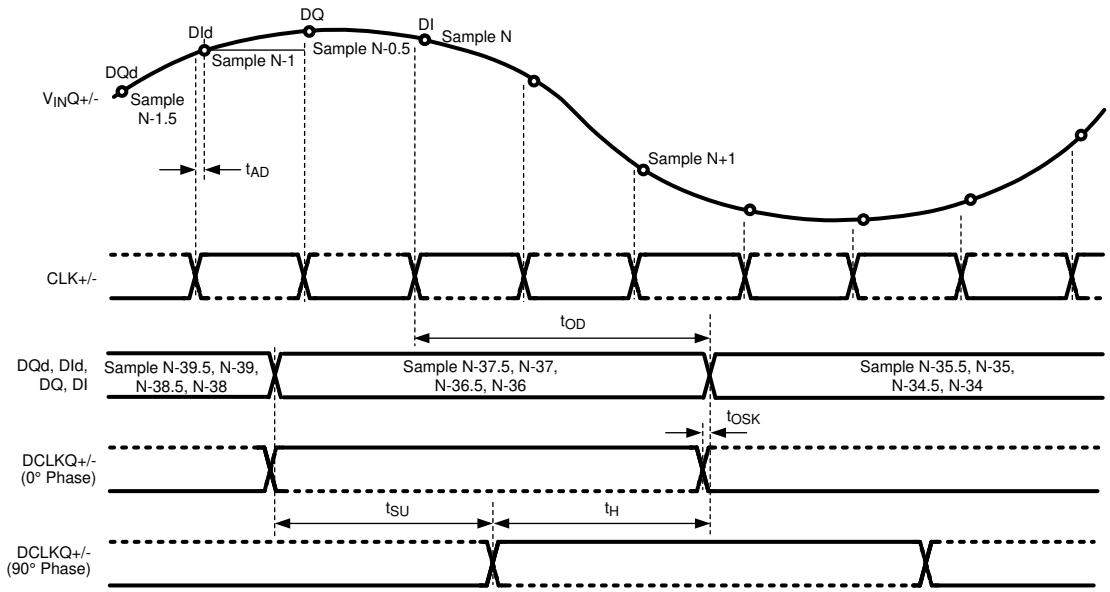


図 6-3. Clocking in Non-LSPSM, 1:4 Demux DES Mode*

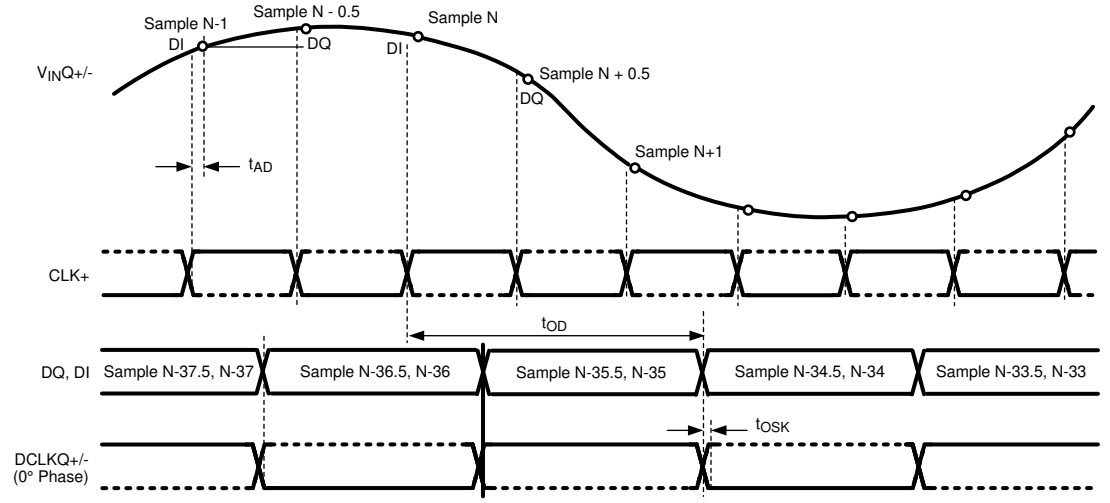


図 6-4. Clocking in Non-LSPSM, Non-Demux Mode DES Mode*

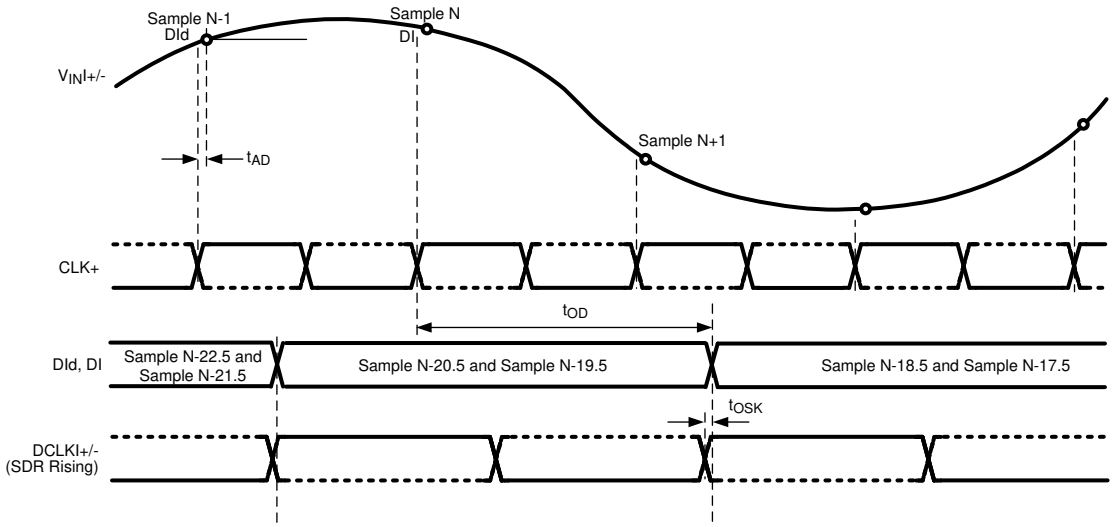


図 6-5. Clocking in LSPSM, 1:2 Demux Mode, Non-DES Mode*

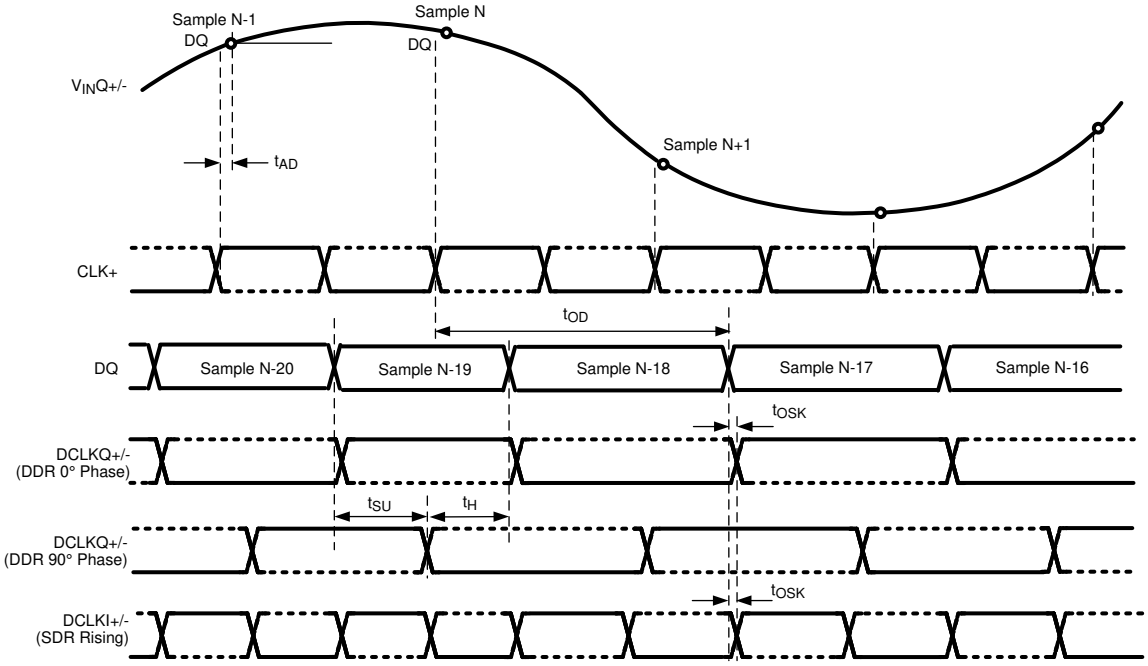


図 6-6. Clocking in LSPSM, Non-Demux Mode, Non-DES Mode*

* The timing for 図 6-1 through 図 6-6 is shown for the one input only (I or Q). However, both I and Q inputs may be used. For this case, the I channel functions precisely the same as the Q channel, with VinI, DCLKI, DId, and DI instead of VinQ, DCLKQ, DQd, and DQ. Both I and Q channel use the same CLK.

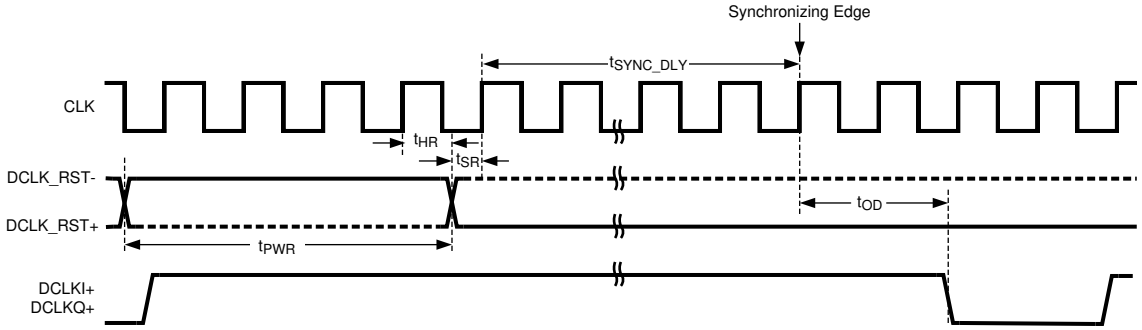


図 6-7. Data Clock Reset Timing (Demux Mode)

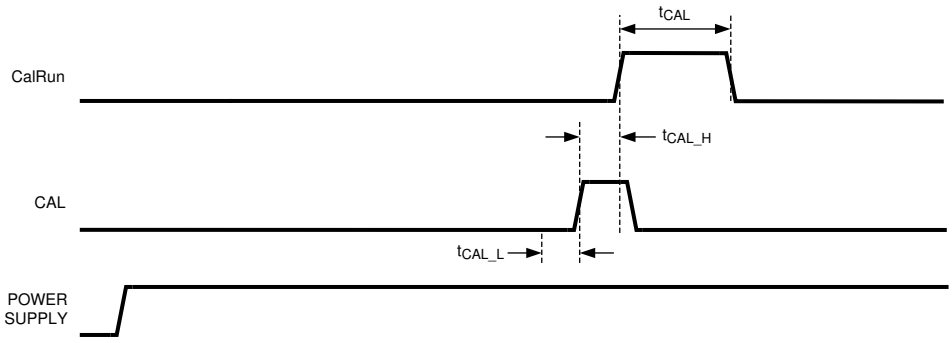


図 6-8. On-Command Calibration Timing

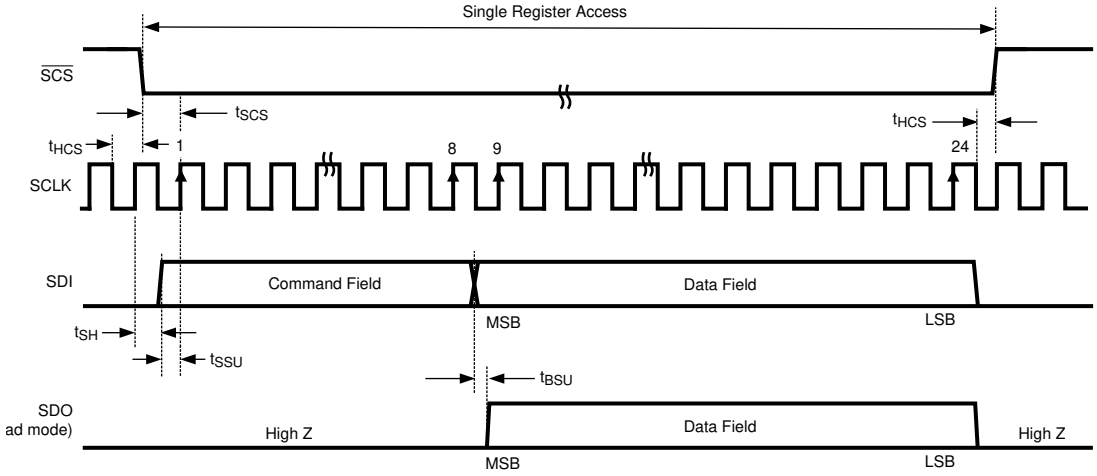


図 6-9. Serial Interface Timing

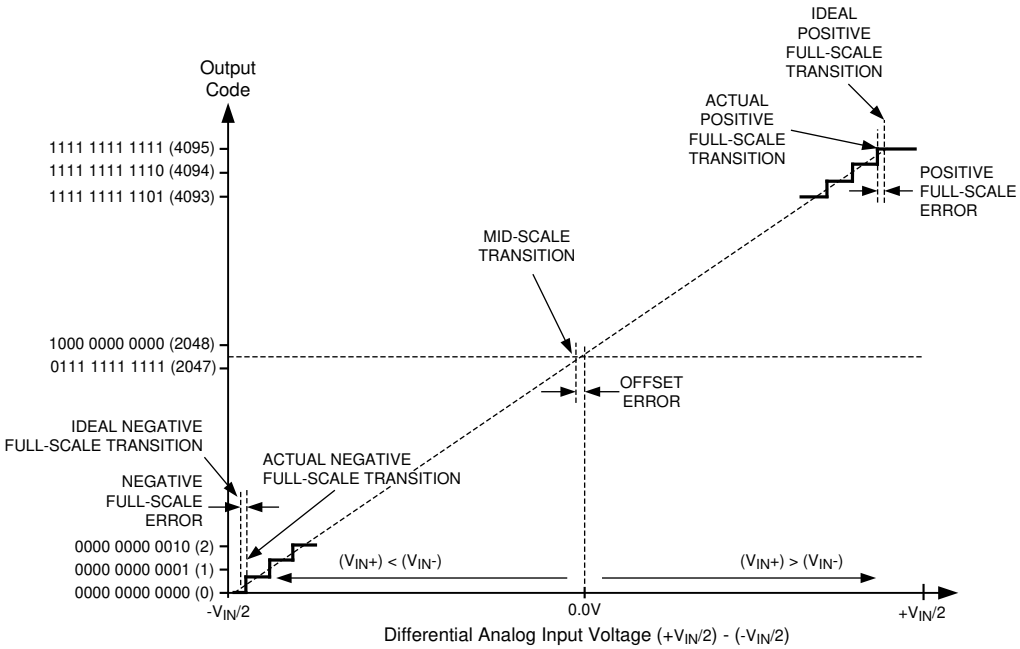


図 6-10. Input / Output Transfer Characteristic

6.19 Typical Characteristics

V_A = V_{DR} = V_{TC} = V_E = 1.9 V, f_{CLK} = 1600 MHz in non-LSPSM and 800 MHz in LSPSM, f_{IN} = 248 MHz, T_A= 25°C, 1:2 demux non-DES mode, and calibration performed after temperature, supply voltage or sample rate change, unless otherwise stated.

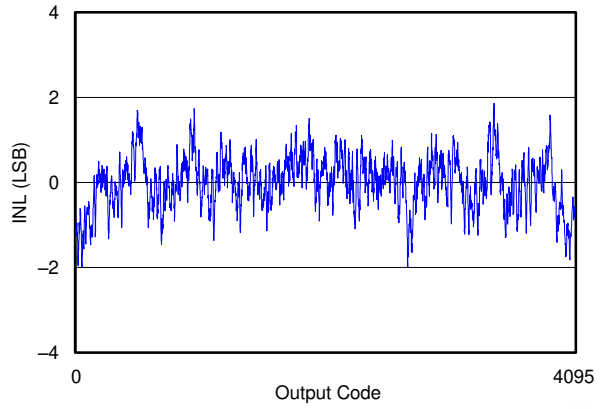


図 6-11. INL vs Code

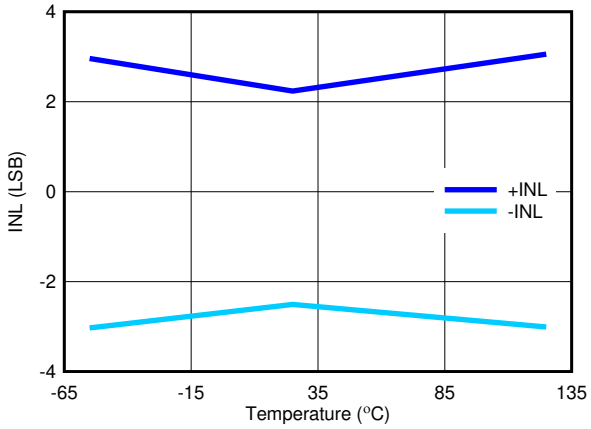


図 6-12. Minimum and Maximum INL vs Temperature

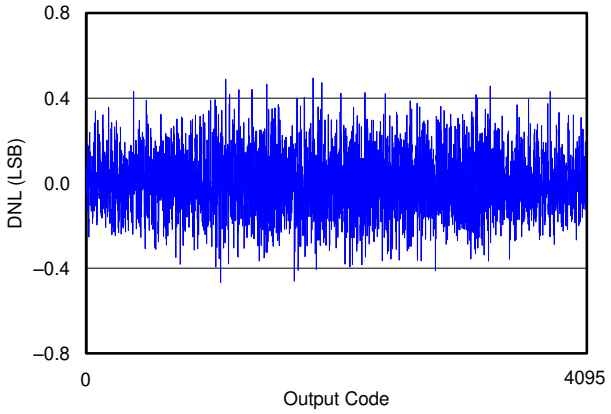


図 6-13. DNL vs Code

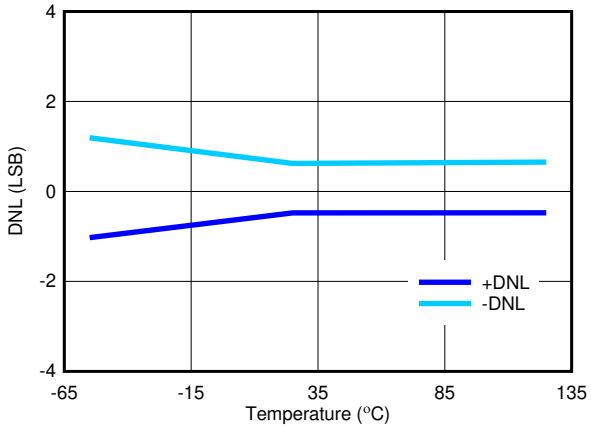


図 6-14. Minimum and Maximum DNL vs Temperature

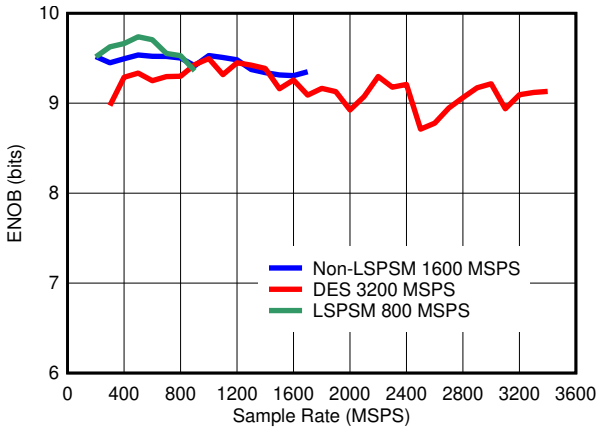


図 6-15. ENOB vs Sample Rate

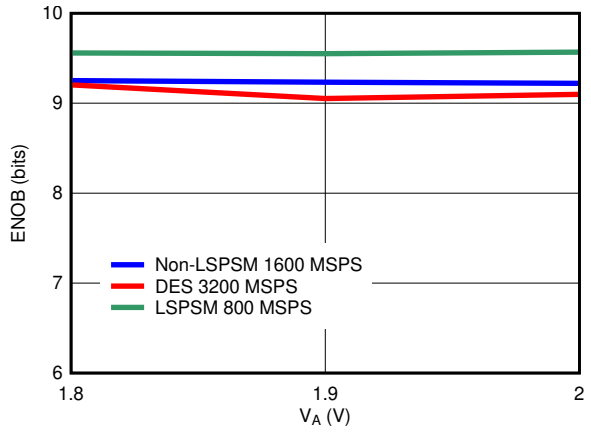


図 6-16. ENOB vs Supply Voltage

6.19 Typical Characteristics (continued)

V_A = V_{DR} = V_{TC} = V_E = 1.9 V, f_{CLK} = 1600 MHz in non-LSPSM and 800 MHz in LSPSM, f_{IN} = 248 MHz, T_A= 25°C, 1:2 demux non-DES mode, and calibration performed after temperature, supply voltage or sample rate change, unless otherwise stated.

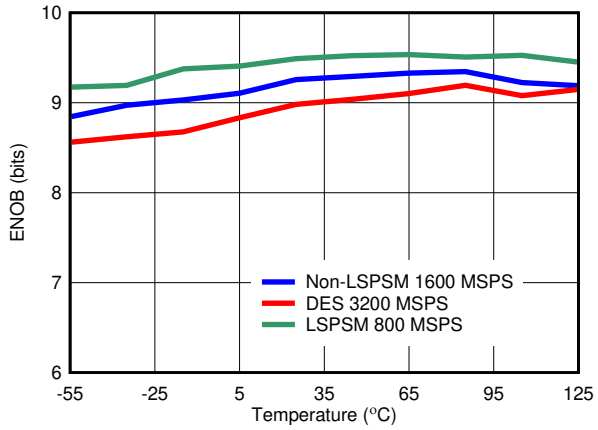


図 6-17. ENOB vs Temperature

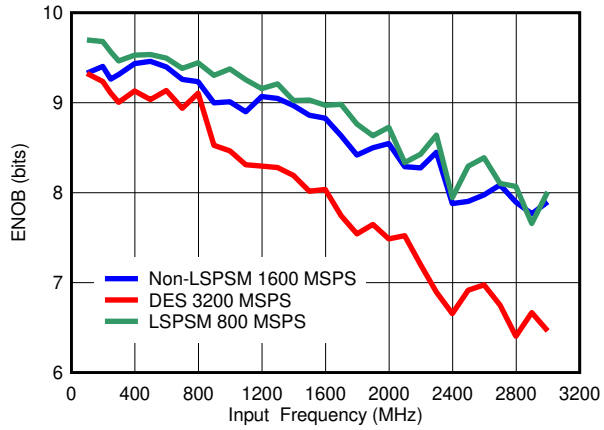


図 6-18. ENOB vs Input Frequency

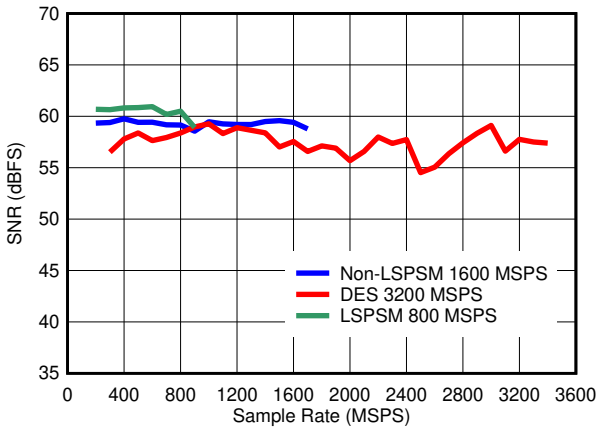


図 6-19. SNR vs Sample Rate

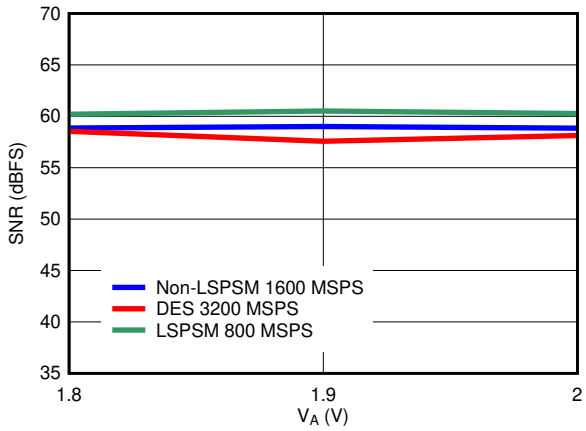


図 6-20. SNR vs Supply Voltage

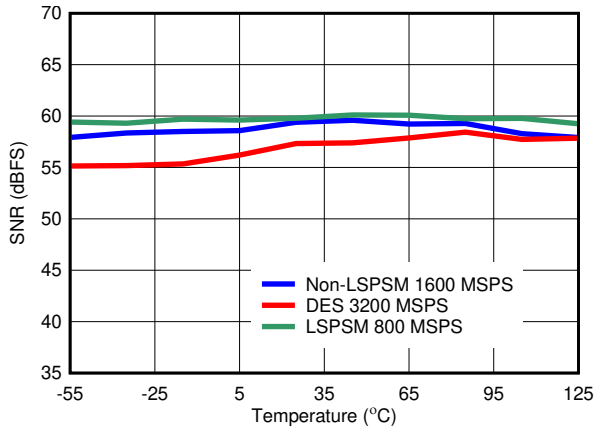


図 6-21. SNR vs Temperature

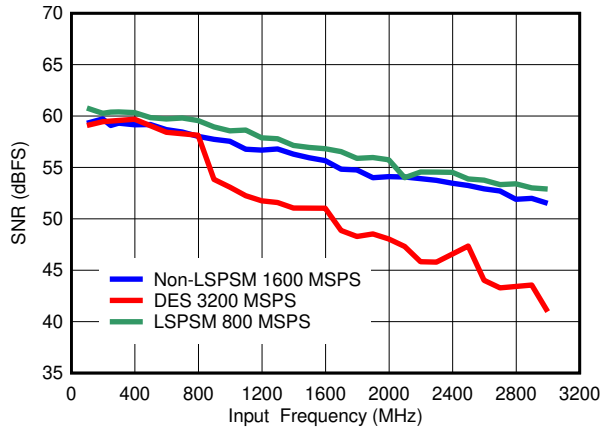


図 6-22. SNR vs Input Frequency

6.19 Typical Characteristics (continued)

V_A = V_{DR} = V_{TC} = V_E = 1.9 V, f_{CLK} = 1600 MHz in non-LSPSM and 800 MHz in LSPSM, f_{IN} = 248 MHz, T_A= 25°C, 1:2 demux non-DES mode, and calibration performed after temperature, supply voltage or sample rate change, unless otherwise stated.

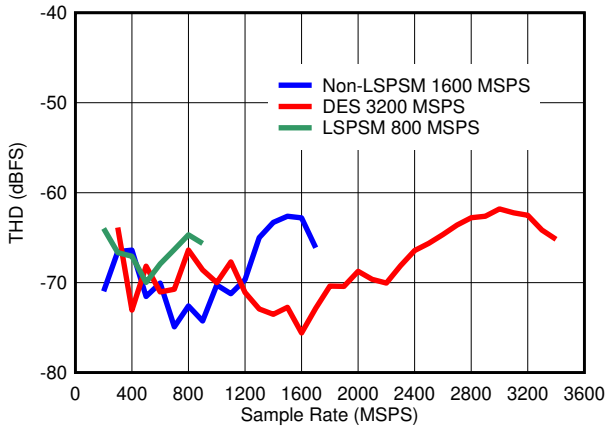


図 6-23. THD vs Sample Rate

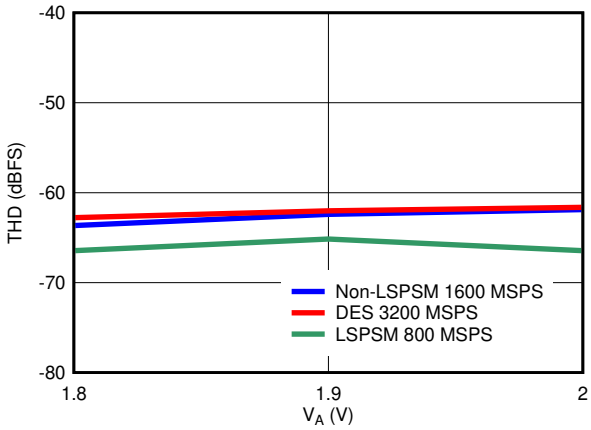


図 6-24. THD vs Supply Voltage

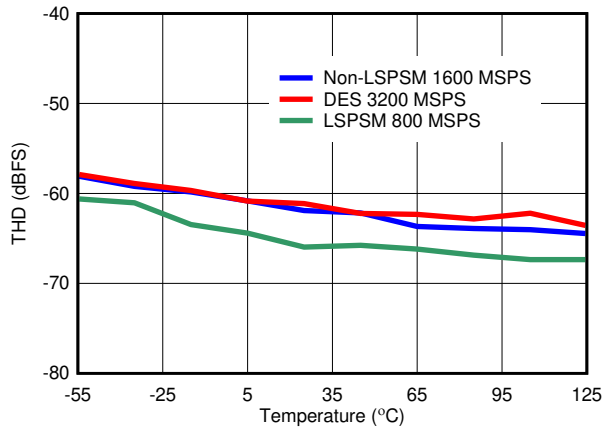


図 6-25. THD vs Temperature

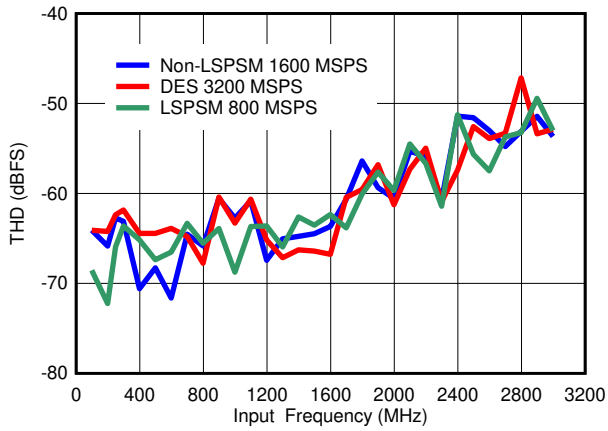


図 6-26. THD vs Input Frequency

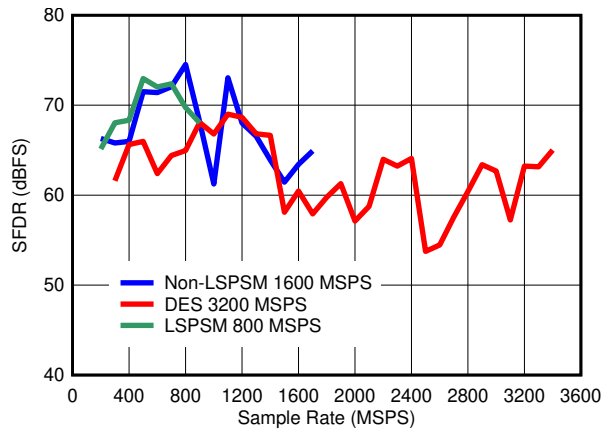


図 6-27. SFDR vs Sample Rate

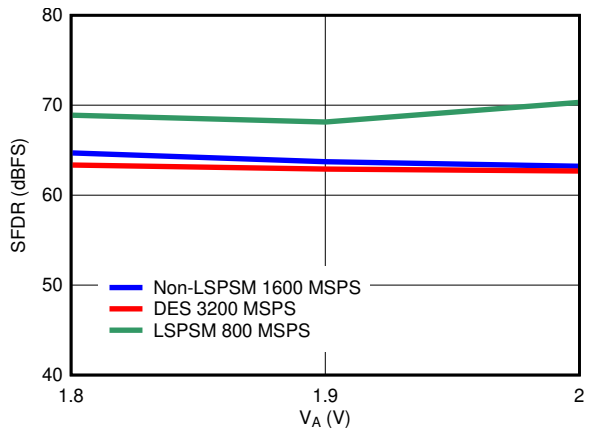


図 6-28. SFDR vs Supply Voltage

6.19 Typical Characteristics (continued)

V_A = V_{DR} = V_{TC} = V_E = 1.9 V, f_{CLK} = 1600 MHz in non-LSPSM and 800 MHz in LSPSM, f_{IN} = 248 MHz, T_A= 25°C, 1:2 demux non-DES mode, and calibration performed after temperature, supply voltage or sample rate change, unless otherwise stated.

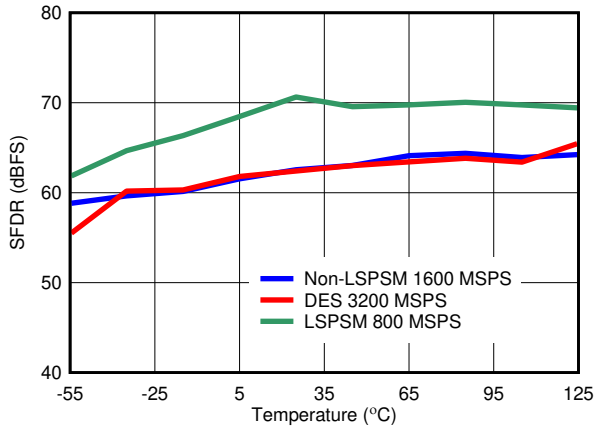


図 6-29. SFDR vs Temperature

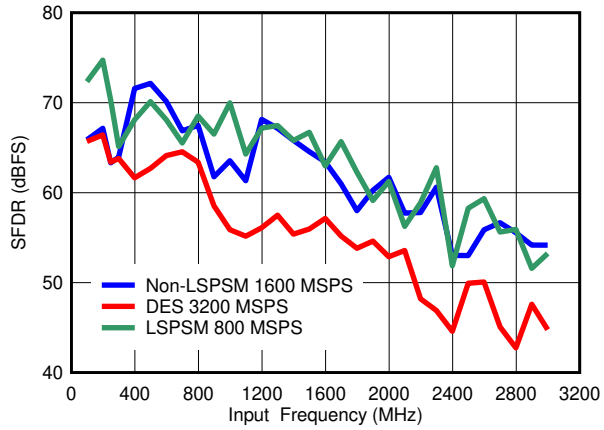
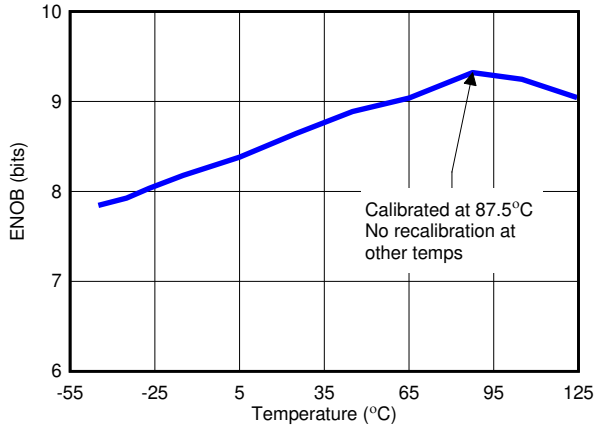
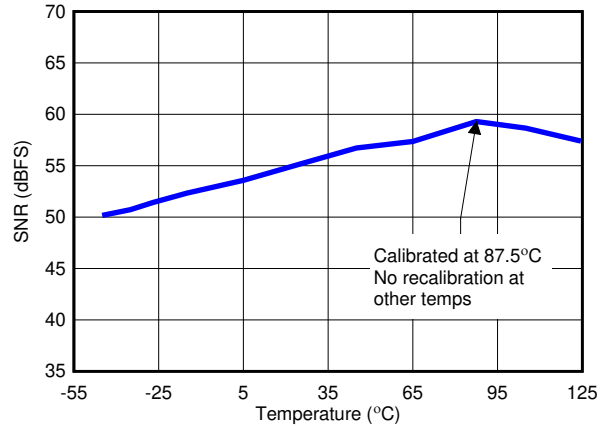


図 6-30. SFDR vs Input Frequency



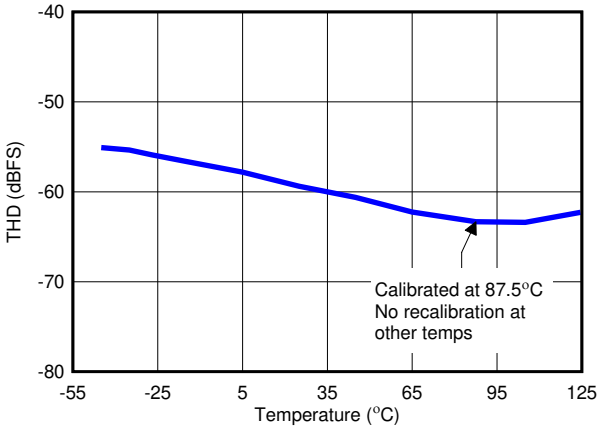
f_{CLK} = 1.6 GHz f_{IN} = 248 MHz

図 6-31. ENOB vs Temperature Calibration at 87.5°C Only



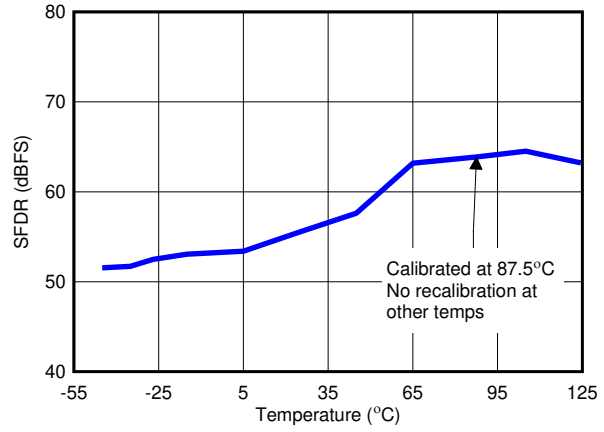
f_{CLK} = 1.6 GHz f_{IN} = 248 MHz

図 6-32. SNR vs Temperature Calibration at 87.5°C Only



f_{CLK} = 1.6 GHz f_{IN} = 248 MHz

図 6-33. THD vs Temperature Calibration at 87.5°C Only



f_{CLK} = 1.6 GHz f_{IN} = 248 MHz

図 6-34. SFDR vs Temperature Calibration at 87.5°C Only

6.19 Typical Characteristics (continued)

$V_A = V_{DR} = V_{TC} = V_E = 1.9$ V, $f_{CLK} = 1600$ MHz in non-LSPSM and 800 MHz in LSPSM, $f_{IN} = 248$ MHz, $T_A = 25°C$, 1:2 demux non-DES mode, and calibration performed after temperature, supply voltage or sample rate change, unless otherwise stated.

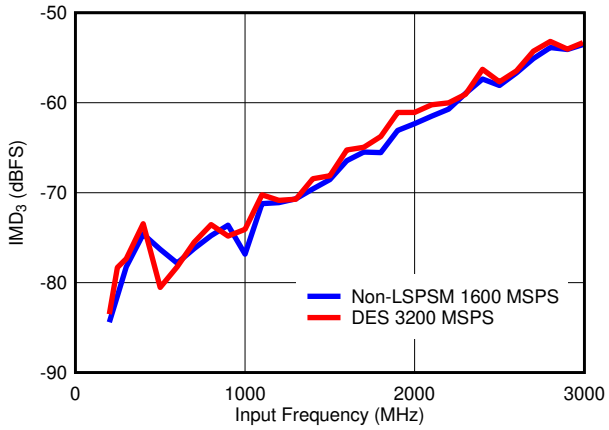


図 6-35. 3rd Order Intermodulation Distortion vs Input Frequency

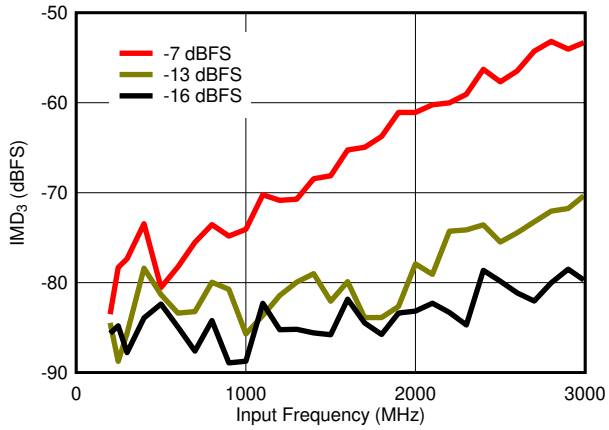


図 6-36. 3rd Order Intermodulation Distortion vs Input Frequency (DES Mode 3200 MSPS)

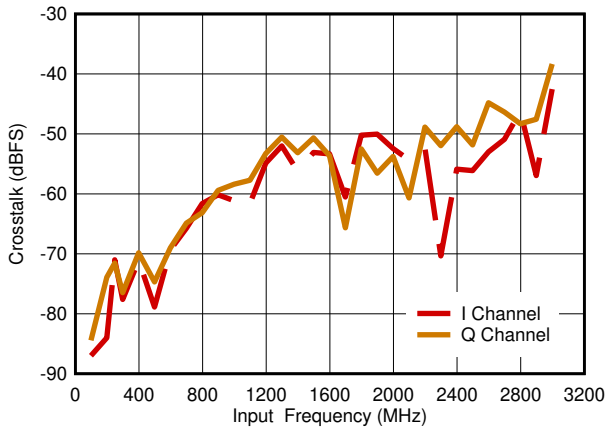


図 6-37. Cross Talk vs Input Frequency

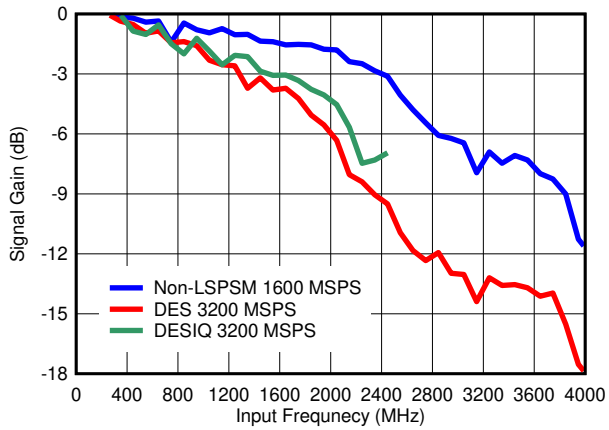


図 6-38. Insertion Loss vs Input Frequency

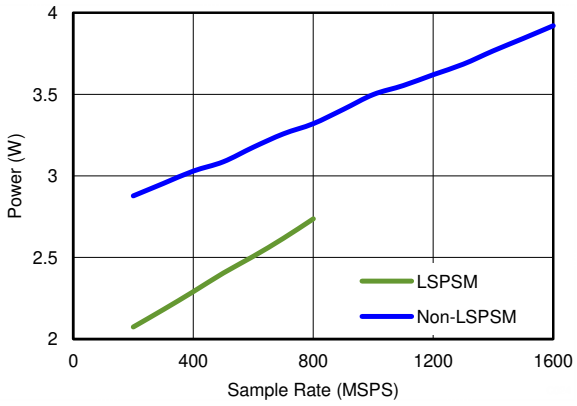


図 6-39. Power Consumption vs Sample Rate

7 Detailed Description

7.1 Overview

The ADC12D1620 device is a versatile analog-to-digital converter (ADC) with an innovative architecture, which permits very high-speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the *Application Information*. This section covers an overview, a description of control modes (extended control mode and non-extended control mode), and features.

The ADC12D1620 device uses a calibrated folding and interpolating architecture that achieves a high effective number of bits (ENOB). The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to correcting other non-idealities, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high-performance, low-power converter.

7.1.1 Operation Summary

A differential analog input is digitized into 12 bits. Differential input signals below the negative full-scale range cause the output word to be all zeroes. Differential inputs above the positive full-scale range results in the output word being all ones. If either case happens, the out-of-range output for the respective channel has a logic-high signal.

There are 4 major sampling modes:

1. Dual-channel ADC with a sampling range of 200 to 1600 MSPS.

2. Single channel, interleaved ADC in dual-edge sampling with a sampling range of 500 to 3200 MSPS.

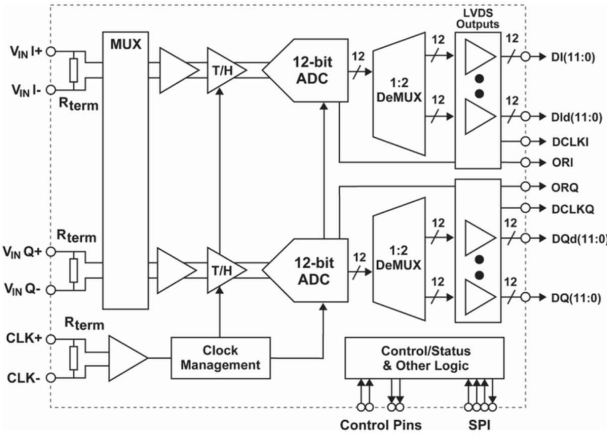
3. Dual-channel ADC in LSPSM with a sampling range of 200 to 800 MSPS.

4. Single channel, interleaved ADC in LSPSM and dual-edge sampling with a sampling range of 500 to 1600 MSPS.

The device has many operating options. Some of these options can be controlled through pin configurations in non-extended control mode (non-ECM or sometimes known as pin-control mode). An expanded feature set is available in extended control mode (ECM) through the serial interface.

Each channel has a selectable output demultiplexer that feeds two LVDS buses. Depending upon the sampling mode and the demux option chosen, the output data rate can be the same, one half, or one quarter the sample rate.

7.2 Functional Block Diagram



7.3 Feature Description

The ADC12D1620 offers many features to make the device convenient to use in a wide variety of applications. 表 7-1 is a summary of the features available, as well as details for the control mode chosen. *N/A* means *Not Applicable*.

表 7-1. Features and Modes

FEATURE	NON-ECM	CONTROL PIN ACTIVE IN ECM	ECM	DEFAULT ECM STATE
INPUT CONTROL AND ADJUST				
AC- and DC-coupled mode selection	Selected through V_{CMO} (Pin C2)	Yes	Not available	N/A
Input full-scale range adjust	Selected through FSR (Pin Y3)	No	Selected through the Configuration Register (Addr: 3**h** and B**h**)	Mid FSR value
Input offset adjust setting	Not available	N/A	Selected through the Configuration Register (Addr: 2**h** and A**h**)	Offset = 0 mV
Low-sampling power-saving mode	Selected through LSPSM (Pin V4)	Yes	Not available	N/A
DES / Non-DES mode selection	Selected through DES (Pin V5)	No	Selected through the DES bit (Addr: 0**h**; Bit: 7)	Non-DES mode
DES mode input selection	Not available	N/A	Selected through the DEQ, DIQ bits (Addr: 0**h**; Bits: 6:5)	N/A
DESCLKIQ mode	Not available	N/A	Selected through the DCK bit (Addr: E**h**; Bit: 6)	N/A
DES timing adjust	Not available	N/A	Selected through the DES Timing Adjust Reg (Addr: 7**h**)	Mid skew offset
Sampling clock phase adjust	Not available	N/A	Selected through the Configuration Register (Addr: C**h** and D**h**)	t_{AD} adjust disabled
OUTPUT CONTROL AND ADJUST				
DDR clock phase selection	Selected through DDRPh (Pin W4)	No	Selected through the DPS bit (Addr: 0**h**; Bit: 14)	0° mode
DDR / SDR DCLK selection	Not available	N/A	Selected through the SDR bit (Addr: 0**h**; Bit: 2)	DDR mode
SDR rising / falling DCLK Selection	Not available	N/A	Selected through the DPS bit (Addr: 0**h**; Bit: 14)	N/A
LVDS differential voltage amplitude selection	Higher amplitude only	N/A	Selected through the OVS bit (Addr: 0**h**; Bit: 13)	Higher amplitude
LVDS common-mode voltage amplitude selection	Selected through V_{BG} (Pin B1)	Yes	Not available	N/A
Output formatting selection	Offset binary only	N/A	Selected through the 2SC bit (Addr: 0**h**; Bit: 4)	Offset binary
Test pattern mode at output	Selected through TPM (Pin A4)	No	Selected through the TPM bit (Addr: 0**h**; Bit: 12)	TPM disabled
Demux/Non-demux mode selection	Selected through NDM (Pin A5)	Yes	Not available	N/A
AutoSync	Not available	N/A	Selected through the Configuration Register (Addr: E**h**)	primary mode, RCOut1, RCOut2 disabled
DCLK reset	Not available	N/A	Selected through the Configuration Register (Addr: E**h**; Bit: 0)	DCLK reset disabled

表 7-1. Features and Modes (continued)

FEATURE	NON-ECM	CONTROL PIN ACTIVE IN ECM	ECM	DEFAULT ECM STATE
Time stamp	Not available	N/A	Selected through the TSE bit (Addr: 0**h**; Bit: 3)	Time stamp disabled
CALIBRATION				
On-command calibration	Selected through CAL (Pin D6)	Yes	Selected through the CAL bit (Addr: 0**h**; Bit: 15)	N/A (CAL = 0)
Calibration Adjust	Not available	N/A	Selected through the Configuration Register (Addr: 4**h**)	t_{CAL}
Read/Write calibration settings	Not available	N/A	Selected through the SSC bit (Addr: 4**h**; Bit: 7)	R/W calibration values disabled
POWER-DOWN				
Power down I channel	Selected through PDI (Pin U3)	Yes	Selected through the PDI bit (Addr: 0**h**; Bit: 11)	I-channel operational
Power down Q channel	Selected through PDQ (Pin V3)	Yes	Selected through the PDQ bit (Addr: 0**h**; Bit: 10)	Q-channel operational

7.3.1 Input Control and Adjust

There are several features and configurations for the input of the ADC12D1620 device that enable it to be used in many different applications. AC- and DC-coupled modes, input full-scale range adjust, input offset adjust, LSPSM, DES/non-DES modes, and sampling clock phase adjust are discussed in the following sections.

7.3.1.1 AC- and DC-Coupled Modes

The analog inputs may be AC- or DC-coupled. See *AC- or DC-Coupled Mode Pin (VCMO)* for information on how to select the desired mode. For applications information, see *DC-Coupled Input Signals* and *AC-Coupled Input Signals*.

7.3.1.2 Input Full-Scale Range Adjust

The input full-scale range for the ADC12D1620 may be adjusted through non-ECM or ECM. In non-ECM, a control pin selects a higher or lower value; see *Full-Scale Input-Range Pin (FSR)*. In ECM, the full-scale input range of the I- and Q-channel inputs may be independently set with 15 bits precision through the I- and Q-channel Full-Scale Range Adjust Registers (Addr: 3**h** and Addr: B**h**, respectively). See V_{IN_FSR} in *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics* for electrical specification details. Note that the higher and lower full-scale input range settings in non-ECM correspond to the middle and minimum full-scale input range settings in ECM. An on-command calibration must be executed following a change of the input full-scale range. See 表 7-16 and 表 7-24 for information about the registers.

7.3.1.3 Input Offset Adjust

The input offset adjust for the ADC12D1620 may be adjusted in ECM with 12 bits precision plus sign through the I- and Q-channel Offset Adjust Registers (Addr: 2**h** and Addr: A**h**, respectively). See *表 7-15* and *表 7-23* for information about the registers.

7.3.1.4 Low-Sampling Power-Saving Mode (LSPSM)

For applications with input clock speeds 200 to 800 MHz, the ADC12D1620 device can be switched to the LSPSM for a reduction in power consumption of approximately 20%. See *Low-Sampling Power-Saving Mode Pin (LSPSM)* for information on how to select the desired mode and details on operation in this mode.

7.3.1.5 DES Timing Adjust

The performance of the ADC12D1620 in DES mode depends on how well the two channels are interleaved (that is, that the clock samples either channel with precisely a 50% duty-cycle); each channel has the same offset (nominally code 2047/2048), and each channel has the same full-scale range. The ADC12D1620 device includes an automatic clock phase background adjustment in DES mode to automatically and continuously

adjust the clock phase of the I and Q channels. In addition to this, the residual fixed timing skew offset may be further manually adjusted, and further reduce timing spurs for specific applications. See DES Timing Adjust (Addr: 7**h**). As the DES timing adjust is programmed from 0**d** to 127**d**, the magnitude of the Fs/2-Fin timing interleaving spur decreases to a local minimum and then increases again. The default, nominal setting of 64**d** may or may not coincide with this local minimum. The user may manually skew the global timing to achieve the lowest possible timing interleaving spur.

7.3.1.6 Sampling Clock Phase Adjust

The sampling clock (CLK) phase may be delayed internally to the ADC up to 825 ps in ECM. This feature helps the system designer remove small imbalances in clock distribution traces at the board level when multiple ADCs are used, or to simplify complex system functions such as beam steering for phase-array antennas.

Additional delay in the clock path also creates additional jitter when using the sampling clock phase adjust. Because the sampling clock phase adjust delays all clocks, including the DCLKs and output data, the user is strongly advised to use the minimal amount of adjustment and verify the net benefit of this feature in their system before relying on it.

7.3.2 Output Control and Adjust

There are several features and configurations for the ADC12D1620 output that make the device ideal for many different applications. This section covers DDR clock phase, LVDS output differential and common-mode voltage, output formatting, test pattern mode, and time stamp.

7.3.2.1 SDR / DDR Clock

The ADC12D1620 output data can be delivered in double data rate (DDR) or single data rate (SDR). For DDR, the DCLK frequency is half the data rate, and data is sent to the outputs on both edges of DCLK; see 図 7-1. The DCLK-to-data phase relationship may be either 0° or 90°. For 0° mode, the data transitions on each edge of the DCLK. Any offset from this timing is t_{OSK}; (see *Converter Electrical Characteristics: AC Electrical Characteristics* for details). For 90° mode, the DCLK transitions in the middle of each data cell. Setup and hold times for this transition, t_{SU} and t_H, may also be found in *Converter Electrical Characteristics: AC Electrical Characteristics*. The DCLK-to-data phase relationship may be selected through the DDRPh pin in non-ECM (see *Dual Data-Rate Phase Pin (DDRPh)*) or the DPS bit in the Configuration Register (Addr: 0**h**; Bit: 14) in ECM. Note that for DDR mode, the 1:2 demux mode is not available in LSPSM.

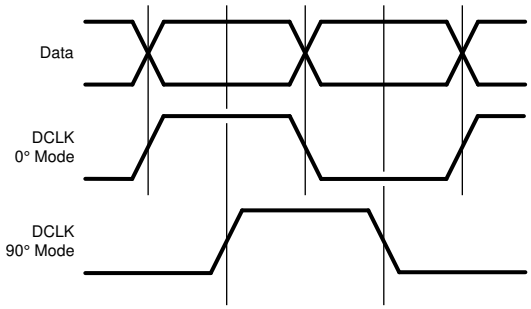


図 7-1. DDR DCLK-to-Data Phase Relationship

For SDR, the DCLK frequency is the same as the data rate, and data is sent to the outputs on a single edge of DCLK; see 図 7-2. The data may transition on either the rising or falling edge of DCLK. Any offset from this timing is t_{OSK}; see *Converter Electrical Characteristics: AC Electrical Characteristics* for details. The DCLK rising or falling edge may be selected through the SDR bit in the Configuration Register (Addr: 0**h**; Bit: 2) in ECM only.

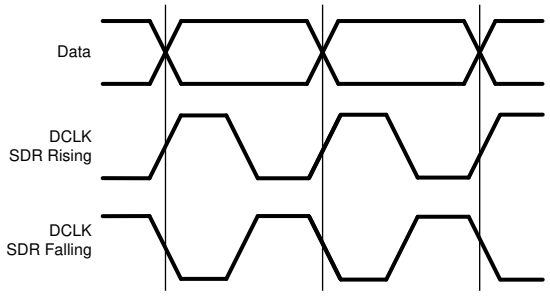


図 7-2. SDR DCLK-to-Data Phase Relationship

7.3.2.2 LVDS Output Differential Voltage

The ADC12D1620 device is available with a selectable higher or lower LVDS output differential voltage. This parameter is V_{OD}, found in *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics*. The desired voltage may be selected through the OVS bit in the Configuration Register (Addr: 0**h**, Bit: 13). For many applications, such as when the LVDS outputs are very close to an FPGA on the same board, the lower setting is sufficient for good performance; this also reduces the possibility for EMI from the LVDS outputs to other signals on the board. See *Configuration Register 1* for more information.

7.3.2.3 LVDS Output Common-Mode Voltage

The ADC12D1620 is available with a selectable higher or lower LVDS output common-mode voltage. This parameter is V_{OS}, found in *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics*. See *LVDS Output Common-Mode Pin (VBG)* for information on how to select the desired voltage.

7.3.2.4 Output Formatting

The formatting at the digital data outputs may be either offset binary or two's complement. The default formatting is offset binary, but two's complement may be selected through the 2SC bit of the Configuration Register (Addr: 0**h**; Bit: 4); see *Configuration Register 1* for more information.

7.3.2.5 Test-Pattern Mode

The ADC12D1620 can provide a test pattern at the four output buses, independent of the input signal, that aids in system debug. In test-pattern mode, the ADC is disengaged, and a test pattern generator is connected to the outputs, including ORI and ORQ. The test pattern output is the same in DES mode or non-DES mode. Each port is given a unique 12-bit word, alternating between 1's and 0's. When the device is programmed into the demux mode, the order of the test pattern is described in 表 7-2. If the I or Q channel is powered down, the test pattern is not output for that channel.

表 7-2. Test Pattern by Output Port in Non-LSPSM Demux Mode

TIME	Qd	Id	Q	I	ORQ	ORI	COMMENTS
T0	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	Pattern Sequence **n**
T1	FFF**h**	FFB**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T2	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	
T3	FFF**h**	FFB**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T4	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	
T5	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	Pattern Sequence **n+1**
T6	FFF**h**	FFB**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T7	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	
T8	FFF**h**	FFB**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T9	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	

表 7-2. Test Pattern by Output Port in Non-LSPSM Demux Mode (continued)

TIME	Qd	Id	Q	I	ORQ	ORI	COMMENTS
T10	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	Pattern Sequence **n+2**
T11	FFF**h**	FFB**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T12	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	
T13	...	...	...	...	...	...	

When the device is programmed into the non-demux mode, the test pattern's order is described in 表 7-3.

表 7-3. Test Pattern by Output Port in Non-LSPSM Non-Demux Mode

TIME	Q	I	ORQ	ORI	COMMENTS
T0	000**h**	004**h**	0**b**	0**b**	Pattern Sequence **n**
T1	000**h**	004**h**	0**b**	0**b**	
T2	FFF**h**	FFB**h**	1**b**	1**b**	
T3	FFF**h**	FFB**h**	1**b**	1**b**	
T4	000**h**	004**h**	0**b**	0**b**	
T5	FFF**h**	FFB**h**	1**b**	1**b**	
T6	000**h**	004**h**	0**b**	0**b**	
T7	FFF**h**	FFB**h**	1**b**	1**b**	
T8	FFF**h**	FFB**h**	1**b**	1**b**	
T9	FFF**h**	FFB**h**	1**b**	1**b**	
T10	000**h**	004**h**	0**b**	0**b**	Pattern Sequence **n+1**
T11	000**h**	004**h**	0**b**	0**b**	
T12	FFF**h**	FFB**h**	1**b**	1**b**	
T13	FFF**h**	FFB**h**	1**b**	1**b**	
T14	...	...	...	...	

表 7-4. Test Pattern by Output Port in LSPSM Demux Mode

TIME	Qd	Id	Q	I	ORQ	ORI	COMMENTS
T0	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	Pattern sequence **n**
T1	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	
T2	008**h**	010**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T3	008**h**	010**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T4	008**h**	010**h**	008**h**	010**h**	0**b**	0**b**	
T5	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	Pattern sequence **n+1**
T6	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	
T7	008**h**	010**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T8	008**h**	010**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T9	008**h**	010**h**	008**h**	010**h**	0**b**	0**b**	
T10	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	Pattern sequence **n+2**
T11	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	
T12	008**h**	010**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T13	...	...	...	...	...	...	

表 7-5. Test Pattern by Output Port in LSPSM Non-Demux Mode

TIME	Q	I	ORQ	ORI	COMMENTS
T0	008**h**	010**h**	0**b**	0**b**	Pattern sequence **n**
T1	FF7**h**	FEF**h**	1**b**	1**b**	
T2	008**h**	010**h**	0**b**	0**b**	
T3	FF7**h**	FEF**h**	1**b**	1**b**	
T4	008**h**	010**h**	0**b**	0**b**	
T5	008**h**	010**h**	0**b**	0**b**	Pattern sequence **n+1**
T6	FF7**h**	FEF**h**	1**b**	1**b**	
T7	008**h**	010**h**	0**b**	0**b**	
T8	FF7**h**	FEF**h**	1**b**	1**b**	
T9	008**h**	010**h**	0**b**	0**b**	
T10	008**h**	010**h**	0**b**	0**b**	Pattern sequence **n+2**
T11	FF7**h**	FEF**h**	1**b**	1**b**	
T12	008**h**	010**h**	0**b**	0**b**	
T13	FF7**h**	FEF**h**	1**b**	1**b**	
T14	...	...	...	...	

7.3.2.6 Time Stamp

The time-stamp feature enables the user to capture the timing of an external trigger event, relative to the sampled signal. When enabled through the TSE bit of the Configuration Register (Addr: 0**h**; Bit: 3), the LSB of the digital outputs (DQd, DQ, DId, DI) captures the trigger information. In effect, the 12-bit converter becomes an 11-bit converter, and the LSB acts as a 1-bit converter with the same latency as the 11-bit converter. Apply the trigger to the DCLK_RST input. It may be asynchronous to the ADC sampling clock.

7.3.3 Calibration Feature

The ADC12D1620 calibration must be run to achieve specified performance. The calibration procedure is exactly the same regardless of how it was initiated or when it is run. Calibration trims the analog input differential termination resistors, the CLK input resistor, and sets internal bias currents that affect the linearity of the converter. This minimizes full-scale error, offset error, DNL and INL, which results in the maximum dynamic performance, as measured by the SNR, THD, SINAD (SNDR), and ENOB pins.

7.3.3.1 Calibration Control Pins and Bits

表 7-6 is a summary of the pins and bits used for calibration. See *Pin Configuration and Functions* for complete pin information and 図 6-8 for the timing diagram.

表 7-6. Calibration Pins

PIN (Bit)	NAME	FUNCTION
D6 (Addr: 0**h**; Bit: 15)	CAL (Calibration)	Initiate calibration; see *セクション 7.5.1.1.4*
(Addr: 4**h**)	Calibration Adjust	Adjust calibration sequence
B5	CalRun (Calibration Running)	Indicates while calibration is running
C1/D2	Rtrim+, Rtrim– (Input termination trim resistor)	External resistor used to calibrate analog and CLK inputs
C3/D3	Rext+, Rext– (External Reference resistor)	External resistor used to calibrate internal linearity

7.3.3.2 How to Execute a Calibration

Calibration may be initiated by holding the CAL pin low for at least t_{CAL_L} clock cycles, then holding it high for at least t_{CAL_H} clock cycles, as defined in *Timing Requirements: Calibration*. The minimum t_{CAL_L} and t_{CAL_H} input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. The time taken by the calibration procedure is specified as t_{CAL}. The CAL pin is active in both ECM and non-ECM. However, in ECM, the CAL pin is logically OR'd with the CAL bit, so both the pin and bit must be set low before executing another calibration with either pin or bit.

TI recommends holding the CAL pin high during normal usage of the ADC12D1620 device to reduce the chance that an SEU causes a calibration cycle.

7.3.3.3 On-Command Calibration

In addition to executing a calibration after power-on and device stabilization, in order to obtain optimal parametric performance TI recommends execution of an on-command calibration whenever the settings or conditions to the device are significantly altered. Some examples include: changing the FSR through either ECM or Non-ECM, power-cycling either channel, and switching into or out of DES mode. For best performance, it is also recommended that an on-command calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly relative to the specific system performance requirements. See 図 *6-31* for the impact temperature change can have on the performance of the device without re-calibration.

Due to the nature of the calibration feature, TI recommends avoiding unnecessary activities on the device while the calibration is taking place. For example, do not read or write to the serial interface or use the DCLK reset feature while calibrating the ADC; doing so impairs the performance of the device until it is re-calibrated correctly. Also, TI recommends not to apply a strong narrow-band signal to the analog inputs during calibration because this may impair the accuracy of the calibration; broad spectrum noise is acceptable.

7.3.3.4 Calibration Adjust

The sequence of the calibration event itself may be adjusted. This feature can be used if a shorter calibration time than the default is required; see t_{CAL} in *Converter Electrical Characteristics: AC Electrical Characteristics*. However, the performance of the device may be compromised when using this feature.

The calibration sequence may be adjusted through the CSS bit of the Calibration Adjust register (Addr: 4**h**; Bit: 14). The default setting of CSS = 1**b** executes both R_{IN} and R_{IN_CLK} calibration (using Rtrim) and internal linearity calibration (using Rext). Executing a calibration with CSS = 0**b** executes only the internal linearity calibration. The first time that calibration is executed, it must be with CSS = 1**b** to trim R_{IN} and R_{IN_CLK}. However, once the device is at its operating temperature, and R_{IN} has been trimmed at least one time, it does not drift significantly.

7.3.3.4.1 Read/Write Calibration Settings

When the ADC performs a calibration, the calibration constants are stored in an array which is accessible through the Calibration Values register (Addr: 5**h**). To save the time it takes to execute a calibration, t_{CAL}, or to allow re-use of a previous calibration result, these values can be read from and written to the register at a later time. For example, if an application requires the same input impedance, R_{IN}, this feature can be used to load a previously determined set of values. For the calibration values to be valid, the ADC must be operating under the same conditions, including temperature, at which the calibration values were originally determined by the ADC.

To read calibration values from the SPI, do the following:

1. Set ADC to desired operating conditions.
2. Set the SSC bit (Addr: 4**h**; Bit: 7) to 1.
3. Read exactly 240 times the Calibration Values register (Addr: 5**h**). The register values are R0, R1, R2... R239 where R0 is a dummy value. The contents of R<239:1> should be stored.
4. Set the SSC bit (Addr: 4**h**; Bit: 7) to 0.
5. Continue with normal operation.

To write calibration values to the SPI, do the following:

1. Set ADC to operating conditions at which Calibration Values were previously read.
2. Set the SSC bit (Addr: 4**h**; Bit: 7) to 1.
3. Write exactly 239 times the Calibration Values register (Addr: 5**h**). The registers should be written with stored register values R1, R2... R239.
4. Make two additional dummy writes of 0000**h**.
5. Set the SSC bit (Addr: 4**h**; Bit: 7) to 0.
6. Continue with normal operation.

7.3.3.5 Calibration and Power-Down

If PDI and PDQ are simultaneously asserted during a calibration cycle, the ADC12D1620 device immediately powers down. The calibration cycle continues when either or both channels are powered back up, but the calibration is compromised due to the incomplete settling of bias currents directly after power up. Therefore, a new calibration must be executed upon powering the ADC12D1620 back up. In general, the ADC12D1620 must be re-calibrated when either or both channels are powered back up, or after one channel is powered down. For best results, this must be done after the device has stabilized to its operating temperature.

7.3.3.6 Calibration and the Digital Outputs

During calibration, the digital outputs (including DI, DId, DQ, DQd and OR) are set logic-low, to reduce noise. The DCLK runs continuously during calibration. After the calibration is completed and the CalRun signal is logic-low, it takes an additional 60 sampling clock cycles before the output of the ADC12D1620 is valid converted data from the analog inputs. This is the time it takes for the pipeline to flush, as well as for other internal processes.

7.3.4 Power Down

On the ADC12D1620, the I and Q channels may be powered down individually. This may be accomplished through the control pins, PDI and PDQ, or through ECM. In ECM, the PDI and PDQ pins are logically OR'd with the PDI and PDQ bits of the Control Register (Addr: 0**h**; Bits: 11:10). See *Power-Down I-Channel Pin (PDI)* and *Power-Down Q-Channel Pin (PDQ)* for more information.

7.3.5 Low-Sampling Power-Saving Mode (LSPSM)

For applications with input clock speeds of 200 to 800 MHz (sample rates of 200 to 800 MSPS in non-DES mode), the ADC may be put in LSPSM using the LSPSM (V4) pin (see セクション *7.5.1.1.5*). LSPSM powers down certain areas of the device, reduces the power consumption by approximately 20%, and may improve the spectral purity of the output. In 1:2 demux mode, the output is in SDR, and the DLCK frequency will be Fs/2 . In non-demux mode, the output is switchable between DDR and SDR; see 表 7-8 for the DCLK frequencies for each mode and output combination.

7.4 Device Functional Modes

7.4.1 DES/Non-DES Mode

The ADC12D1620 device can operate in dual-edge sampling (DES) or non-DES mode. In non-DES mode, inputs are sampled at the sampling clock frequency. Depending on whether channels are powered down, one or two inputs may be sampled. The DES mode enables a single analog input to be sampled by both I and Q channels. One channel samples the input on the rising edge of the sampling clock and the other samples the input signal on the falling edge of the sampling clock. A single input is thus sampled twice per clock cycle, resulting in an overall sample rate of twice the sampling clock frequency. Because DES mode uses both I and Q channels to process the input signal, both channels must be powered up for the DES mode to function properly.

See *Dual-Edge Sampling Pin (DES)* for information on how to select the DES mode. In non-ECM only the I input may be used for the DES mode input. In ECM, either the I or Q input may be selected by first using the DES bit (Addr: 0h; Bit: 7) to select the DES mode. Setting the DEQ bit (Addr: 0h; Bit: 6) selects the Q input, while leaving the default value of DEQ=0 selects the I input.

Two other DES modes are available. These provide improved input bandwidth compared to DESI and DESQ modes, but require driving the I and Q inputs with identical in-phase signals.

The DESIQ mode is selected by setting the DIQ bit (Addr: 0h; Bit: 5). In this mode the I and Q input signals are connected to the I and Q converter channels and also connected to each other internally to enable better I to Q signal matching compared with the DESCLKIQ mode discussed next.

DESCLKIQ mode is similar to the DESIQ mode, except that the I and Q channels remain electrically separate internal to the ADC12D1620. For this reason, the I to Q signal matching is slightly worse, and spurious performance is degraded compared to DESIQ mode. DESCLKIQ input bandwidth is slightly better than the DESIQ bandwidth. The DCK bit (Addr: Eh; Bit: 6) is used to select the 180° sampling-clock mode.

表 7-7 summarizes the relative bandwidth and SFDR performance of the DES sampling modes:

表 7-7. DES Mode Comparison

DES MODE	INPUTS DRIVEN	INPUT BANDWIDTH	SFDR PERFORMANCE
DESI, DESQ	I or Q	Lowest	Highest
DESIQ	I and Q	Mid	Mid
DESCLKIQ	I and Q	Highest	Lowest

In the DES mode, the output data must be carefully interleaved in order to reconstruct the sampled signal. If the device is programmed into the 1:4 demux DES mode, the data is effectively demultiplexed by 1:4. If the sampling clock is 1600 MHz, the effective sampling rate is doubled to 3.2 GSPS, and each of the 4 output buses has an output rate of 800 MSPS. All data is available in parallel. To properly reconstruct the sampled waveform, the four words of parallel data that are output with each DCLK must be correctly interleaved. The sampling order is as follows, from the earliest to the latest: DQd, DId, DQ, DI (see 図 6-3). If the device is programmed into the nondemux DES mode, two words of parallel data are output with each edge of the DCLK in the following sampling order, from the earliest to the latest: DQ, DI (see 図 6-4).

7.4.2 Demux/Non-Demux Mode

The ADC12D1620 device may be in one of two demultiplex modes: demux mode or non-demux mode (also sometimes referred to as 1:1 demux mode). In non-demux mode, the data from the input is simply output at the sampling rate on one 12-bit bus. In demux mode, the data from the input is output at half the sampling rate, on twice the number of buses. Demux/non-demux mode may only be selected by the NDM pin. In non-DES mode, the output data from each channel may be demultiplexed by a factor of 1:2 (1:2 demux Non-DES mode) or not demultiplexed (non-demux non-DES mode). In DES mode, the output data from both channels interleaved may be demultiplexed (1:4 demux DES mode) or not demultiplexed (non-demux DES mode).

See 表 7-8 for a selection of available modes.

表 7-8. Supported Demux, Data Rate Modes

	OUTPUT	MODE	DCLK	RCOUT
NON-LSPSM, NON-DES MODE				
1:2 demux	DDR	0° mode / 90° mode	$F_{CLK}/4$	$F_{CLK}/4$
	SDR	Rising / Falling mode	$F_{CLK}/2$	
1:1 demux	DDR	0° mode only	$F_{CLK}/2$	
	SDR	Not available	N/A	N/A
LSPSM, NON-DES MODE				
1:2 demux	DDR	Not available	N/A	N/A
	SDR	Rising / Falling mode	$F_{CLK}/2$	$F_{CLK}/2$
1:1 demux	DDR	0° mode only	$F_{CLK}/2$	
	SDR	Rising mode only	F_{CLK}	
NON-LSPSM, DES MODE				
1:4 demux	DDR	0° mode / 90° mode	$F_{CLK}/4$	$F_{CLK}/4$
	SDR	Rising / Falling mode	$F_{CLK}/2$	
1:1 demux	DDR	0° mode only	$F_{CLK}/2$	
	SDR	Not Available	N/A	N/A
LSPSM, DES MODE				
1:4 demux	DDR	Not Available	N/A	N/A
	SDR	Rising mode only	$F_{CLK}/2$	$F_{CLK}/2$
1:1 demux	DDR	0° mode / 90° mode	$F_{CLK}/2$	
	SDR	Rising mode only	F_{CLK}	

7.5 Programming

7.5.1 Control Modes

The ADC12D1620 may be operated in one of two control modes: non-extended-control mode (non-ECM) or extended-control mode (ECM). In the simpler non-ECM (also sometimes referred to as pin-control mode), the user affects available configuration and control of the device through the control pins. The ECM provides additional configuration and control options through a serial interface and a set of 16 registers, most of which are available to the user.

7.5.1.1 Non-ECM

In non-ECM, the serial interface is not active, and all available functions are controlled through various pin settings. Non-ECM is selected by setting the $\overline{ECE}$ pin to logic-high. Note that for the control pins, *logic-high* and *logic-low* refer to V_A and GND, respectively. Nine dedicated control pins provide a wide range of control for the ADC12D1620 and facilitate its operation. These control pins provide DES mode selection, demux-mode selection, DDR-phase selection, execute calibration, power down I channel, power down Q channel, test-pattern-mode selection, and full-scale input-range selection. In addition to this, two dual-purpose control pins provide for AC- or DC-coupled mode selection and LVDS output common-mode voltage selection. See 表 7-9 for a summary.

表 7-9. Non-ECM Pin Summary

PIN NAME		LOGIC LOW	LOGIC HIGH	FLOATING
DEDICATED CONTROL PINS				
DES		Non-DES mode	DES mode	Not valid
NDM		Demux mode	Non-demux mode	Not valid
DDRPh	DDR	0° mode	90° mode	Not valid
	SDR	Rising edge	Falling edge	
CAL		See *Calibration Pin (CAL)*		Not valid
LPSSM		Non-LSPSM	LSPSM	Not valid
PDI		I-channel active	Power down I-channel	Power down I-channel
PDQ		Q-channel active	Power down Q-channel	Power down Q-channel
TPM		Non-test pattern mode	Test pattern mode	Not valid
FSR		Lower FS input range	Higher FS input range	Not valid
DUAL-PURPOSE CONTROL PINS				
V_{CMO}		AC-coupled operation	Not allowed	DC-coupled operation
V_{BG}		Not allowed	Higher LVDS common-mode voltage	Lower LVDS common-mode voltage

7.5.1.1.1 Dual-Edge Sampling Pin (DES)

The dual-edge sampling (DES) pin selects whether the ADC12D1620 is in DES mode (logic-high) or non-DES mode (logic-low). DES mode means that a single analog input is sampled by both I and Q channels in a time-interleaved manner. One of the ADCs samples the input signal on the rising sampling clock edge (duty cycle corrected); the other ADC samples the input signal on the falling sampling clock edge (duty cycle corrected). In non-ECM, only the I input may be used for DES mode, also known as DESI mode. In ECM, the Q input may be selected through the DEQ bit of the Configuration Register (Addr: 0**h**; Bit: 6), also known as DESQ mode. In ECM, both the I and Q inputs may be selected, also known as DESIQ or DESCLKIQ mode.

To use this feature in ECM, use the DES bit in the Configuration Register (Addr: 0**h**; Bit: 7). See *DES/Non-DES Mode* for more information.

7.5.1.1.2 Non-Demultiplexed Mode Pin (NDM)

The non-demultiplexed mode (NDM) pin selects whether the ADC12D1620 is in demux mode (logic-low) or non-demux mode (logic-high). In non-demux mode, the data from the input is produced at the sampled rate at a single 12-bit output bus. In demux mode, the data from the input is produced at half the sampled rate and at twice the number of output buses. For non-DES mode, each I or Q channel produces its data on one or two buses for non-demux or demux mode, respectively. For DES mode, the selected channel produces its data on two or four buses for non-demux or demux mode, respectively.

This feature is pin-controlled only and remains active during both non-ECM and ECM. See *Demux/Non-Demux Mode* for more information.

7.5.1.1.3 Dual Data-Rate Phase Pin (DDRPh)

The dual data-rate phase (DDRPh) pin selects whether the ADC12D1620 is in 0° mode (logic-low) or 90° mode (logic-high) for DDR mode. For DDR mode, the data may transition either with the DCLK transition (0° mode) or halfway between DCLK transitions (90° mode). If the device is in SDR mode, the DDRPh pin selects whether the data transitions on the rising edge of DCLK (logic-low) or the falling edge of DCLK (logic-high). The DDRPh pin selects the mode for both the I channel: DI- and DId-to-DCLKI phase relationship and for the Q channel: DQ- and DQd-to-DCLKQ phase relationship.

To use this feature in ECM, use the DPS bit in the Configuration Register (Addr: 0**h**; Bit: 14). See *SDR / DDR Clock* for more information.

7.5.1.1.4 Calibration Pin (CAL)

The calibration (CAL) pin may be used to execute an on-command calibration. The effect of calibration is to maximize the dynamic performance. To initiate an on-command calibration through the CAL pin, bring the CAL pin high for a minimum of t_{CAL_H} input clock cycles after it has been low for a minimum of t_{CAL_L} input clock cycles (see *Converter Electrical Characteristics: AC Electrical Characteristics* clock cycle specification). TI recommends holding the CAL pin high during normal usage of the ADC12D1620 device to reduce the chance that an SEU causes a calibration cycle. In ECM, this pin remains active and is logically OR'd with the CAL bit.

To use this feature in ECM, use the CAL bit in the Configuration Register (Addr: 0**h**; Bit: 15). See *Calibration Feature* for more information.

7.5.1.1.5 Low-Sampling Power-Saving Mode Pin (LSPSM)

The LSPSM pin selects whether the device is in non-LSPSM (logic-low) or LSPSM (logic-high). In LSPSM, the input clock is limited to 800 MHz, and the sample rate in non-DES mode is limited to 800 MSPS.

The LSPSM pin remains active in ECM. See *Low-Sampling Power-Saving Mode (LSPSM)* for more details.

7.5.1.1.6 Power-Down I-Channel Pin (PDI)

The power-down I-channel (PDI) pin selects whether the I channel is powered down (logic-high) or active (logic-low). The digital data output pins, DI and DId, (both positive and negative) are put into a high impedance state when the I channel is powered down. Upon return to the active state, the pipeline contains meaningless information and must be flushed. The supply currents (typicals and limits) are available for the I channel powered down or active and may be found in *Converter Electrical Characteristics: Power Supply Characteristics*. Recalibrate the device following a power-cycle of PDI (or PDQ).

The PDI pin remains active in ECM, and either the PDI pin or the PDI bit of the Configuration Register (Addr: 0**h**; Bit: 11) may be used to power-down the I channel. See *Power Down* for more information.

7.5.1.1.7 Power-Down Q-Channel Pin (PDQ)

The power-down Q-channel (PDQ) pin selects whether the Q channel is powered down (logic-high) or active (logic-low). This pin functions similarly to the PDI pin, except that it applies to the Q channel; review the information in *Power-Down I-Channel Pin (PDI)* and apply to the PDQ pin as well. The PDI and PDQ pins function independently of each other to control whether each I or Q channel is powered down or active.

The PDQ pin remains active in ECM, and either the PDQ pin or the PDQ bit of the Configuration Register (Addr: 0**h**; Bit: 10) may be used to power-down the Q channel. See *Power Down* for more information.

7.5.1.1.8 Test-Pattern Mode Pin (TPM)

The test-pattern-mode (TPM) pin selects whether the output of the ADC12D1620 is a test pattern (logic-high) or the converted analog input (logic-low). The ADC12D1620 can provide a test pattern at the four output buses, independentl of the input signal, to aid in system debug. In TPM, the ADC is disengaged, and a test pattern generator is connected to the outputs, including ORI and ORQ. See *Test-Pattern Mode* for more information.

7.5.1.1.9 Full-Scale Input-Range Pin (FSR)

The full-scale input-range (FSR) pin selects whether the full-scale input range for both the I channel and Q channel is higher (logic-high) or lower (logic-low). The input full-scale range is specified as V_{IN_FSR} in *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics*. In non-ECM, the full-scale input range for each I and Q channel may not be set independently, but it is possible to do so in ECM. The device must be calibrated following a change in FSR to obtain optimal performance.

To use this feature in ECM, use the I- and Q-channel Full Scale Range Adjust registers (Addr: 3**h** and B**h**, respectively). See *Input Control and Adjust* for more information.

7.5.1.1.10 AC- or DC-Coupled Mode Pin (V_{CMO})

The V_{CMO} pin serves a dual purpose. When functioning as an output, it provides the optimal common-mode voltage for the DC-coupled analog inputs. When functioning as an input, it selects whether the device is AC-coupled (logic-low) or DC-coupled (floating). The V_{CMO} pin is always active, in both ECM and non-ECM.

7.5.1.1.11 LVDS Output Common-Mode Pin (V_{BG})

The V_{BG} pin serves a dual purpose. When functioning as an output, it provides a buffered copy of the bandgap reference voltage. When functioning as an input, it selects whether the LVDS output common-mode voltage is higher (logic-high) or lower (floating). The LVDS output common-mode voltage is specified as V_{OS} and may be found in *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics*. The V_{BG} pin is always active, in both ECM and non-ECM.

7.5.1.2 Extended Control Mode

In extended control mode (ECM), most functions are controlled through the serial interface. In addition to this, several of the control pins remain active. See 表 7-1 for details. ECM is selected by setting the $\overline{ECE}$ pin to logic-low. Each time the ADC is powered up the configuration register values are in an unknown state. Therefore all registers must be user configured to the default and/or desired values before device use. If the ECE pin is set to logic-high (non-ECM), then the registers are reset to their default values. Therefore, a simple way to reset the registers is by toggling the ECE pin. Four pins on the ADC12D1620 device control the serial interface: $\overline{SCS}$, SCLK, SDI, and SDO. This section covers the serial interface. (See also *Register Definitions*.)

7.5.1.2.1 Serial Interface

The ADC12D1620 offers a serial interface that allows access to the sixteen control registers within the device. The serial interface is a generic 4-wire (optionally 3-wire) synchronous interface that is compatible with SPI type interfaces that are used on many micro-controllers and DSP controllers. Each serial interface access cycle is exactly 24 bits long. A register-read or register-write can be accomplished in one cycle. The signals are defined in such a way that the user can opt to simply join SDI and SDO signals in their system to accomplish a single, bidirectional SDI/O signal. A summary of the pins for this interface may be found in 表 7-10. See 図 6-9 for the timing diagram and *Timing Requirements: Serial Port Interface* for timing specification details. Control register contents are retained when the device is put into power-down mode. If this feature is unused, the SCLK, SDI, and, $\overline{SCS}$ pins may be left floating because they each have an internal pullup.

表 7-10. Serial Interface Pins

PIN	NAME
C4	$\overline{SCS}$ (serial chip select bar)
C5	SCLK (serial clock)
B4	SDI (serial data in)
A3	SDO (serial data out)

$\overline{SCS}$: Each assertion (logic-low) of this signal starts a new register access, that is, the SDI command field must be ready on the following SCLK rising edge. The user is required to de-assert this signal after the 24th clock. If the $\overline{SCS}$ is de-asserted before the 24th clock, no data read/write occurs. For a read operation, if the $\overline{SCS}$ is asserted longer than 24 clocks, the SDO output holds the D0 bit until $\overline{SCS}$ is de-asserted. For a write operation, if the $\overline{SCS}$ is asserted longer than 24 clocks, data write occurs normally through the SDI input upon the 24th clock. Setup and hold times, t_{SCS} and t_{HCS}, with respect to the SCLK must be observed. $\overline{SCS}$ must be toggled in between register access cycles.

SCLK: This signal is used to register the input data (SDI) on the rising edge and to source the output data (SDO) on the falling edge. The user may disable the clock and hold it at logic-low. There is no minimum frequency requirement for SCLK; see f_{SCLK} in *Timing Requirements: Serial Port Interface* for more details.

SDI: Each register access requires a specific 24-bit pattern at this input, consisting of a command field and a data field. If the SDI and SDO wires are shared (3-wire mode), during read operations it is necessary to tri-state the primary must be tristate while the data field is output by the ADC on SDO. The primary must be tri-state before the falling edge of the 8^{th} clock. If SDI and SDO are not shared (4-wire mode), then this is not necessary. Setup and hold times, t_{SH} and t_{SSU}, with respect to the SCLK must be observed.

SDO: This output is normally tri-state and is driven only when $\overline{SCS}$ is asserted, the first 8 bits of command data have been received and it is a READ operation. The data is shifted out, MSB first, starting with the falling edge of the 8th clock. At the end of the access, when $\overline{SCS}$ is de-asserted, this output is tri-state once again. If an invalid

address is accessed, the data sourced will consist of all zeroes. If it is a read operation, there is a bus turnaround time, t_{BSU}, from when the last bit of the command field was read in until the first bit of the data field is written out.

表 7-11 shows the serial interface bit definitions.

表 7-11. Command and Data Field Definitions

BIT NO.	NAME	COMMENTS
1	Read/Write (R/W)	1**b** indicates a read operation. 0**b** indicates a write operation.
2-3	Reserved	Bits must be set to 10**b**.
4-7	A<3:0>	16 registers may be addressed. The order is MSB first.
8	X	This is a "don't care" bit.
9-24	D<15:0>	Data written to or read from addressed register.

The serial data protocol is shown for a read and write operation in 図 7-3 and 図 7-4, respectively.

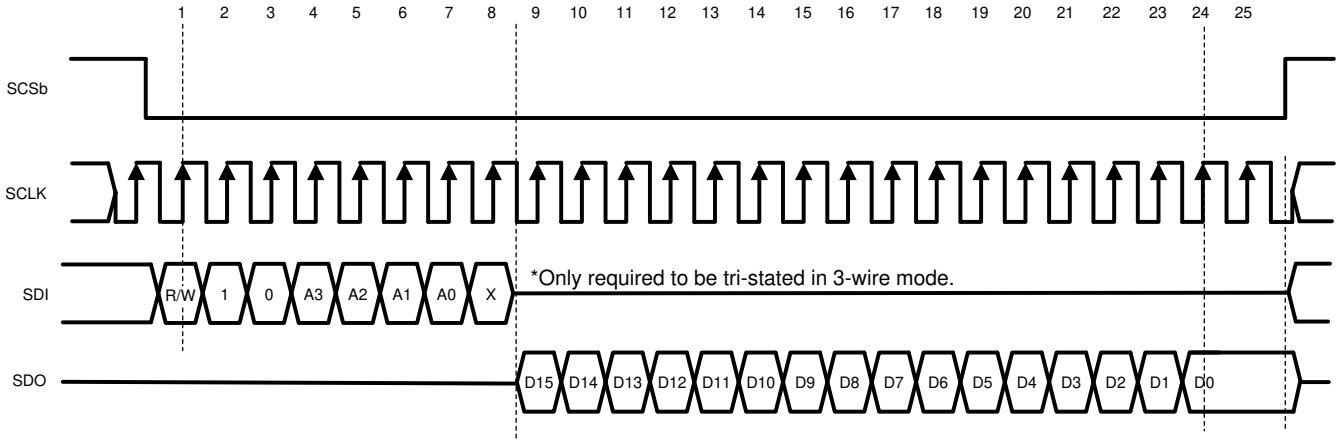


図 7-3. Serial Data Protocol - Read Operation

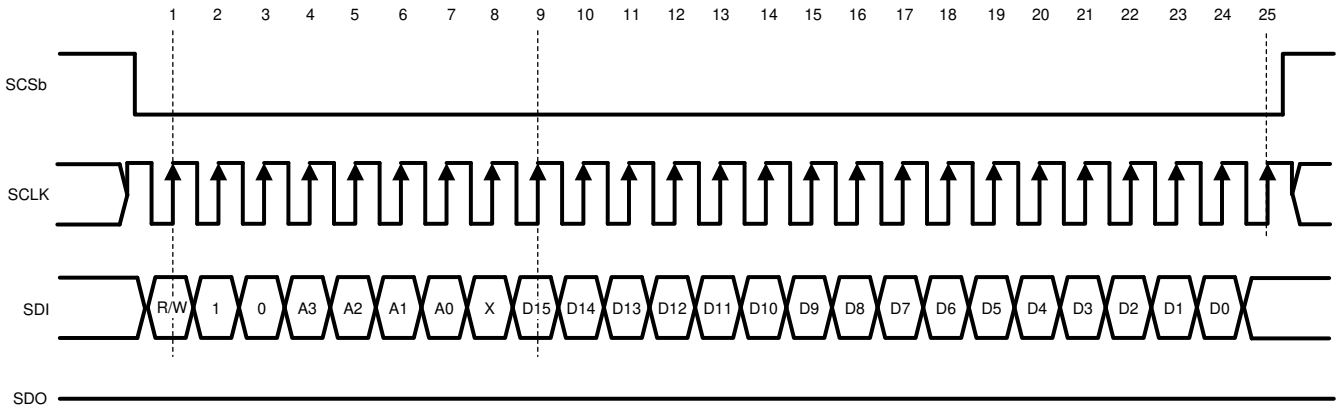


図 7-4. Serial Data Protocol - Write Operation

7.6 Register Maps

7.6.1 Register Definitions

Eleven read/write registers provide several control and configuration options in the extended control mode. When the device is in non-extended control mode (non-ECM), the registers have the settings shown in the "**DV**" rows and cannot be changed. See 表 7-12 for a summary.

表 7-12. Register Addresses

A3	A2	A1	A0	HEX	REGISTER ADDRESSED
0	0	0	0	**0h**	Configuration Register 1
0	0	0	1	**1h**	Reserved
0	0	1	0	**2h**	I-channel Offset Adjust
0	0	1	1	**3h**	I-channel Full-Scale Range Adjust
0	1	0	0	**4h**	Calibration Adjust
0	1	0	1	**5h**	Calibration Values
0	1	1	0	**6h**	Reserved
0	1	1	1	**7h**	DES Timing Adjust
1	0	0	0	**8h**	Reserved
1	0	0	1	**9h**	Reserved
1	0	1	0	**Ah**	Q-channel Offset Adjust
1	0	1	1	**Bh**	Q-channel Full-Scale Range Adjust
1	1	0	0	**Ch**	Aperture Delay Coarse Adjust
1	1	0	1	**Dh**	Aperture Delay Fine Adjust
1	1	1	0	**Eh**	AutoSync
1	1	1	1	**Fh**	Reserved

表 7-13. Configuration Register 1

Addr: 0**h** (0000**b**)									Default Values: 2000**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAL	DPS	OVS	TPM	PDI	PDQ	Res	LFS	DES	DEQ	DIQ	2SC	TSE	SDR	Reserved	
DV (1)	0	0	1	0	0	0	0	0/1	0	0	0	0	0	0	0	0

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bit 15	CAL: Calibration enable. When this bit is set to 1**b**, an on-command calibration is initiated. This bit is not reset automatically upon completion of the calibration. Therefore, the user must reset this bit to 0**b** and then set it to 1**b** again to execute calibration. This bit is logically OR'd with the CAL Pin; both bit and pin must be set to 0**b** before either is used to execute a calibration. TI recommends holding the CAL pin high during normal usage of the ADC12D1620 device to reduce the chance that an SEU causes a calibration cycle.		
Bit 14	DPS: DCLK phase select. In DDR, set this bit to 0**b** to select the 0° mode DDR data-to-DCLK phase relationship and to 1**b** to select the 90° mode. In SDR, set this bit to 0**b** to transition the data on the rising edge of DCLK; set this bit to 1**b** to transition the data on the falling edge of DCLK.		
Bit 13	OVS: Output voltage select. This bit sets the differential voltage level for the LVDS outputs including Data, OR, and DCLK. 0**b** selects the lower level and 1**b** selects the higher level. See V_{OD} in *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics* for details.		
Bit 12	TPM: Test pattern mode. When this bit is set to 1**b**, the device continually outputs a fixed digital pattern at the digital data and OR outputs. When set to 0**b**, the device continually outputs the converted signal, which was present at the analog inputs. See *Test-Patterm Mode* for details about the TPM pattern.		
Bit 11	PDI: Power-down I channel. When this bit is set to 0**b**, the I channel is fully operational; when it is set to 1**b**, the I channel is powered-down. The I channel may be powered-down through this bit or the PDI pin, which is active, even in ECM.		
Bit 10	PDQ: Power-down Q channel. When this bit is set to 0**b**, the Q channel is fully operational; when it is set to 1**b**, the Q channel is powered-down. The Q channel may be powered-down through this bit or the PDQ pin, which is active, even in ECM.		
Bit 9	Reserved. Must be set as shown.		
Bit 8	LFS: Low-frequency select. If the sampling clock (CLK) is at or below 300 MHz in non-LSPSM, set this bit to 1**b** for improved performance. In LSPSM, the device is automatically in LFS, and this bit is inactive.		
Bit 7	DES: Dual-edge sampling mode select. When this bit is set to 0**b**, the device operates in the non-DES mode; when it is set to 1**b**, the device operates in the DES mode. See *DES/Non-Des Mode* for more information.		
Bit 6	DEQ: DES Q input select, also known as DESQ mode. When the device is in DES mode, this bit selects the input that the device operates on. The default setting of 0**b** selects the I input and 1**b** selects the Q input.		
Bit 5	DIQ: DES I and Q input, also known as DESIQ mode. When in DES mode, setting this bit to 1**b** shorts the I and Q inputs internally to the device. In this mode, both the I and Q inputs must be externally driven; see *DES/Non-Des Mode* for more information. If the bit is left at its default 0**b**, the I and Q inputs remain electrically separate. The allowed DES modes settings are shown below. For DESCLKIQ mode, see the 表 7-27 register (Addr E**h**).		
	MODE	**ADDR 0h, BIT<7:5>**	**ADDR Eh, BIT<6>**
	Non-DES mode	000**b**	0**b**
	DESI mode	100**b**	0**b**
	DESQ mode	110**b**	0**b**
	DESIQ mode	101**b**	0**b**
	DESCLKIQ mode	000**b**	1**b**
Bit 4	2SC: Two's complement output. For the default setting of 0**b**, the data is output in offset binary format; when set to 1**b**, the data is output in two's complement format.		
Bit 3	TSE: Time stamp enable. For the default setting of 0**b**, the time stamp feature is not enabled; when set to 1**b**, the feature is enabled. See *Output Control and Adjust* for more information about this feature.		
Bit 2	SDR: Single data rate. For the default setting of 0**b**, the data is clocked in dual data rate; when set to 1**b**, the data is clocked in single data rate. See *Output Control and Adjust* for more information about this feature. Note that for DDR mode, the 1:2 demux mode is not available in LSPSM. See *Supported Demux , Data Rate Modes* for a selection of available modes.		
Bits 1:0	Reserved. Must be set as shown.		

表 7-14. Reserved

Addr: 1**h** (0001**b**)									Default Values: 2907**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV (1)	0	0	1	0	1	0	0	1	0	0	0	0	0	1	1	1

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:0	Reserved. Must be set as shown.

表 7-15. I-Channel Offset Adjust

Addr: 2**h** (0010**b**)									Default Values: 0000**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved			OS	OM(11:0)											
DV (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:13	Reserved. Must be set to 0**b**.	
Bit 12	OS: Offset sign. The default setting of 0**b** incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bit to 1**b** incurs a negative offset of the set magnitude.	
Bits 11:0	OM(11:0): Offset magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0**d** to 45 mV for OM(11:0) = 4095**d** in steps of ~11 µV. Monotonicity is specified by design only for the 9 MSBs.	
	CODE	**OFFSET [mV]**
	0000 0000 0000 (default)	0
	1000 0000 0000	22.5
	1111 1111 1111	45

表 7-16. I-Channel Full Scale Range Adjust

Addr: 3**h** (0011**b**)									Default Values: 4000**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	FM(14:0)														
DV (1)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bit 15	Reserved. Must be set to 0**b**.	
Bits 14:0	FM(14:0): FSR magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 600 mV (0**d**) to 1000 mV (32767**d**) with the default setting at 800 mV (16384**d**). Monotonicity is specified by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in non-ECM. A greater range of FSR values is available in ECM, that is, FSR values above 800 mV. See V_{IN_FSR} in *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics* for characterization details.	
	CODE	**FSR [mV]**
	000 0000 0000 0000	600
	100 0000 0000 0000 (default)	800
	111 1111 1111 1111	1000

表 7-17. Calibration Adjust

Addr: 4**h** (0100**b**)									Default Values: DB4B**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	CSS	Reserved						SSC	Reserved						
DV (1)	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bit 15	Reserved. Must be set as shown.
Bit 14	CSS: Calibration sequence select. The default 1**b** selects the following calibration sequence: reset all previously calibrated elements to nominal values, do R_{IN} calibration, do internal linearity calibration. Setting CSS = 0**b** selects the following calibration sequence: do not reset R_{IN} to its nominal value, skip R_{IN} calibration, do internal linearity calibration. The calibration must be completed at least one time with CSS = 1**b** to calibrate R_{IN}. Subsequent calibrations may be run with CSS = 0**b** (skip R_{IN} calibration) or 1**b** (full R_{IN} and internal linearity calibration).
Bits 13:8	Reserved. Must be set as shown.
Bit 7	SSC: SPI scan control. Setting this control bit to 1**b** allows the calibration values, stored in Addr: 5**h**, to be read/written. When not reading/writing the calibration values, this control bit should left at its default 0**b** setting. See *Calibration Feature* for more information.
Bits 6:0	Reserved. Must be set as shown.

表 7-18. Calibration Values

Addr: 5**h** (0101**b**)									Default Values: XXXX**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SS(15:0)															
DV (1)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:0	SS(15:0): SPI scan. When the ADC performs a self-calibration, the values for the calibration are stored in this register and may be read from/written to it. Set the SSC of the Calibration Adjust register (Addr: 4**h**, Bit: 7) to read/write. See *Calibration Feature* for more information.

表 7-19. Reserved

Addr: 6**h** (0110**b**)									Default Values: 1C2E**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV (1)	0	0	0	1	1	1	0	0	0	0	1	0	1	1	1	0

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:0	Reserved. Must be set as shown.

表 7-20. DES Timing Adjust

Addr: 7**h** (0111**b**)									Default Values: 8142**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DTA(6:0)							Reserved								
DV (1)	1	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:9	DTA(6:0): DES mode timing adjust. In the DES mode, the time at which the falling edge sampling clock samples relative to the rising edge of the sampling clock may be adjusted; the automatic duty cycle correction continues to function. See *Input Control and Adjust* for more information. The nominal step size is 30 fs.
Bits 8:0	Reserved. Must be set as shown.

表 7-21. Reserved

Addr: 8**h** (1000**b**)									Default Values: 0F0F**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

表 7-21. Reserved (continued)

Name	Reserved															
DV (1)	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:0	Reserved. Must be set as shown.

表 7-22. Reserved

Addr: 9**h** (1001**b**)									Default Values: 0000**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:0	Reserved. Must be set as shown.

表 7-23. Q-Channel Offset Adjust

Addr: A**h** (1010**b**)									Default Values: 0000**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved			OS	OM(11:0)											
DV (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:13	Reserved. Must be set to 0**b**.	
Bit 12	OS: Offset sign. The default setting of 0**b** incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bit to 1**b** incurs a negative offset of the set magnitude.	
Bits 11:0	OM(11:0): Offset magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0**d** to 45 mV for OM(11:0) = 4095**d** in steps of ~11 µV. Monotonicity is specified by design only for the 9 MSBs.	
	CODE	**OFFSET [mV]**
	0000 0000 0000 (default)	0
	1000 0000 0000	22.5
	1111 1111 1111	45

表 7-24. Q-Channel Full-Scale Range Adjust

Addr: B**h** (1011**b**)									Default Values: 4000**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	FM(14:0)														
DV (1)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bit 15	Reserved. Must be set to 0**b**.	
Bits 14:0	FM(14:0): FSR magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 600 mV (0**d**) to 1000 mV (32767**d**) with the default setting at 800 mV (16384**d**). Monotonicity is specified by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in ECM, that is, FSR values above 800 mV. See V_{IN_FSR} in *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics* for characterization details.	
	CODE	**FSR [mV]**
	000 0000 0000 0000	600
	100 0000 0000 0000 (default)	800
	111 1111 1111 1111	1000

表 7-25. Aperture Delay Coarse Adjust

Addr: C**h** (1100**b**)									Default Values: 0004**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM(11:0)												STA	DCC	Res	
DV (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:4	CAM(11:0): Coarse adjust magnitude. This 12-bit value determines the amount of delay that is applied to the input CLK signal. The range is 0-ps delay for CAM(11:0) = 0**d** to a maximum delay of 825 ps for CAM(11:0) = 2431**d** (±95 ps due to PVT variation) in steps of ~340 fs. For code CAM(11:0) = 2432**d** and above, the delay saturates and the maximum delay applies. Additional, finer delay steps are available in register D**h**. The STA (Bit 3) must be selected to enable this function.
Bit 3	STA: Select t_{AD} Adjust. Set this bit to 1**b** to enable the t_{AD} adjust feature, which makes both coarse and fine adjustment settings, that is, CAM(11:0) and FAM(5:0), available.
Bit 2	DCC: Duty cycle correct. This bit can be set to 0**b** to disable the automatic duty-cycle stabilizer feature of the chip. This feature is enabled by default.
Bits 1:0	Reserved. Must be set to 0**b**.

表 7-26. Aperture Delay Fine Adjust

Addr: D**h** (1101**b**)									Default Values: 0000**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FAM(5:0)						Reserved									
DV (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:10	FAM(5:0): Fine aperture adjust magnitude. This 6-bit value determines the amount of additional delay that is applied to the input CLK when the clock phase adjust feature is enabled through STA (Addr: C**h**; Bit: 3). The range is straight binary from 0 ps delay for FAM(5:0) = 0**d** to 2.3 ps delay for FAM(5:0) = 63**d** (±300 fs due to PVT variation) in steps of ~36 fs.
Bits 9:0	Reserved. Must be set as shown.

表 7-27. AutoSync

Addr: E**h** (1110**b**)									Default Values: 0003**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRC(8:0)								DCK	Res	SP(1:0)			ES	DOC	DR
DV (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:7	DRC(8:0): Delay reference clock. These bits may be used to increase the delay on the input reference clock when synchronizing multiple ADCs. The delay may be set from a minimum of 0s (0**d**) to a maximum of 1200 ps (319**d**). The delay remains the maximum of 1200 ps for any codes above or equal to 319**d**. See *Synchronizing Multiple ADC12D1620 Devices in a System* for more information.
Bit 6	DCK: DESCLKIQ mode. Set this bit to 1**b** to enable Dual-Edge Sampling, in which the Sampling Clock samples the I and Q inputs 180° out of phase with respect to one , that is, the DESCLKIQ mode. To select the DESCLKIQ mode, Addr: 0**h**, Bits <7:5> must also be set to 000**b**. See *Input Control and Adjust* for more information.
Bit 5	Reserved. Must be set as shown.
Bits 4:3	SP(1:0): Select phase. These bits select the phase of the reference clock that is latched. The codes correspond to the following phase shift: 00 = 0° 01 = 90° 10 = 180° 11 = 270°
Bit 2	ES: Enable secondary. Set this bit to 1**b** to enable the secondary mode of operation. In this mode, the internal divided clocks are synchronized with the reference clock coming from the primary ADC. The primary clock is applied on the input pins RCLK. If this bit is set to 0**b**, then the device is in primary mode.
Bit 1	DOC: Disable output reference clocks. In non-LSPSM, setting this bit to 0**b** sends a CLK/4 signal on RCOut1 and RCOut2; in LSPSM, setting this bit to 0**b** sends a CLK/2 signal on RCOut1 and RCOut2. The default setting of 1**b** disables these output drivers. This bit functions as described, regardless of whether the device is operating in primary or secondary mode, as determined by ES (Bit 2).
Bit 0	DR: Disable reset. The default setting of 1**b** leaves the DCLK_RST functionality disabled. Set this bit to 0**b** to enable DCLK_RST functionality.

表 7-28. Reserved

Addr: F**h** (1111**b**)									Default Values: 001D**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV (1)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

(1) *DV* means *Default Value*. Refer to *Extended Control Mode* for more information on setting ECM default values.

Bits 15:0	Reserved. This address is read only.

8 Application Information Disclaimer

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Analog Inputs

The ADC12D1620 device continuously converts any signal that is present at the analog inputs, as long as a CLK signal is also provided to the device. This section covers important aspects related to the analog inputs including: acquiring the input, driving the ADC in DES mode, the reference voltage and FSR, out-of-range indication, AC-DC-coupled signals, and single-ended input signals.

8.1.1.1 Acquiring the Input

The aperture delay, t_{AD}, is the amount of delay, measured from the sampling edge of the clock input, after which signal present at the input pin is sampled inside the device. Data is acquired at the rising edge of CLK+ in non-DES mode and both the falling and rising edges of CLK+ in DES mode. In Non-DES mode, the I and Q channels always sample data on the rising edge of CLK+. In DES mode, that is, DESI, DESQ, DESIQ, and DESCLKIQ, the I-channel samples data on the rising edge of CLK+, and the Q-channel samples data on the falling edge of CLK+. The digital equivalent of that data is available at the digital outputs a constant number of sampling clock cycles later for the DI, DQ, DId and DQd output buses, also known as latency, depending on the demultiplex mode which is selected. In addition to the latency, there is a constant output delay, t_{OD}, before the data is available at the outputs. See t_{OD} in the *Converter Electrical Characteristics: AC Electrical Characteristics*, and also see t_{LAT}, t_{AD}, and t_{OD} in *Converter Electrical Characteristics: AC Electrical Characteristics*.

8.1.1.2 Driving the ADC in DES Mode

The ADC12D1620 can be configured as either a 2-channel, 1.6 GSPS device (Non-DES mode) or a 1-channel 3.2-GSPS device (DES mode). When the device is configured in DES mode, there is a choice for with which input to drive the single-channel ADC. These are the 3 options:

DES – externally driving the I-channel input only. This is the default selection when the ADC is configured in DES mode. It may also be referred to as DESI for added clarity.

DESQ – externally driving the Q-channel input only.

DESIQ, DESCLKIQ – externally driving both the I- and Q-channel inputs. VinI+ and VinQ+ must be driven with the exact same signal. VinI- and VinQ- must be driven with the exact same signal, which is the differential complement to the one driving VinI+ and VinQ+.

The input impedance for each I and Q input is 100-Ω differential (or 50-Ω single-ended), so the trace to each VinI+, VinI-, VinQ+, and VinQ- must always be 50-Ω single-ended. If a single I or Q input is being driven, then that input presents a 100-Ω differential load. For example, if a 50-Ω single-ended source is driving the ADC, a 1:2 balun transforms the impedance to 100-Ω differential. However, if the ADC is being driven in DESIQ mode, then the 100-Ω differential impedance from the I input appears in parallel with the Q input for a composite load of 50-Ω differential, and a 1:1 balun would be appropriate. See 図 8-1 for an example circuit driving the ADC in DESIQ mode. A recommended part selection uses the mini-circuits TC1-1-13MA+ balun with C_{couple} = 0.22 µF.

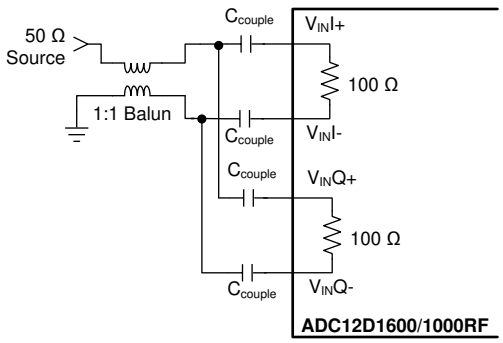


図 8-1. Driving DESIQ Mode

when only one channel is used in non-DES mode or the ADC is driven in DESI or DESQ mode, terminate the unused analog input to reduce any noise coupling into the ADC. See 表 8-1 for details.

表 8-1. Unused Analog Input Recommended Termination

MODE	POWER DOWN	COUPLING	RECOMMENDED TERMINATION
Non-DES	Yes	AC-DC	Tie Unused+ and Unused– to V_{BG}
DES/Non-DES	No	DC	Tie Unused+ and Unused– to V_{BG}
DES/Non-DES	No	AC	Tie Unused+ to Unused–

8.1.1.3 FSR and the Reference Voltage

The full-scale analog-differential input range (V_{IN_FSR}) of the ADC12D1620 is derived from an internal bandgap reference. In Non-ECM, this full-scale range has two settings controlled by the FSR pin; see *Full-Scale Input-Range Pin (FSR)*. The FSR Pin operates on both I and Q channels. In ECM, the full-scale range may be independently set with 15 bits of precision for each channel through the I- and Q-channel Full-Scale Range Adjust Registers (Addr: 3**h** and Addr: B**h**, respectively); see 表 7-16 and 表 7-24 for information about the registers. The best SNR is obtained with a higher full-scale input range, but better distortion and SFDR are obtained with a lower full-scale input range. It is not possible to use an external analog reference voltage to modify the full-scale range, and this adjustment should only be done digitally, as described.

A buffered version of the internal bandgap reference voltage is made available at the V_{BG} pin for the user. The V_{BG} pin can drive a load of up to 80-pF and source or sink up to 100 µA. It must be buffered if current higher than 100 µA is required. This pin remains as a constant reference voltage regardless of what full-scale range is selected and may be used for a system reference. V_{BG} is a dual-purpose pin and it may also be used to select a higher LVDS output common-mode voltage; see *LVDS Output Common-Mode Pin (VBG)*.

8.1.1.4 Out-Of-Range Indication

Differential input signals are digitized to 12 bits, based on the full-scale range. Signal excursions beyond the full-scale range, that is, greater than $+V_{IN\_FSR}/2$ or less than $– V_{IN\_FSR}/2$, are clipped at the output. An input signal above the FSR results in all 1's at the output; an an input signal that is below the FSR results in all 0's at the output. When the conversion result is clipped for the I-channel input, the out-of-range I-channel (ORI) output is activated so that ORI+ goes high and ORI– goes low while the signal is out of range. This output is active as long as accurate data on either or both of the buses is outside the range of 000**h** to FFF**h**. The Q channel has a separate ORQ, which functions similarly.

8.1.1.5 AC-Coupled Input Signals

The ADC12D1620 analog inputs require a precise common-mode voltage. This voltage is generated on-chip when AC-coupling mode is selected. See *AC- and DC-Coupled Modes* for more information about how to select AC-coupled mode.

In AC-coupled mode, the analog inputs must of course be AC-coupled. For an ADC12D1620 used in a typical application, this may be accomplished by on-board capacitors, as shown in 図 8-2.

When the AC-coupled mode is selected, terminate unused channels as shown in 表 8-1. Do not connect an unused analog input directly to ground.

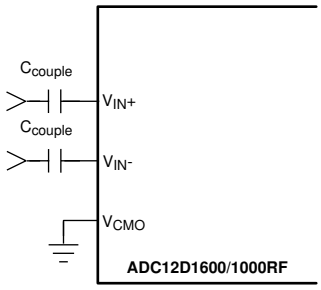


図 8-2. AC-Coupled Differential Input

The analog inputs for the ADC12D1620 are internally buffered; this simplifies the task of driving these inputs and the RC pole, which is generally used at sampling ADC inputs, is not required. If the user desires to place an amplifier circuit before the ADC, take care to choose an amplifier with adequate noise and distortion performance, and adequate gain at the frequencies used for the application.

8.1.1.6 DC-Coupled Input Signals

In DC-coupled mode, the ADC12D1620 differential inputs must have the correct common-mode voltage. This voltage is provided by the device itself at the V_{CMO} output pin. TI recommends using this voltage because the V_{CMO} output potential changes with temperature, and the common-mode voltage of the driving device should track this change. Full-scale distortion performance falls off as the input common-mode voltage deviates from V_{CMO}. Therefore, TI recommends keeping the input common-mode voltage within 100 mV of V_{CMO} (typical), although this range may be extended to ±150 mV (maximum). See V_{CMI} in *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics* and ENOB vs V_{CMI} in *Typical Characteristics*. Performance in AC- and DC-coupled modes are similar, provided that the input common mode voltage at both analog inputs remains within 100 mV of V_{CMO}.

8.1.1.7 Single-Ended Input Signals

The analog inputs of the ADC12D1620 are not designed to accept single-ended signals. The best way to handle single-ended signals is to first convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun transformer, as shown in 図 8-3.

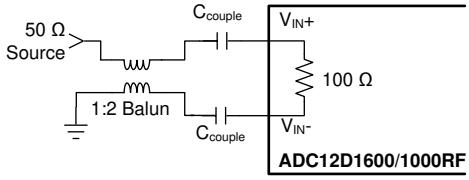


図 8-3. Single-Ended to Differential Conversion Using a Balun

When selecting a balun, it is important to understand the input architecture of the ADC. Match the impedance of the analog source to the on-chip 100-Ω differential input termination resistor of the device. The range of this termination resistor is specified as R_{IN} in *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics*.

8.1.2 Clock Inputs

The ADC12D1620 has a differential clock input, CLK+ and CLK–, which must be driven with an AC-coupled, differential clock signal. This provides the level shifting necessary so that the clock can be driven with LVDS,

PECL, LVPECL, or CML levels. The clock inputs are internally terminated to 100-Ω differential and self-biased. This section covers coupling, frequency range, level, duty-cycle, jitter, and layout considerations.

8.1.2.1 CLK Coupling

The clock inputs of the ADC12D1620 must be capacitively coupled to the clock pins as indicated in 図 8-4.

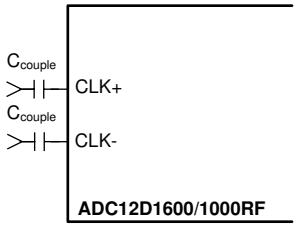


図 8-4. Differential Input Clock Connection

Selection of capacitor value depends on the clock frequency, capacitor component characteristics, and other system economic factors.

8.1.2.2 CLK Frequency

Although the ADC12D1620 device is tested and its performance is specified with a differential 1.6-GHz sampling clock, it typically functions well over the input clock-frequency range; see $f_{CLK\ (min)}$ and $f_{CLK\ (max)}$ in *Converter Electrical Characteristics: AC Electrical Characteristics*. Operation up to $f_{CLK\ (max)}$ is possible if the maximum ambient temperatures indicated are not exceeded. Operating at sample rates above $f_{CLK\ (max)}$ for the maximum ambient temperature may result in reduced device reliability and product lifetime. This is due to the fact that higher sample rates results in higher power consumption and die temperatures. If in non-LSPSM and f_{CLK} < 300 MHz, enable LFS in the Control Register (Addr: 0**h**; Bit: 8). In LSPSM, the LFS bit is already enabled.

8.1.2.3 CLK Level

The input clock amplitude is specified as V_{IN_CLK} in *Converter Electrical Characteristics: AC Electrical Characteristics*. Input clock amplitudes above the maximum V_{IN_CLK} may result in increased input offset voltage. This causes the converter to produce an output code other than the expected 2047/2048 when both input pins are at the same potential. Insufficient input clock levels result in poor dynamic performance. Both of these results may be avoided by keeping the clock input amplitude within the specified limits of V_{IN_CLK}.

8.1.2.4 CLK Duty Cycle

The duty cycle of the input clock signal can affect the performance of any ADC. The ADC12D1620 device features a duty-cycle-clock correction circuit, which can maintain performance over the 20%-to-80% specified clock duty-cycle range. This feature is enabled by default and provides improved ADC clocking, especially in the dual-edge sampling (DES) mode.

8.1.2.5 CLK Jitter

High-speed, high-performance ADCs such as the ADC12D1620 require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency, and the input signal amplitude relative to the ADC input full-scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be:

$$t_{J(MAX)} = (V_{IN(P-P)} / V_{FSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN})) \quad (1)$$

where

- $t_{J(MAX)}$ is the rms total of all jitter sources in seconds
- $V_{IN(P-P)}$ is the peak-to-peak analog input signal
- V_{FSR} is the full-scale range of the ADC
- N is the ADC resolution in bits
- f_{IN} is the maximum input frequency, in Hertz, at the ADC analog input

$t_{J(MAX)}$ is the square root of the sum of the squares (RSS) of the jitter from all sources, including: ADC input clock, system, input signals, and the ADC itself. Because the effective jitter added by the ADC is beyond user control, TI recommends keeping the sum of all other externally added jitter to a minimum.

8.1.2.6 CLK Layout

The ADC12D1620 clock input is internally terminated with a trimmed 100-Ω resistor. The differential input clock line pair must have a characteristic impedance of 100 Ω and (when using a balun), be terminated at the clock source in that (100-Ω) characteristic impedance.

It is good practice to keep the ADC input clock line as short as possible, tightly coupled, keep it well away from any other signals, and treat it as a transmission line. Otherwise, other signals can introduce jitter into the input clock signal. Also, the clock signal can introduce noise into the analog path if it is not properly isolated.

8.1.3 LVDS Outputs

The data, ORI, ORQ, DCLKI and DCLKQ outputs are LVDS. The electrical specifications of the LVDS outputs are compatible with typical LVDS receivers available on ASIC and FPGA chips; however, they are not IEEE or ANSI communications standards compliant due to the low 1.9-V supply used on this device. Terminate these outputs with a 100-Ω differential resistor placed as closely as possible to the receiver. If the 100-Ω differential resistance is built into the receiver, an externally placed resistor is not necessary. This section covers common-mode and differential voltage, and data rate.

8.1.3.1 Common-Mode and Differential Voltage

The LVDS outputs have selectable common-mode and differential voltage, V_{OS} and V_{OD}; see *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics* and also see *Output Control and Adjust* for more information.

Selecting the higher V_{OS} also increases V_{OD} slightly. The differential voltage, V_{OD}, may be selected for the higher or lower value. For short LVDS lines and low noise systems, satisfactory performance may be achieved with the lower V_{OD}. This also results in lower power consumption. If the LVDS lines are long and/or the system in which the ADC12D1620 is used is noisy, it may be necessary to select the higher V_{OD}.

8.1.3.2 Output Data Rate

The data is produced at the output at the same rate it is sampled at the input. The minimum recommended input clock rate for this device is $f_{CLK(MIN)}$; see *Converter Electrical Characteristics: AC Electrical Characteristics*. However, it is possible to operate the device in 1:2 demux mode and capture data from just one 12-bit bus; for example, just DI (or DId) although both DI and DId are fully operational. This decimates the data by two and effectively halves the data rate.

8.1.3.3 Terminating Unused LVDS Output Pins

If the ADC is used in non-demux mode, only the DI and DQ data outputs will have valid data present on them. The DId and DQd data outputs may be left not connected; if unused, they are internally tri-state.

Similarly, if the Q channel is powered-down (that is, PDQ is logic-high), the DQ data output pins, DCLKQ and ORQ, may be left not connected.

8.1.4 Synchronizing Multiple ADC12D1620 Devices in a System

The ADC12D1620 has two features to assist the user with synchronizing multiple ADCs in a system: AutoSync and DCLK reset. The AutoSync feature is new and designates one ADC12D1620 as the primary ADC and other ADC12D1620 devices in the system as secondary ADCs. The DCLK reset feature performs the same function as the AutoSync feature, but is the first-generation solution to synchronizing multiple ADCs in a system; it is disabled by default. For applications in which there are multiple primary and secondary ADC12D1620 devices in a system, AutoSync may be used to synchronize the secondary ADC12D1620 devices to each respective primary ADC12D1620, and the DCLK reset may be used to synchronize the primary ADC12D1620 devices to each other.

If the AutoSync or DCLK reset feature is not used, see 表 8-2 for recommendations about terminating unused pins.

表 8-2. Unused AutoSync and DCLK Reset Pin Recommendation

PIN(s)	UNUSED TERMINATION
RCLK+, RCLK–	Do not connect.
RCOUT1+, RCOUT1–	Do not connect.
RCOUT2+, RCOUT2–	Do not connect.
DCLK_RST+	Connect to GND with a 1-kΩ resistor.
DCLK_RST-	Connect to V_A with a 1-kΩ resistor.

8.1.4.1 AutoSync Feature

AutoSync is a new feature which continuously synchronizes the outputs of multiple ADC12D1620 devices in a system. It may be used to synchronize the DCLK and data outputs of one or more secondary ADC12D1620 devices to one primary ADC12D1620. Several advantages of this feature include: no special synchronization pulse required, any upset in synchronization is recovered upon the next DCLK cycle, and the primary/secondary ADC12D1620 devices may be arranged as a binary tree so that any upset quickly propagates out of the system.

An example system is shown in 図 8-5, which consists of one primary ADC and two secondary ADCs. For simplicity, only one DCLK is shown; in reality, there is DCLKI and DCLKQ, but they are always in phase with one another.

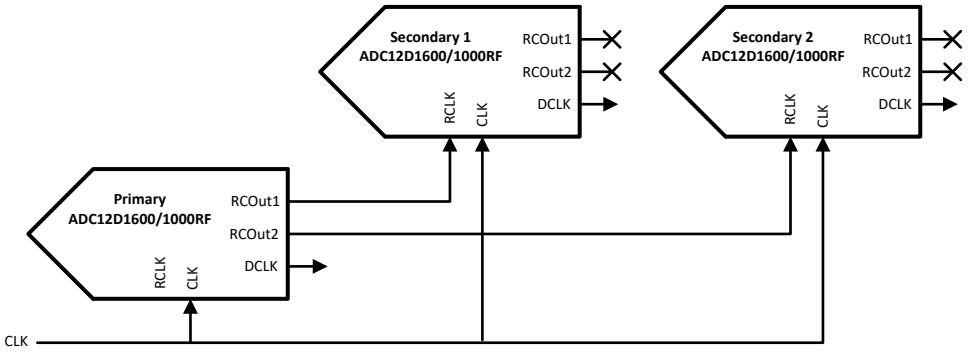


図 8-5. AutoSync Example

In order to synchronize the DCLK (and data) outputs of multiple ADCs, the DCLKs must transition at the same time, as well as be in phase with one another. The DCLK at each ADC is generated from the CLK after some latency, plus t_{OD} minus t_{AD}. Therefore, in order for the DCLKs to transition at the same time, the CLK signal must

reach each ADC at the same time. To tune out any differences in the CLK path to each ADC, the t_{AD} adjust feature may be used. However, using the t_{AD} adjust feature also affects when the DCLK is produced at the output. If the device is in demux mode, there are four possible phases that each DCLK may be generated on because the typical CLK = 1GHz and DCLK = 250 MHz for this case. The RCLK signal controls the phase of the DCLK, so that each secondary DCLK is on the same phase as the primary DCLK.

The AutoSync feature may only be used through the Control Registers. For more information, see *AN-2132 Synchronizing Multiple GSPS ADCs in a System: The AutoSync Feature*.

8.1.4.2 DCLK Reset Feature

The DCLK reset feature is available through ECM, but it is disabled by default. DCLKI and DCLKQ are always synchronized, by design, and do not require a pulse from DCLK_RST to become synchronized.

The DCLK_RST signal must observe certain timing requirements, which are shown in 図 6-7 of *セクション 6.16*. The DCLK_RST pulse must be of a minimum width, and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These timing specifications are listed as t_{PWR}, t_{SR} and t_{HR} and may be found in *セクション 6.13*.

The DCLK_RST signal can be asserted asynchronously to the input clock. If DCLK_RST is asserted, the DCLK output is held in a designated state (logic-high) in demux mode; in non-demux mode, the DCLK continues to function normally. Depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted, there are t_{SYNC_DLY} CLK cycles of systematic delay and the next CLK rising edge synchronizes the DCLK output with those of other ADC12D1620 devices in the system. For 90° mode (DDRPh = logic-high), the synchronizing edge occurs on the rising edge of CLK, 4 cycles after the first rising edge of CLK after DCLK_RST is released. For 0° mode (DDRPh = logic-low), this is 5 cycles instead. The DCLK output is enabled again after a constant delay of t_{OD}.

For both demux and non-demux modes, there is some uncertainty about how DCLK comes out of the reset state for the first DCLK_RST pulse. For the second (and subsequent) DCLK_RST pulses, the DCLK comes out of the reset state in a known way. Therefore, if using the DCLK reset feature, TI recommends applying one *dummy* DCLK_RST pulse before using the second DCLK_RST pulse to synchronize the outputs. This recommendation applies each time the device or channel is powered-on.

When using DCLK_RST to synchronize multiple ADC12D1620 devices, the select-phase bits in the Control Register (Addr: E**h**, Bits: 4:3) must be the same for each primary ADC12D1620.

8.1.5 Temperature Sensor

The ADC12D1620 has an on-die temperature diode connected to the Tdiode+ and Tdiode– pins that may be used to monitor the die temperature. In 図 8-6, the LM95213 is used to monitor the temperature of an ADC12D1620 as well as an FPGA, see 図 8-6. Typical temperature diode voltage to temperature characteristic is:

$$T_J = \frac{(V_{diode} - 0.84161)}{-0.0015} \quad (2)$$

for

- 1-mA diode forward current

If this feature is unused, the Tdiode+ and Tdiode– pins may be left floating.

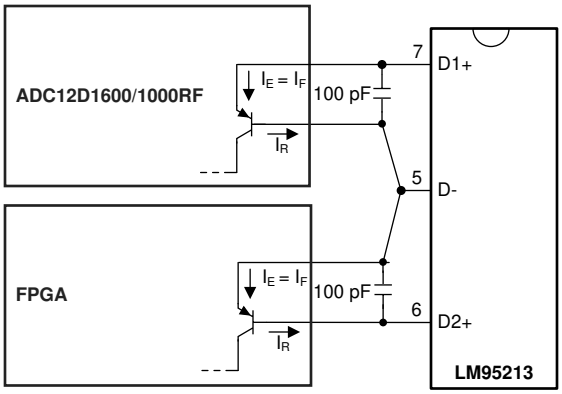


図 8-6. Typical Temperature Sensor Application

8.2 Radiation Environments

Careful consideration must be given to environmental conditions when using a product in a radiation environment.

8.2.1 Total Ionizing Dose

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the POA. Testing and qualification of these products is done on a wafer level according to MIL-STD-883, Test Method 1019. Wafer level TID data are available with lot shipments.

8.2.2 Single Event Latch-Up and Functional Interrupt

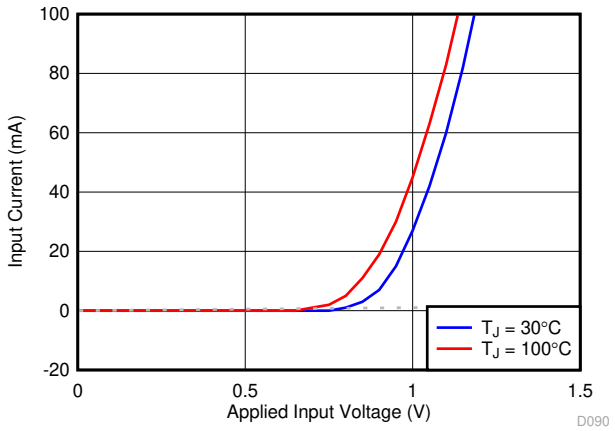
One time single event latch-up (SEL) and single event functional interrupt (SEFI) testing was performed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LETth) shown in the *Features* section is the maximum LET tested. A test report is available upon request.

8.2.3 Single Event Upset

A report on single event upset (SEU) is available upon request.

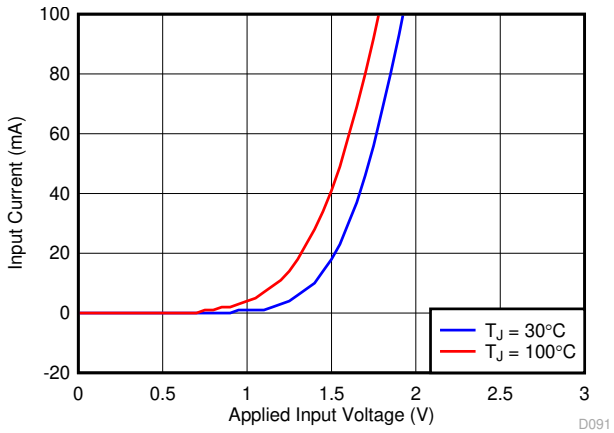
8.3 Cold Sparing

The ADC12D1620QML-SP has been designed for cold sparing with no reduction in operational lifetime or increase in FIT rate as long as certain conditions are met. Cold sparing is defined as a device in which all power supplies are either floating (high-impedance) or grounded. When cold sparing, all output pins must be either floating or clamped to ground through ESD diodes of the receiving device and not pulled up to an active power supply voltage. Input pins may be driven low (or grounded) or driven to other voltages as long as they are within the Recommended Operating Conditions. Input pins (digital and analog) must maintain a maximum input level of 2.15 V and maximum input current of 50 mA per pin when cold sparing. The input current at each pin is a function of the voltage applied to the pin, the ESD diode IV curve, the power down pin settings, and conditions of the V_A supply. See 図 8-7 to 図 8-9 for typical IV curves.



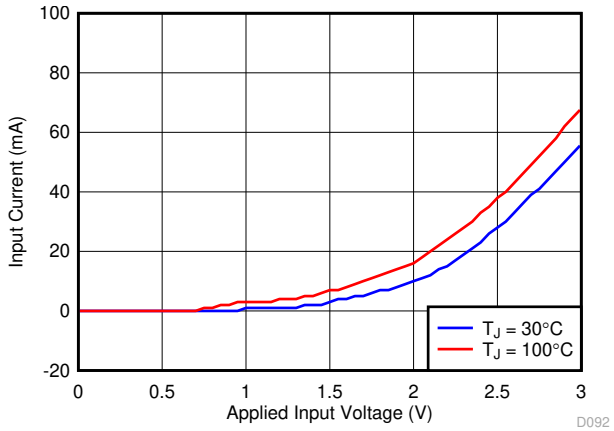
V_A = GND

図 8-7. ESD Diode Current



V_A = HiZ PDI = PDQ = Low

図 8-8. ESD Diode Current



V_A = HiZ PDI = PDQ = High

図 8-9. ESD Diode Current

9 Power Supply Recommendations

9.1 System Power-On Considerations

9.1.1 Control Pins

Upon power-on, the control pins must be set to the proper configuration per 表 7-9, ensuring the absolute maximum values in *セクション 6.1* are not violated. This can be done through either pullup and pulldown resistors to V_A and V_{GND} or through an FPGA or ASIC. If using an FPGA or ASIC, TI does not recommended writing to the control pins or SPI before power is applied to the ADC12D1620 device.

9.1.2 Power On in Non-ECM

If the device is in non-ECM at power on, the control registers are configured in the default mode shown in 表 7-1 and *セクション 7.6.1*. The device may be run in non-ECM or switched to ECM and have the registers changed through the SPI per *セクション 7.5.1.2*. After the device has been configured and has stabilized, run a calibration per *セクション 7.3.3*.

9.1.3 Power On in ECM

If the device is in ECM at power on, the control registers come up in an unknown, random state. The registers must be configured through the SPI per *セクション 7.5.1.2*, or the registers can be set to the default settings in 表 7-1 by toggling the $\overline{ECE}$ pin logic-high and then logic-low. After the device has been configured and has stabilized, run a calibration per *セクション 7.3.3*.

9.1.4 Power-on and Data Clock (DCLK)

Many applications use the DCLK output for a system clock. For the ADC12D1620 device, each I channel and Q channel has its own DCLKI and DCLKQ, respectively. The DCLK output is always active, unless that channel is powered down or the DCLK reset feature is used while the device is in demux mode. As the supply to the device ramps, the DCLK also comes up. While the supply is too low, there is no output at DCLK. As the supply continues to ramp, DCLK functions intermittently with irregular frequency, but the amplitude continues to track with the supply. Much below the low end of operating supply range of the ADC12D1620, the DCLK is already fully operational.

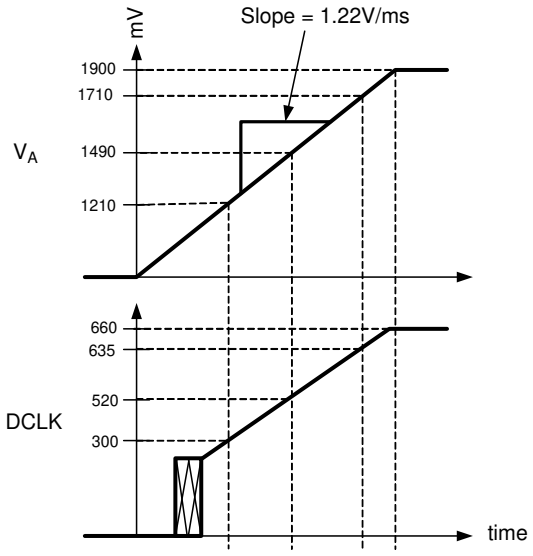


図 9-1. Supply and DCLK Ramping

10 Layout

10.1 Layout Guidelines

10.1.1 Power Planes

Source all supply buses for the ADC from a common linear voltage regulator. This ensures that all power buses to the ADC are turned on and off simultaneously. This single source is split into individual sections of the power plane, with individual decoupling and connections to the different power supply buses of the ADC. Due to the low voltage but relatively high supply-current requirement, the optimal solution may be to use a switching regulator to provide an intermediate low voltage, which is then regulated down to the final ADC supply voltage by a linear regulator.

Power for the ADC must be provided through a broad plane, which is located on one layer adjacent to the ground plane(s). Placing the power and ground planes on adjacent layers provides low-impedance decoupling of the ADC supplies, especially at higher frequencies. The output of a linear regulator must feed into the power plane through a low-impedance, multi-via connection. The power plane must be split into individual power peninsulas near the ADC. Each peninsula must feed a particular power bus on the ADC, with decoupling for that power bus connecting the peninsula to the ground plane near each power/ground pin pair. Using this technique can be difficult on many printed circuit CAD tools. To work around this, 0-Ω resistors can be used to connect the power source net to the individual nets for the different ADC power buses. As a final step, the 0-Ω resistors can be removed, and the plane and peninsulas can be connected manually after all other error checking is completed.

10.1.2 Bypass Capacitors

TI's general recommendation is to have one 100-nF capacitor for each power/ground pin pair. The capacitors must be surface-mount multi-layer ceramic-chip capacitors similar to Panasonic part number ECJ-0EB1A104K.

10.1.3 Ground Planes

Grounding must done using continuous full ground planes to minimize the impedance for all ground return paths and provide the shortest possible image/return path for all signal traces.

10.1.4 Power System Example

See 図 10-1 for an example with continuous ground planes (except where clear areas are needed to provide appropriate impedance management for specific signals). Power is provided on one plane, with the 1.9-V ADC supply being split into multiple zones or peninsulas for the specific power buses of the ADC. Decoupling capacitors are connected between these power bus peninsulas and the adjacent ground planes using vias. The capacitors are located as close as possible to the individual power/ground pin pairs of the ADC. In most cases, this means the capacitors are located on the opposite side of the PCB to the ADC.

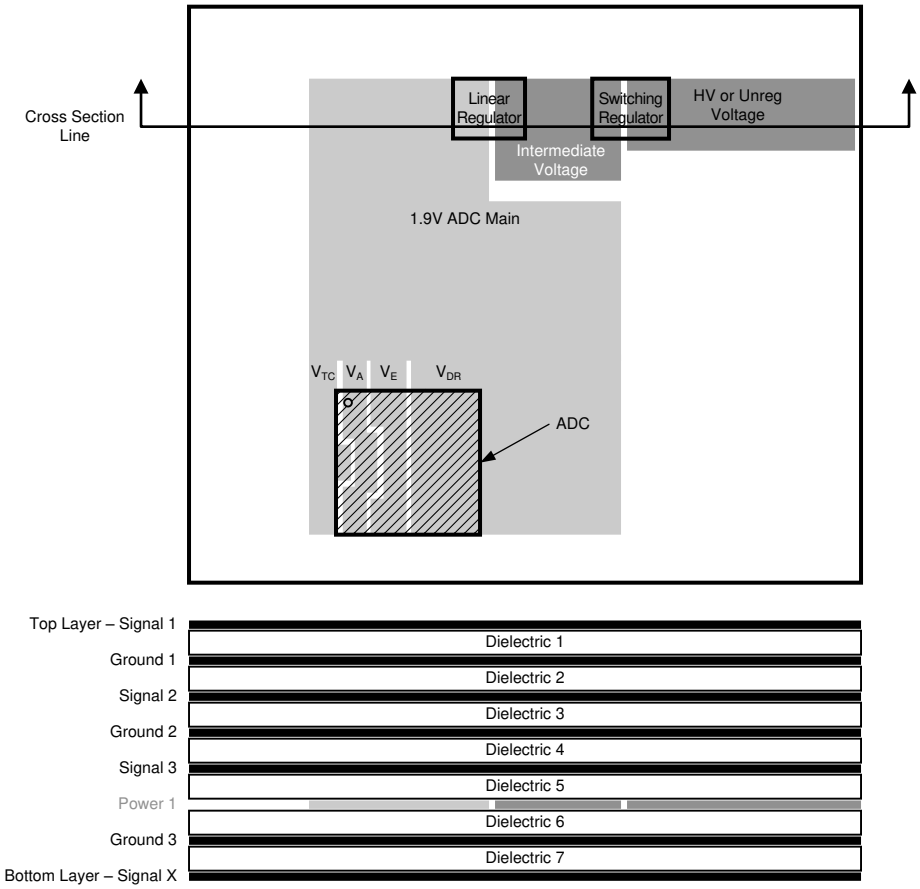


図 10-1. Power and Grounding Example

10.2 Layout Example

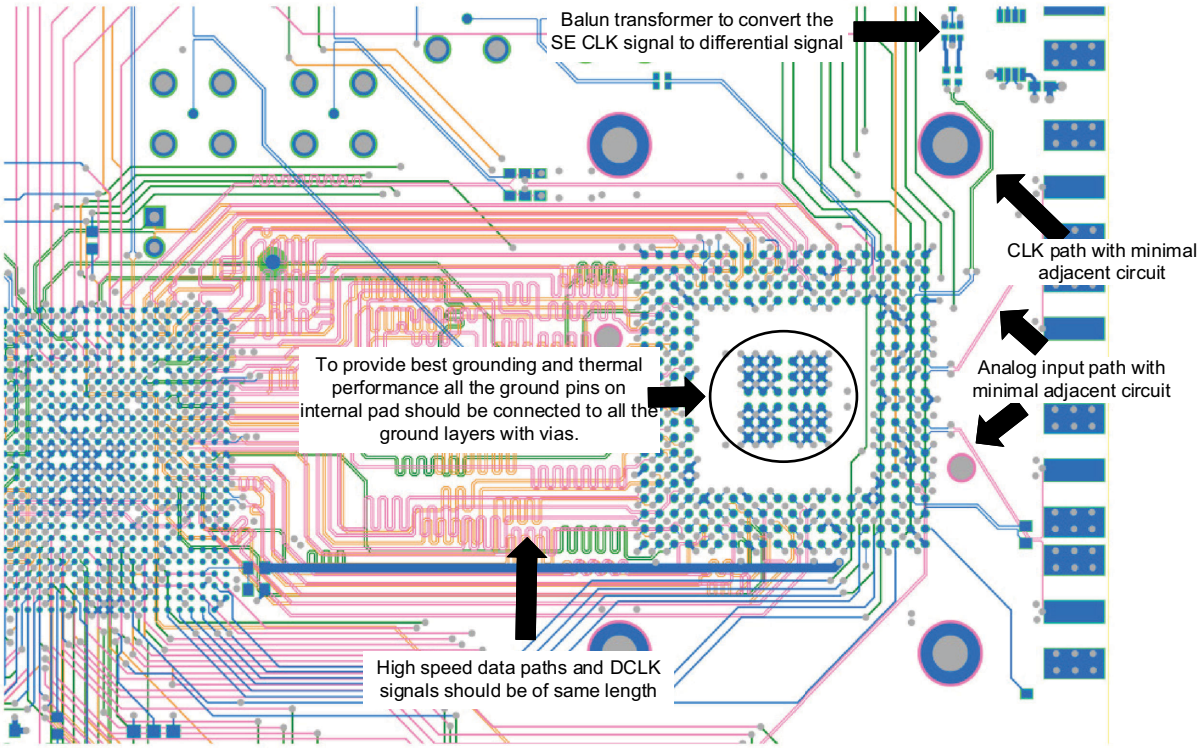


図 10-2. ADC12D1620 Layout Example: Top Side and Inner Layers

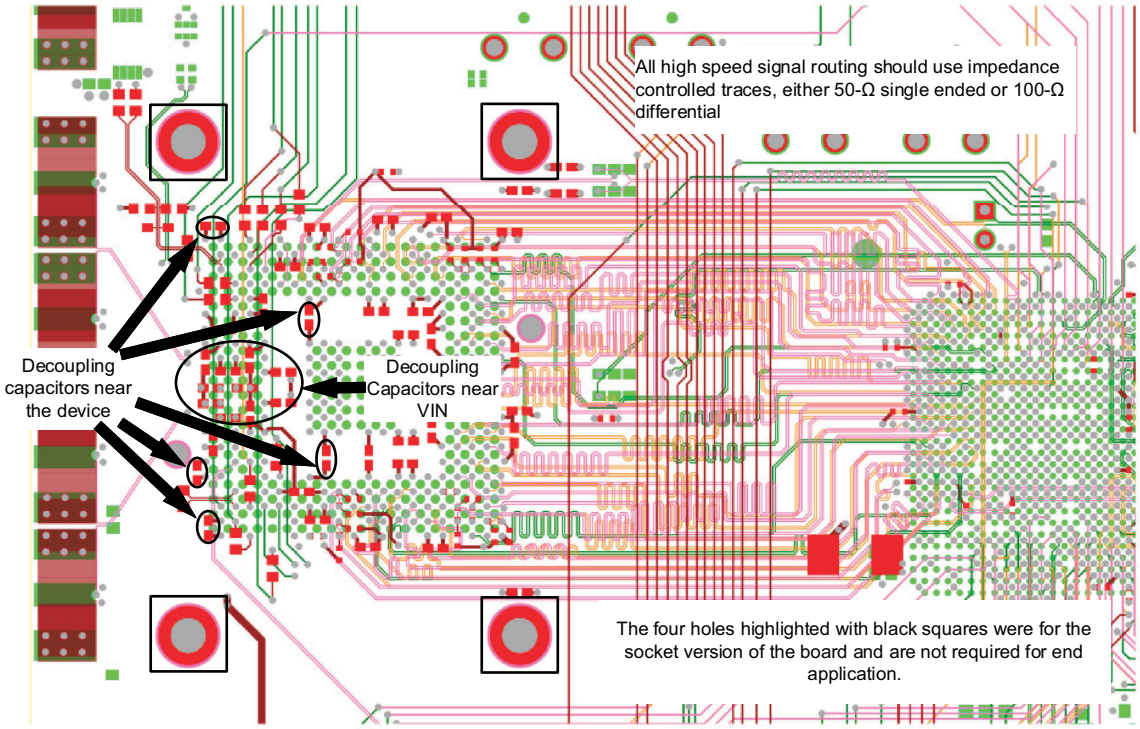


図 10-3. ADC12D1620 Layout Example: Bottom Side and Inner Layers

10.3 Thermal Considerations

The CCGA package is a modified ceramic-land-grid array with an added heat sink. The signal pins on the outer edge are 1.27-mm pitch, while the pins in the center attached to the heat sink are 1 mm. The smaller pitch for the center pins is to improve the thermal resistance. The center pins of the package are attached to the back of the die through a heat sink. Connecting these pins to the PCB ground planes with a low thermal resistance path is the best way to remove heat from the ADC. These pins must also be connected to the ground planes through low impedance path for electrical purposes.

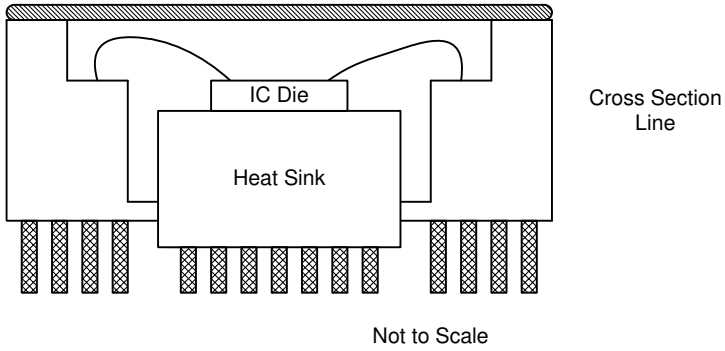


図 10-4. CPGA Conceptual Drawing

10.4 Board Mounting Recommendation

Proper thermal profile is required to establish re-flow under the package and ensure all joints meet profile specifications.

表 10-1. Solder Profile Specification

RANGE UP	PEAK TEMPERATURE (T_{PK})	MAXIMUM PEAK TEMPERATURE	RAMP DOWN
≤ 4°C/sec	210°C ≤ t_{PK} ≤ 215°C	≤ 220°C	≤ 5°C/sec

The 220°C peak temperature is driven by the requirement to limit the dissolution of lead from the high-melt pin to the eutectic solder. Too much lead increases the effective melting point of the board-side joint and makes it much more difficult to remove the device if module rework is required.

Cool-down rates and methods affect CCGA assemble yield and reliability. Picking up boards or opening the oven while solder joints are in molten state can disturb the solder joint. Do not pick up boards until the solder joints have fully solidified. Board warping may potentially cause CCGA lifting off pads during cooling and this condition can also cause pin cracking when severe. This warping is a result of a high differential cooling rate between the top and bottom of the board. Both conditions can be prevented by using even top and bottom cooling.

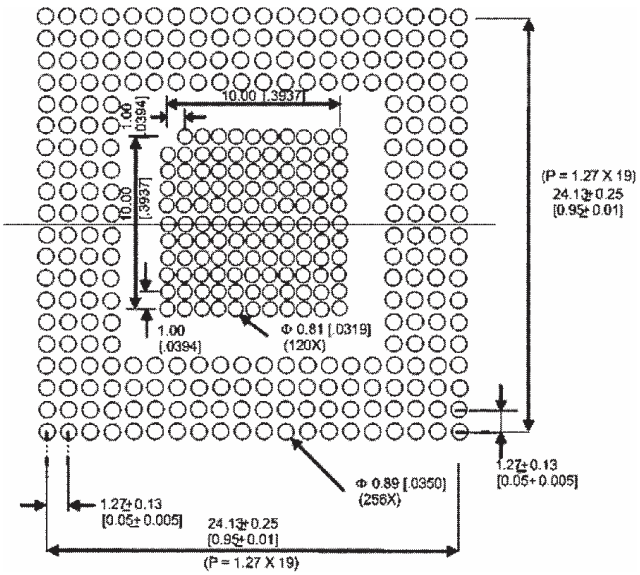


図 10-5. Landing Pattern Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

APERTURE (SAMPLING) DELAY is the amount of delay, measured from the sampling edge of the CLK input, after which the signal present at the input pin is sampled inside the device.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample-to-sample. Aperture jitter can be effectively considered as noise at the input.

CODE ERROR RATE (CER) is the probability of error and is defined as the probable number of word errors on the ADC output per unit of time divided by the number of words seen in that amount of time. A CER of 10^{-18} corresponds to a statistical error in one word about every 31.7 years for the adc12d1620QML-SP .

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. It is measured at the relevant sample rate, f_{CLK}, with f_{IN} = 1 MHz sine wave.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is method of specifying signal-to-noise and distortion ratio, or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and states that the converter is equivalent to a perfect ADC of this many (ENOB) number of bits.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from offset and full-scale errors. the positive gain error is the offset error minus the positive full-scale error. The negative gain error is the negative full-scale error minus the offset error. The gain error is the negative full-scale error minus the positive full-scale error; it is also equal to the positive gain error plus the negative gain error.

GAIN FLATNESS is the measure of the variation in gain over the specified bandwidth. For example, for the adc12d1620QML-SP, from D.C. to Fs/2 is to 800 MHz for the non-DES mode and from D.C. to Fs/2 is 1600 MHz for the DES mode.

INTEGRAL NON-LINEARITY (INL) is a measure of worst-case deviation of the ADC transfer function from an ideal straight line drawn through the ADC transfer function. The deviation of any given code from this straight line is measured from the center of that code value step. The best fit method is used.

INSERTION LOSS is the loss in power of a signal due to the insertion of a device, for example the adc12d1620, expressed in dB.

INTERMODULATION DISTORTION (IMD) is a measure of the near-in 3rd order distortion products ($2f_2 – f_1$, $2f_1 – f_2$), which occur when two tones that are close in frequency (f_1, f_2) are applied to the ADC input. It is measured from the input tone's level to the higher of the two distortion products (dBc) or simply the level of the higher of the two distortion products (dBFS).

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^N \quad (3)$$

where

- V_{FS} is the differential full-scale amplitude V_{IN_FSR} as set by the FSR input
- N is the ADC resolution in bits, which is 12 for the adc12d1620

LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) DIFFERENTIAL OUTPUT VOLTAGE (V_{ID} and V_{OD}) is two times the absolute value of the difference between the V_D+ and V_D- signals; each signal measured with respect to ground. V_{OD} peak is $V_{OD,P}$= (V_D+ – V_D–) and V_{OD} peak-to-peak is $V_{OD,P\text{-}P}$= 2 × (V_D+ – V_D–); for this product, the V_{OD} is measured peak-to-peak.

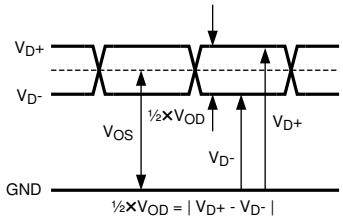


図 11-1. LVDS Output Signal Levels

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the D+ and D– pins output voltage with respect to ground; that is , [(V_D+) +(V_D-)]/2. See 図 11-1.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential −V_{IN} / 2 with the FSR pin low. For the adc12d1620 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

NOISE FLOOR DENSITY is a measure of the power density of the noise floor, expressed in dBFS/Hz and dBm/Hz. '0 dBFS' is defined as the power of a sinusoid that precisely uses the full-scale range of the ADC.

NOISE POWER RATIO (NPR) is the ratio of the sum of the power inside the notched bins to the sum of the power in an equal number of bins outside the notch, expressed in dB.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8 k samples to result in an average code of 2047.5.

OUTPUT DELAY (t_{OD}) is the time delay (in addition to latency) after the rising edge of CLK+ before the data update is present at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2 V to 0 V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of input clock cycles between initiation of conversion and when that data is presented to the output driver stage. The data lags the conversion by the latency plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential +V_{IN} / 2. For the ADC12D1620 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

SIGNAL-TO-NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the fundamental for a single-tone to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL-TO-NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the fundamental for a single tone to the rms value of all of the other spectral components below half the input clock frequency, including harmonics but excluding DC.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding DC.

$R_{\theta JA}$ is the thermal resistance between the junction to ambient.

$R_{\theta JB}$ is the thermal resistance between the junction and the circuit board close to the outer pins.

$R_{\theta JT}$ is the thermal resistance between the junction and the case, measured at the lid of the package.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}} \quad (4)$$

where

- A_{f1} is the RMS power of the fundamental (output) frequency
- A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

11.1.2 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Engineering Samples

Engineering samples are available for order and are identified by the "MPR" in the orderable device name (see Packaging Information in the Addendum). Engineering (MPR) samples meet the performance specifications of the datasheet at room temperature only and have not received the full space production flow or testing. Engineering samples may be QCI rejects that failed tests that would not impact the performance at room temperature, such as radiation or reliability testing.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962F1220502VXF	Active	Production	CCGA (NAA) | 376	36 | EIAJ TRAY (10+1)	ROHS Exempt	SNPB	Level-1-NA-UNLIM	-55 to 125	F1220502VXF ADC12D1620
5962F1220502VXF.A	Active	Production	CCGA (NAA) | 376	36 | EIAJ TRAY (10+1)	ROHS Exempt	SNPB	Level-1-NA-UNLIM	-55 to 125	F1220502VXF ADC12D1620
ADC12D1620CCMLS	Active	Production	CCGA (NAA) | 376	36 | EIAJ TRAY (10+1)	-	Call TI	Call TI	-55 to 125	ADC12D1620CC MLS
ADC12D1620CCMLS.A	Active	Production	CCGA (NAA) | 376	36 | EIAJ TRAY (10+1)	-	Call TI	Call TI	-55 to 125	ADC12D1620CC MLS
ADC12D1620CCMPR	Active	Production	CCGA (NAA) | 376	36 | EIAJ TRAY (10+1)	-	Call TI	Call TI	25 to 25	ADC12D1620CC (MPR, MPR E.S.)
ADC12D1620CCMPR.A	Active	Production	CCGA (NAA) | 376	36 | EIAJ TRAY (10+1)	-	Call TI	Call TI	25 to 25	ADC12D1620CC (MPR, MPR E.S.)
ADC12D1620LGMLS	Active	Production	CLGA (FVA) | 256	1 | EIAJ TRAY (10+1)	-	Call TI	Call TI	-55 to 125	ADC12D1620LG MLS
ADC12D1620LGMLS.A	Active	Production	CLGA (FVA) | 256	1 | EIAJ TRAY (10+1)	-	Call TI	Call TI	-55 to 125	ADC12D1620LG MLS
ADC12D1620LGMPR	Active	Production	CLGA (FVA) | 256	1 | EIAJ TRAY (10+1)	-	Call TI	Call TI	25 to 25	(ADC12D1620CC, ADC 12D1620LG) (MPR, MPR E.S.)
ADC12D1620LGMPR.A	Active	Production	CLGA (FVA) | 256	1 | EIAJ TRAY (10+1)	-	Call TI	Call TI	25 to 25	(ADC12D1620CC, ADC 12D1620LG) (MPR, MPR E.S.)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

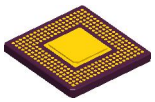
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

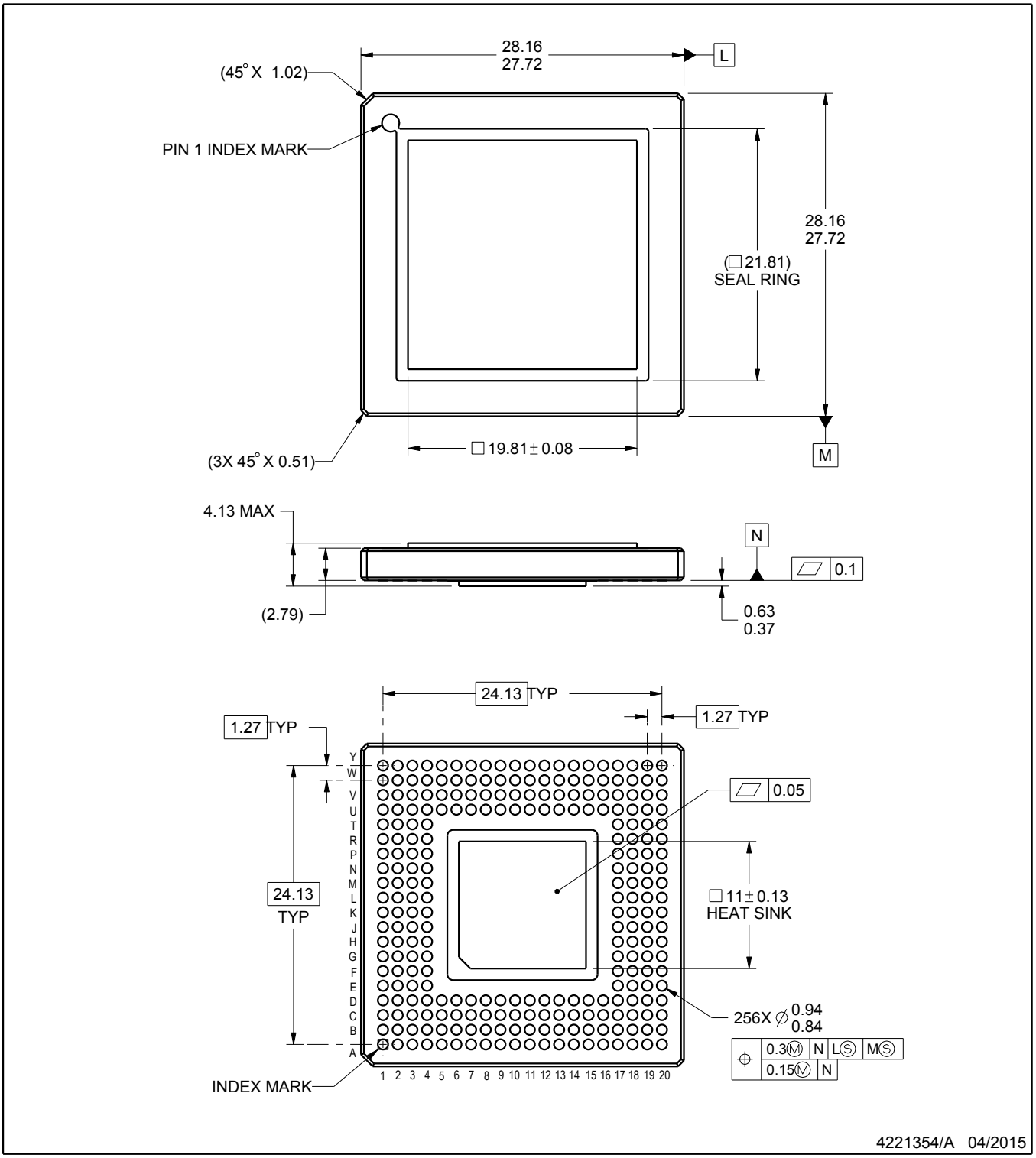


PACKAGE OUTLINE

FVA0256A

CLGA - 4.13 mm max height

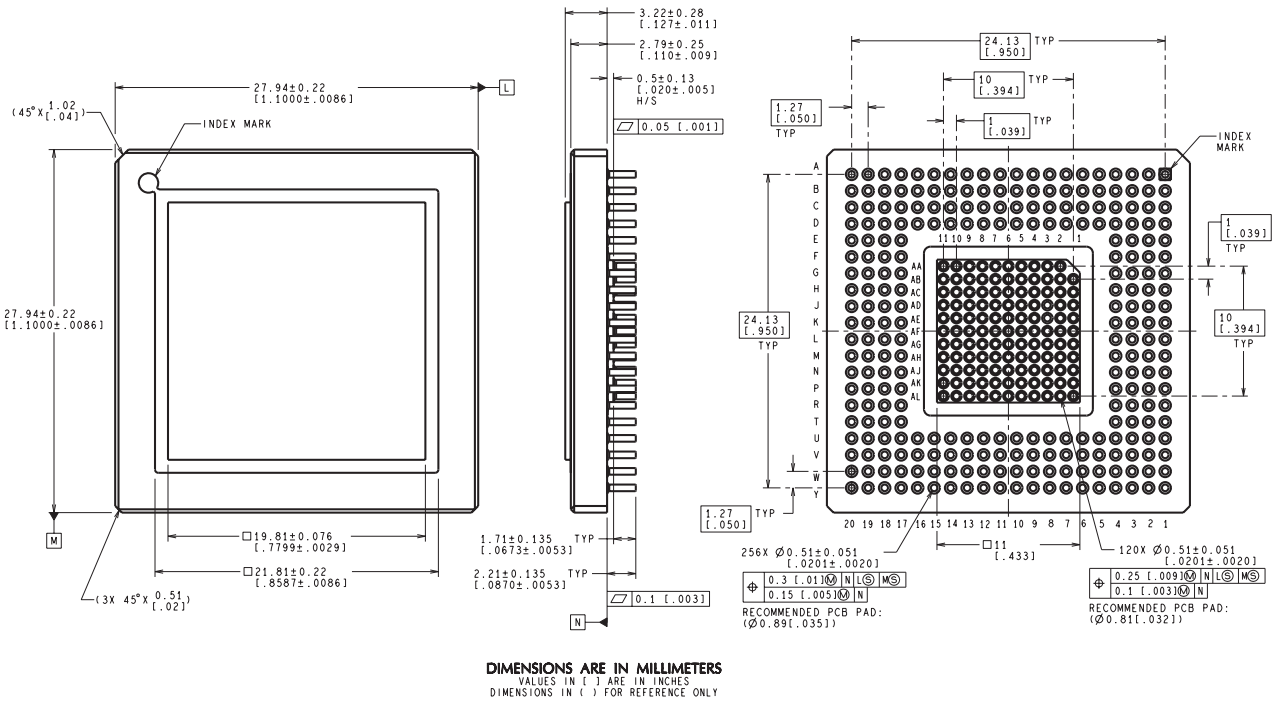
Ceramic Land Grid Array



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

NAA0376A



DIMENSIONS ARE IN MILLIMETERS
VALUES IN [ ] ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

CCC376A (Rev D)

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月