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Contents

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Using the ADS8361 with the MSP430 USI port

By Tom Hendrick (Email: t-hendrick@ti.com)
Applications Engineer, Data Acquisition Products

Introduction

The ADS8361 is a dual, 16-bit, 500-kSPS, analog-to-digital converter (ADC) with four fully differential input channels grouped into two pairs for high-speed, simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differentially to the input of the ADC. This provides excellent common-mode rejection of 80 dB at 50 kHz, which is important in high-noise environments.

MSP430 devices such as the new MSP430F2013, which contain a universal serial interface (USI), can be used in a very simple and straightforward interface that requires no "glue logic" and very little software overhead. Applications that require precise timing of simultaneous data acquisition channels can use this interface to achieve desired system results.

Hardware

The hardware used to produce the timing diagrams in Figures 2 and 3 includes the eZ430-F2013 Development Tool and the ADS8361EVM.

ADS8361EVM

The ADS8361 is a member of the motor control products family of serial ADCs available from Texas Instruments (TI). The EVM provides a platform to demonstrate the functionality of the ADS8361 ADC with various TI DSPs and microcontrollers while allowing easy access to all analog and digital signals for customized end-user applications. For more information on the EVM, see Reference 1.

eZ430-F2013 Development Tool

The eZ430-F2013 is a complete MSP430 development tool including all the hardware and software necessary to evaluate the MSP430F2013. The hardware is provided in a convenient USB stick form factor. The eZ430-F2013 uses the IAR Embedded Workbench integrated development environment (IDE) to provide full emulation with the option of designing a stand-alone system or detaching the removable target board to integrate into an existing design. For more information, visit www.ti.com/ez430

Hardware interface

A simple three-wire interface is the minimum requirement to connect the eZ430-F2013 and the ADS8361EVM (see Table 1). The hardware connections are shown in Figure 1. The CLOCK, (RD + CONVST), and Serial Data A pins from the ADS8361 are connected respectively to the SCLK, MOSI, and MISO pins of the USI port. The chip select ($\overline{CS}$) pin is grounded because only one ADC is placed on the port. If more than one device is on the bus, then chip select should be controlled by any available GPIO on the MSP430 device.

Figure 1. Hardware interface block diagram

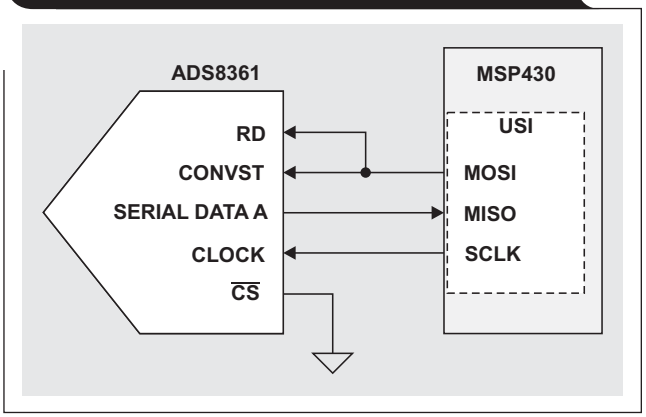


Table 1. Cable requirements

ADS8361EVM	eZ430-F2013
J2.1 — $\overline{CS}$*	Optional GPIO
J2.3 — CLOCK	P1.5
J2.13 — Serial Data A	P1.7
J2.7 — (RD + CONVST)**	P1.6

* $\overline{CS}$ can be held to ground by placing a shunt jumper from J2.1 to J2.2.
** (RD + CONVST) is created by placing the shunt jumper in location W2 on pins 1 and 2.

Software interface

All of the software was written and compiled using the Kickstart version of IAR Embedded Workbench for the MSP430. This software is the free version of the IDE and is available for download at www.ti.com/ez430 under "TOOL SUPPORT." The code used in these examples is available upon request.

USI settings

The USI module provides the basic functionality to support synchronous serial communication schemes. The USI includes built-in hardware functionality to ease the implementation of SPI communication. The USI module also includes interrupts to further reduce the software overhead.

USI control registers 0 and 1 (USICTL0 and USICTL1) set up the basic operation of the serial interface. The port is configured in SPI master mode by setting bits 3, 5, 6, and 7 in USICTL0. The USI counter interrupt is set in

USICTL1 to provide an efficient means of SPI communication with minimal software overhead.

The serial clock polarity, source, and speed are controlled by settings in the USI clock control register (USICKCTL). For the purposes of this article, the polarity of the clock is set to zero (dwells low), and the clock source is the SMCLK with a division factor of one.

Bit clocking and shift register configuration are controlled in the USI port by the bit settings in the USI bit count register (USICNT). The USICNT register has 5 bits that provide up to 32 SCLK cycles per transfer. Setting the USICNT to 0×13 transmits 19 serial clocks from the MSP430 to the ADS8361 on each conversion cycle. Setting the USI16B bit in the USICNT register causes the shift register to act as a 16-bit transmit/receive buffer. Transmitted data is MSB-aligned and commences with the first SCLK cycle.

Starting a conversion

Connecting the MOSI output of the USI port to both the RD and the CONVST inputs on the ADS8361 starts a conversion cycle, and the conversion results are presented on the serial data output pins of the device.

The ADS8361 will begin to output the conversion results (MSB first) on the fourth SCLK cycle. Since the shift register holds the last 16 bits of received data, the entire 16-bit conversion result is captured for further processing. The timing diagram in Figure 2 shows the entire process.

ADS8361 operating modes

The ADS8361 has four operational modes controlled by the M0 and M1 pins. The ADS8361EVM provides jumpers to statically set the operating mode. Using GPIO output on the MSP430 permits the operating mode to be controlled by the microprocessor as well.

For two-channel operation, the EVM should be configured in Mode I or II. Depending on the MSP430 being used, the user has several options on how to receive conversion results. Devices with multiple serial ports can receive data from both the Serial Data A and Serial Data B outputs of the ADS8361. This method involves setting up one port as an SPI master and the other as an SPI slave. The master SPI port would share SCLK with the slave port, and the two serial output pins would be routed to MISO and MOSI.

Two-channel simultaneous sampling

In the case of the eZ430-F2013, there is only a single serial port, which means the ADS8361 must be set in Mode II to receive conversion results from the two simultaneously sampled input channels. This mode presents both conversion results at the Serial Data A output pin (see Figure 3).

Figure 2. Complete single-channel conversion cycle

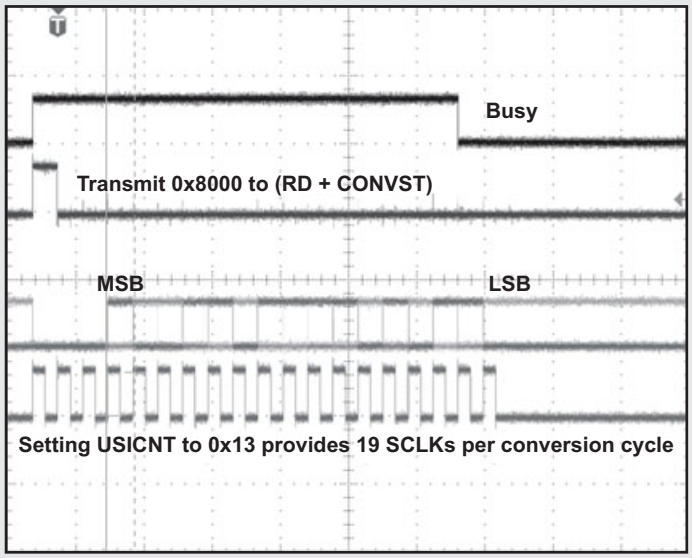
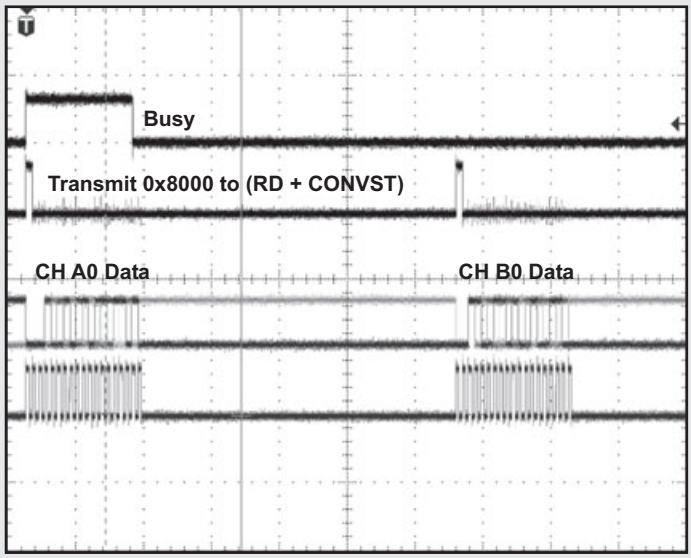


Figure 3. Complete two-channel conversion cycle



ADS8361 channel ID bits

The serial output stream of the ADS8361 also incorporates two channel ID bits so the controller can use software methods to decipher the received channel information. The first ID bit determines the channel pair, A or B. The second ID bit determines the sampled channel, 0 or 1. In Mode II operation, two of the input channels are converted and a single ID bit is included in the output data stream.

The A/B-channel ID bit is not used in this mode because the pair of inputs sampled depends on the A0 input control pin of the ADS8361. When A0 is low, the channel A0/B0 input pairs are sampled. When A0 is high, the channel A1/B1 input pairs are sampled.

The ADS8361EVM provides a jumper to statically set the input pair via the A0 pin. This too can be controlled if desired with a GPIO on the MSP430, letting the user realize up to four-channel operation—two pairs of simultaneously sampled inputs.

Four-channel sampling

Modes III and IV allow the user to realize four-channel operation of the ADS8361. Mode III provides data from the Serial Data A and B outputs. Receiving data from all four conversions in this mode would require two serial ports configured in a master/slave relationship as described previously.

Mode IV allows a single serial port to receive all four conversion results via the Serial Data A output. In this mode, both the A/B- and 0/1-channel ID bits are passed through to the conversion results. What becomes problematic in this mode when used with the eZ430-F2013 is that the ID bits are essentially lost in the shift register. It is possible to recover these bits via software, but this increases software overhead and adds unnecessary complexity.

When operating in four-channel sequential mode, the ADS8361 can be initialized in such a way that channel integrity can be maintained without the need to decipher the ID bits at all. Using available GPIO, this can be done with a simple software loop at the start of the program that actively manipulates the state of the A0, M0, and M1 inputs. An alternative is to simply ignore the first set of conversion results. The ADS8361 powers up in Mode I by default; if M0 and M1 are fixed to V_{CC} at power up, the device will enter Mode IV operation with the second conversion cycle. This action presents channel A0 data with the third SPI transfer, followed sequentially by channels B0, A1, and B1.

Conclusion

Using the high-performance ADS8361 with the USI port of MSP430 processors is a relatively simple and straightforward task. Very little software overhead is involved; there is no need to shift or concatenate conversion results as was the case in the simple 8-bit SPI interface of the older UART port found in previous generations of the MSP430. The interface method described in this article brings a new level of flexibility to MSP430 applications that require multichannel, simultaneous data acquisition.

References

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Document Title	**TI Lit. #**
1. "ADS7861/8361 EVM User's Guide"	slau094
2. "Dual, 500kSPS, 16-Bit, 2 + 2 Channel, Simultaneous Sampling Analog-to-Digital Converter," ADS8361 Datasheet	sbas230
3. "MSP430x2xx Family User's Guide"	slau144

Related Web sites

dataconverter.ti.com
www.ti.com/ez430
www.ti.com/msp430
www.ti.com/sc/device/ADS8361
www.ti.com/sc/device/MSP430F2013

TPS61059 powers white-light LED as photoflash or movie light

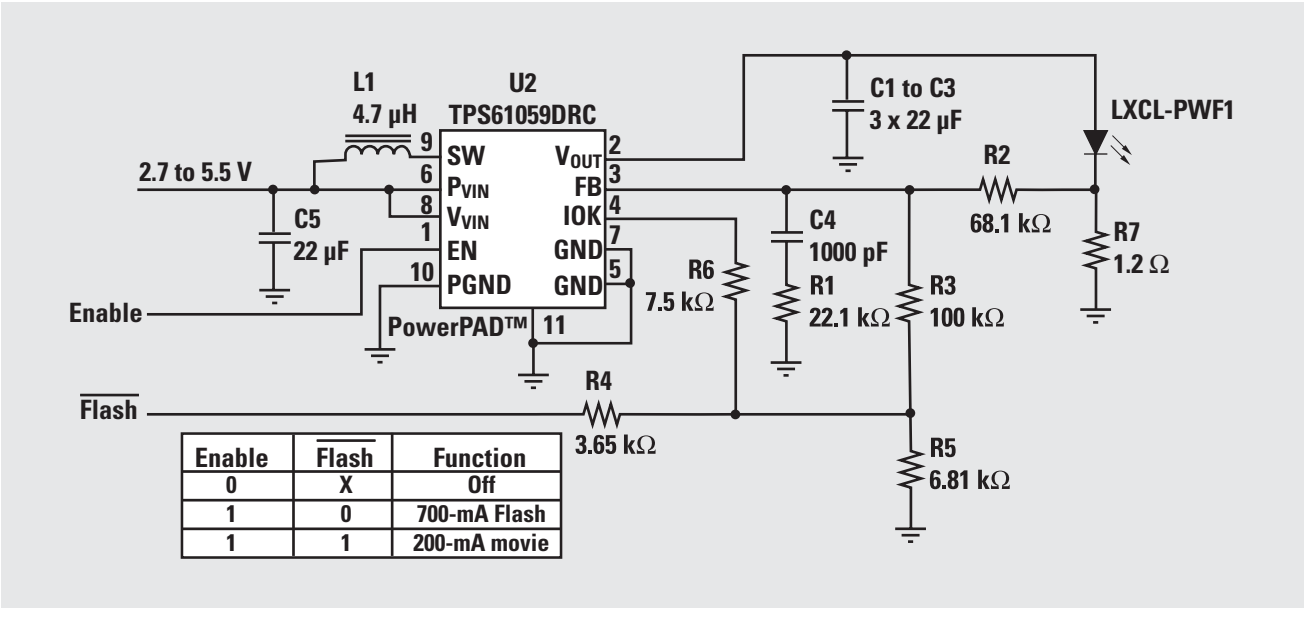
By Scot Lester (Email: scotlester@ti.com)
Portable Power DC/DC Applications

Manufacturers of smart phones, cell phones, and PDAs are incorporating digital camera technology into their products so they can be used as cameras as well as for their intended use. Each of these devices uses a megapixel CCD camera that generally performs poorly in low-light conditions such as indoors, on cloudy days, or in the morning or evening. To provide a photoflash function for these low-light conditions, manufacturers are starting to turn to new high-power, white-light LEDs. These LEDs output a wide light spectrum and are compact and easy to control. They operate at much lower voltages than Xenon gas-discharge tubes, which require hundreds of volts to flash. Additionally, white-light LEDs can be left on continuously to provide lighting for digital movie photography.

One challenge in using white-light LEDs is powering them with the wide input-voltage range that batteries present. A white-light LED can have a forward voltage ranging from 3.2 to 4.8 V. This falls in the middle of most battery input-voltage ranges, which means the converter needs to be able to step up or step down the input voltage to maintain the forward voltage of the LED.

The Texas Instruments (TI) TPS61058 and TPS61059 are synchronous boost converters for driving high-current LEDs for photoflash and movie-light applications. The TPS61058 can provide up to 500 mA and the TPS61059 up to 800 mA of LED current from a 3.3-V source. The TPS6105x family of boost converters has a special down mode that allows it to step down the input voltage when the input voltage is higher than the forward voltage of the LED. Thus, the TPS61058/9 can both step up and step down the input voltage, allowing these devices to drive a wide range of LEDs from a wide range of input voltages. Figure 1 shows the TPS61059 configured to provide 700 mA of current for an LED photoflash or a constant 200 mA of current for a movie light from an input battery voltage between 2.7 and 5.5 V. Two digital inputs are used to select the LED's mode of operation—off, photoflash, or movie light. The photoflash, movie-light, and soft-start current supplied by the TPS6105x are programmed by an external resistor network that allows the TPS6105x to drive a variety of high-power white-light LEDs.

Figure 1. TPS61059 configured for 700-mA LED photoflash or 200-mA LED movie light



Enable	Flash	Function
0	X	Off
1	0	700-mA Flash
1	1	200-mA movie

The TPS6105x achieves up to 93% efficiency in movie-light mode and up to 81% efficiency in high-current photoflash mode (see Figure 2). During shutdown, the device completely disconnects the LED from the input source to prevent draining the battery and consumes a low 100 nA of quiescent current.

Additional features are integrated-circuit protection for soft start, thermal shutdown, and open or shorted LEDs, and an integrated anti-ring power switch for low-EMI operation in noise-sensitive applications. All of this is packaged in a 10-pin QFN, which allows for a total solution size of less than 80 mm^2.

Reference

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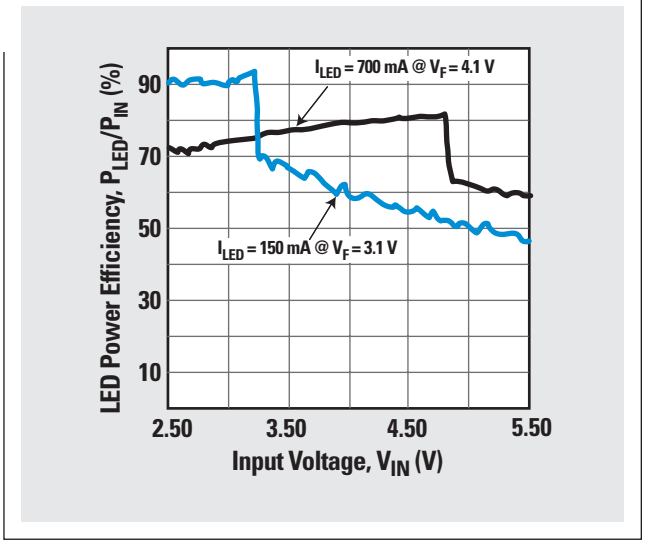
Document Title	TI Lit. #
1. "Synchronous Boost Converter with Down Mode High Power White LED Driver," TPS61058/9 Datasheet	.slvs572

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS61058
www.ti.com/sc/device/TPS61059

Figure 2. TPS61059 LED power efficiency versus input voltage



TPS65552A powers portable photoflash

By Scot Lester (Email: scotlester@ti.com)
Portable Power DC/DC Applications

Upper-end equipment for film-based or digital photography requires Xenon flash tubes to photograph in low-light conditions. Xenon flash tubes provide a burst of high-intensity light that is essential for photography of objects at a distance, moving at high speeds, or in low-light conditions. The light spectrum generated by a Xenon gas-discharge tube closely replicates that of the sun, providing very accurate color reproduction.

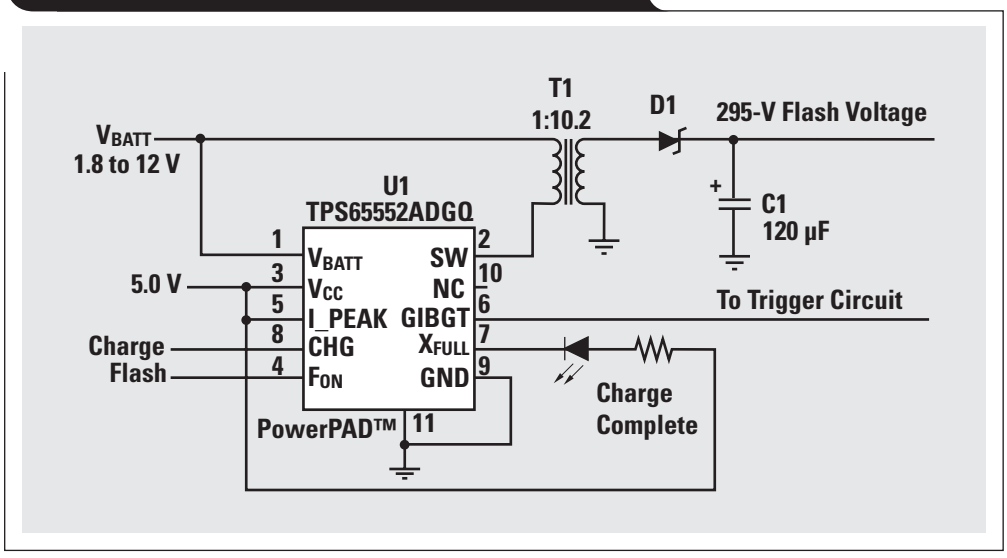
Xenon flash tubes require a high voltage across their electrodes to flash once a trigger signal is applied. This voltage is typically around 300 V. All of the energy needed to flash the lamp is stored in a bulk capacitor called a photoflash capacitor. Once the lamp is triggered, all of the energy stored in the photoflash capacitor is discharged through the flash tube to produce light. The stored energy in the photoflash capacitor is provided by a specialized boost converter that charges the photoflash capacitor up to 300 V from a much lower battery-input voltage. In the past, this converter was built of bulky discrete components that were difficult to incorporate into the space available in small devices such as cameras.

The Texas Instruments (TI) TPS65552A greatly simplifies and reduces the size of the photoflash charger circuit. Figure 1 shows a photoflash capacitor charger based on this device. The TPS65552A provides all the necessary charging controls, output feedback, charge completion status, insulated gate bipolar transistor (IGBT) driver, and circuit protections necessary to implement a small, efficient photoflash charger.

The TPS65552A is based on a flyback topology. The output voltage is sensed during the off period of the internal switch, at which time the output voltage is reflected back to the input through the transformer. This eliminates the need for a bulky, high-voltage feedback network on the output and also provides electrical isolation from the input to the output. Once the output voltage reaches its target value, the TPS65552A automatically stops charging and an open-collector output goes low, thus signaling a "ready to flash" condition. This output can drive a status-indicating LED or an input to a microcontroller.

The I_PEAK pin of the TPS65552A controls the peak current that flows through the primary of the flyback transformer, T1, during each switch cycle. To adjust the capacitor charging time, the primary current can be dynamically adjusted from 0.9 to 1.8 A by changing the voltage applied to the I_PEAK pin. This feature allows a microcontroller to dynamically control the current draw of the charger for power management. For example, in a digital still camera,

Figure 1. TPS65552A photoflash capacitor charger



a microcontroller can reduce the charger current when a high-current zoom motor is operating, so that both the zoom motor and charger can function at the same time without exceeding the maximum current capability of the camera's battery (see Figure 2). This feature can also be used to extend battery run time. Reducing the peak currents during charging reduces the average current consumption so that a weak battery can still charge the photoflash capacitor.

Historically, the flash has been triggered with a push-button switch or a silicon-controlled rectifier (SCR). However, newer flash modes such as red-eye reduction use multiple bursts of the Xenon lamp. The lamp is triggered for a short flash that does not fully discharge the photoflash capacitor. Then, after a short delay, the lamp is retriggered for the main flash. The push button and SCR cannot reliably start and stop the lamp midflash. The IGBT is capable of handling the currents, which are typically 150 A during a flash. However, like a MOSFET, the IGBT gate requires a large current pulse to quickly turn on; so a high-current driver is required.

The TPS65552A has an integrated high-current buffer to drive the IGBT gate used in the trigger circuit. The IGBT can be driven on and off during flashes to support flash modes such as red-eye reduction or evaluated through the lens (E-TTL).

Reference

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Document Title **TI Lit. #**

1. "Integrated Photo Flash Charger and IGBT Driver," TPS65552A Datasheet slvs567

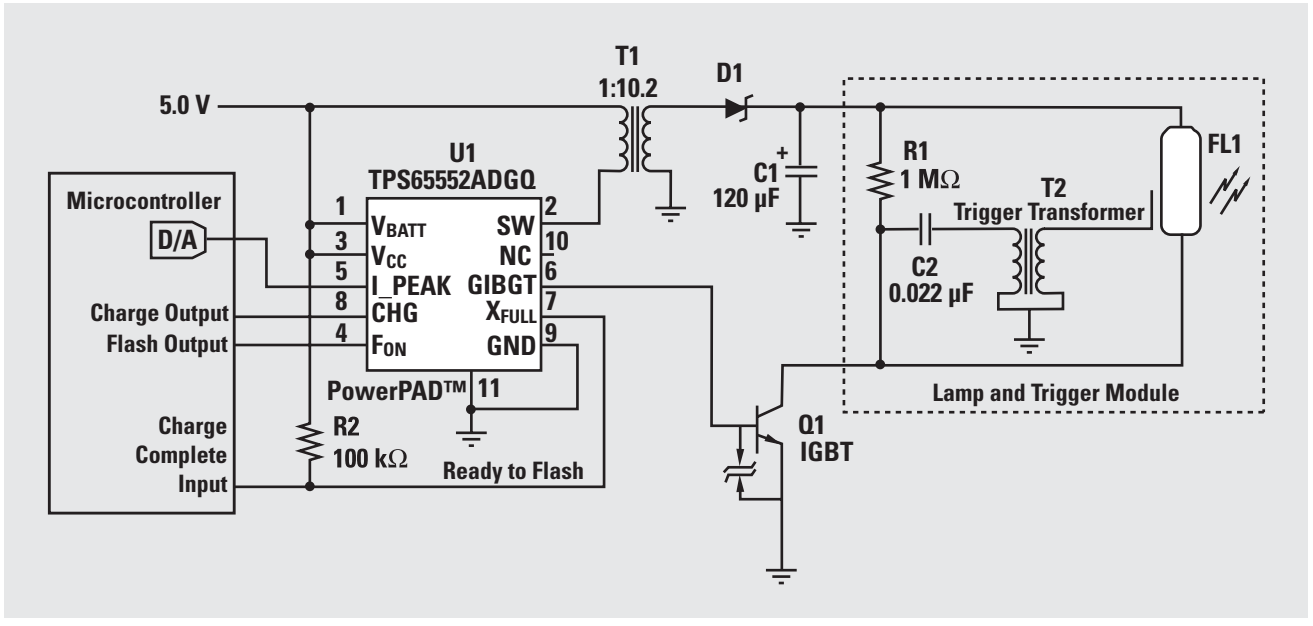
Related Web sites

power.ti.com
www.ti.com/sc/device/TPS65552A

Table 1. Typical parts list for circuit in Figure 2

DEVICE	DESIGNATOR	DESCRIPTION	MANUFACTURER
330 FW 120A	C1	Capacitor, aluminum, 120 µF, 330 VDC, ±20%	Rubycon
C3216X7R2J223KT	C2	Capacitor, ceramic, 0.022 µF, 630 V, X7R, 10%	TDK
ES1G	D1	Diode, rectifier, 1 A, 400 V	Diodes Inc.
36FT050	FL1	Flash tube, 400 V max	Xicon
SSM25G45EM	Q1	Transistor, N-channel IGBT, 450 V, 150 A	Silicon Standard
CTX16-17360	T1	Transformer, flyback, 1:10.2	Coiltronics
422-2304	T2	Transformer, trigger	Xicon

Figure 2. Complete photoflash module with power and flash management



Single-chip bq2403x power-path manager charges battery while powering system

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The lithium-ion (Li-ion) battery is widely adopted in portable devices because of its high energy density on both a gravimetric and volumetric basis. Users of applications such as smartphones, PDAs, and MP3 players want to be able to operate the device from an input source without a battery. This requires a power architecture with two separate paths for device system power and battery charging, called "power-path management."

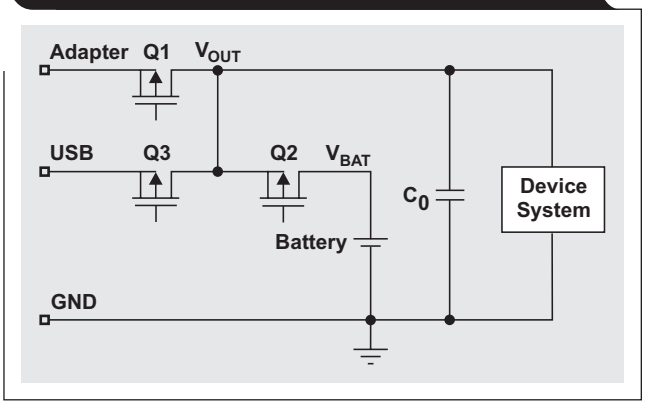
Dynamic power-path-management (DPPM) battery charger

In the most commonly used battery-charging and system-power configuration, the system load is directly connected to the battery-charger output. This architecture is simple and low-cost but can cause improper charge termination and false safety-timer warnings due to ineffective control of the battery charge current.

The bq2403x family of DPPM battery chargers has a power-sharing capability of simultaneously powering the system and charging the battery. This eliminates the charge-termination and safety-timer issues, minimizes the ac adapter power rating, and improves system reliability. It also allows the system to operate while charging a deeply discharged battery.

Figure 1 is a block diagram of a simplified power-path-management battery charger. When the ac adapter is plugged in, MOSFET Q1 is used to preregulate the system bus voltage, V_{OUT}, which is higher than the maximum battery regulation voltage, V_{BAT}. This establishes a direct path from the adapter input to the system. The MOSFET Q2 is dedicated to charging the battery, so there is no interaction between the battery and the system. When a USB is present and selected, the MOSFET Q3 is fully turned on, the Q3 output provides almost the same voltage as the USB output, and the MOSFET Q2 controls the battery charging.

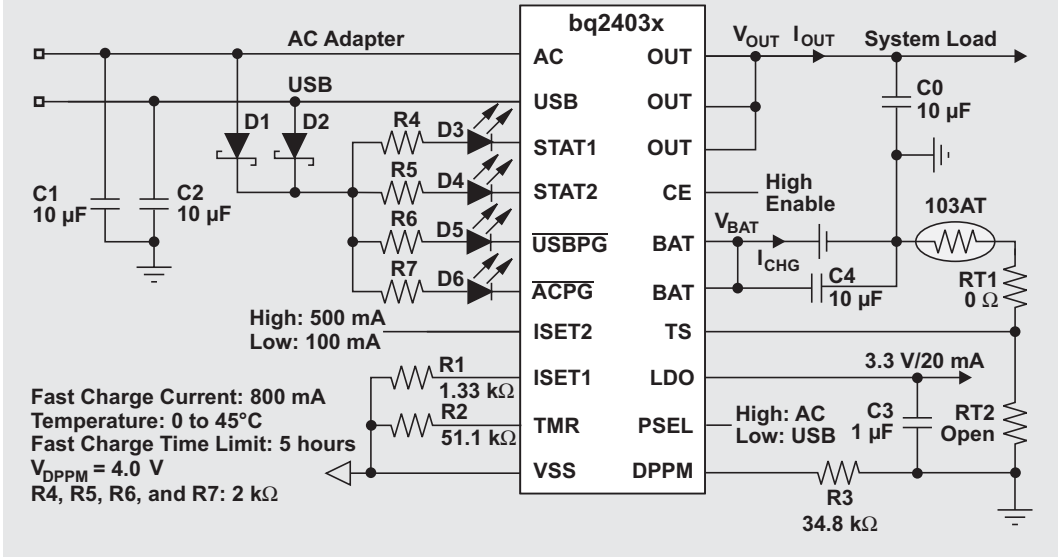
Figure 1. Simplified power-path-management battery charger



DPPM actively monitors the system bus voltage. If the system bus voltage drops to a preset value due to a limited amount of input current from the adapter or USB, the battery-charging current is reduced until the output voltage stops dropping. The DPPM control tries to reach a steady-state condition where the system gets its needed current and the battery is charged with the remaining current. Because of this, the adapter is designed based on average power from the system, not on maximum peak system power. This allows the designer to use a smaller power rating and a cheaper adapter.

Figure 2 shows a typical DPPM applications circuit. When the total current from the system and battery charger exceeds the current limit of the ac adapter or USB, the capacitors connected to the system bus start to discharge and system bus voltage begins to drop. When the system bus voltage drops to the predetermined threshold set by the DPPM pin, the charge current is reduced to prevent a system crash from overloading the ac adapter. If the system

Figure 2. DPPM battery charger



bus voltage cannot be maintained even when the charge current is reduced to 0 A, the battery will temporarily discharge and provide power to the system to avoid a system crash. This is called "battery supplement mode" and is shown in Figure 3 along with the DPPM experimental waveforms.

The DPPM voltage threshold, V_{DPPM}, is set by resistor R3 and is typically below the regulation voltage at the OUT pin to safely keep the system operating. R3 is calculated by

$$R3 = \frac{1.15 \times V_{DPPM}}{100\ \mu A}.$$

R1 is used to set the fast charge current and is given by

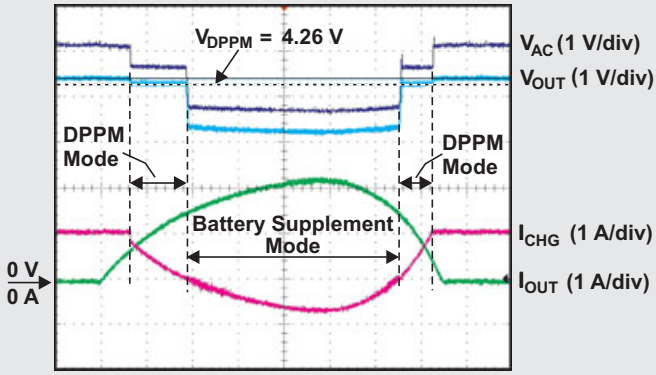
$$R1 = \frac{450 \times 2.5\ V}{I_{CHG}}.$$

R2 is used to set the safety-timer value. Typically the temperature qualification for allowing a Li-ion battery to be charged is between 0°C and 45°C. RT1 and RT2 are programmed for different temperature ranges.

The battery charger can select either ac or USB power as the main power source through the PSEL pin, and maximum current is also selectable through ISET2 when the USB port is selected.

Three power MOSFETs and a power controller are integrated in a thermally enhanced 3.5 × 4.5-mm QFN package. A thermal regulation loop reduces the charge current to prevent the silicon temperature from getting higher than 125°C. Whenever the charge current is reduced either by active thermal regulation or by active DPPM, the safety-timer duration is automatically increased to prevent an unexpected false safety-timer warning. Charge termination is also disabled when either DPPM or the thermal regulation loop is active. This approach prevents false charge termination.

Figure 3. DPPM experimental waveforms



Conclusion

DPPM reduces the battery-charging current while powering the system load when the system bus voltage drops to a predetermined threshold due to limited input current. DPPM also completely eliminates the issues of battery and system interaction such as false charge termination and false safety-timer warnings. The DPPM battery charger is ideal for power systems that simultaneously charge the battery.

Related Web sites

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Complete battery-pack design for one- or two-cell portable applications

By Michael Vega (Email: m-vega3@ti.com)
Portable Power Management Applications

Introduction

Although voltage measurement alone has been used in many portable products to approximate the remaining capacity of the battery, this method may have an error of up to 50%. The relationship between cell voltage and capacity will vary as a function of discharge rate, temperature, and cell aging. For example, a high discharge rate results in a greater voltage drop than a low discharge rate for the same depletion in capacity. Similar characteristics can be noticed when a cell is discharged at varying temperatures.

With the growing demand for products with longer run times, system designers need a more accurate solution. Using a gas-gauge IC to measure the charge that enters or leaves a battery will provide a much better estimate of battery capacity over a broad range of application power levels.

Gas-gauging principle

A gas gauge is an IC that autonomously monitors the capacity of a battery, which it reports to a processor that makes system power-management decisions. A good gas gauge requires at a minimum the means to measure battery voltage, pack temperature, and current; a microprocessor; and a proven gas-gauging algorithm.

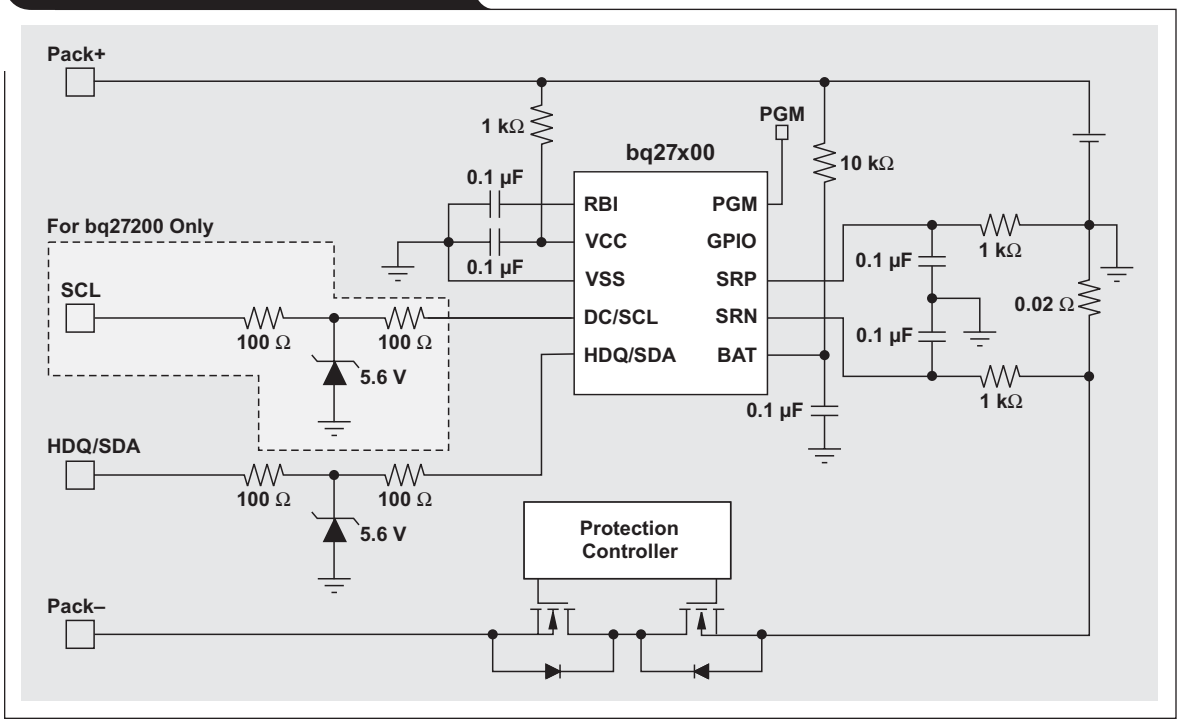
The bq2650x and bq27x00 are complete gas gauges that have an analog-to-digital converter (ADC) for voltage and temperature measurements, and another ADC for current and charge sensing. These gas gauges also have an internal microprocessor that runs Texas Instruments (TI) gas-gauging algorithms. These algorithms compensate for self-discharge, aging, temperature, and discharge rate in lithium-ion (Li-ion) cells. The microprocessor frees the host system processor from constantly making these calculations.

The gas gauges have information such as "Remaining State of Capacity," and the bq27x00 family provides "Run Time to Empty." The information is available any time the host queries. It is up to the host to notify the end user of the battery information either by means of LEDs or messages displayed on a screen. Using the gas gauges is very easy, as the system processor needs only an I^2C or an HDQ communication driver.

Battery-pack circuit description

Figure 1 depicts the application circuit within the battery pack. The battery pack will have at least three to four external terminals available depending on which gas-gauge IC is used.

Figure 1. Typical application circuit



The VCC and BAT pins will tap into the cell voltage for IC power and battery-voltage measurement. A low-value sense resistor is placed at the ground end of the battery cell so that the voltage across the sense resistor can be monitored by the gas gauge's high-impedance SRP and SRN inputs. The current through the sense resistor helps determine the amount of energy that has been charged to or discharged from the battery. When selecting a sense resistor value, the designer must consider that the voltage across it should be no more than 100 mV. A resistor value that is too low may introduce errors at low currents. A board layout must ensure that the connections from SRP and SRN to the sense resistor are as close as possible to the sense resistor's ends; i.e., they are Kelvin connections.

The HDQ/SDA and SCL pins are open-drain devices that each require an external pull-up resistor. The resistor should be on the host or main application side so that the sleep function of the gas gauge is enabled whenever a battery pack is disconnected from the portable device. A recommended pull-up resistor value is 10 kΩ.

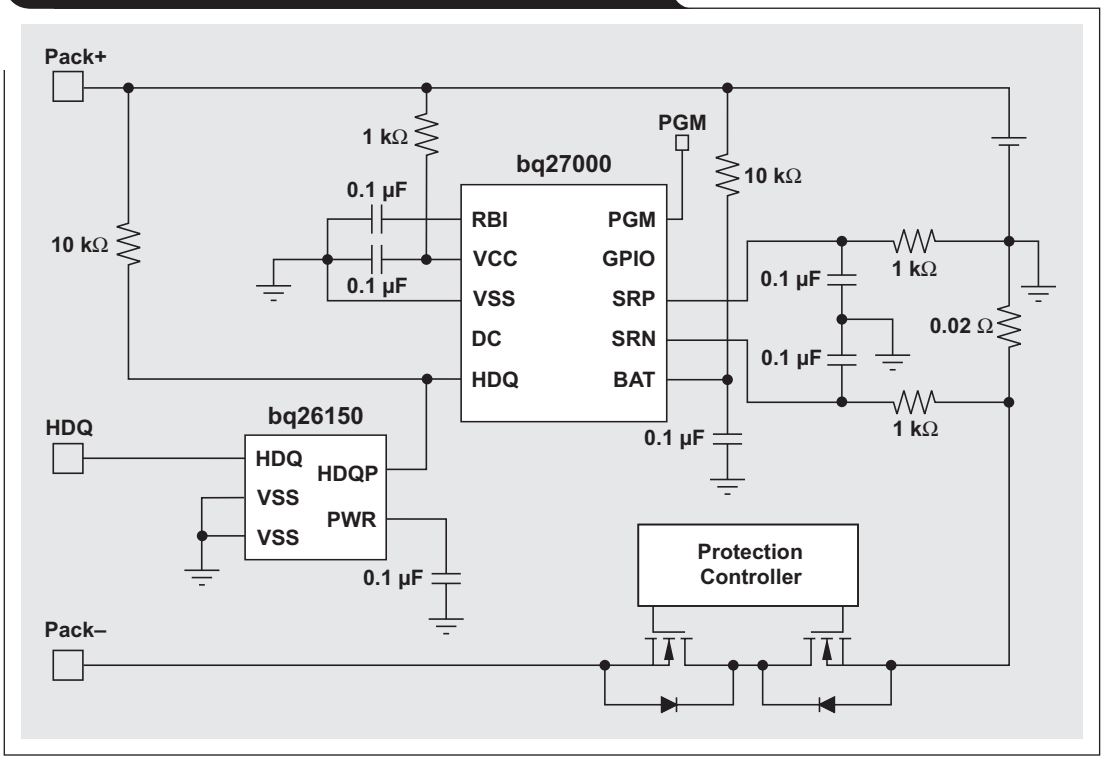
Battery-pack authentication

Rechargeable batteries for a portable device must be replaced before the life of the device expires. This has opened up a huge market for counterfeiters to supply cheap replacement batteries that may not have the safety and protection circuits required by the original equipment manufacturer.

Therefore, in addition to gas-gauging functionality, a battery pack may include an authentication feature (see Figure 2). The host challenges the battery pack, which contains an IC (TI's bq26150) that calculates a cyclic redundancy check (CRC). This CRC is based on the challenge and the CRC polynomial secretly defined within the IC. The host also calculates the CRC and compares values to determine if authentication is successful. If not, the host decides whether to try again or disallow powering of the system through the battery.

Once the battery is authenticated, the bq26150 is given a command to ensure that all communication through the data line is relayed between the host and the gas gauge.

Figure 2. Circuit with bq27000 and authentication IC



From that point on, the host can follow up on the gas gauge's functionality. The whole authentication process must be repeated upon disconnection from and reconnection to the battery.

Two-cell applications

Figure 3 shows the typical application circuit for supporting two Li-ion cells with the bq26500. An adjustable voltage regulator is added for multicell support. The BAT pin of the gas gauge is connected to the positive side of the bottom cell for a scaled battery-pack voltage measurement.

The host is required to interpret the scaled pack voltage measured by the gas gauge to determine the end-of-discharge threshold and charge termination. Information such as "Remaining State of Capacity" can be used as it is reported by the gas gauge.

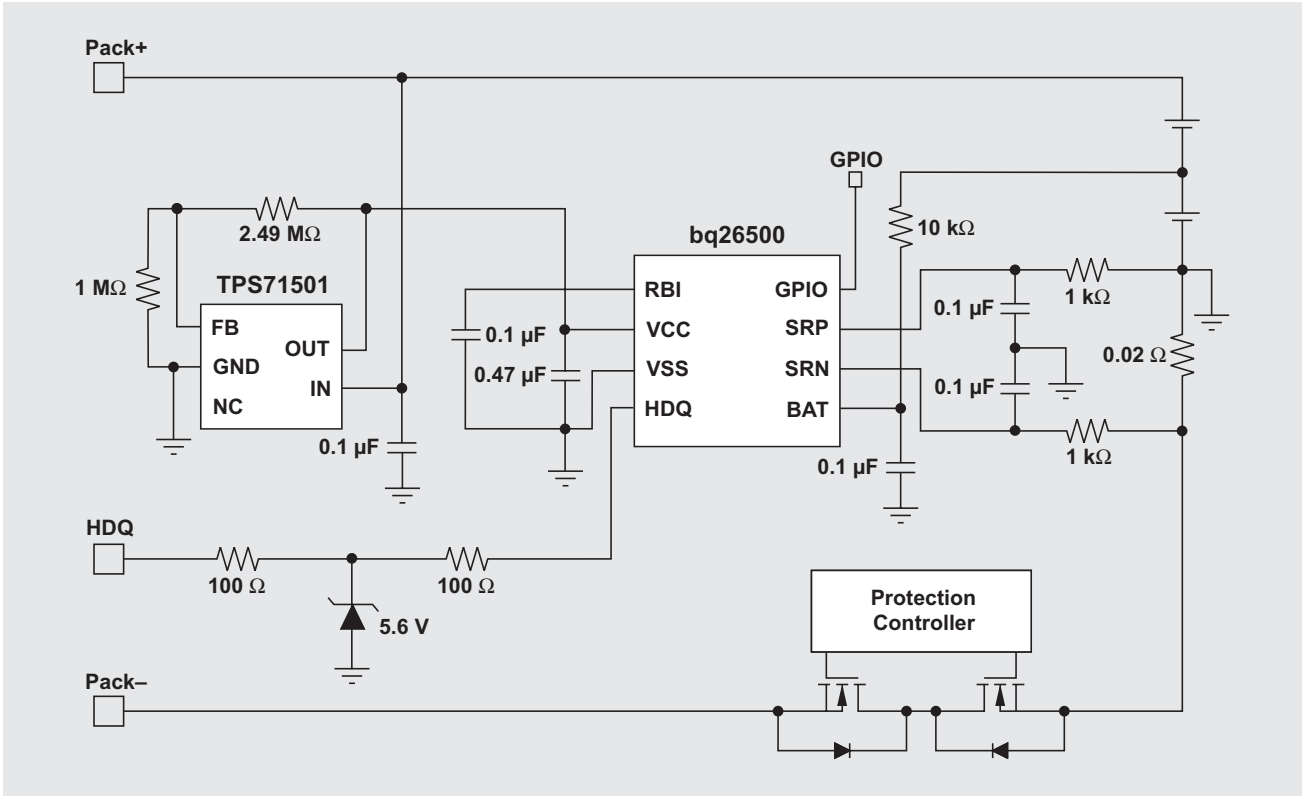
Conclusion

The bq2650x and bq27x00 provide battery manufacturers a simple alternative for battery-capacity reporting. The host can obtain a remaining-capacity value just by reading a register from the gas gauge and can then display the result to the end user. By using a gas gauge, the end user can use as much of a battery's charge as possible without being very conservative, because the capacity estimate will be more accurate than that obtained by just measuring cell voltage. The gas gauges can be used in different configurations, permitting authentication features and operation within two-cell applications.

Related Web sites

power.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with bq26150, bq26500, bq27000, bq27200, or TPS71501

Figure 3. Two-cell application with bq26500



Improved CAN network security with TI's SN65HVD1050 transceiver

By Steve Corrigan (Email: s-corrigan1@ti.com)
New Product Definition

A CAN transceiver must reliably transmit data in extremely harsh operating environments that place an extraordinary electrical burden on the device. Since the transceiver is typically the only interface between expensive node electronics and the CAN bus, many operational security features of the Texas Instruments (TI) SN65HVD1050 take on additional importance in CAN applications. These features include electromagnetic (EM) immunity, low EM emissions, noise rejection, electrostatic discharge (ESD) protection, fault tolerance, and protection during hot plugging or power cycling.

EM immunity

As the EM spectrum becomes more fully utilized, EM fields radiated by a wide range of devices are increasing the probability of interference with other electronic equipment. Due in part to the wireless revolution in electronics, EM interference is increasingly becoming a widespread concern.

Every electronic device has its own unique EM characteristics. The inductance and capacitance of any circuit may develop a common-mode resonance at discrete frequencies that either amplify or attenuate emissions.

The HVD1050 CAN transceiver is designed and tested for EM compatibility without malfunction or degradation of performance in rugged EM environments. "Compatibility" in this definition means both low emissions and high immunity to external EM fields.

Low EM emissions: Balanced signaling and common-mode output

An important requirement of products intended for networking applications is that they behave in a way that does not interfere with the operation of other nearby components or systems. The desired behavior is referred to as "low radiated emissions" and is typically tested according to various quantitative requirements specified at the system or electronic module level.

EM noise is generated by imbalanced high-frequency voltage or current switching. In a CAN transceiver, system-level emission performance must be translated into transceiver characteristics. Specifically, driver output signals are typically mismatched on CANH and CANL, and the resultant EM fields fail to differentially cancel each other as equal and opposite. This output mismatch (displayed in Figures 1 and 2) is referred to in TI datasheets as the peak-to-peak common-mode output voltage, $V_{OC(PP)}$, and may be considered to be a figure of merit for balanced differential signaling.

Measurement of the common-mode output signal is believed to provide all the information necessary to predict performance of system-level emissions. Both time and frequency representations of the output common-mode signal can be analyzed for the purpose of evaluating emissions behavior.

Figure 1. Typical CAN bus $V_{OC(PP)}$ waveform

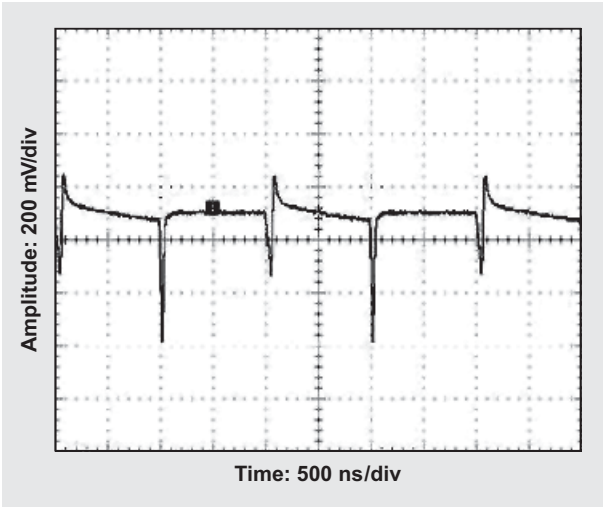


Figure 2. $V_{OC(PP)}$ test setup

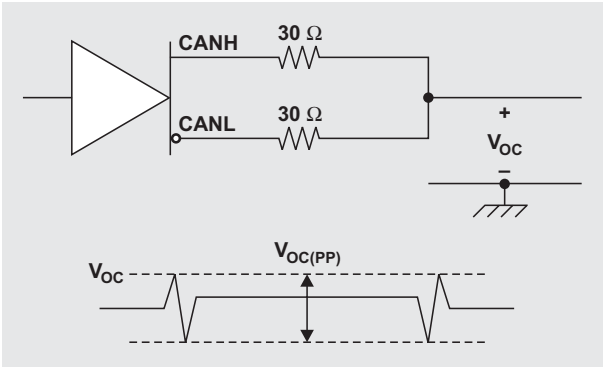
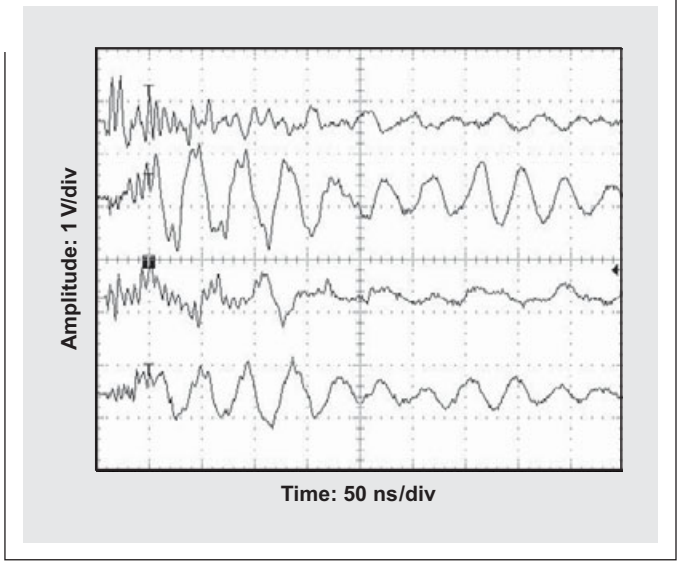


Figure 3. Common-mode noise coupled onto four twisted-pair bus lines



High immunity: Common-mode noise rejection

Common-mode noise rejection is an inherent feature of true differential receivers, just as it is with other differential-input circuits such as operational amplifiers. Differential signal pairs are physically close together and are generally exposed to the same noise sources—noise common to each wire. This ensures that exposure to EM fields is nearly equal and common to each line, canceling the differential influence from magnetic field coupling by reversing the polarity in adjacent loops of twist in twisted-pair wiring.

Unwanted noise of various magnitudes easily links the antenna-like bus lines of CAN applications. Pulsing motor controllers, switch-mode power supplies, and fluorescent lighting are typical noise sources that couple onto bus lines (displayed in Figure 3).

A CAN transceiver not specifically designed to reject this coupled noise will respond as if it were data on a bus and send corrupted and meaningless data to a controller.

TI's HVD1050 CAN transceiver is specifically designed and tested for its ability to reject this noise over an extremely wide (–12-V to +12-V) common-mode operating range. The high degree to which the differential receiver rejects coupled noise is evidence of the careful electrical and mechanical design of the receiver components that ensures that input matching is as close to ideal as possible.

Voltage transients and integrated-circuit protection

ESD can occur in any of four ways: A charged body can touch an IC; a charged IC can touch a grounded surface; a charged machine can touch an IC; or an electrostatic field can induce a voltage across a dielectric that is sufficient to break it down. It becomes readily apparent that a high ESD rating indicates not only a robust transceiver but a robust circuit design as well.

Comparable CAN transceivers on the market provide only 4-kV ESD protection, while the HVD1050 CAN transceiver has an ESD rating of 8 kV when tested in accordance with the Human Body Model (HBM) of JEDEC Standard 22 A114-B. With this ESD rating, the HVD1050 is much better suited to harsh electrical environments than the earlier transceiver versions of other vendors.

To ensure the HVD1050's robustness, it is also tested to ±200 V in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6, and 7.

Fault tolerance

Bus hangs and dominant time-out

CAN bus operators occasionally report that all bus communication comes to a halt when a faulty node places a continuous dominant bit on the bus. This stuck-dominant condition occurs either from a faulty controller or from random slivers of wire, a solder ball, or metal shaving shorts across a transceiver's input (TXD) pin and the adjoining ground (GND) pin.

A dominant-time-out circuit in the HVD1050 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD. If no rising edge occurs before the time-out constant of the circuit expires, the driver is output-disabled, releasing the bus from the stuck-dominant condition. Once the fault is corrected, the circuit is reset by the next rising edge on TXD.

Crushed-cable and short-circuit protection

Bus-cable polarity reversals, accidentally crushed cable, and unintentional shorts of the bus wires to power supplies or ground are common in many CAN applications. To provide protection from these real-world operating events that are common on 24-V industrial buses, the HVD1050 provides short-circuit protection from –27 V up to +40 V. This short-circuit protection extends over any length of time and guarantees that the device will continue normal operation once the fault is removed.

Additional circuit protection is provided with the thermal shutdown circuitry. In the event of a bus short with a runaway current condition, the HVD1050 automatically shuts the device down when thermal conditions exist that could damage internal circuitry.

Hot plugging, power cycling, and glitch-free outputs

Adding additional components to a network most often requires shutting down the entire network to prevent costly system errors. Therefore the ability to plug directly into an operating system becomes a valued asset in many CAN applications.

Plugging an unpowered module directly into a powered system is referred to as “hot plugging” and requires that the transceiver output remain stable during the unpowered to power-up transition without disturbing ongoing network communications.

Many CAN transceivers on the market today have a very low output impedance when unpowered. This causes the device to sink any signal present on the bus and effectively shuts down all data transmission.

For this purpose, the HVD1050’s bus pins are biased internally to a high-impedance recessive state. This provides for a power-up into a known recessive condition without disturbing ongoing bus communication. It also maintains the integrity of the bus when power or ground is added to or removed from the circuit.

Together these features of the HVD1050 serve to greatly enhance the operational security of any CAN application.

Related Web sites

interface.ti.com
www.ti.com/sc/device/SN65HVD1050

Index of Articles

Data Acquisition

Power Management

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