Power-management solutions for telecom systems improve performance, cost, and size

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Deregulation and competition in wire line and wireless infrastructure telecommunications systems have accelerated the need for lower-cost equipment solutions with ever-increasing bandwidth. The challenge of power-management requirements for telecom equipment continues to grow. Increasingly, designers are asked to provide more voltage rails for a variety of digital signal processors (DSPs), field programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs), and microprocessors. In short, they are required to generate more voltages, at higher currents, more efficiently, with less noise, in a smaller space. And, if that isn't challenge enough, the solution has to cost less, too!

Deploying access equipment closer to the subscriber requires smaller enclosures (pad and pole mounting) that must survive in a tougher environment. Infrastructure equipment is being designed for smaller footprints, as central office space comes at a premium. Factors driving power management are size, thermal management, cost, and electrical performance (regulation, transient response, and noise generation). This article provides a basic understanding of the evolution of board-mounted power systems, and how the latest generation can achieve higher performance and lower cost—in a smaller footprint.

Size/efficiency/cost

The need to address size, efficiency, and cost simultaneously has ignited renewed interest in power architectures. The first generation of board-mounted power used a power architecture known as a distributed power architecture (DPA) (see Figure 1). This architecture used an isolated (brick) power module for every voltage rail. It worked well when there were limited rails, but cost and PCB space increased significantly with each added voltage rail. Sequencing of the voltage rails also was difficult and required adding external circuitry, which in turn increased cost and board space.

To deal with the size and cost constraints of DPA, second-generation systems moved to a fixed-voltage intermediate bus architecture (IBA) (Figure 2). An IBA uses a single, isolated-brick power module and many nonisolated, point-of-load (POL) DC/DC converters. The POLs can be either power modules, such as the Texas Instruments (TI) PTH series, or discrete buck converters. The isolated converter works over the same input-voltage range as the first generation, either 36 to 75 V or 18 to 36 V. It creates an IBA supply that is regulated to 3.3 V, 5 V, or 12 V. The voltage choice is up to the system designer. This design results in less board space, lower cost, and easier sequencing of the

Figure 1. Typical DPA architecture

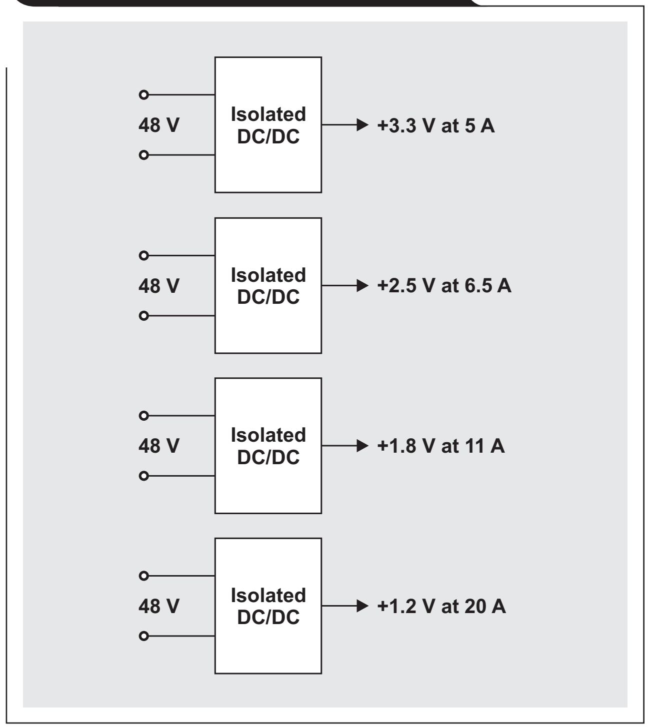
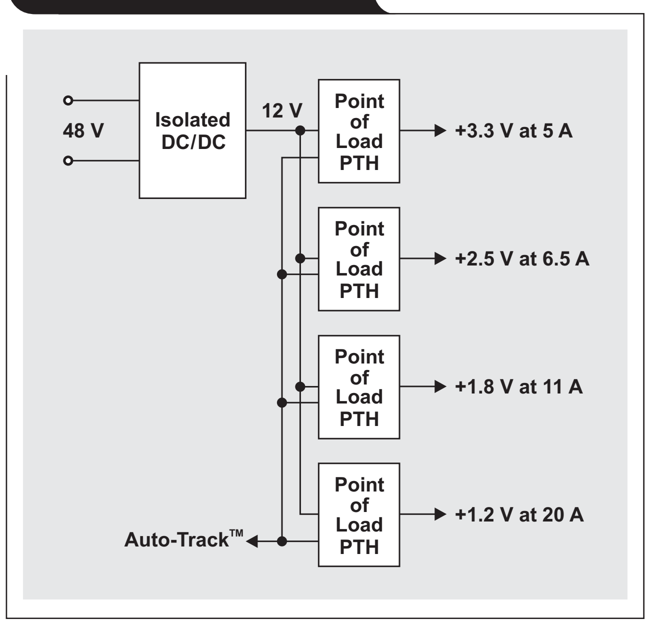


Figure 2. Fixed-voltage IBA



voltages due to features such as TI's Auto-Track™. The only drawback of this architecture is reduced efficiency due to the double conversion required for each voltage.

Today, most telecom systems use a fixed-voltage IBA. However, a higher-efficiency and smaller-footprint solution is needed as access-equipment designs evolve to sealed enclosures with no forced air cooling. As every designer knows, the best way to get rid of heat in a system is not to create it. The main focus for improving efficiency is the front-end isolated converter, since all of the power goes through it. The proven way to increase isolated-converter efficiency is to run the converter at a fixed duty cycle and not regulate the output. This method led to the unregulated intermediate bus architecture (Figure 3).

This architecture uses an unregulated bus converter that creates an output voltage as a ratio of the input voltage. In the example, an ALD17 5:1 converter creates an output voltage that is 1⁄5 of the input. This technique allows a 150-W system/board to be designed with a 1⁄16 brick, achieving 96% efficiency for the first conversion stage. Unregulated voltage became possible when wide-input (4.5- to 14-V) PWMs and power modules such as TI's T2 products were introduced. This architecture is limited by the bus converters' maximum input range of 36 to 55 V to keep the input voltage to POLs less than 12 V. The 12-V maximum is necessary because, for POLs to generate output voltages of 1 V or less, the input voltage cannot exceed 10 to 12 times the output. However, an increasing number of telecom original equipment manufacturers (OEMs) are considering a move to this limited input range for the significant cost savings, size reduction, and efficiency improvements obtained with this architecture.

Some telecom OEMs insist on maintaining the traditional, wider input-voltage specification of 36 to 75 V with input transients of up to 100 V. For these requirements, the power industry has responded with the quasiregulated IBA (Figure 4). The main difference between this and the unregulated IBA is that if the input voltage exceeds 55 to 60 V, the quasiregulated IBA regulates the output voltage to around 10 V. The drawback of this approach is that the isolated power module must increase in size to accommodate the regulation circuitry, and its efficiency is reduced when the input voltage exceeds 55 V. An example of this kind of product is the TI PTQB series.

Figure 3. Unregulated IBA

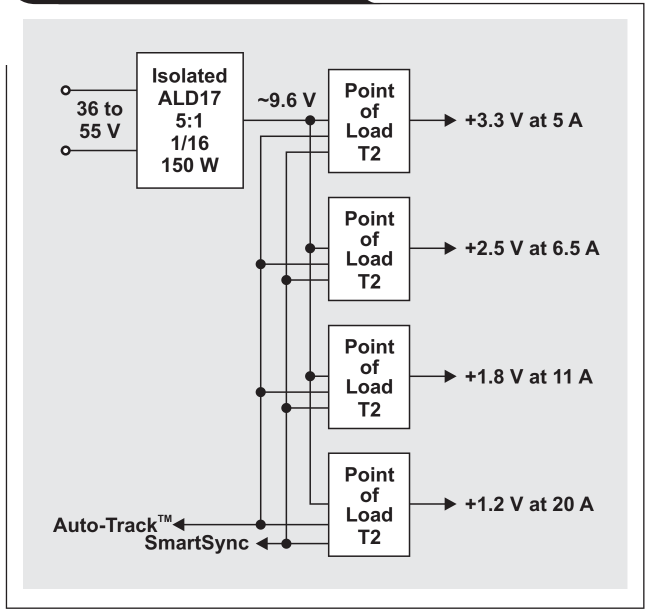
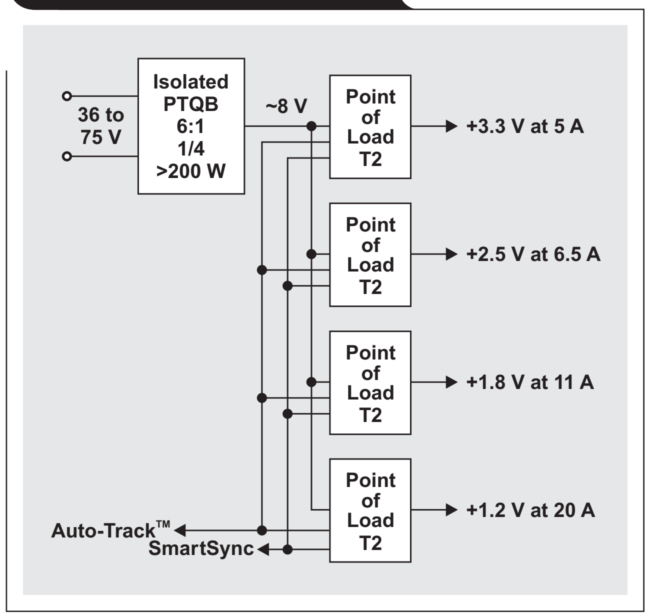


Figure 4. Quasiregulated IBA

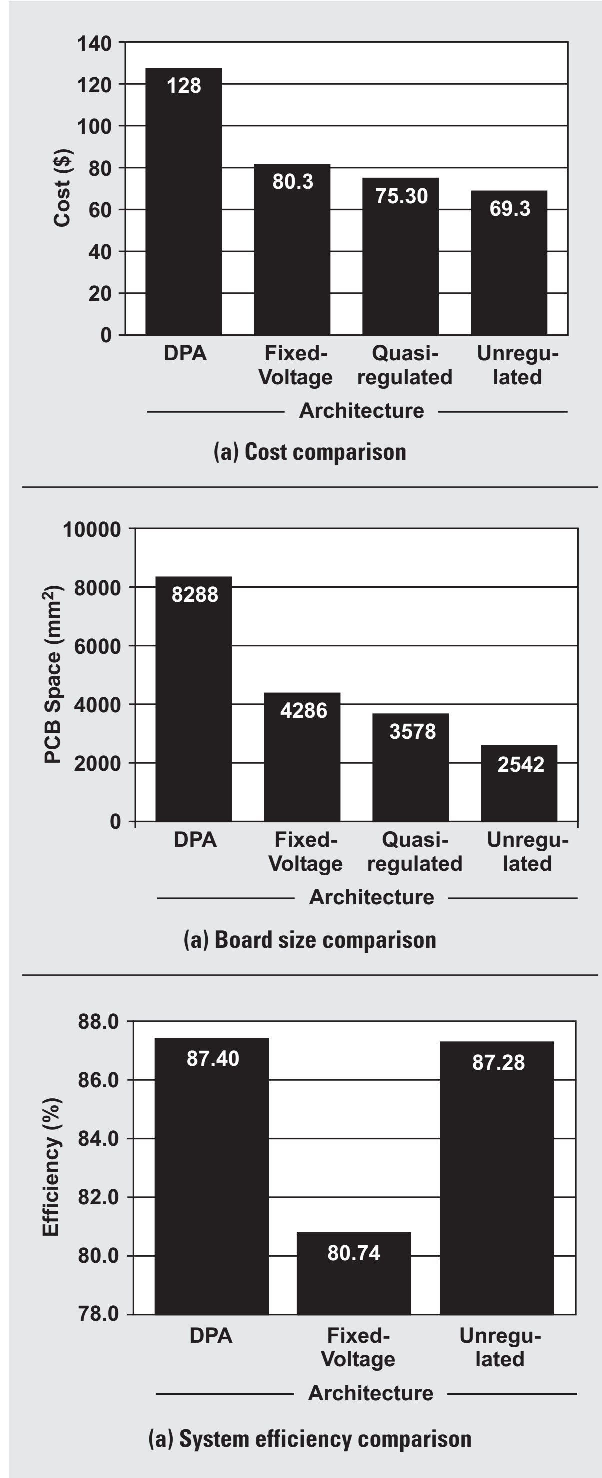


Architecture comparison

To provide a meaningful comparison, each example in Figures 2, 3, and 4 has identical output-voltage and current requirements. The examples are based on a theoretical base station utilizing multiple high-performance DSPs with associated analog and digital circuits. The output voltages are 3.3 V at 5 A, 2.5 V at 6.5 A, 1.8 V at 11 A, and 1.2 V at 20 A. For a comparison of the architectures described earlier, see Figure 5. The graphs indicate that the ultimate dream is indeed possible. A quasiregulated or unregulated power system can provide higher efficiency in less space at lower cost. The most notable improvement of the quasi/unregulated IBA over the second-generation, fixed-voltage IBA is efficiency. As shown in Figure 5, power-conversion efficiency increased by almost 7%. This translates to a thermal load reduction of 14 W for a 200-W system.

Power modules were used in these examples because they provide the greatest power density and are the solution of choice at many telecom OEMs. Discrete POLs can be used in all systems to reduce cost, but the board space will increase by a factor of two.

Figure 5. Comparison of architectures



Electrical performance

The remaining challenge for the designer is to meet the increasing electrical demands of the high-performance DSPs and ASICs at the heart of each system. Primary performance issues are voltage regulation, current transient response, and noise.

Regulation and current transient response are closely linked. To get higher performance with lower power in a smaller size, digital semiconductors are fabricated with smaller-geometry transistors that require ever-decreasing voltages. Sub-1-V core-voltage requirements are now becoming the standard. Along with this low voltage have come increasingly tighter tolerances. It is now common practice to specify a total voltage tolerance of 3% that includes line (variations in input voltage), load (small deviations in load current), time, temperature, and current transients. This leaves the power designer with only 30 mV of headroom to accommodate everything the digital system requires. About half of the tolerance budget (15 mV) is usually absorbed by the DC parameters of line, load, time, and temperature. The remaining 15 mV is then available to deal with sudden changes in current (1 to 3 clock cycles) due to computational or data-transmission loads.

This tolerance budget challenges the power-system designer to minimize voltage deviation in the presence of these current transients. If the core voltage (V_{CC}) exceeds the specified tolerance limits, the digital IC may initiate a reset or have logic errors. To prevent this, designers need to pay close attention to the transient performance of the

POL modules being used. Digital loads such as the latest gigahertz DSPs require extremely fast transient responses with very low voltage deviation. To achieve these targets, many additional output capacitors are usually added to the DC/DC converter to provide hold-up time until its feedback loop can respond. The power module, including this added capacitance to meet transient-voltage tolerances, represents the complete power solution.

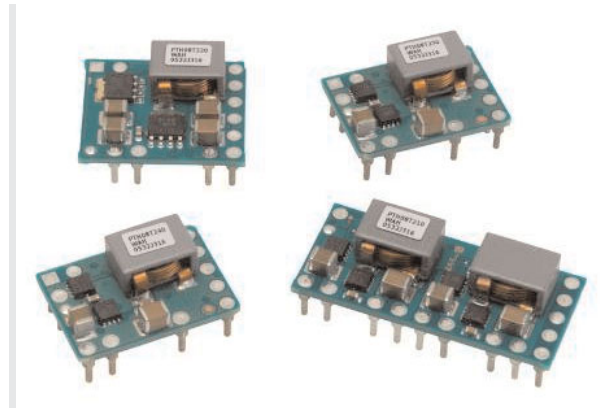
Capacitors have been evolving over the years, with volumetric efficiencies getting better all the time. Even with higher volumetric efficiency, the overall power solution can be over twice the size of the power module alone. This requires a large allocation on the PCB that is usually not available in today's physically smaller systems. What's more, the cost of power-supply materials can be more than double the cost of the power module when the cost of capacitors is added in.

With innovations in DC/DC power-module technology, system designers now are able to achieve faster transient response and less voltage deviation while using less output capacitance. An example is the T2 series next-generation PTH modules (Figure 6) from TI. These devices incorporate a new patented technology called TurboTrans™ that allows custom tuning of the module to meet a specific transient-load requirement. Tuning is accomplished with a single external resistor.

TurboTrans can achieve up to an eightfold reduction in output capacitance, which lowers the cost of capacitors and saves PCB space. Another benefit of this technology is that using a capacitor with ultralow equivalent series resistance (ESR) provides enhanced module-circuit stability. These newer Oscon, polymer-tantalum, and ceramic output capacitors have the additional benefit of being able to withstand high-temperature, lead-free soldering processes.

The final performance hurdle for isolated and POL converters is noise. When switching POLs run at different frequencies and share a common input bus, frequencies resulting from the sum and difference of those frequencies can create beat frequencies that make EMI filtering difficult.

Figure 6. T2 series power modules with TurboTrans™



As an example, if a system has two POLs with one operating at 300 kHz and a second at 301 kHz, the beat frequency is 1 kHz. This can require larger, more complex system filters. T2 power modules from TI have a SmartSync feature that lets the designer synchronize the switching frequency of multiple T2 modules to a specific frequency, which eliminates beat frequencies and makes EMI filtering easier. SmartSync can be used to set the frequency so that switching noise is minimized in a particular frequency band (i.e., xDSL transmission frequencies). TurboTrans and SmartSync are standard features on T2 power modules that add no additional cost to the systems described earlier.

A telecom system built with state-of-the-art power modules allows the system designer to reduce system size, decrease dissipated power, meet the power demands of high-performance digital circuits, and reduce the cost of power compared to regulated-voltage IBA systems.

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