EVM User's Guide: LP-AM261

AM261x LaunchPad User Guide

Description

The AM261x LaunchPad™ development kit is a simple and inexpensive hardware evaluation module (EVM) for the Texas Instruments™ Sitara™ AM261x series of microcontrollers (MCUs). This EVM provides an easy way to start developing on the AM261x MCUs with on-board emulation for programming and debugging as well as user-controlled buttons and LEDs for a simple user interface.

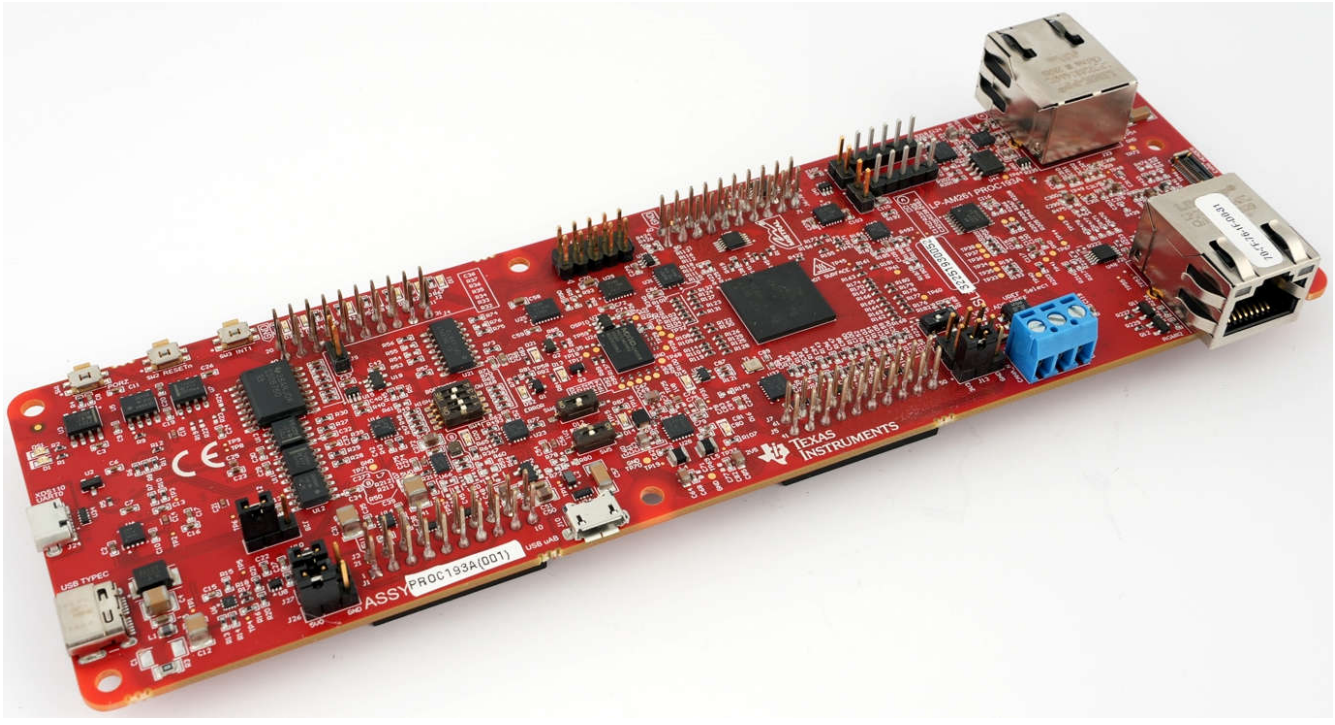
Get Started

1. Order the AM261x LaunchPad Evaluation Board (EVM)
2. Download the latest Code Composer Studio™ Integrated Development Environment (IDE) and the AM261x MCU PLUS Software Development Kit

Features

The AM261x LaunchPad has the following features:

- AM2612 Dual-core ARM® Cortex®-R5F MCU
- 2x independent BoosterPack XL connector sites (80 total pins) for rapid prototyping and use with supported TI BoosterPack hardware
- Multiple industrial and automotive networking protocols supported through programmable real-time unit (PRU), modular controller area network (MCAN), local interconnect network (LIN), RGMII and MII interfaces
- On-board XDS110 debug probe
- On-board 64Mb Macronix OSPI flash and 128Mb AP Memory OSPI PSRAM



1 Evaluation Module Overview

1.1 Introduction

The LP-AM261 LaunchPad Evaluation Module is a single-board development platform that can be used to evaluate the performance of the AM261x microcontroller. The LaunchPad architecture includes all the necessary power, reset, and clock logic to operate the AM261x device.

The 80-pin AM261x LaunchPad is intended to provide a well-filtered, robust design that is capable of working in most environments. This document provides the hardware details of the AM261x LaunchPad and explains the functions of the on-board peripherals, locations of jumpers and connectors, and configurations of switches and muxes present on the PCB.

1.1.1 Preface: Read This First

1.1.1.1 Sitara MCU+ Academy

Texas Instruments offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

1.1.1.2 Important Usage Notes

Note

The AM261x LaunchPad requires a 5V, 3A power supply to function. A 5V, 3A power supply is not included in the kit and must be ordered separately. The *Belkin USB-C Wall Charger* is known to work with the LaunchPad and supplied type-C cable. For more information on power requirements refer to Section 2.2.

Note

The AM261x SoC (U1) on the LaunchPad can reach and exceed temperatures of 55℃ during high power consumption use cases as per internal testing. This user guide statement is to alert users to this temperature condition.

Caution	Caution Hot surface. Contact may cause burns. Do not touch!

Note

External Power Supply or Power Accessory Requirements:

- Nominal output voltage: 5VDC
- Max output current: 3000mA
- Power Delivery

Note

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE,CCC,PSE, etc.

1.2 Kit Contents

The Sitara AM261x LaunchPad Development Kit contains the following items:

- LP-AM261 development board
- USB micro-B cable
- USB Type-C cable

The kit does not include:

- USB type-C 5V/3A AC/DC supply

- DP83826-EVM-AM2 Ethernet Add-on Board

1.3 Device Information

1.3.1 System Architecture Overview

The below image shows the overall top level architecture of the AM261x LaunchPad.

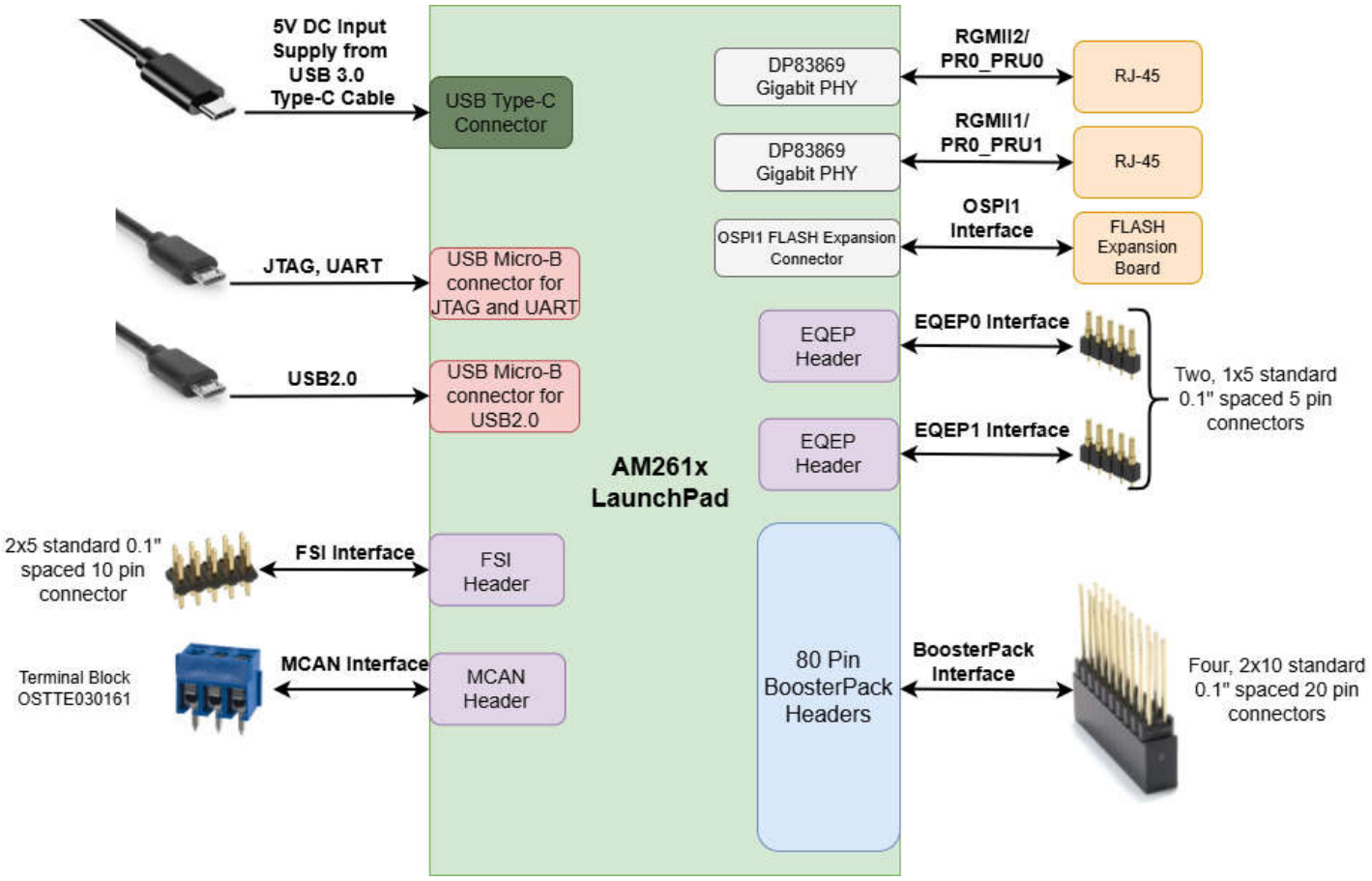


Figure 1-1. System Architecture

1.3.2 Component Identification

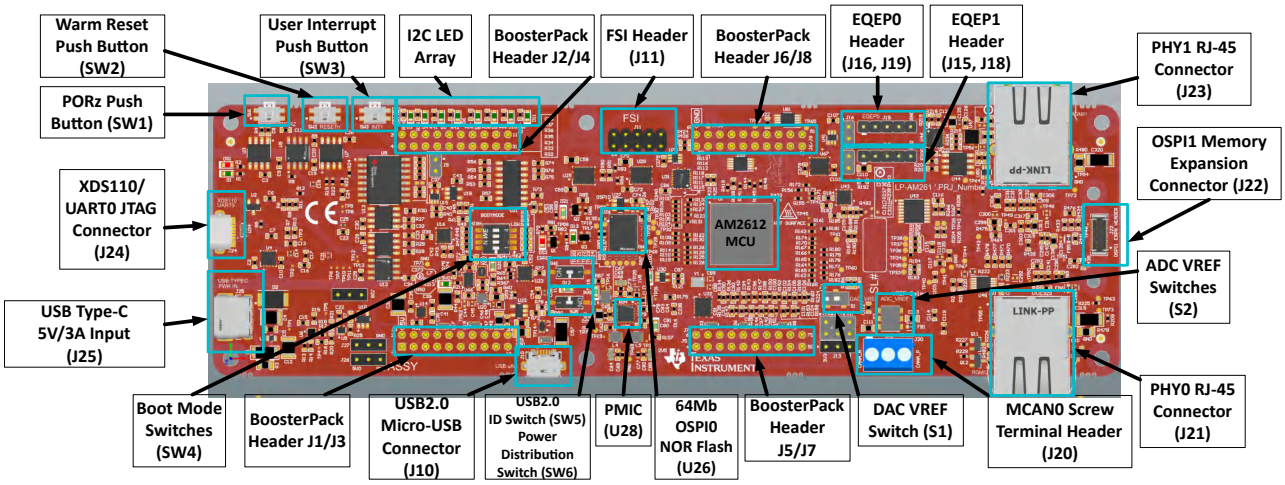


Figure 1-2. AM261x LaunchPad Top Components Identification

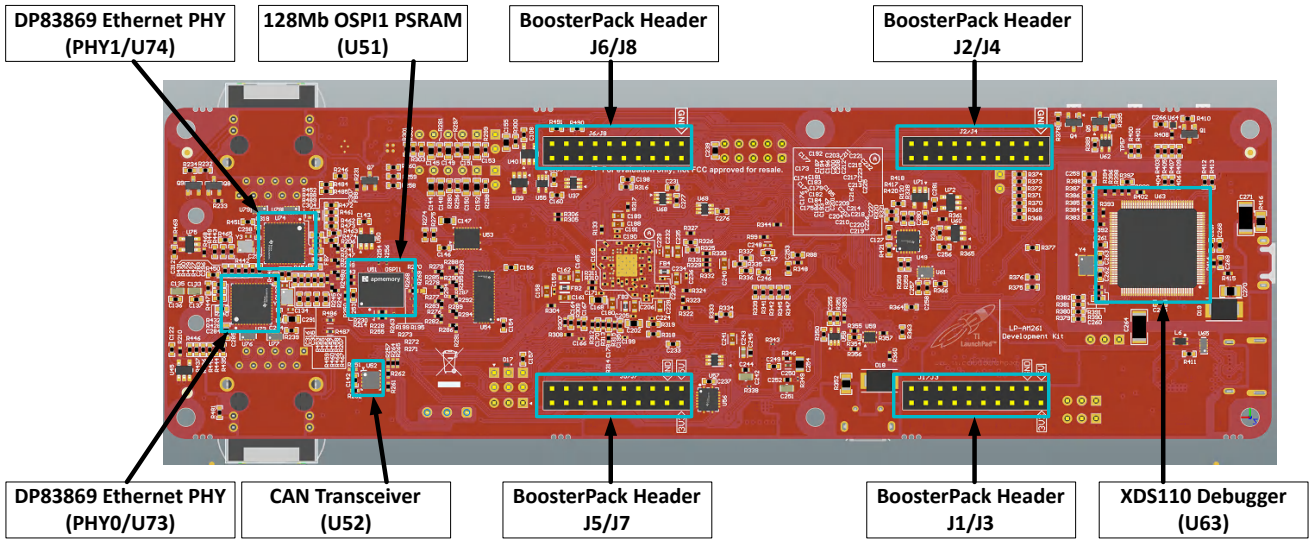


Figure 1-3. AM261x LaunchPad Bottom Components Identification

1.3.3 Functional Block Diagram

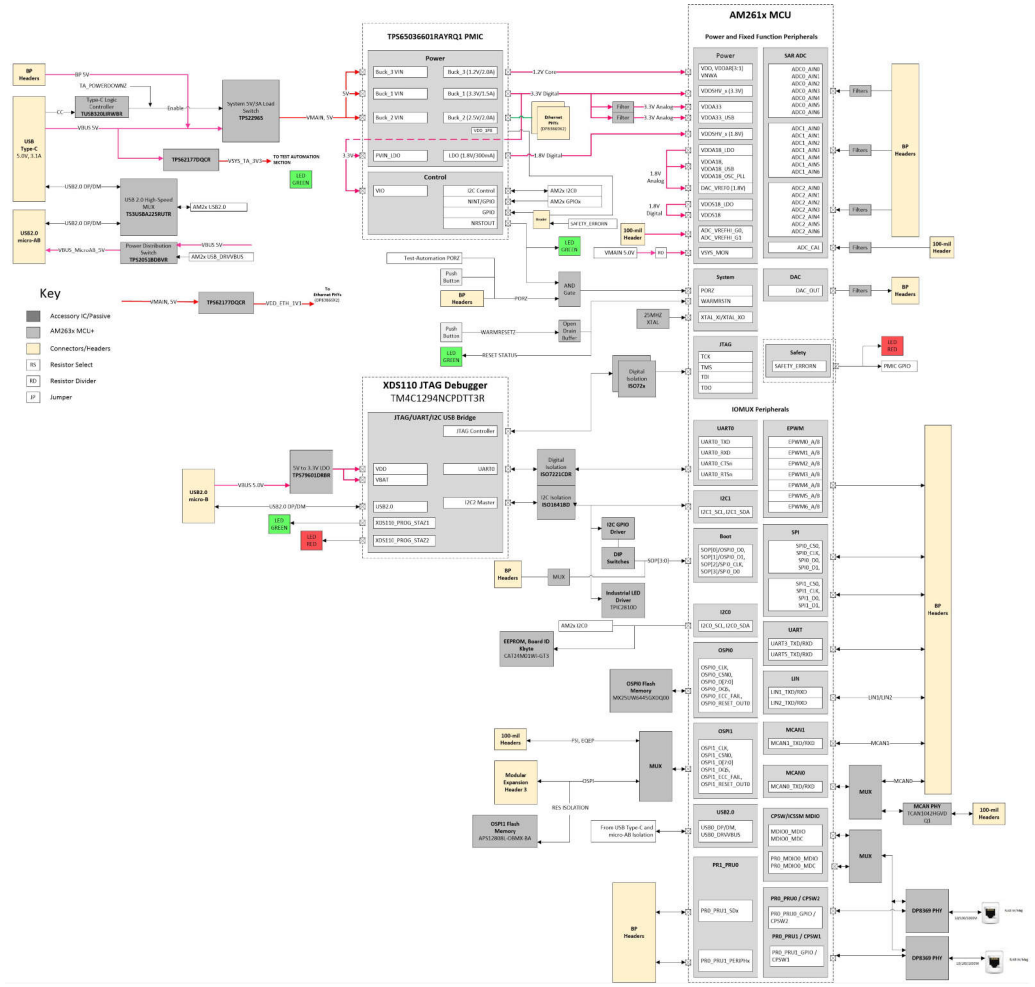


Figure 1-4. AM261x LaunchPad Functional Block Diagram

1.3.4 BoosterPacks

The AM261x LaunchPad development kit provides an easy and inexpensive way to develop applications with the AM261x Series microcontroller. BoosterPacks are add-on boards that follow a pin-out standard created by Texas Instruments. The TI and third-party ecosystem of BoosterPacks greatly expands the peripherals and potential applications that you can easily explore with the AM261x LaunchPad. For a detailed look at the pinout of the AM261x LaunchPad BoosterPack headers, refer to Section 2.12.

You can also build your own BoosterPack by following the design guidelines on TI's website. Texas Instruments even helps you promote your BoosterPack to other members of the community. TI offers a variety of avenues for you to reach potential customers with your solutions.

1.3.5 Device Information

The AM261x Sitara Arm® Microcontrollers are part of Sitara AM26x real-time MCU families designed to meet the complex real-time processing needs of next generation industrial and automotive embedded products. With scalable Arm® Cortex®-R5F performance and an extensive set of peripherals, AM261x device is designed for a broad range of applications while offering safety features and optimized peripherals for real time control.

Key features and benefits:

- Peripherals supporting system level connectivity such as Gigabit Ethernet, USB, OSPI/QSPI, CAN, UARTs, SPI and GPIOs.
- Granular firewalls managed by Hardware Security Manager (HSM) enable developers to implement stringent security minded system design requirements.
- Up to two R5F cores in cluster with 256KB of shared Tightly Coupled Memory (TCM) per core along with 1.5MB of shared SRAM, greatly reducing the need for external memory.

1.3.5.1 Security

The AM261x LaunchPad features a High Security, Field Securable (HS-FS) device. An HS-FS device has the ability to use a one time programming to convert the device from HS-FS to High Security, Security Enforced (HS-SE) device.

The AM261x device leaves the TI factory in an HS-FS state where customer keys are not programmed and has the following attributes:

- Does not enforce the secure boot process
- M4 JTAG port is closed
- R5 JTAG port is open
- Security Subsystem firewalls are closed
- SoC Firewalls are open
- ROM Boot expects a TI signed binary (encryption is optional)
- TIFS-MCU binary is signed by the TI private key

The One Time Programmable (OTP) keywriter converts the secure device from HS-FS to HS-SE. The OTP keywriter programs customer keys into the device efuses to enforce secure boot and establish a root of trust. The secure boot requires an image to be encrypted (optional) and signed using customer keys, which will be verified by the SoC. A secure device in the HS-SE state has the following attributes:

- M4, R5 JTAG ports are both closed
- Security Subsystems and SoC Firewalls are both closed
- TIFS-MCU and SBL need to be signed with active customer key

2 Hardware

2.1 Setup

Note

When the LaunchPad is used in a high-voltage setup, the user is responsible to confirm that the voltages and isolation requirements are identified and understood prior to energizing the board or simulation. When energized, the LaunchPad or components connected to the LaunchPad cannot be touched.

2.1.1 Standalone Configuration

Note

The standalone configuration is used for most software development use cases that do not require the use of an external BoosterPack. BoosterPack setup will vary depending on the hardware required.

In this configuration, Code Composer Studio™ connects to the LaunchPad by JTAG and enables software development. The on-board XDS110 debug probe enumerates a virtual COM port (VCP) for communication with the AM261x MCU by UART.

Follow these steps to set up the AM261x LaunchPad in its default configuration:

1. Collect the required equipment
   a. AM261x LaunchPad (LP-AM261)
   b. 5V/3A USB Type-C power supply
   c. Micro-USB cable
2. Verify that the switch settings are correct on the LaunchPad
   a. Use SW4 to select the desired boot mode (Boot Mode Selection)
   b. Use S1 and S2 to select the desired ADC voltage reference mode (if applicable for the application) (ADC and DAC)
3. Connect the 5V/3A USB Type-C power supply to connector J25 of the LaunchPad
4. Connect the micro-USB cable to connector J24 of the LaunchPad
5. Verify the power status LEDs (D7, D12, D14, D15, D16) on the LaunchPad are turned on
6. The LaunchPad is ready for use. Follow the steps in Software to get started on developing software

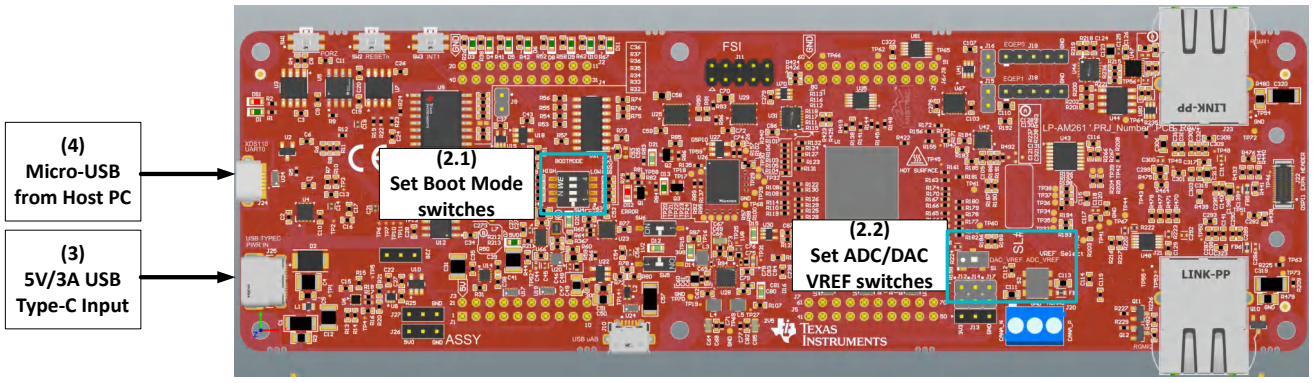


Figure 2-1. LP-AM261 Standalone Configuration

2.2 Power Requirements

The AM261x LaunchPad is powered from a 5V, 3A USB type-C input. The following sections describe the power distribution network topology that supply the AM261x LaunchPad, supporting components and the reference voltages.

Power supply solutions that are compatible with the AM261x LaunchPad:

- When using the USB type-C input:
  - 5V, 3A power adapter with USB-C receptacle
  - 5V, 3A power adapter with captive USB-C cable
  - PC USB type-C port that has Power Delivery classification
    - Thunderbolt
    - Battery behind USB logo

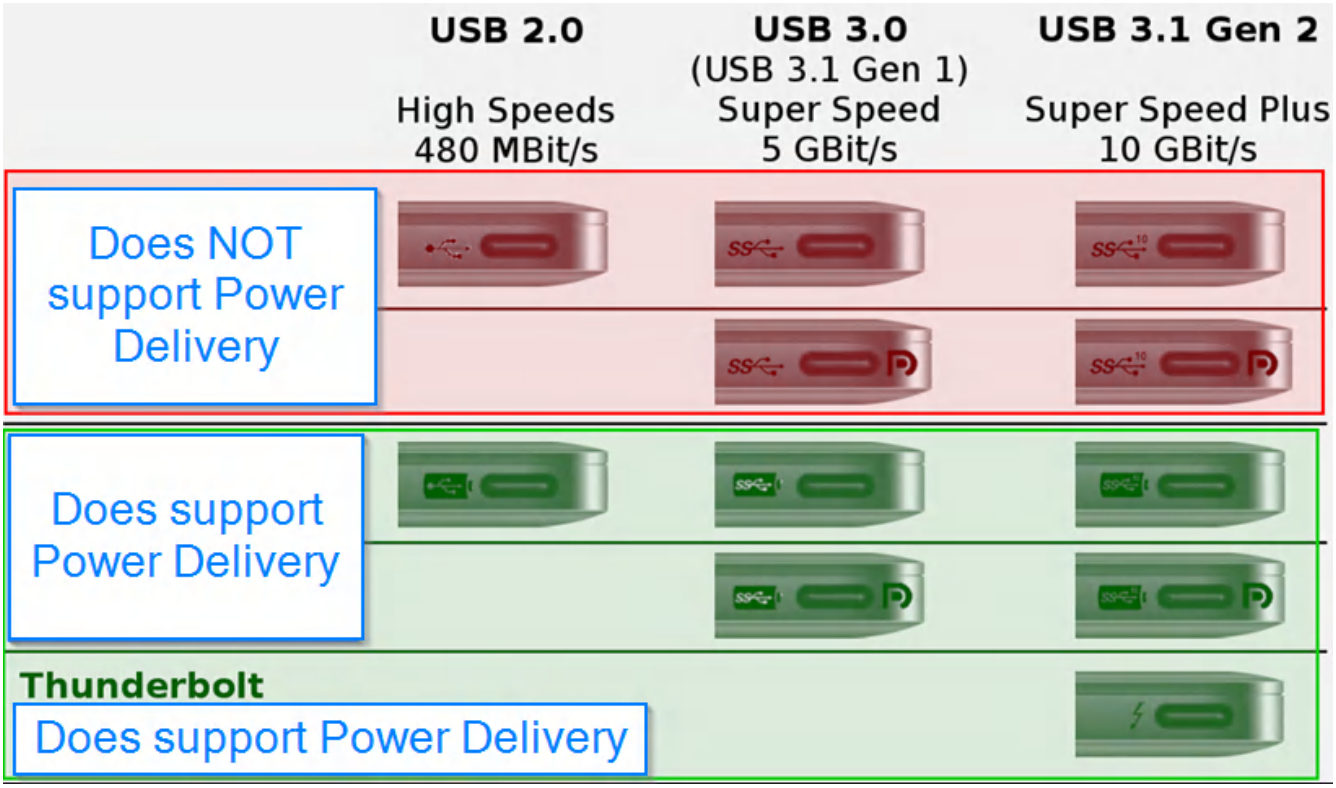


Figure 2-2. USB Type-C Power Delivery Classification

Power supply solutions that are **NOT** compatible with the AM261x LaunchPad:

- When using USB type-C input:
  - Any USB adapter cables such as:
    - Type-A to type-C
    - micro-B to type-C
    - DC barrel jack to type-C
  - 5V, 1.5A power adapter with USB-C captive cable or receptacle
  - PC USB type-C port not capable of 3A

2.2.1 Power Input Using USB Type-C Connector

The AM261x LaunchPad is powered through a USB Type-C connection. The USB Type-C source must be capable of providing 3A at 5V and advertises the current sourcing capability through the CC1 and CC2 signals. On the AM261x LaunchPad, the CC1 and CC2 nets from the USB Type-C connector are interfaced to the port controller IC (TUSB320). This device uses the CC pins to determine port attach and detach, cable orientation, role detection, and port control for Type-C current mode. The CC logic detects the Type-C current mode as default, medium, or high.

The Port pin is pulled down to ground with a resistor to configure it as upward facing port (UFP) mode. VBUS detection is implemented to determine a successful attach in UFP mode. The OUT1 and OUT2 pins are connected to a NOR gate. Active low on both the OUT1 and OUT2 pins advertises high current (3A) in the attached state which enables the VUSB_5V0 power switch to provide the VSYS_5V0 supply - which powers the PMIC and LDOs.

In UFP mode, the port controller IC constantly presents pull down resistors on both CC pins. The port controller IC also monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The port controller IC de-bounces the CC pins and waits for VBUS detection before successfully attaching. As a UFP, the port controller device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs.

The AM261x LaunchPad power requirement is 5V at 3A. If the source is not capable of providing the required power, the output at the NOR gate becomes low and disables the VUSB_5V0 power switch. Therefore, if the power requirement is not met, all power supplies except VCC3V3_TA remain in the off state. The board gets powered on completely only when the source can provide 5V at 3A.

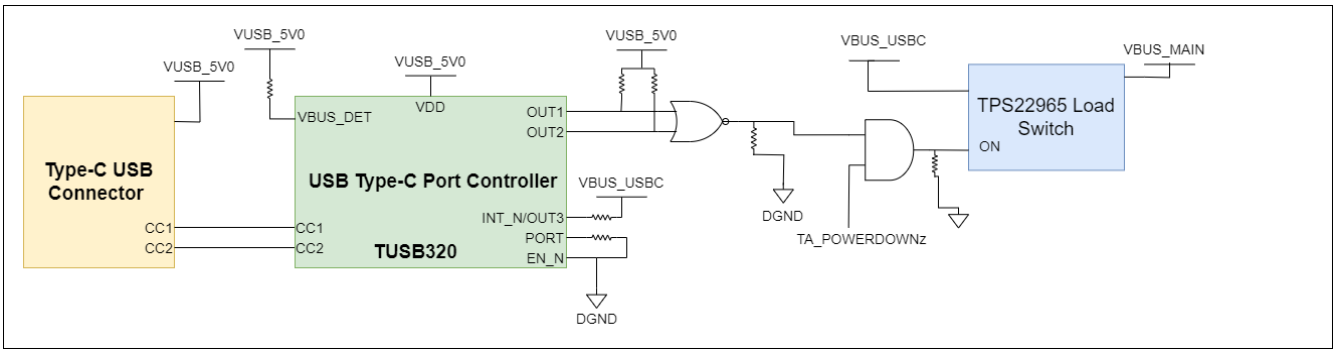


Figure 2-3. Type-C CC Configuration

Table 2-1. Current Sourcing Capability and State of USB Type-C Cable

OUT1	OUT2	Advertisement
H	H	Default current in unattached state
H	L	Default current in attached state
L	H	Medium current (1.5A) in attached state
L	L	High current (3.0A) in attached state

The AM261x LaunchPad system power solution is PMIC-based. The on-board PMIC supplies the output of its three buck converters and one LDO regulator for each of the power rails. The PMIC generates the supplies required for the AM261x microcontroller and all other EVM peripherals. During the initial stage of the power supply, 5V supplied by the type-C USB connector is used to generate all of the necessary voltages required by the LaunchPad.

Table 2-2. Voltage Rail Generation

Component	Reference Designator	Function	Voltage In	Voltage Out
TPS650360	U28	• Core Digital 1.25V • System 3.3V • System 1.8V • Ethernet Port 2.5V	• Buck_1 VIN - 5.0V • Buck_2 VIN - 5.0V • LDO VIN - 3.3V • Buck_3 VIN - 5.0V	• Buck_1 VOUT - 3.3V • Buck_2 VOUT - 2.5V • LDO VOUT - 1.8V • Buck_3 VOUT - 1.25V

2.2.2 Power Tree

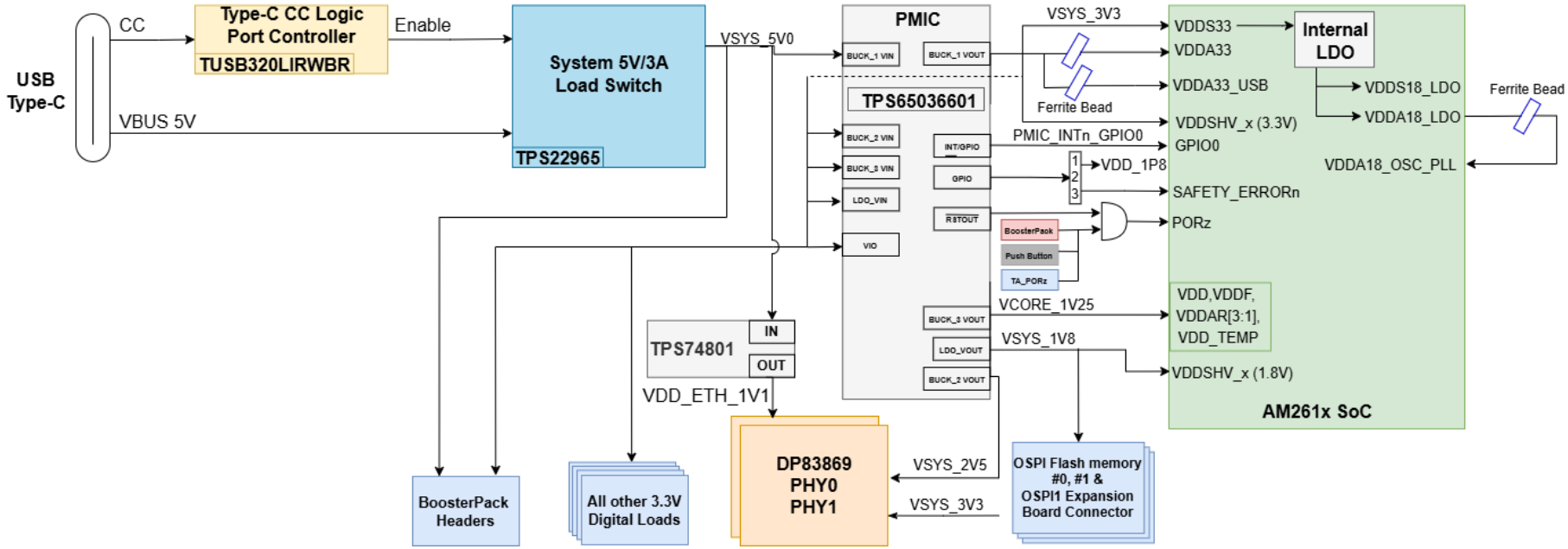


Figure 2-4. Power Tree Diagram of AM261x LaunchPad

2.2.3 Power Status LEDs

Multiple power-indication LEDs are provided onboard to indicate to users the output status of major supplies. The LEDs indicate power across various domains.

Table 2-3. Power Status LEDs

Name	Default Status	Operation	Function
D7	ON	VSYS_5V0	Power indicator for supply 5V voltage
D14	ON	VSYS_3V3	Power indicator for generated 3.3V voltage
D16	ON	VSYS_2V5	Power indicator for generated 2.5V voltage
D12	ON	VDD_1V25	Power indicator for generated 1.25V power-good voltage
D15	ON	VSYS_1V8	Power indicator for generated 1.8V voltage
D13	OFF	WARMRSTN	Power indication for WARMRSTN
DS2	OFF	SAFETY_ERROR	Power error indication for SAFETY_ERROR
D1	OFF	XDS_PROGSTAZ1	LED will glow after micro-B connection is made
DS1	OFF	XDS_PROGSTAZ2	LED will glow to indicate communication over JTAG

Note

DS2 LED that corresponds to SAFETY_ERROR is always ON.

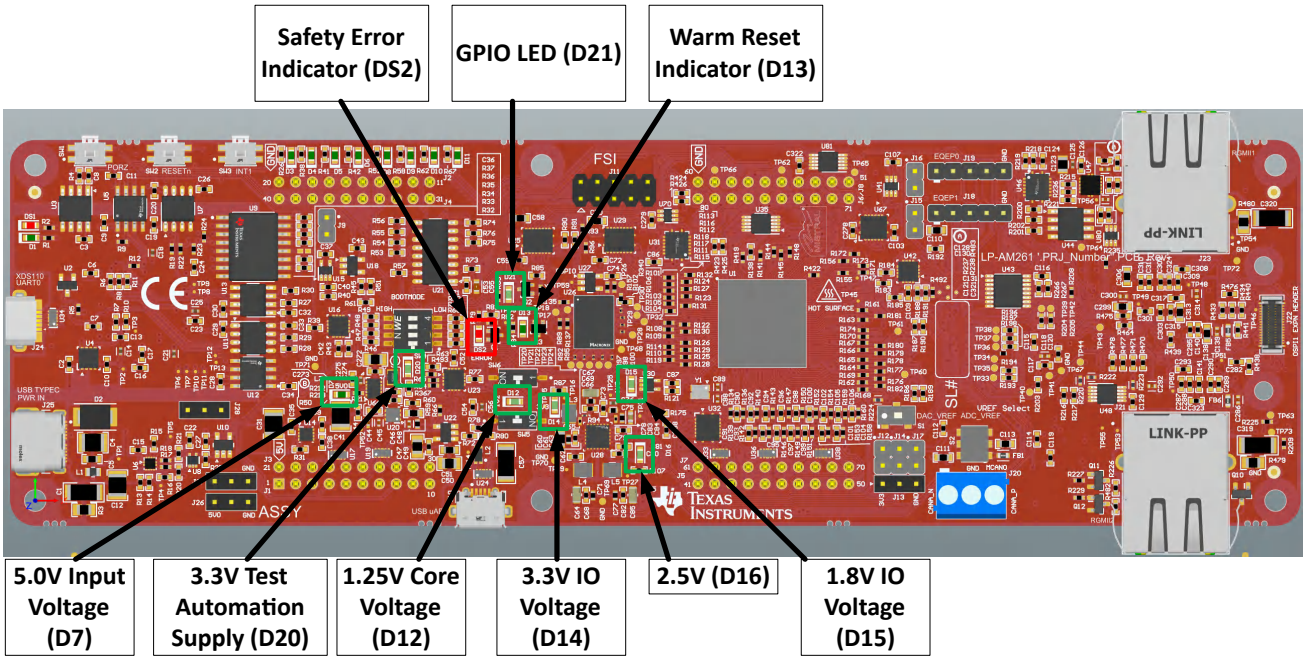


Figure 2-5. Power Status LEDs

2.3 Header Information

The AM261x LaunchPad can be interfaced with external hardware through various on-board headers. These headers provide access to a number of pins on the AM261x device and other signals found on the LP-AM261 board.

2.3.1 OSPI Expansion Connector

The LP-AM261 has a 30-pin high density connector for connecting an external OSPI memory to interface with the OSPI1 peripheral on the AM261x MCU. The pinout is detailed in Table 2-4 below:

Table 2-4. OSPI Expansion Connector (J22)

EVM Connection	Pin	Pin	EVM Connection
GND	1	2	VSYS_1V8
VSYS_1V8	3	4	GND
OSPI1_RESET_OUT0	5	6	OSPI1_ECC_FAIL
OSPI1_CSn0	7	8	OSPI1_CSn1
GND	9	10	OSPI1_CLK
GND	11	12	OSPI1_DQS
GND	13	14	OSPI1_D0
OSPI1_D1	15	16	OSPI1_D2
OSPI1_D3	17	18	GND
OSPI1_D4	19	20	OSPI1_D5
OSPI1_D6	21	22	OSPI1_D7
GND	23	24	-
-	25	26	-
-	27	28	-
-	29	30	-

For more information, see Section 2.10.1.1.

2.3.2 ADC/DAC External VREF Headers

The AM261x LaunchPad has headers for connecting external voltage references to the ADC and DAC peripherals. The header pinouts are detailed in the tables below:

Table 2-5. DAC External VREF Header (J12)

Pin	EVM Connection
1	DAC_EXT_VREF
2	GND

Table 2-6. ADC External VREF Header (J17)

Pin	EVM Connection
1	ADC_EXT_VREF
2	GND

Table 2-7. ADC Calibration Header (J14)

Pin	EVM Connection
1	ADC_CAL0

Table 2-7. ADC Calibration Header (J14) (continued)

Pin	EVM Connection
2	GND

For more information, see Section 2.10.12.

2.3.3 FSI Header

The LP-AM261 has a 10-pin Fast Serial Interface (FSI) header for interfacing with the AM261x FSI peripheral. The pinout is shown in Table 2-8 below.

Table 2-8. FSI Header (J11) Pinout

EVM Connection	Pin	Pin	EVM Connection
FSIRX0_CLK	1	2	FSITX0_CLK
GND	3	4	GND
FSIRX0_D0	5	6	FSITX0_D0
FSIRX0_D1	7	8	FSITX0_D1
GND	9	10	VSYS_3V3

For more information on the FSI implementation, see Section 2.10.8.

2.3.4 EQEP Headers

The LP-AM261 terminates the EQEP0 and EQEP1 peripheral signals to a set of breakout headers for use with external encoder hardware.

Table 2-9. EQEP0 Headers - J19 and J16

Pin	EVM Connection
J19.1	EQEP0_A
J19.2	EQEP0_B
J19.3	EQEP0_INDEX
J19.4	VSYS_5V0
J19.5	GND
J16.1	EQEP0_STROBE
J16.2	GND

Table 2-10. EQEP1 Headers - J18 and J15

Pin	EVM Connection
J18.1	EQEP1_A
J18.2	EQEP1_B
J18.3	EQEP1_INDEX
J18.4	VSYS_5V0
J18.5	GND
J15.1	EQEP1_STROBE
J15.2	GND

For more information on EQEP, see Section 2.10.13.

2.4 Push Buttons

The LaunchPad supports multiple user push buttons that provide reset inputs and user interrupts to the AM261x SoC.

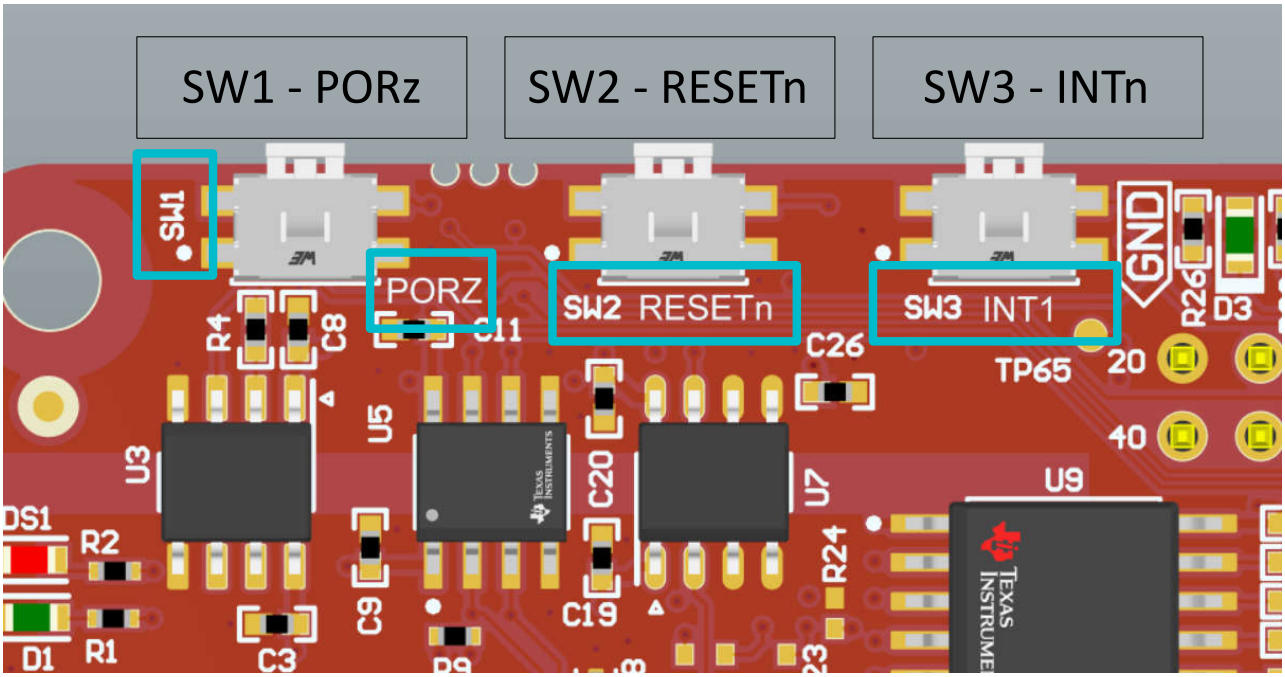


Figure 2-6. Push Buttons

Table 2-11 lists the push buttons that are placed on the top side of the AM261x LaunchPad.

Table 2-11. LaunchPad Push Buttons

Push Button	Signal	Function
SW1	PORz	SoC PORz reset input
SW2	RESETz	SoC warm reset input
SW3	INT1	User Interrupt Signal

2.5 Reset

Figure 2-7 shows the reset architecture of the AM261x LaunchPad

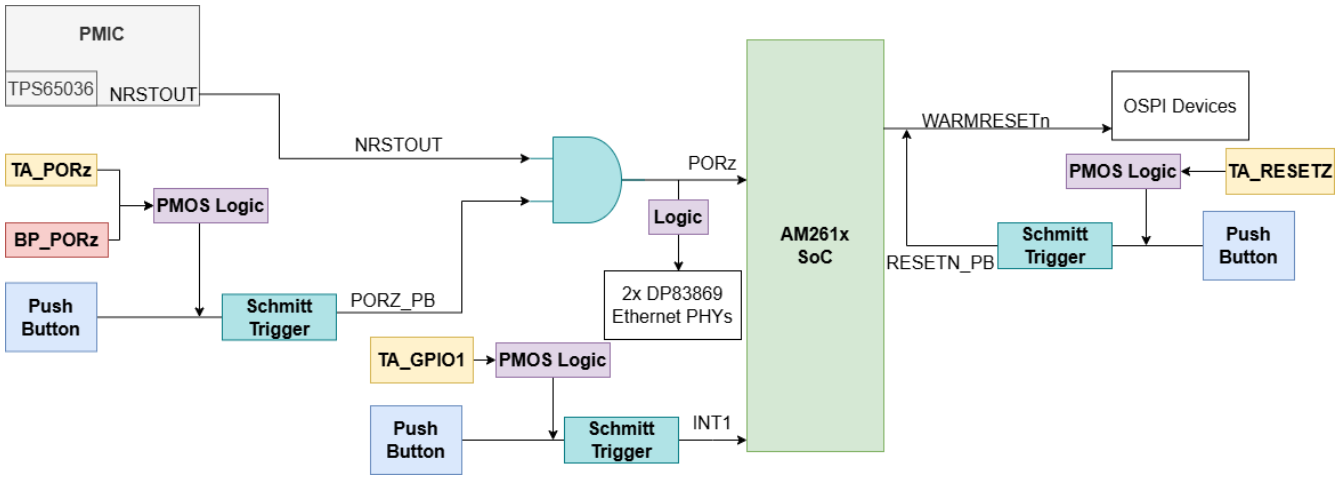


Figure 2-7. Reset Architecture

The AM261x LaunchPad has the following resets:

- PORz (Power On Reset)
- WARMRESETn (Warm Reset)

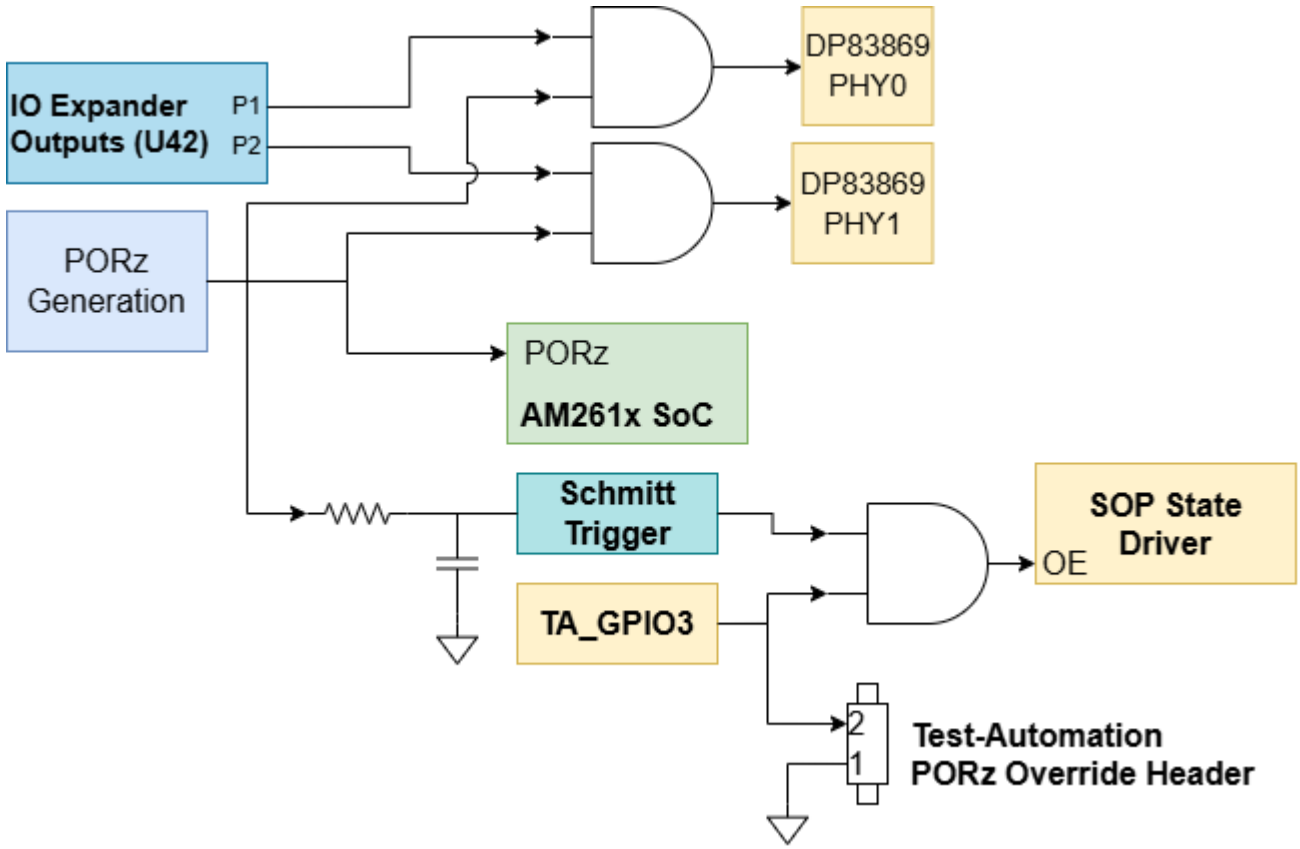


Figure 2-8. PORZ Reset Signal Tree

PORz

The PORz signal is driven by a 2-input AND gate that generates a power on reset for the MAIN domain when:

- The PMIC's (TPS650360) NRSTOUT is driven low
- The user push button (SW1) is pressed.
- A P-Channel MOSFET gate's signal is logic LOW which causes V_{GS} of the PMOS to be less than zero. The PORz signal connects to the PMOS drain which is tied directly to ground. The signals that can create the logic LOW input to the PMOS gate are:
  - TA_PORZ output from the Test Automation header
  - BP_PORZ output from either of the BoosterPack sites.

The PORz signal is tied to:

- AM261x SoC PORz input
- Both Ethernet add-on board connector reset logic
- Boot mode State Driver (U61) output enable input
  - There is an RC filter to create a 1ms delay from GND to 3.0V such that the SOP State Driver's output enable input is low longer than the required SOP hold time following a PORz de-assertion.

WARMRESETn

The WARMRESETn signal creates a warm reset to the MAIN domain when:

- The user push button (SW2) is pressed.

The WARMRESETn signal is tied to:

- AM261x SoC WARMRESETN output
- RESETN_PB signal that is created from push button + PMOS logic
- OSPI0 and OSPI1 device reset logic

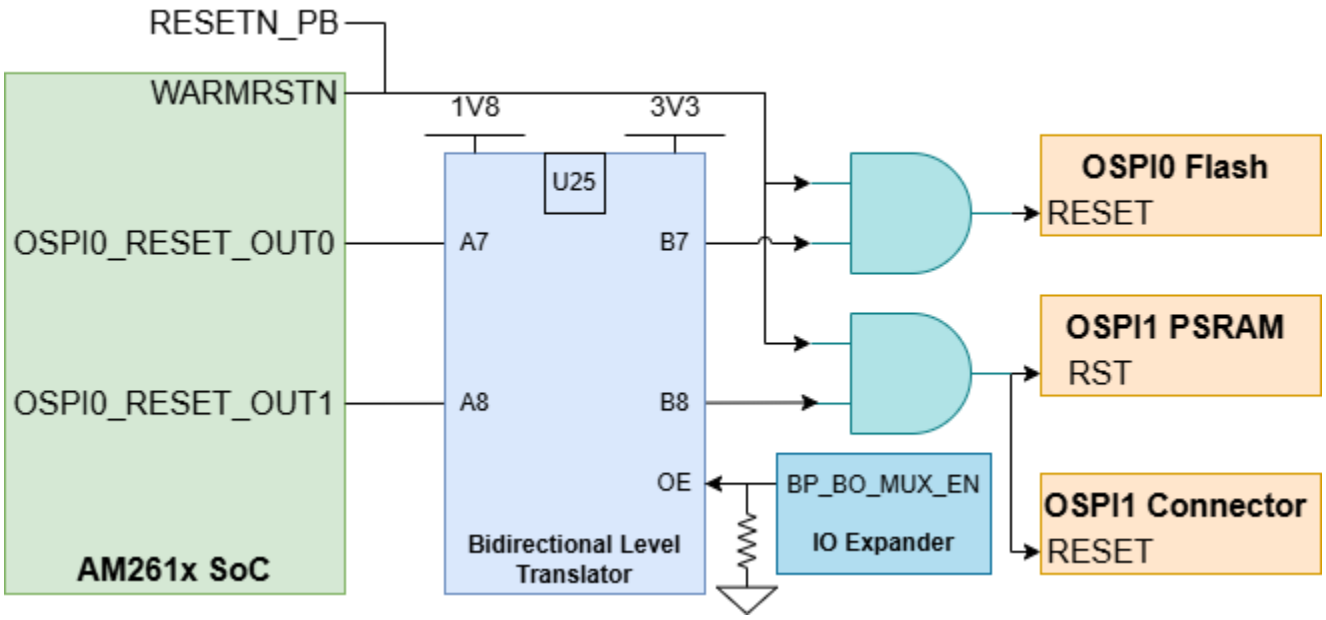


Figure 2-9. WARMRESETn Reset Signal Tree

Note

OSPI0_RESET_OUT0 is pinmuxed from GPIO61, which has a known issue associated with the AM261x boot ROM. At boot, the ROM code sets GPIO61 to OSPI0_RESET_OUT0 and drives the pin low to reset an external flash device. However, due to an error in the OSPI controller configuration, the pin does not drive high once the flash device has been reset, thus holding the flash device in reset and preventing proper boot. The bidirectional level translator (U25) is disabled by default through a pull resistor connected to the Output Enable pin. This prevents the OSPI0_RESET_OUT0 (on GPIO61) from pulling the input to the AND gate low before the device boots from the OSPI0 flash. The OSPI0_RESET_OUT0 net is pulled high at the AND gate. Once the device boots, OSPI0_RESET_OUT0 can be configured in software as an OSPI reset, and the level translator (U25) can be enabled from the I2C-controlled IO expander (U23). For more information on this boot ROM issue, see the AM261x Errata Document.

INTn

The AM261x LaunchPad also has an external interrupt to the SoC , INT1, that occurs when:

- The user push button (SW3) is pressed

2.6 Clock

The AM261x SoC requires a 25MHz clock input for XTAL_XI. The AM261x LaunchPad uses a 25MHz crystal for the SoC clock source. The LaunchPad also has two 25MHz Crystals onboard for the Ethernet PHY clocking which can be connected to the ethernet port connectors on the board using ethernet add-on boards. The SoC clock signal output CLKOUT1 can be used as a clock source for an Ethernet PHY on an attached Ethernet add-on board. The resistors (R211 & R214) must be removed from the traces connecting the 25MHz Crystals to Ethernet Connector 0 and Ethernet Connector 1. Mount the appropriate resistors (R212 & R213) for CLKOUT1 to be routed to both of the Ethernet add-on board connectors to connect the CLKOUT1 net to the XI pin of the Ethernet PHYs on the add-on boards.

The LaunchPad also has a on board crystal (Y4) of frequency 16MHz which is clock source for the XDS110 for UART-USB JTAG support.

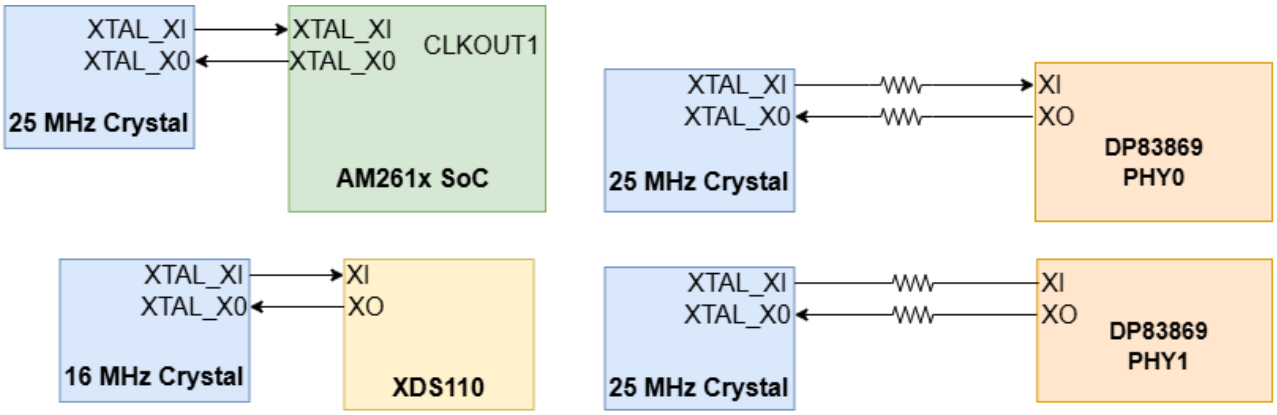


Figure 2-10. AM261x LaunchPad Clock Tree

2.7 Boot Mode Selection

The boot mode for the AM261x is selected by a DIP (Dual In-Line Package) switch (SW4) or the test automation header. The test automation header uses an I2C expansion buffer to drive the boot mode when PORz is toggled. The supported boot modes are shown in Table 2-12. The DIP Switch configurations for each boot mode are shown in Table 2-13.

Note

The Boot Mode DIP Switch Positions on the LP-AM261 are the **inverse** of the SOPx settings. For example, if a boot mode setting calls for SOP3=0, then SW4.4=1.

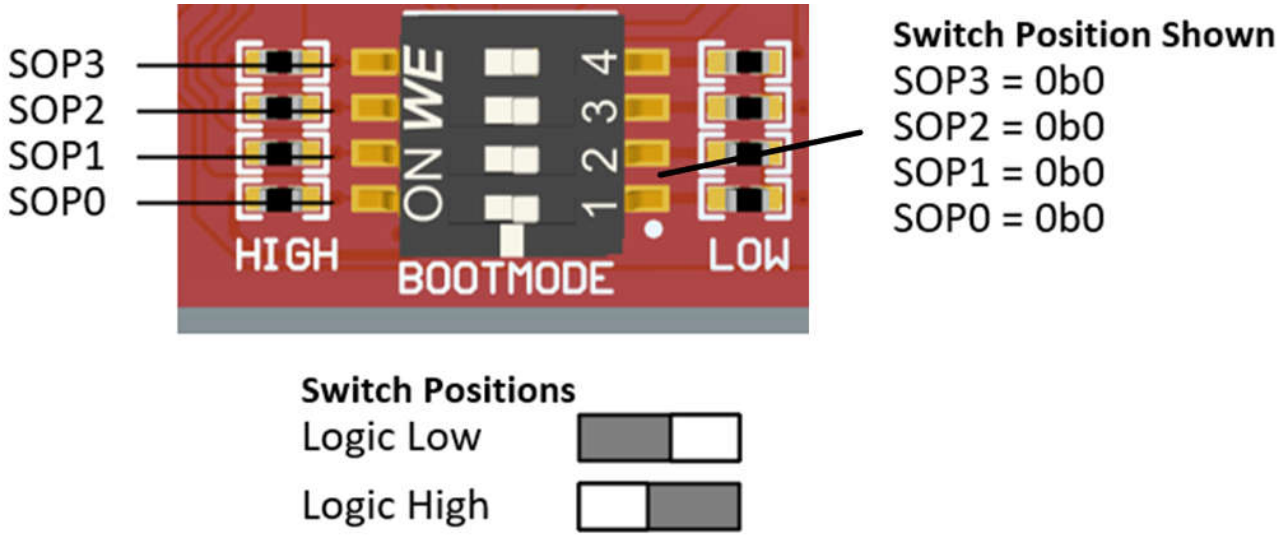


Figure 2-11. Boot mode DIP Switch Positions - LP AM261x E2 SW1 SOP Switches

Table 2-12. Supported Boot Modes

Boot Mode or Peripheral	Boot Media or Host	ROM Activity / Notes
OSPI-OSPI (4S), 50MHz, SDR, 0x6B	Flash Memory	ROM configures OSPI controller in OSPI 4S mode and downloads image from external flash, supports UART fallback boot mode if any failures
UART, XMODEM, 115200bps	External Host	ROM configures UART0 with baud rate of 115200 bps and downloads image from external PC terminal using x-modem protocol
OSPI-OSPI (1S), 50MHz, SDR, 0x0B	Flash Memory	ROM configures OSPI controller in OSPI 1S mode and downloads image from external flash, supports UART fallback boot mode if any failures
OSPI (8S), SDR, 33 MHz, 0x8B	Flash Memory	ROM configures OSPI controller in 8S mode and downloads image from external flash, supports UART fallback boot mode if any failures
DevBoot	N/A	To support SBL development, R5-will come up with ROM eclipsed, PLLs are initialized, No L2, TCMA and TCMB PBIST are performed, No L2 and TCM memInit. Supported only on FS devices

Table 2-12. Supported Boot Modes (continued)

Boot Mode or Peripheral	Boot Media or Host	ROM Activity / Notes
xSPI (1S->8D), 20 MHz, SFDP	Flash Memory, External Host	ROM configures OSPI controller in xSPI 8D mode, Reads SFDP table for read command and downloads image from external flash, Flashes with SFDP are of JEDEC standard Rev D only supported. In case of any failure it falls back to UART boot mode
USB DFU	External Host	ROM configures USB controller to work in device mode and download the image into L2 memory to process. In case of any failure it falls back to UART boot mode. Supports USB 2.0 device mode at High-Speed (HS, 480 Mbps)

Table 2-13. Boot Mode Selection

Boot Mode	AM261x SOP[3:0]	SW4.4 (SOP3 Inverse)	SW4.3 (SOP2 Inverse)	SW4.2 (SOP1 Inverse)	SW4.1 (SOP0 Inverse)
OSPI-OSPI (4S), 50MHz, SDR, 0x6B	**0000**	1	1	1	1
UART, XMODEM, 115200bps	**0001**	1	1	1	0
OSPI-OSPI (1S), 50MHz, SDR, 0x0B	**0010**	1	1	0	1
OSPI (8S), SDR, 33 MHz, 0x8B	**0011**	1	1	0	0
DevBoot	**1011**	0	1	0	0
xSPI (1S->8D), 20 MHz, SFDP	**1100**	0	0	1	1
USB DFU	**1110**	0	0	0	1

2.8 GPIO Mapping

Table 2-14. GPIO Mapping Table

GPIO Description	GPIO	Functionality	Net Name	Active Status
GPIO LED	GPIO84	GPIO	AM261_LED_GPIO84	LOW
Interrupt To SoC	GPIO124	Interrupt	AM261_INT_PB_GPIO124	LOW

2.9 IO Expander

The AM261x LaunchPad has two TCA6408ARGTR IO Expanders that provide general-purpose I/O expansion and bidirectional voltage translation for processors through I2C communication.

The TCA6408A consists of one 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high) Register. At power on, the I/Os are configured as inputs. The system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output Register. The polarity of the Input Port Register can be inverted with the Polarity Inversion Register. All registers can be read by the system controller. The AM261x MCU communicates with the IO Expander through the I2C0 bus. The signals coming out of the IO Expander are shown in Figure 2-12. Refer to the TCA6408ARGTR Data sheet for the programming guide for TCA6408ARGTR.

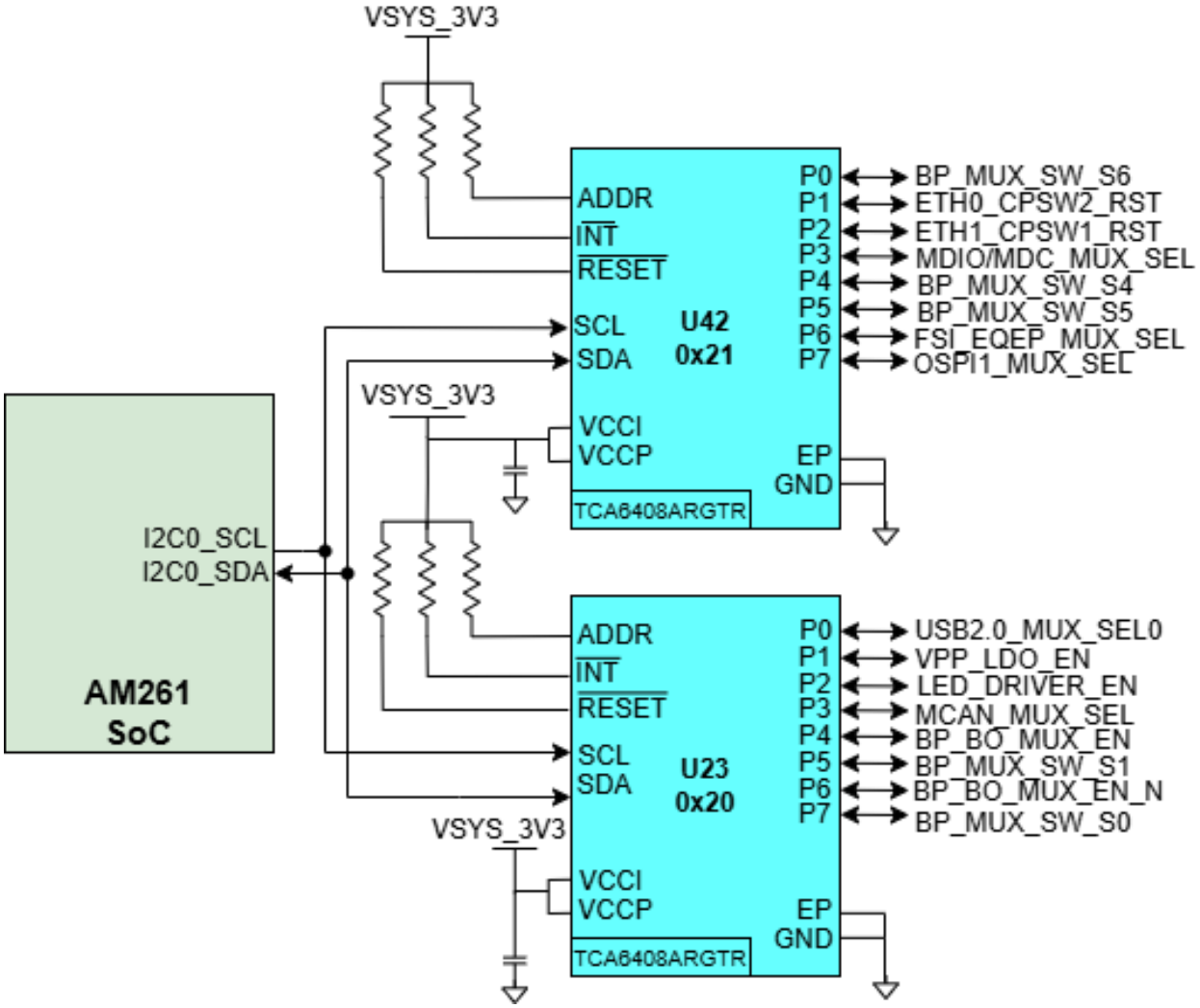


Figure 2-12. IO Expander

Table 2-15. IO Expander 1 GPIO Mapping (U42)

IO#	Net Name	GPIO Description	Active Status
P0	BP_MUX_SW_S6	Alternate BoosterPack function mux U81 select	PREFERABLE
P1	ETH0_CPSW2_RST	DP83869 PHY (U73) Reset	LOW
P2	ETH1_CPSW1_RST	DP83869 PHY (U74) Reset	LOW
P3	MDIO/MDC_MUX_SEL	MDIO/MDC mux select	PREFERABLE
P4	BP_MUX_SW_S4	Alternate BoosterPack function mux U46 select	PREFERABLE
P5	BP_MUX_SW_S5	Alternate BoosterPack function mux U80 select	PREFERABLE
P6	FSI_EQEP_MUX_SEL	FSI/EQEP mux select	PREFERABLE
P7	OSPI1_MUX_SEL	OSPI1 mux select	PREFERABLE

Table 2-16. IO Expander 2 GPIO Mapping (U23)

IO#	Net Name	GPIO Description	Active Status
P0	USB2.0_MUX_SEL0	USB mux select	PREFERABLE
P1	VPP_LDO_EN	1.7V LDO enable	HIGH
P2	LED_DRIVER_EN	LED driver enable	LOW
P3	MCAN_MUX_SEL	MCAN mux select	PREFERABLE
P4	BP_BO_MUX_EN	EPWM bidirectional level translator enable	HIGH
P5	BP_MUX_SW_S1	Input 1 to XOR gate controlling alternate boosterpack function mux	PREFERABLE
P6	BP_BO_MUX_EN_N	Alternate boosterpack function mux output enable	LOW
P7	BP_MUX_SW_S0	Input 0 to XOR gate controlling alternate boosterpack function mux	PREFERABLE

2.10 Interfaces

2.10.1 Memory Interfaces

2.10.1.1 OSPI

OSPI Flash

The LP-AM261 has a 64Mb, 1.8V OSPI flash memory device (MX25UW6445GXDQ00) connected to the OSPI0 interface of the AM261x MCU. The OSPI flash device is powered by the 1.8V LDO output from the PMIC. The AM261x can boot from binary images flashed to this memory device connected to OSPI0.

Note

There is a known limitation with the OSPI0 flash reset with a workaround implemented on the LP-AM261. For more details, see Section 6.2.2.

OSPI PSRAM

The LP-AM261 has a 128Mb, 1.8V PSRAM memory device (APS12808L-OBMX-BA) connected to the OSPI1 interface of the AM261x MCU. The OSPI PSRAM is powered by the 1.8V LDO output from the PMIC. The AM261x can utilize this interface for external memory.

Note

AM261x cannot boot from the PSRAM device connected to OSPI1.

OSPI Expansion Connector

The AM261x OSPI1 signal traces have the option to be routed to a 30-pin high-density connector for connecting compatible OSPI memory add-on boards. Table 2-17 details the resistor modifications that need to be made in order to enable the OSPI1 routing path to the expansion connector.

Table 2-17. OSPI Expansion Connector Resistor Mods

LP-AM261 Net	DNI Resistor	Populate Resistor
EX_OSPI1_CLK	R242	R245
EX_OSPI1_D0	R291	R286
EX_OSPI1_D1	R282	R276
EX_OSPI1_D2	R294	R289
EX_OSPI1_D3	R283	R277
EX_OSPI1_D4	R292	R287
EX_OSPI1_D5	R284	R278
EX_OSPI1_D6	R295	R290
EX_OSPI1_D7	R285	R279
EX_OSPI1_DQS	R293	R288
EX_OSPI1_CSn0	R248	R243
EX_OSPI1_ECC_FAIL	R249	R244
EX_OSPI1_RSTn	R247	R241

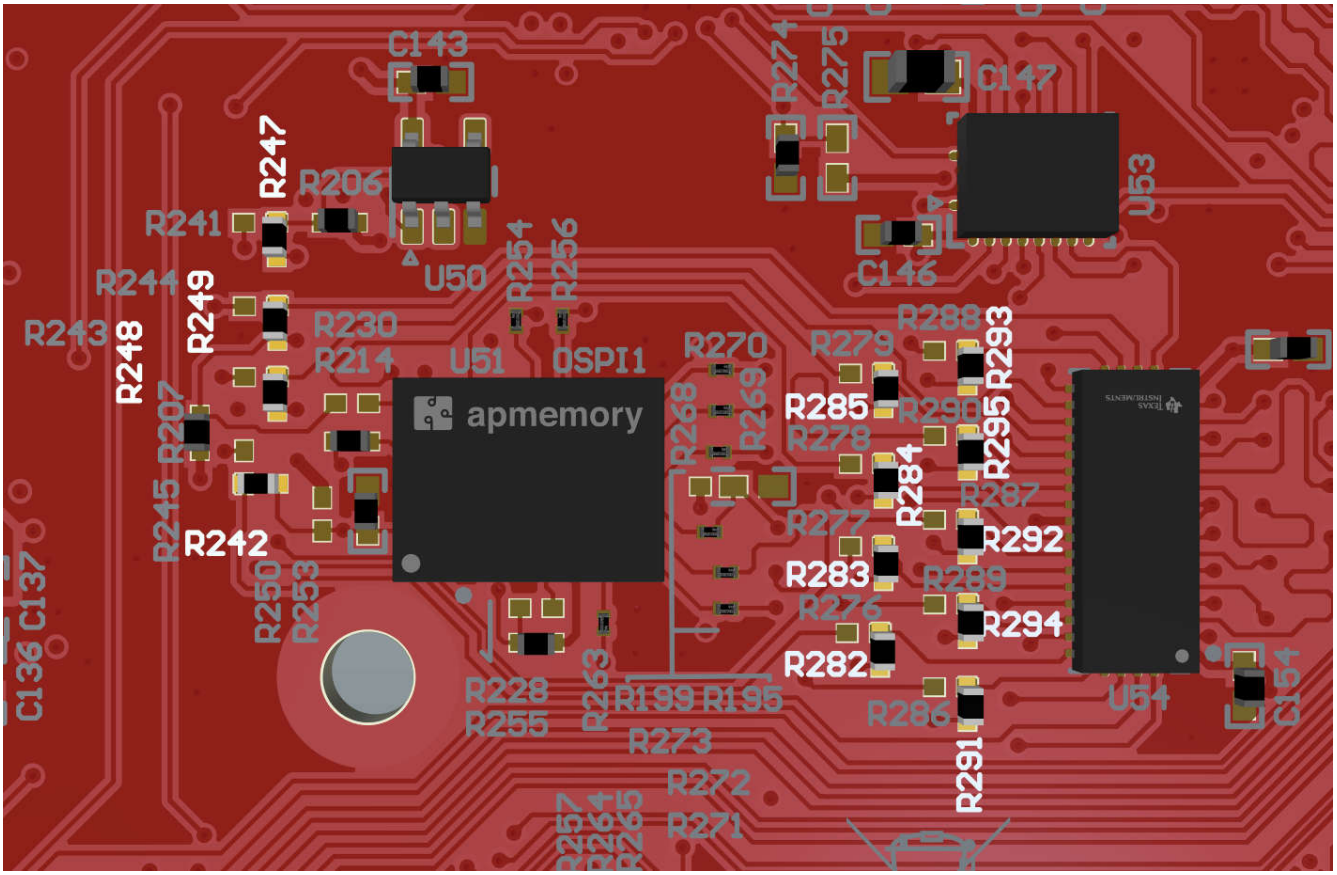


Figure 2-13. OSPI1 Expansion Connector - Depopulate Resistors

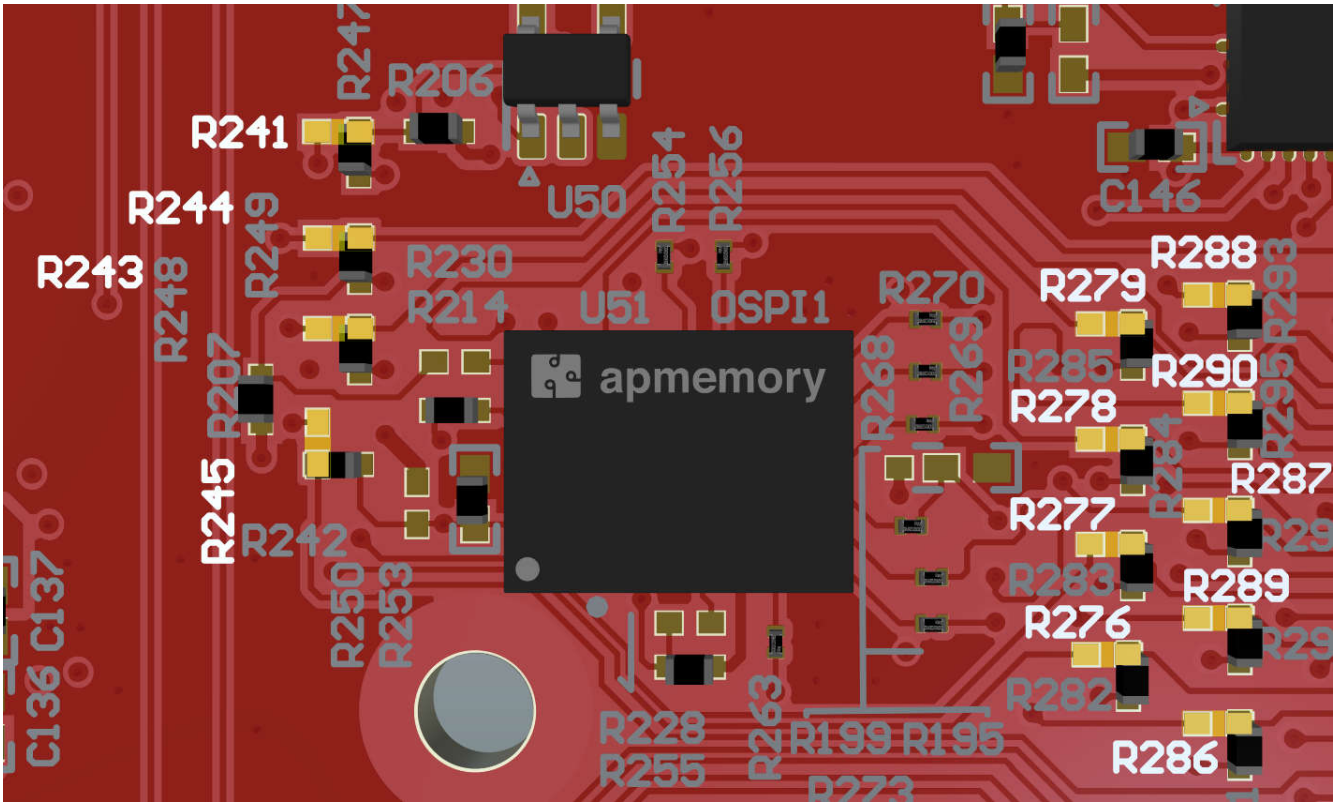


Figure 2-14. OSPI1 Expansion Connector - Populate Resistors

The pinout of the OSPI Expansion Connector can be found in Section 2.3.1, *OSPI Expansion Connector*.

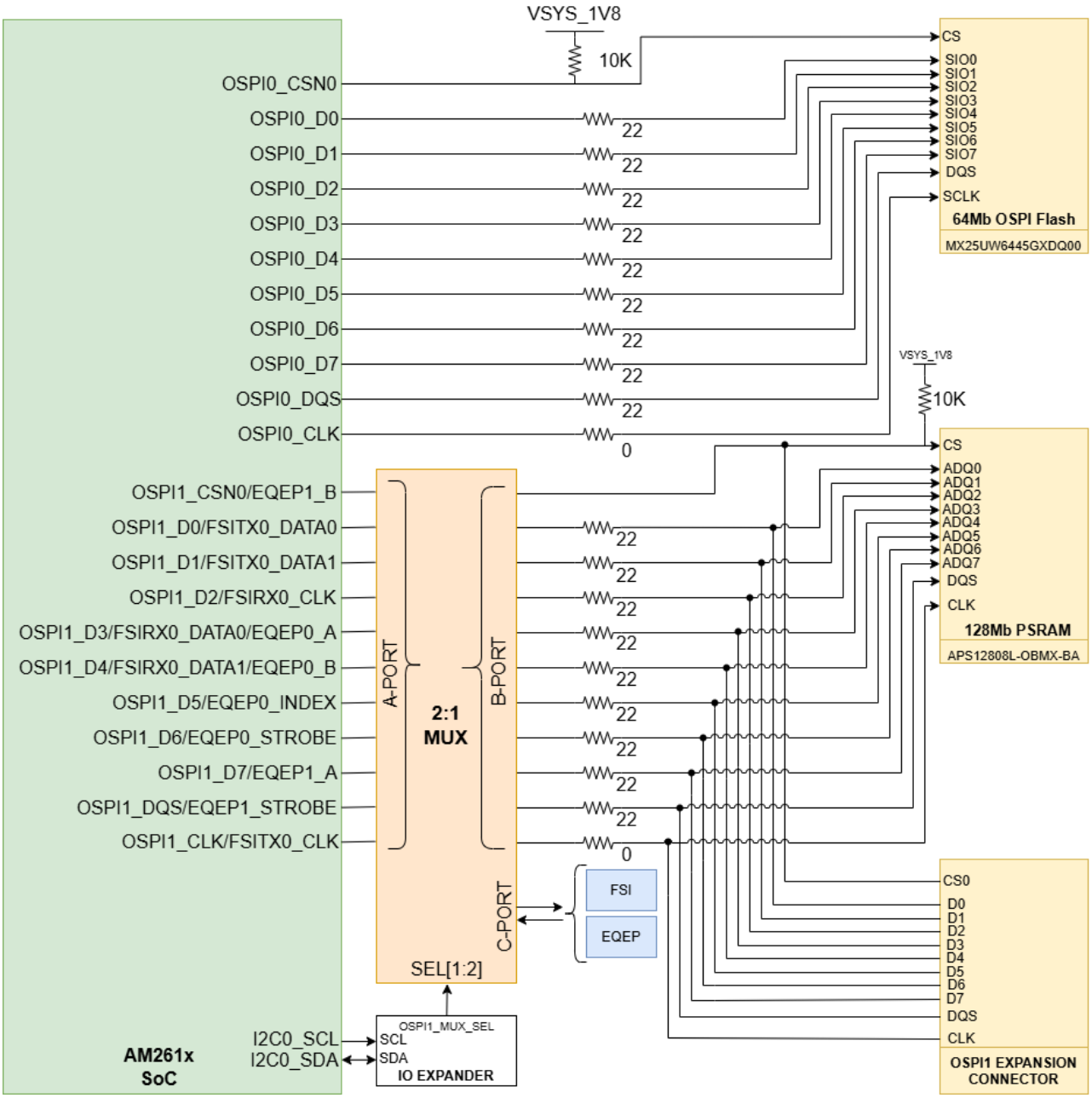


Figure 2-15. LP-AM261 OSPI Interface

2.10.1.2 Board ID EEPROM

The AM261x LaunchPad has a I2C-based 1Mbit EEPROM (CAT24M01WI-GT3) to store board configuration details. The Board ID EEPROM is connected to the I2C1 interface of the AM261x MCU. The default I2C address of the EEPROM is set to 0x51 by pulling up the address pin A0 to 3.3V, and pulling down the address pins A1 and A2 to ground. The Write Protect pin for the EEPROM is by pulled to ground by default. Therefore, Write Protect is disabled.

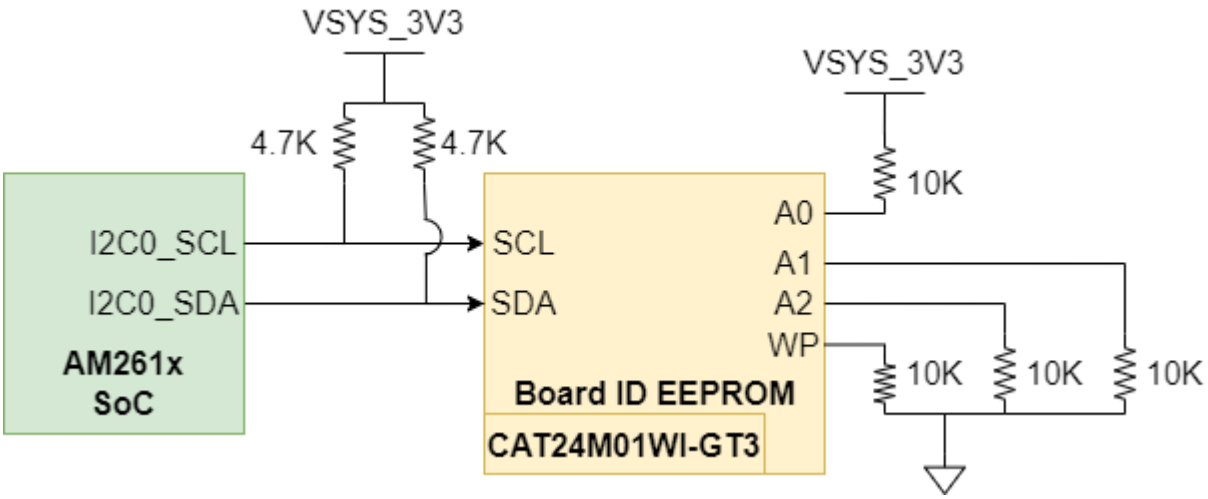


Figure 2-16. Board ID EEPROM

2.10.2 Ethernet Interface

The LP-AM261 has two DP83869 gigabit Ethernet PHYs with RJ-45 connectors for enabling RGMII or MII Ethernet evaluation and development. The Ethernet peripheral to PHY connectivity is detailed in the following table:

Table 2-18. Ethernet Peripheral - PHY Connections

Ethernet Signals	PHY 0 (U73)	PHY 1 (U74)
RGMII1		✓
RGMII2	✓	
CPSW MDIO	✓ (via MUX)	✓ (via MUX)
PR0_PRU0	✓	
PR0_PRU1		✓
PRU MDIO	✓ (via MUX)	✓ (via MUX)

2.10.2.1 Ethernet PHY 0 - RGMII2 / PR0_PRU0

The AM261x LaunchPad utilizes a 48-pin Ethernet PHY (DP83869HMRGZT) connected to RGMII2, or the PR0_PRU0 instance of the on-die Programmable Real-time Unit and Industrial Communication Sub System (PRU-ICSS). The RGMII2 and PR0_PRU0 signals are interrnally pinmuxed on the AM261x MCU, and can be software controlled depending on the application.

The PHY is configured to advertise 1-Gb operation. The Ethernet data signals of the PHY are terminated to an RJ45 connector. The RJ45 connector is used on the board for Ethernet 10/100/1000Mbps connectivity with integrated magnetics and LEDs for link and activity indication.

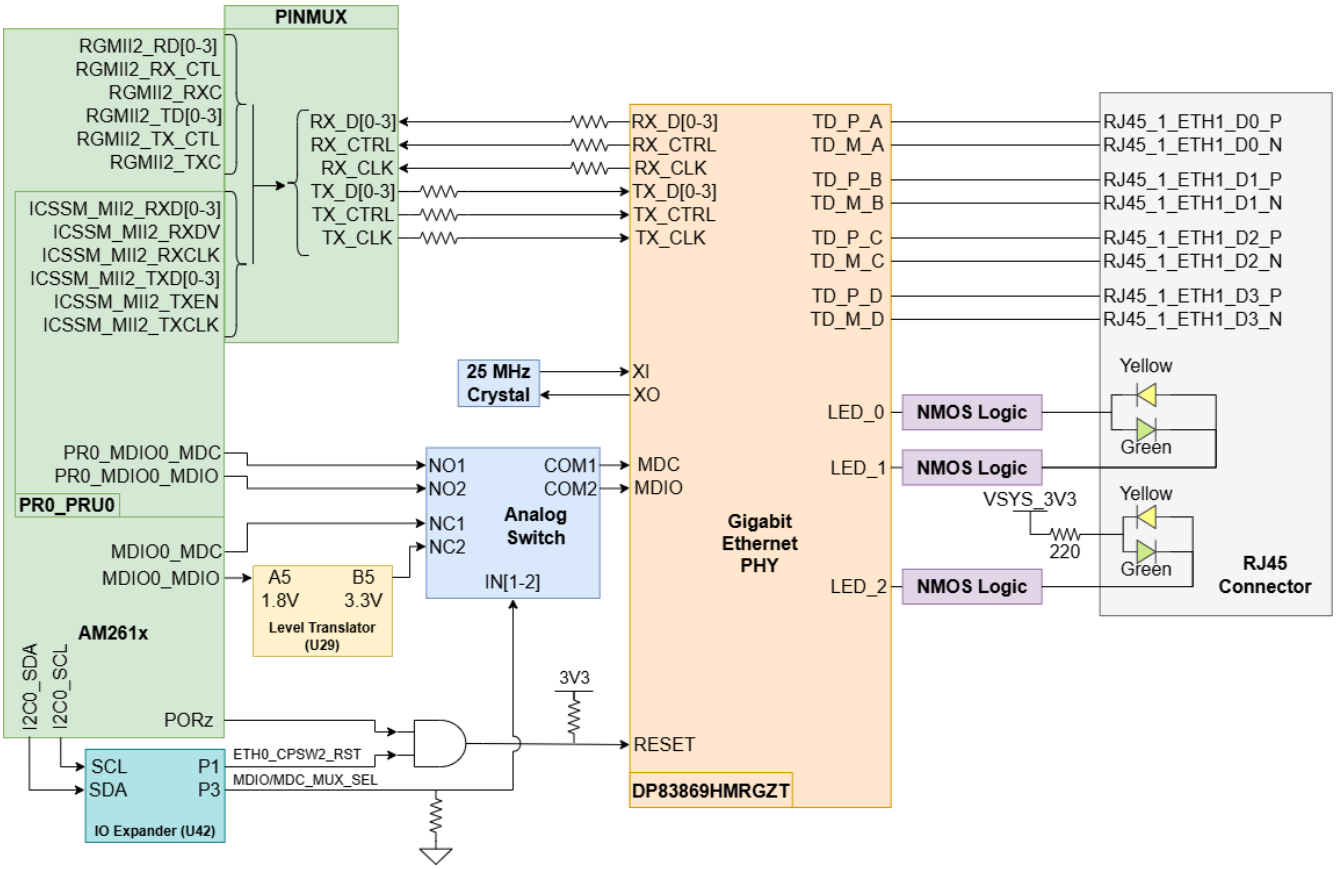


Figure 2-17. Ethernet PHY 0

The Ethernet PHY requires three separate power sources. VDDIO is the 3.3V, system generated supply. There are dedicated LDOs for the 1.1V and 2.5V supplies for the Ethernet PHY.

There are series termination resistors on the transmit clock and data signals located near the SoC. There are series termination resistors on the receive clock and data signals near the Ethernet PHY.

The CPSW MDIO data signal from the AM261x MCU to the PHY is passed through a bi-directional level translator in order to shift the IO level from 1.8V to 3.3V for compatibility with the DP83869 PHY. The CPSW MDIO clock signal does not require level shifting, as it originates from a 3.3V IO pin at the AM261x MCU. Because CPSW Ethernet and PRU Ethernet have independent MDIO signals, an analog switch (TS5A23159DGSR/U48) selects between the CPSW MDIO/MDC and the PRU MDIO/MDC signals to be routed to the Ethernet PHY. The analog switch is controlled by a GPIO signal from the I2C-controlled IO Expander (U42).

Table 2-19. CPSW/PRU-ICSS MDIO Switch (U48)

MDIO/MDC_MUX_SEL	Condition	Switch Function
LOW (default)	CPSW MDIO	NC to COM, COM to NC
HIGH	PRU MDIO	NO to COM, COM to NO

The reset input for the Ethernet PHY is controlled by the PORz AM261x MCU output signal ANDed with an output from the I2C-controlled IO Expander (U42), ETH0_CPSW2_RST.

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

Table 2-20. Ethernet PHY 0 Strapping Resistors

Functional Pin	Default Mode	Mode in LaunchPad	Function
RX_D0	0	3	PHY address: 0011
RX_D1	0	0	
JTAG_TDO/GPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	
LED_0	0	0	Auto-negotiation, 10/100/1000 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port Mirroring Disabled

Note

Each strap pin has an internal pull down resistance of 2.49kΩ

Note

RX_D0 and RX_D1 are on a 4-level strap resistor mode scheme. All other signals are 2-level strap resistor modes.

2.10.2.2 Ethernet PHY 1 - RGMII1 / PR0_PRU1

The AM261x LaunchPad utilizes a 48-pin Ethernet PHY (DP83869HMRGZT) connected to RGMII1, or the PR0_PRU1 instance of the on-die Programmable Real-time Unit and Industrial Communication Sub System (PRU-ICSS). The RGMII1 and PR0_PRU1 signals are interrnally pinmuxed on the AM261x MCU, and can be software controlled depending on the application.

The PHY is configured to advertise 1-Gb operation. The Ethernet data signals of the PHY are terminated to an RJ45 connector. The RJ45 connector is used on the board for Ethernet 10/100/1000Mbps connectivity with integrated magnetics and LEDs for link and activity indication.

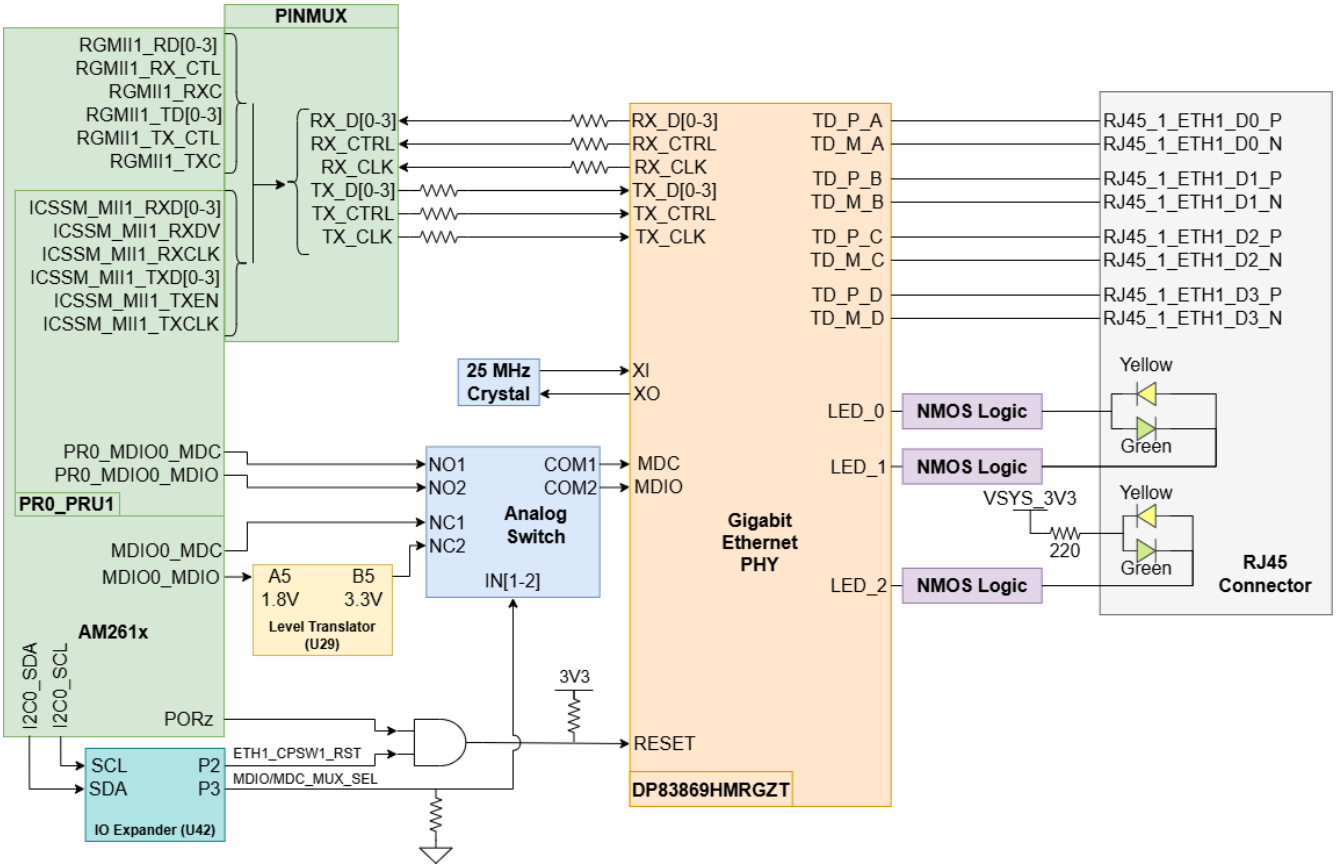


Figure 2-18. Ethernet PHY 1

The Ethernet PHY requires three separate power sources. VDDIO is the 3.3V, system generated supply. There are dedicated LDOs for the 1.1V and 2.5V supplies for the Ethernet PHY.

There are series termination resistors on the transmit clock and data signals located near the SoC. There are series termination resistors on the receive clock and data signals near the Ethernet PHY.

The CPSW MDIO data signal from the AM261x MCU to the PHY is passed through a bi-directional level translator in order to shift the IO level from 1.8V to 3.3V for compatibility with the DP83869 PHY. The CPSW MDIO clock signal does not require level shifting, as it originates from a 3.3V IO pin at the AM261x MCU. Because CPSW Ethernet and PRU Ethernet have independent MDIO signals, an analog switch (TS5A23159DGSR/U48) selects between the CPSW MDIO/MDC and the PRU MDIO/MDC signals to be routed to the Ethernet PHY. The analog switch is controlled by a GPIO signal from the I2C-controlled IO Expander (U42).

Table 2-21. CPSW/PRU-ICSS MDIO Switch (U48)

MDIO/MDC_MUX_SEL	Condition	Switch Function
LOW (default)	CPSW MDIO	NC to COM, COM to NC
HIGH	PRU MDIO	NO to COM, COM to NO

The reset input for the Ethernet PHY is controlled by the PORz AM261x MCU output signal ANDed with an output from the I2C-controlled IO Expander (U42), ETH1_CPSW1_RST.

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

Table 2-22. Ethernet PHY 1 Strapping Resistors

Functional Pin	Default Mode	Mode in LP	Function
RX_D0	0	0	PHY address: 1100
RX_D1	0	3	
JTAG_TDO/GPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	
LED_0	0	0	Auto-negotiation, 1000/100/10 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port Mirroring Disabled

Note

Each strap pin has an internal pull down resistance of 2.49kΩ

Note

RX_D0 and RX_D1 are on a 4-level strap resistor mode scheme. All other signals are 2-level strap resistor modes.

2.10.3 I2C

The AM261x LaunchPad uses two AM261x SoC inter-integrated circuit (I2C) instances to operate as a controller for various targets. I2C data and clock lines are pulled up to the 3.3V system voltage supply.

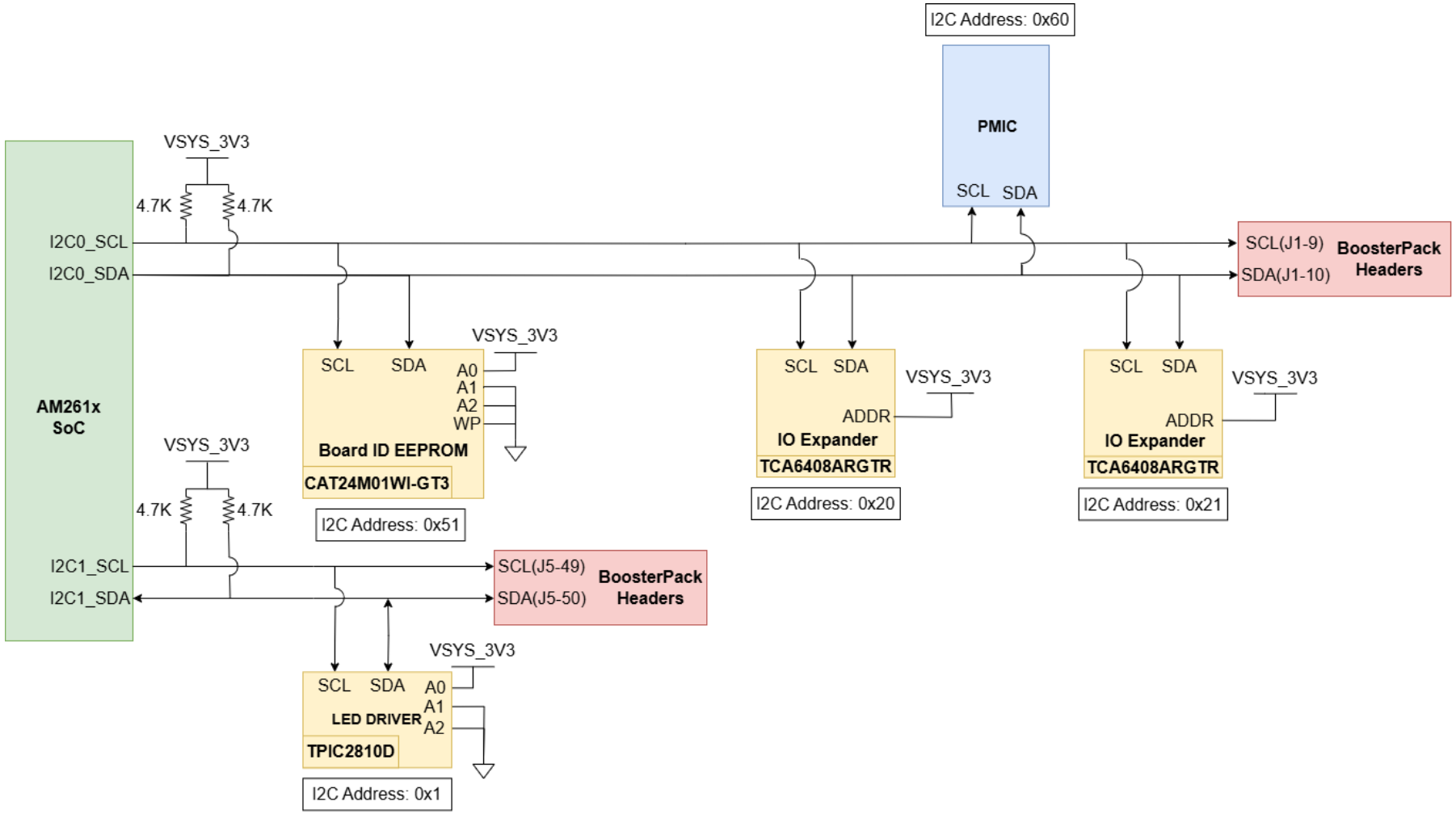


Figure 2-19. LP-AM261 I2C Interface

Table 2-23. I2C Addressing

Target	I2C Instance	I2C Addres Bit Description	Device Addressing	LaunchPad Config.	I2C Address
Board ID EEPROM	I2C0	The first 4 bits of the device address are set to 1010, the next two are set by the A2 and A1 pins, the seventh bit, a16, is the most significant internal address bit	0b10110[A2][A1][a16] A1 and A2 are connected to ground	0b1010001	0x51

Table 2-23. I2C Addressing (continued)

Target	I2C Instance	I2C Addres Bit Description	Device Addressing	LaunchPad Config.	I2C Address
LED Driver	I2C1	The first four bits of the target address are 0000, the following three are determined by A2, A1, and A0	0b0000[A2][A1][A0] A2 and A1 are connected to ground A0 is connected to 3.3V supply	0b0000001	0x01
BoosterPack Headers	I2C0, I2C1	Target dependent			
IO Expander #1	I2C0	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	IO_ADDR pin connected to 3.3V supply	0b0100001	0x21
IO Expander #2	I2C0	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	IO_ADDR pin connected to 3.3V supply	0b0100000	0x20
PMIC	I2C0	7 bit device address for the PMIC is 1100000	0b1100000	0b1100000	0x60

Note

Underlined address bits are fixed based on the device addressing and cannot be configured.

2.10.3.1 Industrial Application LEDs

The AM261x LaunchPad has an LED Driver (TPIC2810D) that is used for controlling the Industrial Communication LED array. The driver is connected to eight green LEDs and has an I2C address of 0x01.

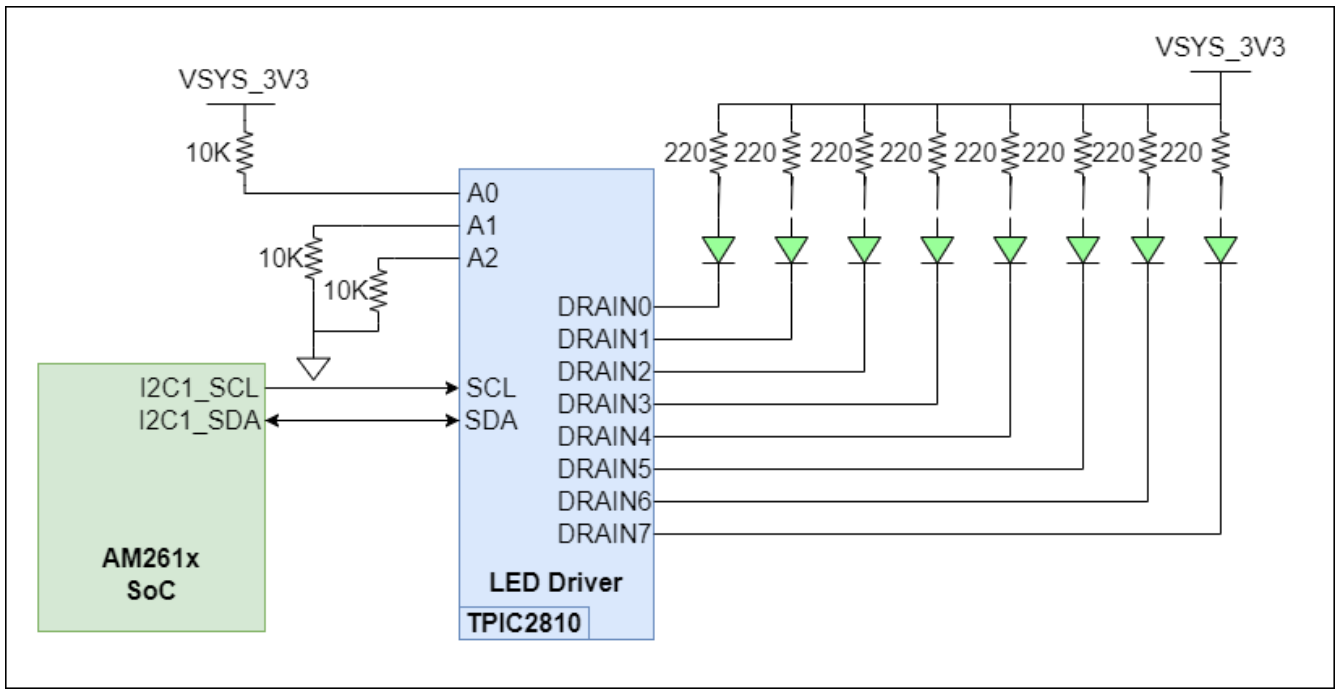


Figure 2-20. Industrial Application I2C LED Array

2.10.4 SPI

The AM261x LaunchPad maps two SPI instances (SPI0, SPI2) from the AM261x MCU to the BoosterPack headers. Series termination resistors are placed near the SoC for each SPI clock and SPI D0 signal. There are a series of muxes that route the SPI0 signals to the BoosterPack headers depending on the BoosterPack mode selected. The following tables detail the mux select signals for routing SPI0 signals to the BoosterPack headers:

Table 2-24. U68 Mux Select

BP_MUX_SW_S3 (GPIO43)	Mux Output (COM)
0	**SPI0_D1**
1	PR1_PRU1_GPIO15

Table 2-25. U56 Mux Select

BP_MUX_SW_S0	BP_MUX_SW_S1	Mux Output (4A)
0	**0**	**SPI0_CLK**
0	1	PR1_PRU1_GPIO2
1	**0**	**SPI0_CLK**
1	**1**	**SPI0_CLK**

Table 2-26. U67 Mux Select

BP_MUX_SW_S0	BP_MUX_SW_S1	Mux Output (4A)
0	**0**	**SPI0_CS0**
0	1	SDFM0_D2
1	0	PR1_PRU1_GPIO1
1	**1**	**SPI0_CS0**

Table 2-27. U31 Mux Select

BP_MUX_SW_S0	BP_MUX_SW_S1	Mux Output (1A)
0	**0**	**SPI0_D0**
0	1	SDFM1_D1
1	0	SDFM1_D1
1	**1**	**SPI0_D0**

All SPI2 signals are directly routed to the boosterpack.

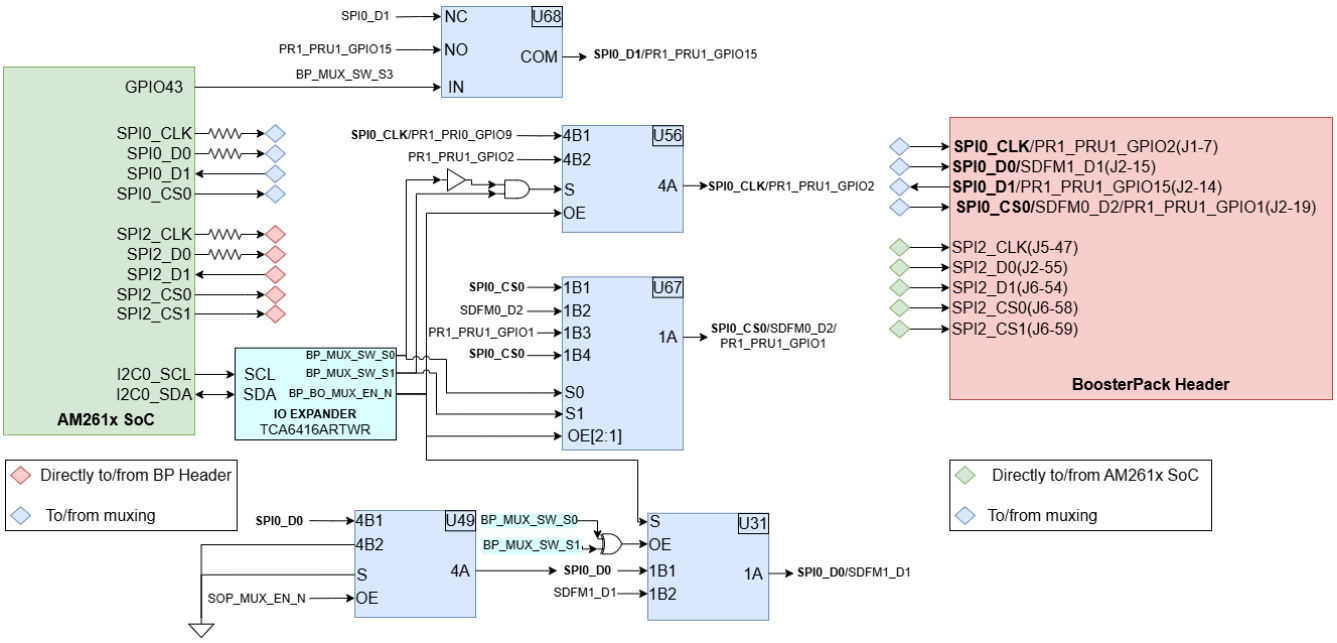


Figure 2-21. LP-AM261 SPI Interface

2.10.5 UART

The AM261x LaunchPad uses the XDS110 as a USB2.0 to UART bridge for terminal access. UART0 transmit and receive signals of the AM261x SoC are mapped to the XDS110 with a dual channel isolation buffer (ISO7721DR) for translating from the 3.3V IO voltage supply to the 3.3V XDS supply. The XDS110 is connected to a micro-B USB connector for the USB 2.0 signals. ESD protection is provided to the USB 2.0 signals by a transient voltage suppression device (TPD4E02B04DQAR). The micro-B USB connector's VBUS 5V power is mapped to a low dropout regulator (TPS79601DRBR) to generate the 3.3V XDS110 supply. A separate 3.3V supply for the XDS110 allows for the emulator to maintain a connection when power to the LaunchPad is removed.

Two instances of UART3 are brought out to the BoosterPack headers. If the pinmux on AM261x pins C19 and C18 are configured for UART3 TXD/RXD, the signals can be accessed on header J1. If the pinmux on AM261x pins A14 and B14 are configured for UART, the signals can be accessed on header J5. Multiplexers are included on the paths from the AM261x MCU to the BoosterPack headers to enable other BoosterPack modes. The logic tables for these muxes are shown below:

Table 2-28. U46 Mux Select

BP_MUX_SW_S4	BP_BO_MUX_EN_N	Mux Output (1A)
0	0	Hi-Z
0	1	**UART3_RXD**
1	0	Hi-Z
1	1	SDFM1_D0

Table 2-29. U80 Mux Select

BP_MUX_SW_S5	COM
0	UART3_TXD
1	PR1_PRU1_GPIO3

Table 2-30. U37 Mux Select

BP_MUX_SW_S1	COM
0	UART3_RXD
1	PR1_PRU0_GPIO19

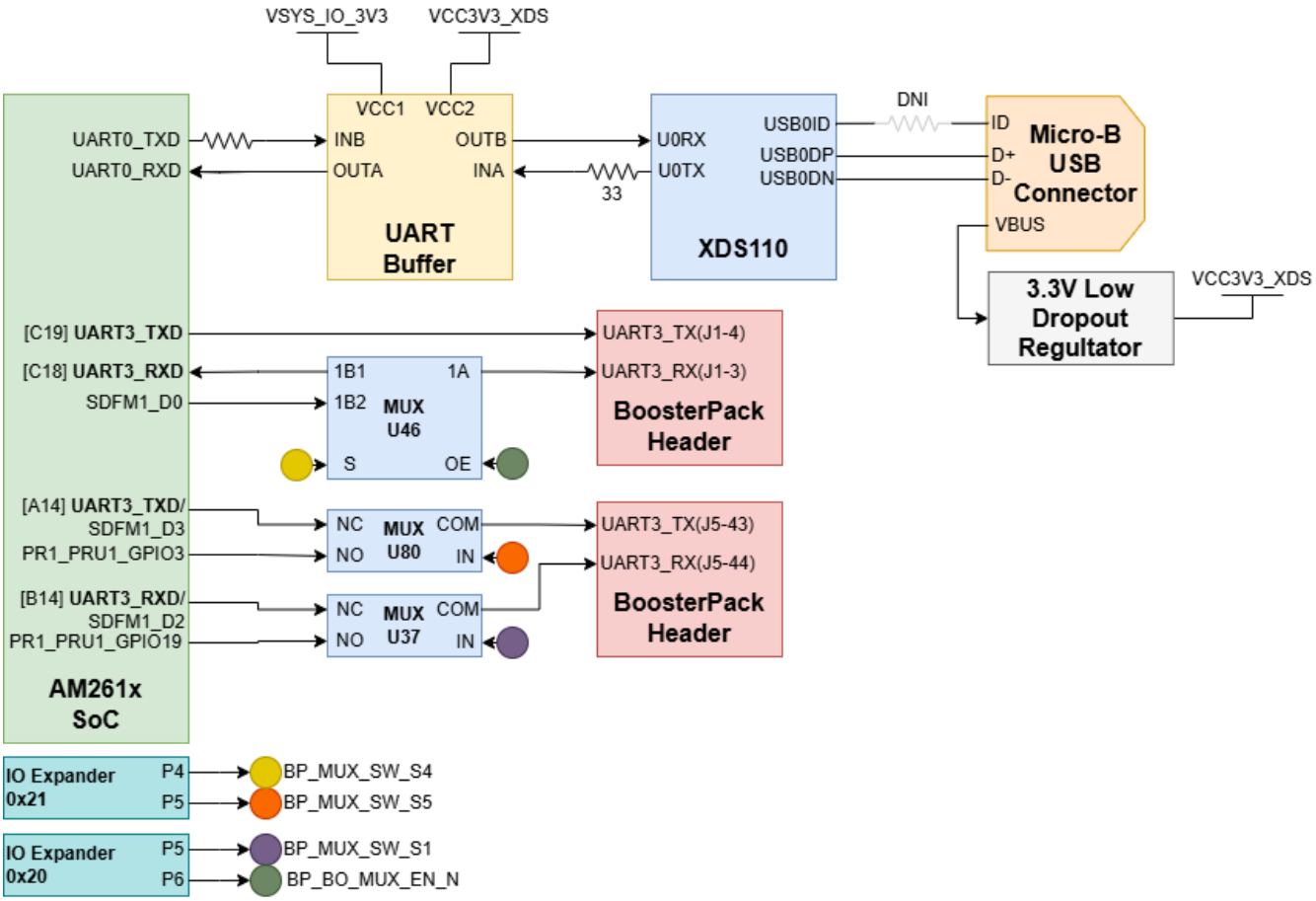


Figure 2-22. LP-AM261 UART Interface

2.10.6 MCAN

The AM261x LaunchPad is equipped with a single MCAN Transceiver (TCAN1044VDRBTQ1) that is connected to the MCAN0 interface of the AM261x MCU. The MCAN Transceiver has two power inputs: VIO is the transceiver 3.3V system level shifting supply voltage and VCC is the transceiver 5V supply voltage. The AM261x MCU CAN data transmit data input is mapped to TXD of the transceiver and the CAN receive data output of the transceiver is mapped to the MCAN RX signal of the MCU.

The system has a 120Ω split termination on the CANH and CANL signals to improve EMI performance. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

The low and high level CAN bus input output lines are terminated to a three pin screw-terminal header.

The standby control signal is an AM261x GPIO signal. The STB control input has a pullup resistor that is used to put the transceiver in low-power standby mode to prevent excessive system power. Below is a table that shows the operating modes of the MCAN transceiver based on the STB control input logic.

Table 2-31. MCAN Transceiver Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

MCAN0 and MCAN1 are routed to the BoosterPack Headers through a series of muxes. The following table details the mux select signals for routing MCAN1 signals to the BoosterPack Headers.

Table 2-32. U35 Mux Select

MCAN_MUX_SEL	Mux Output
0	MCAN0_RX/TX to BoosterPack Headers
1	MCAN0_RX/TX to MCAN Transceiver

Table 2-33. U31 Mux Select

BP_MUX_SW_S0	BP_MUX_SW_S1	Mux Output (3A)	Mux Output (2A)
0	**0**	**MCAN0_TX**	**MCAN1_RX**
0	1	SDFM0_D0	PR1_PRU0_GPIO9
1	0	SDFM0_D0	PR1_PRU0_GPIO9
1	**1**	**MCAN0_TX**	**MCAN1_RX**

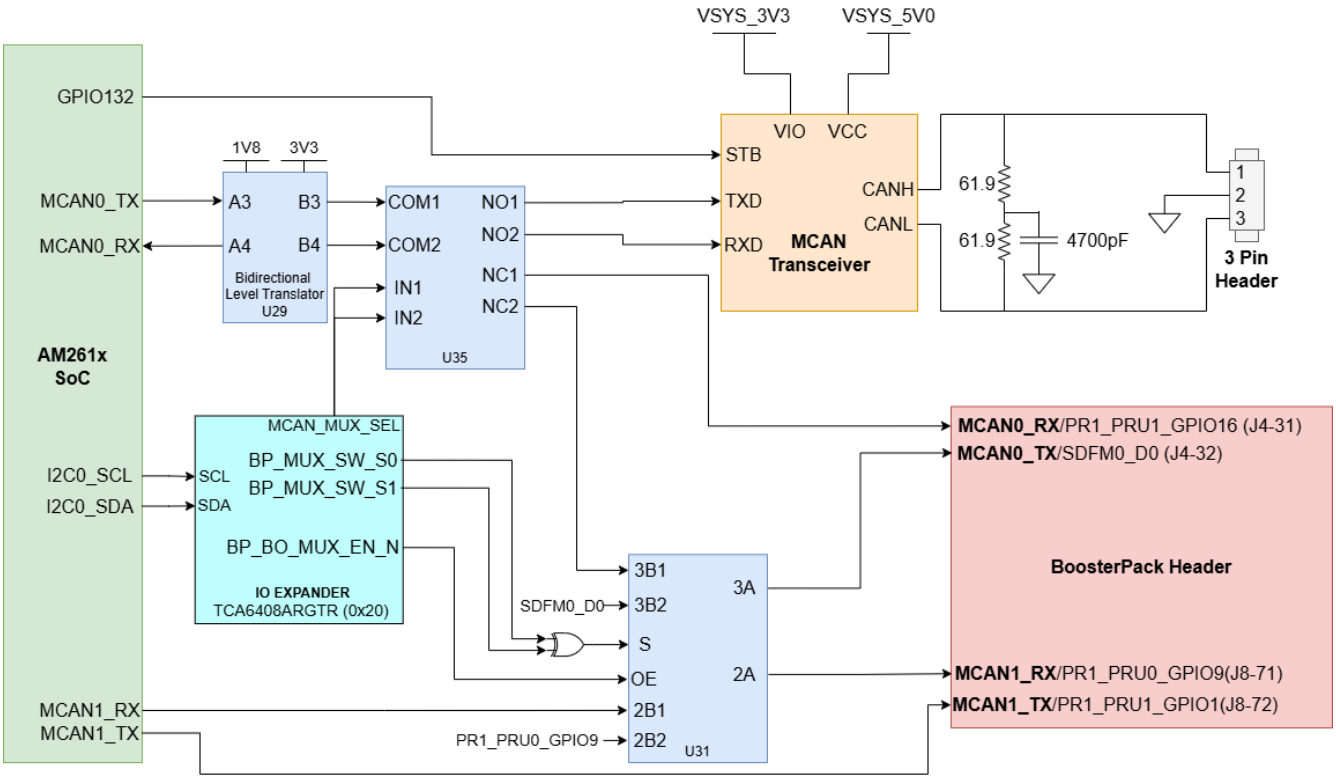


Figure 2-23. LP-AM261 MCAN Interface

2.10.7 SDFM

Two instances of the Sigma-Delta Filter Module (SDFM) peripheral are routed out from the AM261x MCU to the BoosterPack headers. There are a series of multiplexers along the SDFM signal paths in order to enable multiple BoosterPack header modes. The mux logic and block diagram are shown below:

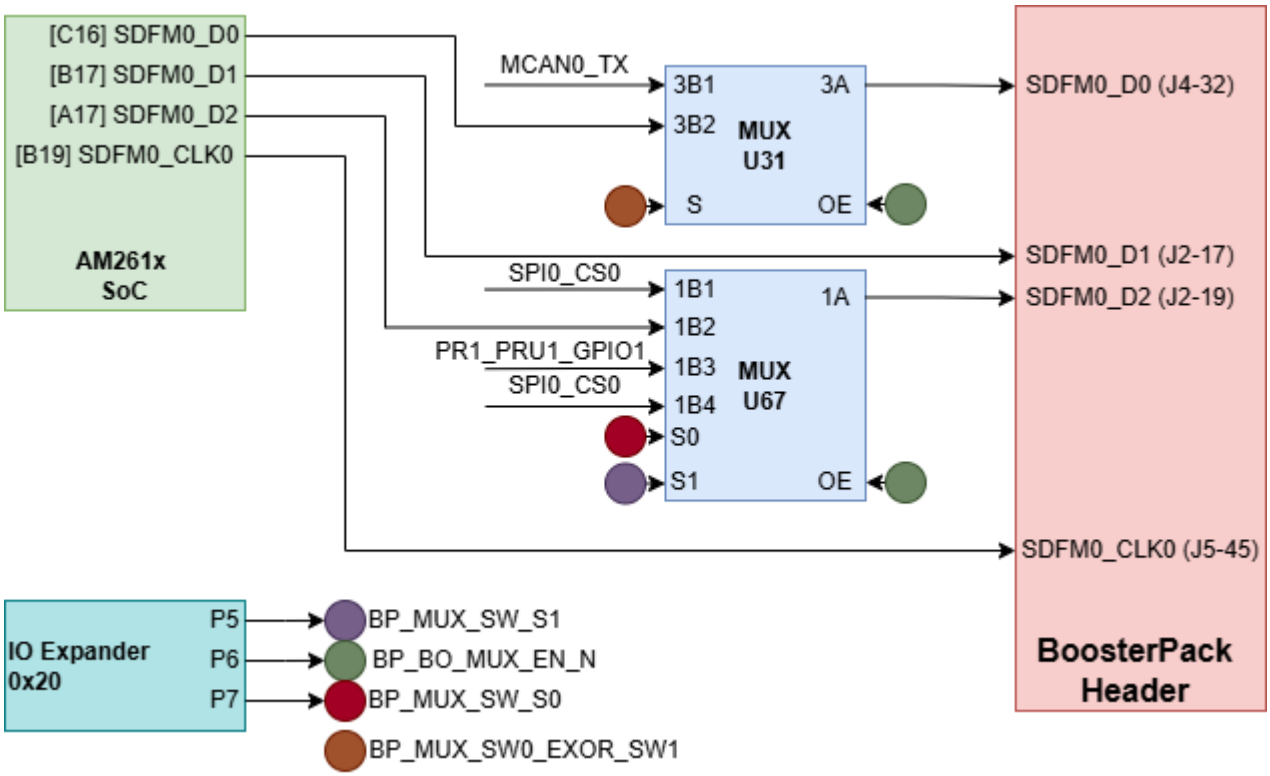


Figure 2-24. SDFM0

Note

BP_MUX_SW0_EXOR_SW1 is the output of a logical XOR between BP_MUX_SW_S0 and BP_MUX_SW_S1

Table 2-34. U31 Mux Select

BP_MUX_SW_S0	BP_MUX_SW_S1	BP_MUX_SW0_EXOR_SW1	Mux Output (3A)
0	0	0	MCAN0_TX
0	**1**	**1**	**SDFM0_D0**
1	**0**	**1**	**SDFM0_D0**
1	1	0	MCAN0_TX

Table 2-35. U67 Mux Select

BP_MUX_SW_S0	BP_MUX_SW_S1	Mux Output (1A)
0	0	SPI0_CS0
0	1	PR1_PRU1_GPIO1
1	**0**	**SDFM0_D2**
1	1	SPI0_CS0

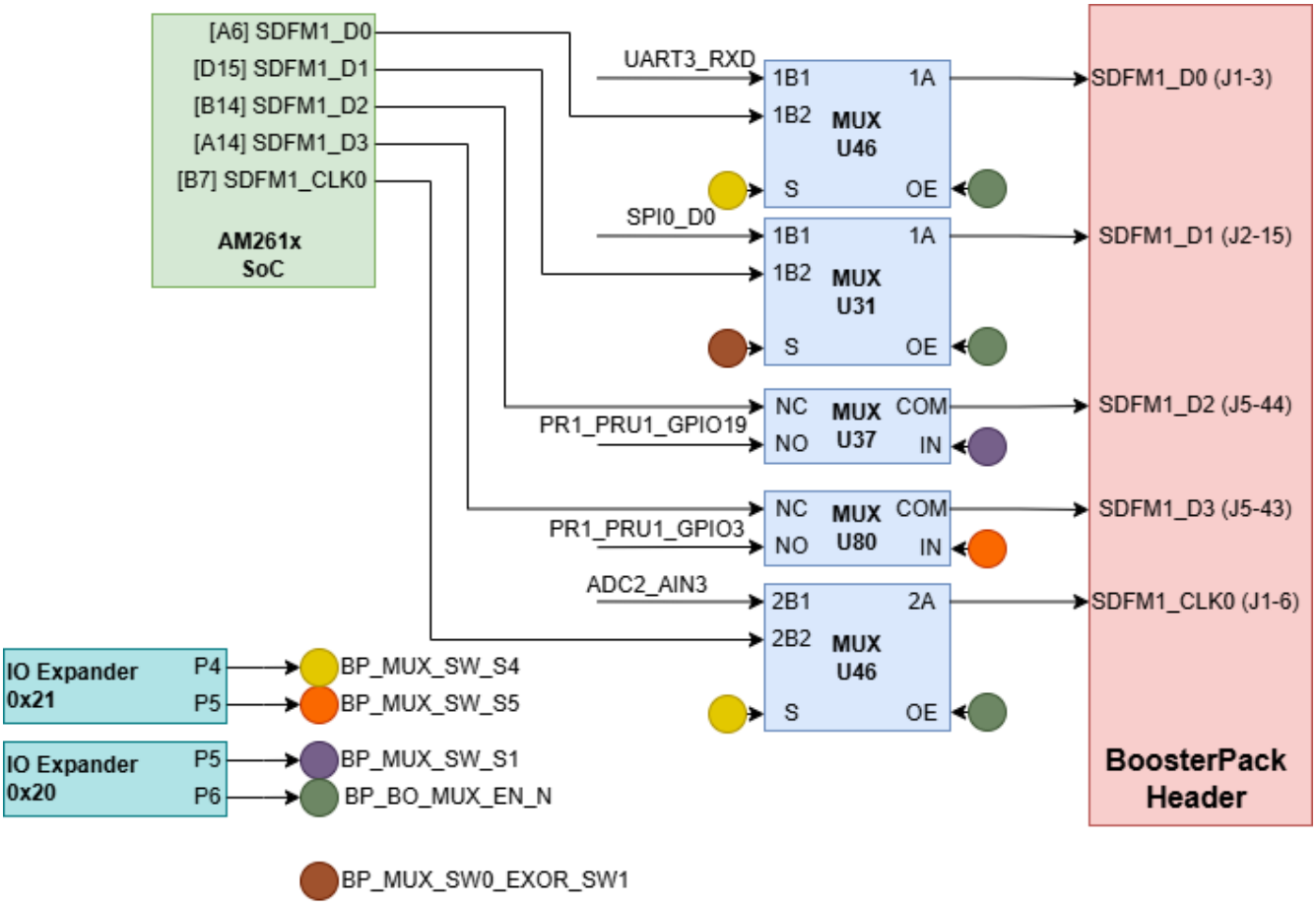


Figure 2-25. SDFM1

Table 2-36. U46 Mux Select

BP_MUX_SW_S4	Mux Output (1A)
0	UART3_RXD
1	**SDFM1_D0**

Table 2-37. U31 Mux Select

BP_MUX_SW_S0	BP_MUX_SW_S1	BP_MUX_SW0_EXOR_SW1	Mux Output (3A)
0	0	0	SPI0_D0
0	**1**	**1**	**SDFM1_D1**
1	**0**	**1**	**SDFM1_D1**
1	1	0	SPI0_D0

Table 2-38. U37 Mux Select

BP_MUX_SW_S1	Mux Output (COM)
0	**SDFM1_D2**
1	PR1_PRU1_GPIO19

Table 2-39. U80 Mux Select

BP_MUX_SW_S5	Mux Output (COM)
0	**SDFM1_D3**
1	PR1_PRU1_GPIO3

Table 2-40. U46 Mux Select

BP_MUX_SW_S4	Mux Output (2A)
0	ADC2_AIN3
1	**SDFM1_CLK0**

2.10.8 FSI

The AM261x LaunchPad supports a Fast Serial Interface peripheral by terminating the AM261x FSI RX and TX signals to a 10-pin header. The interface has two lines of data and a clock line for both the receive and transmit signals. The 10-pin header is connected to the 3.3V System voltage supply. The AM261x internal pinmux can be used to select between FSI signals and other functionality of the associated pins. A 2:1 mux selects between FSI and OSPI1 signals, and routes to the appriopriate hardware on the PCB.

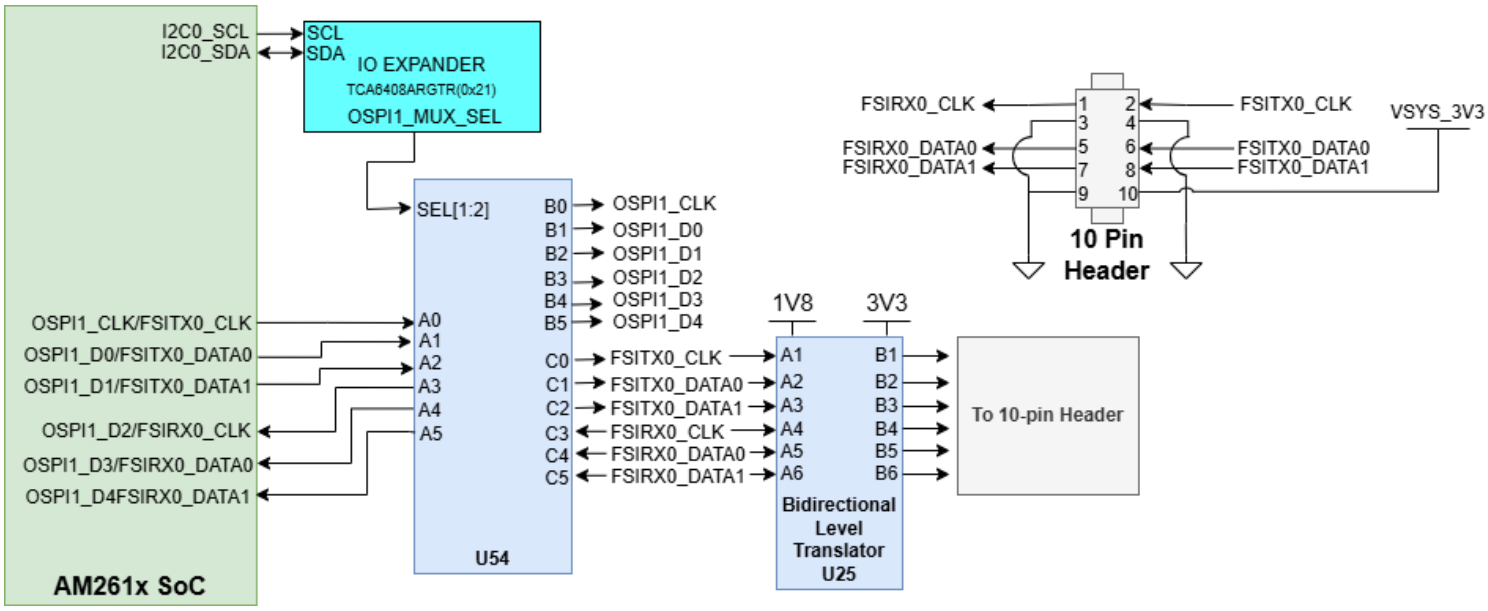


Figure 2-26. LP-AM261 FSI Interface

Table 2-41. U54 Mux Select

OSPI1_MUX_SEL	Output
0	OSPI1 Signals
1	FSI Signals

2.10.9 JTAG

The AM261x LaunchPad includes an XDS110 class on-board emulator. The LaunchPad includes all circuitry needed for XDS110 emulation. The emulator uses a USB 2.0 Micro-B connector to interface the USB 2.0 signals that are generated from the UART-USB bridge. The VBUS power from the connector is used to power the emulator circuit so that the connection to the emulator is not lost when power to the LaunchPad is removed.

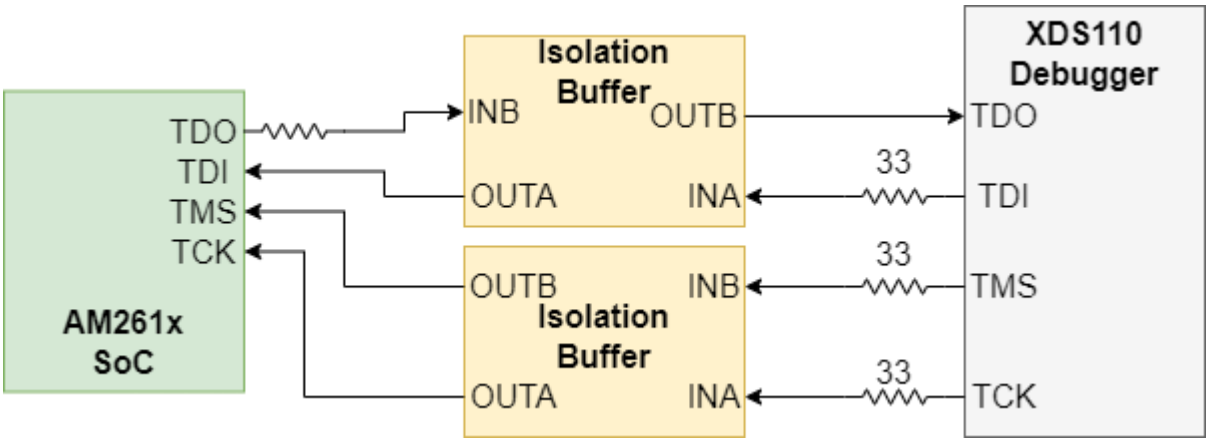


Figure 2-27. JTAG Interface to XDS110

2.10.10 Test Automation Pin Mapping

The following table details the Test Automation GPIO mapping.

Table 2-42. Test Automation GPIO and I2C Mapping

Signal Name	Description	Direction
TA_POWERDOWNZ	When logic low, disables the 5V Supply	Output
TA_PORZ	When logic low, connects the PORz signal to ground due to PMOS V_{GS} being less than zero creating a power on reset to the MAIN domain	Output
TA_RESETZ	When logic low, connects the WARM RESETn signal to ground due to PMOS V_{GS} being less than zero creating a warm reset to the MAIN domain	Output
TA_GPIO1	When logic low, connects the INTn signal to ground due to PMOS V_{GS} being less than zero creating an interrupt to SoC	Output
TA_GPIO3	When logic low, disables the boot mode buffer output enable	Output
TA_GPIO4	Reset signal for boot mode IO Expander	Output
TA_I2C_SCL	I2C Clock signal used to communicate with bootmode IO expander to change the boot modes.	Output
TA_I2C_SDA	I2C Data signal used to communicate with bootmode IO expander to change the boot modes.	Output

2.10.11 LIN

The AM261x LaunchPad supports Local Interconnect Network communication with two LIN instances mapped to the BoosterPack header.

Note

The AM261x does **not** have an onboard LIN Transceiver

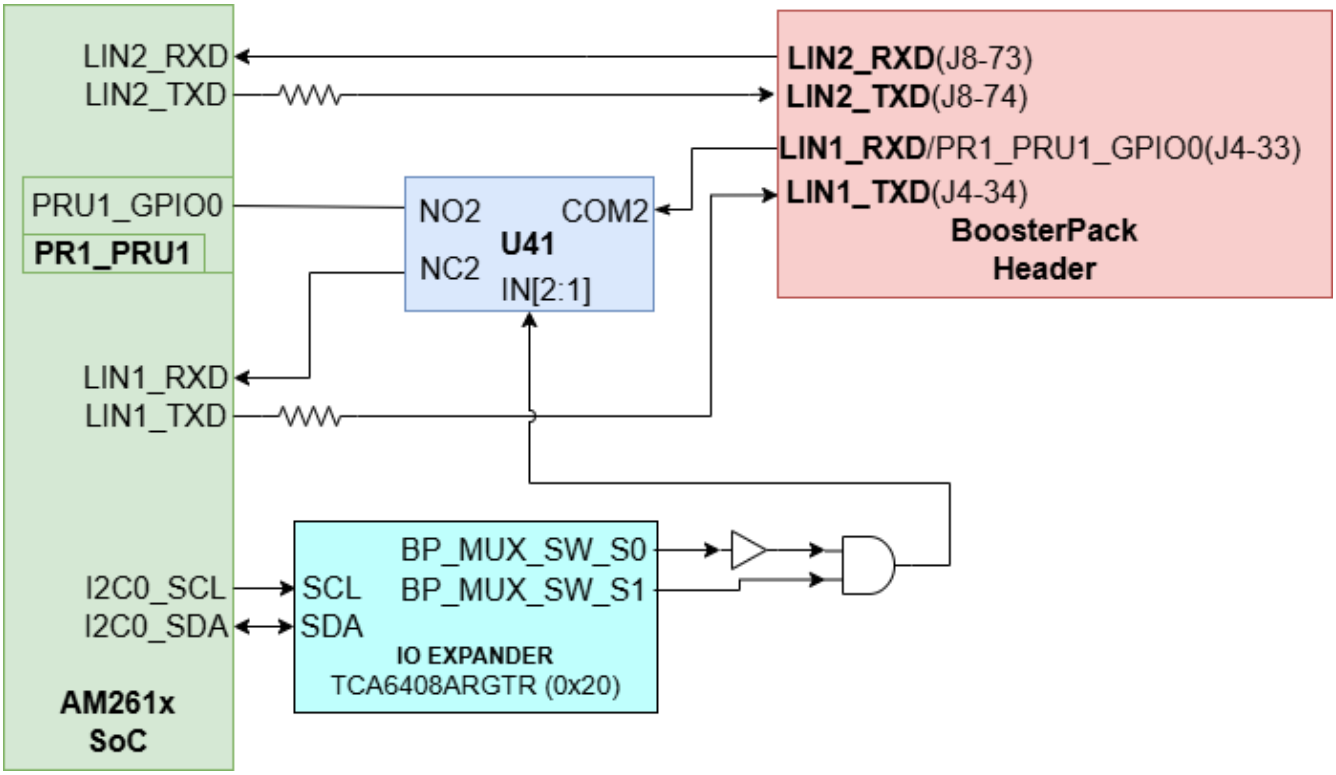


Figure 2-28. LIN Instances to BoosterPack Header

LIN2_TXD, LIN2_RXD and LIN1_TXD signals are directly routed to BoosterPack connectors. LIN1_RXD is routed through a mux. The mux selection table is shown below.

Table 2-43. U41 Mux Select

BP_MUX_SW_S0	BP_MUX_SW_S1	Mux Output (COM2)
0	**0**	**LIN1_RXD**
0	1	PR1_PRU1_GPIO0
1	**0**	**LIN1_RXD**
1	**1**	**LIN1_RXD**

2.10.12 ADC and DAC

The AM261x LaunchPad maps 20 ADC inputs to the BoosterPack header. All of the ADC inputs that are used in the LaunchPad are ESD protected.

There are several muxes that determine the path of the ADC input signals depending on the BoosterPack mode selected. shows the mux select signal logic used in the BoosterPack mode muxes.

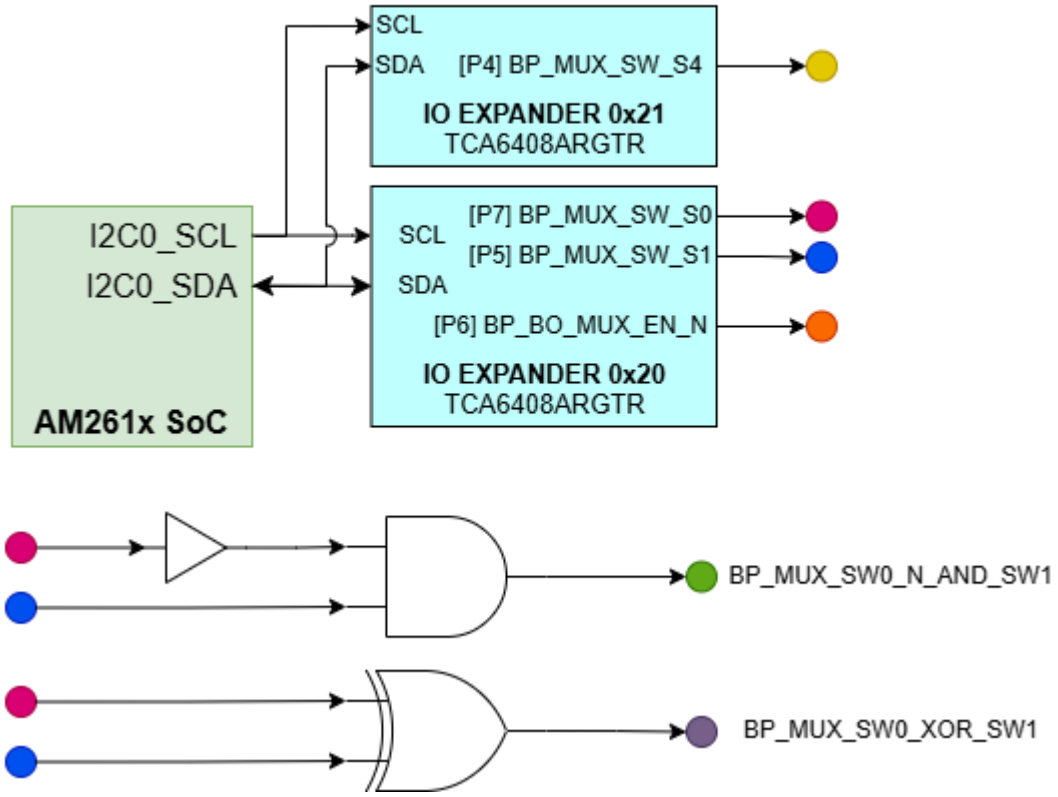


Figure 2-29. BoosterPack Mode Mux Select Logic

Table 2-44. Mux Select Logic Outputs

BP_MUX_SW_S0	BP_MUX_SW_S1	BP_MUX_SW0_N_AND_SW1	BP_MUX_SW0_XOR_SW1
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

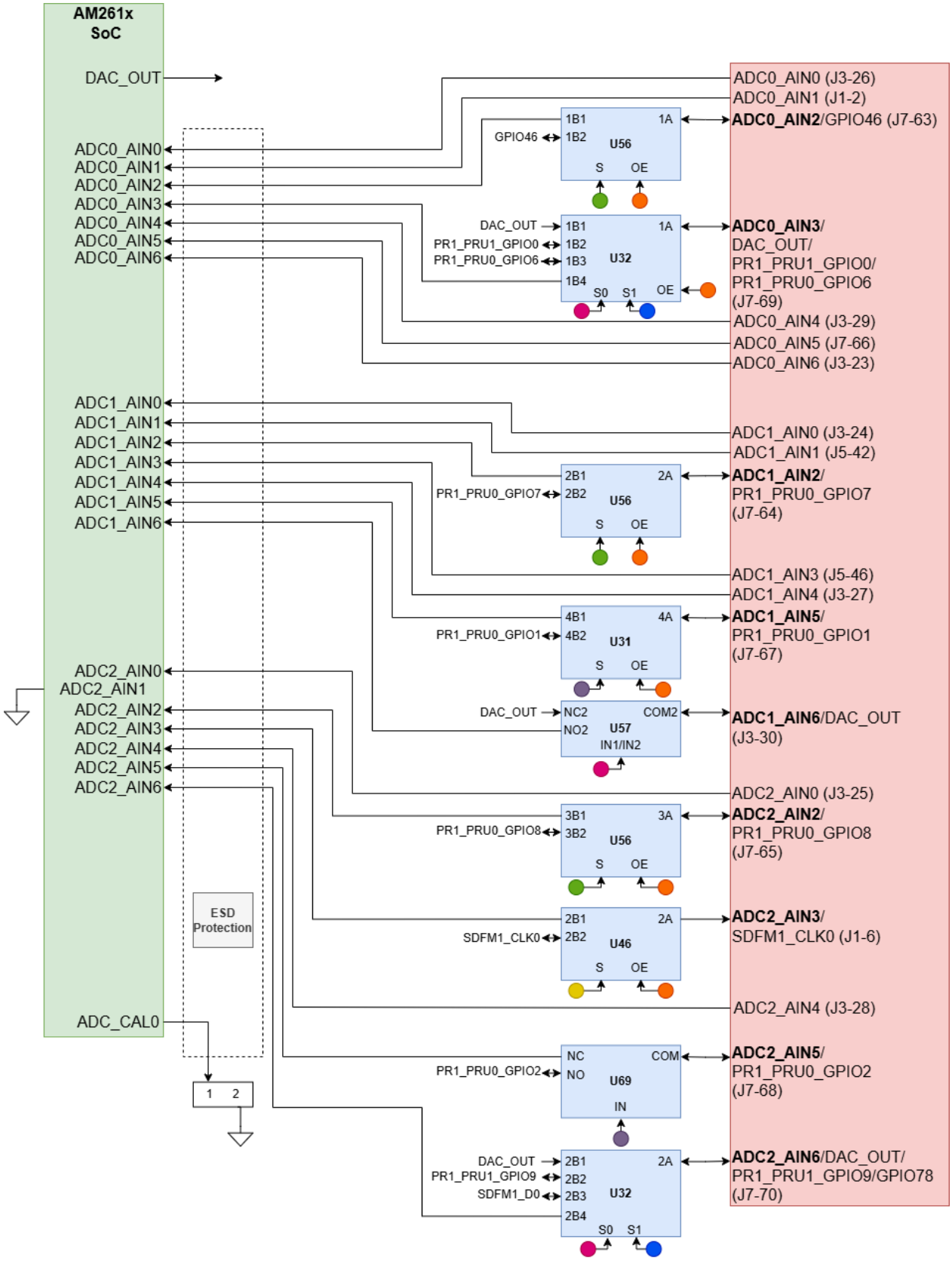


Figure 2-30. ADC/DAC Interface

The ADC and DAC require a voltage reference. The AM261x LaunchPad has two switches that allow the user to select the ADC and DAC voltage reference.

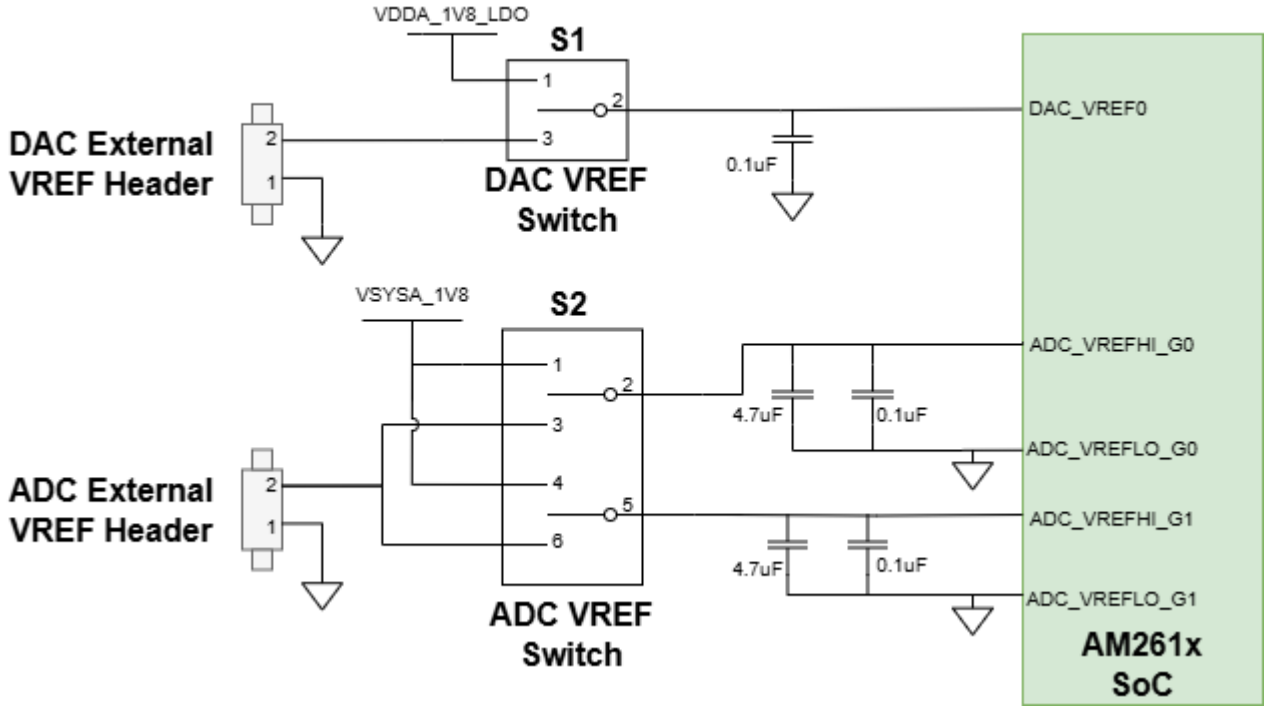


Figure 2-31. ADC and DAC VREF Switches

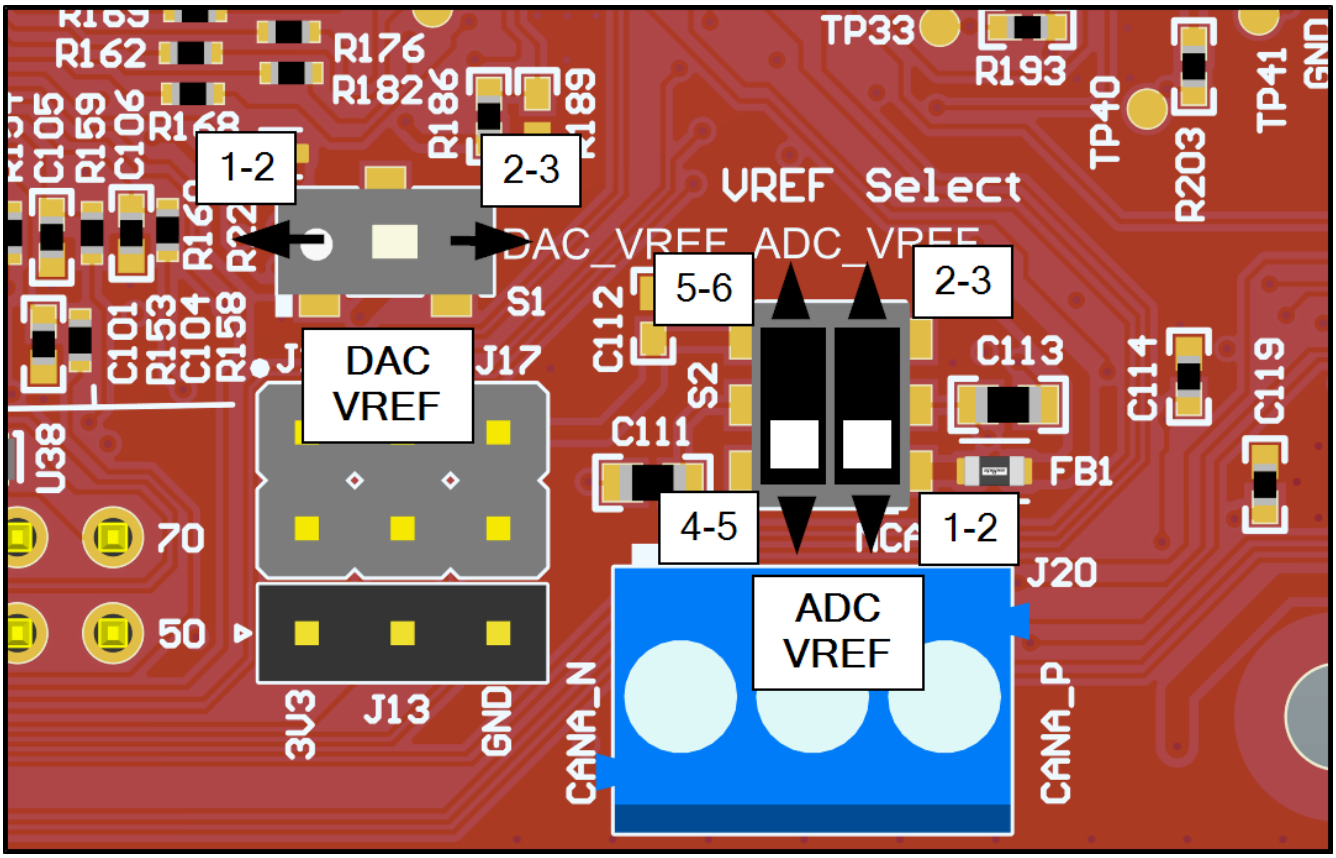


Figure 2-32. LP-AM261 ADC/DAC VREF Switches

The DAC VREF Switch (S1) is a single pole double throw switch that controls the input of the ADC VREF inputs of the AM261x SoC.

Note

The DAC VREF switch must be in the **Pin 1-2** position for SDK examples to function properly.

Table 2-45. DAC VREF Switch

DAC VREF Switch Position	Reference Selection
Pin 1-2 (LEFT)	AM261x on-die LDO
Pin 2-3 (RIGHT)	External DAC VREF Header

The ADC VREF Switch (S2) contains two single pole double throw switches that controls the input of the ADC VREF inputs of the AM261x SoC.

Note

The ADC VREF switches must be in position **1-2** and **4-5** for SDK examples to function properly.

Table 2-46. ADC VREF Switch

ADC VREF Switch Position	Reference Selection
Pin 1-2 (DOWN)	On-board PMIC 1.8V output
Pin 2-3 (UP)	External ADC VREF Header
Pin 4-5 (DOWN)	On-board PMIC 1.8V output
Pin 5-6 (UP)	External ADC VREF Header

2.10.13 EQEP

The AM261x LaunchPad internally muxes the eQEP, FSI and OSPI1 signals. The eQEP0 instance of the AM261x is terminated to two headers (J19, J16). The eQEP1 instance of the AM261x is terminated to two headers (J18, J15).

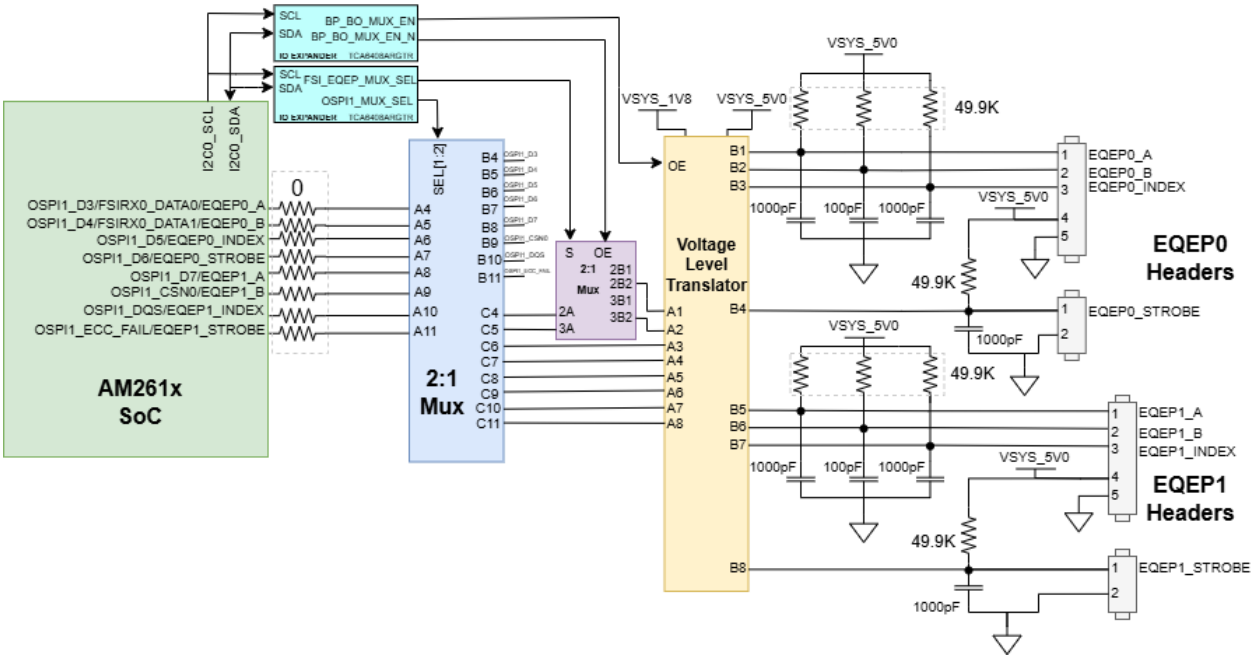


Figure 2-33. EQEP Signal Mapping

All eQEP signals have series termination resistors between the AM261x SoC and the Voltage Level Translator (TXB0108RGYR). The voltage level shifter is responsible for translating the 1.8V to 5V.

2.10.14 EPWM

The AM261x LaunchPad maps 12 PWM channels (6 PWM_A/B pairs) to the BoosterPack Header. Each EPWM signal has a series termination resistor. For the mapping of each EPWM signal refer to Section 2.11.

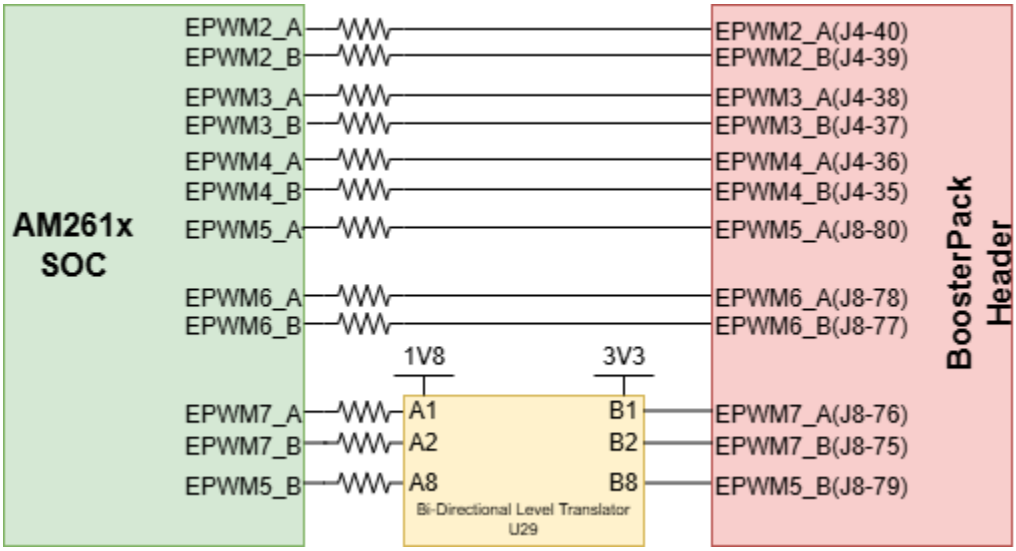


Figure 2-34. EPWM Signal Mapping to BoosterPack Header

2.10.15 USB

The LP-AM261 has one USB2.0 interface connected to the USB0 peripheral on the AM261x MCU.

AM261x supports USB DFU Bootmode. Boot mode selection and details are given in Bootmode

On the LaunchPad, the USB0_DM and USB0_DP nets are routed through a 2:1 mux to either the Micro-USB receptacle (J10) or the USB Type-C connector (J25). Each USB interface signal is then routed to a common mode choke to reduce noise on the high-speed USB signal bus. The nets are passed through a TPD4E02B04 ESD protection diode, and are terminated at their respective connectors. Figure 2-35 details the USB implementation on LP-AM261.

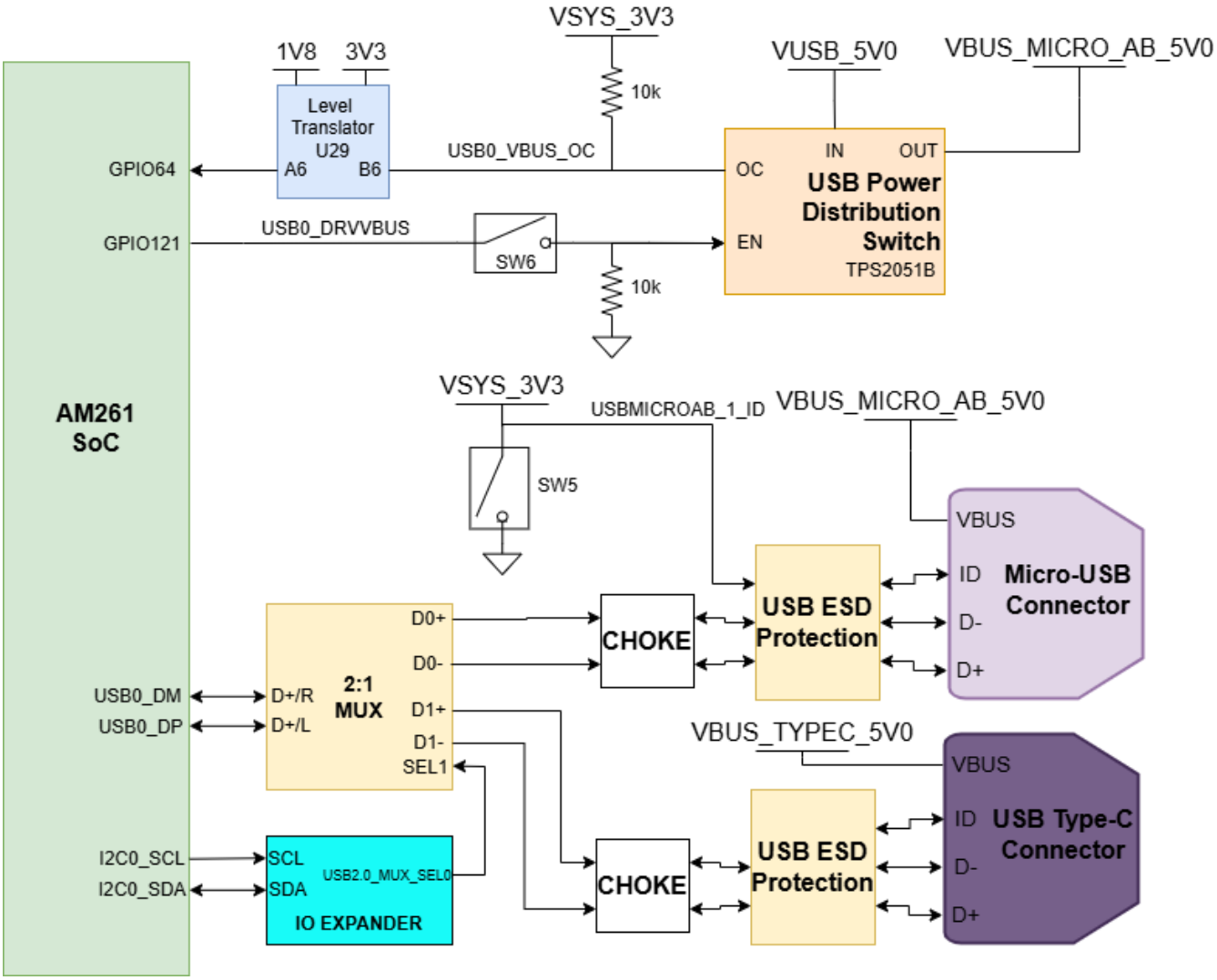


Figure 2-35. LP-AM261 USB Interface

Micro-USB Interface

The USB0 interface routing to the Micro-USB Connector (J10) is the default mux selection on the LP-AM261. The USB mode of operation using the Micro-USB interface is controlled using a set of DIP switches - SW5 and SW6. The USB mode switch settings are detailed below:

Table 2-47. Micro-USB Interface USB Mode Switch Settings

SW6 (USB0_DRVVBUS)	SW5 (USBMICROAB_ID)	USB Mode
OFF / RIGHT	OFF / LEFT	Device Mode
ON / LEFT	ON / RIGHT	Host Mode

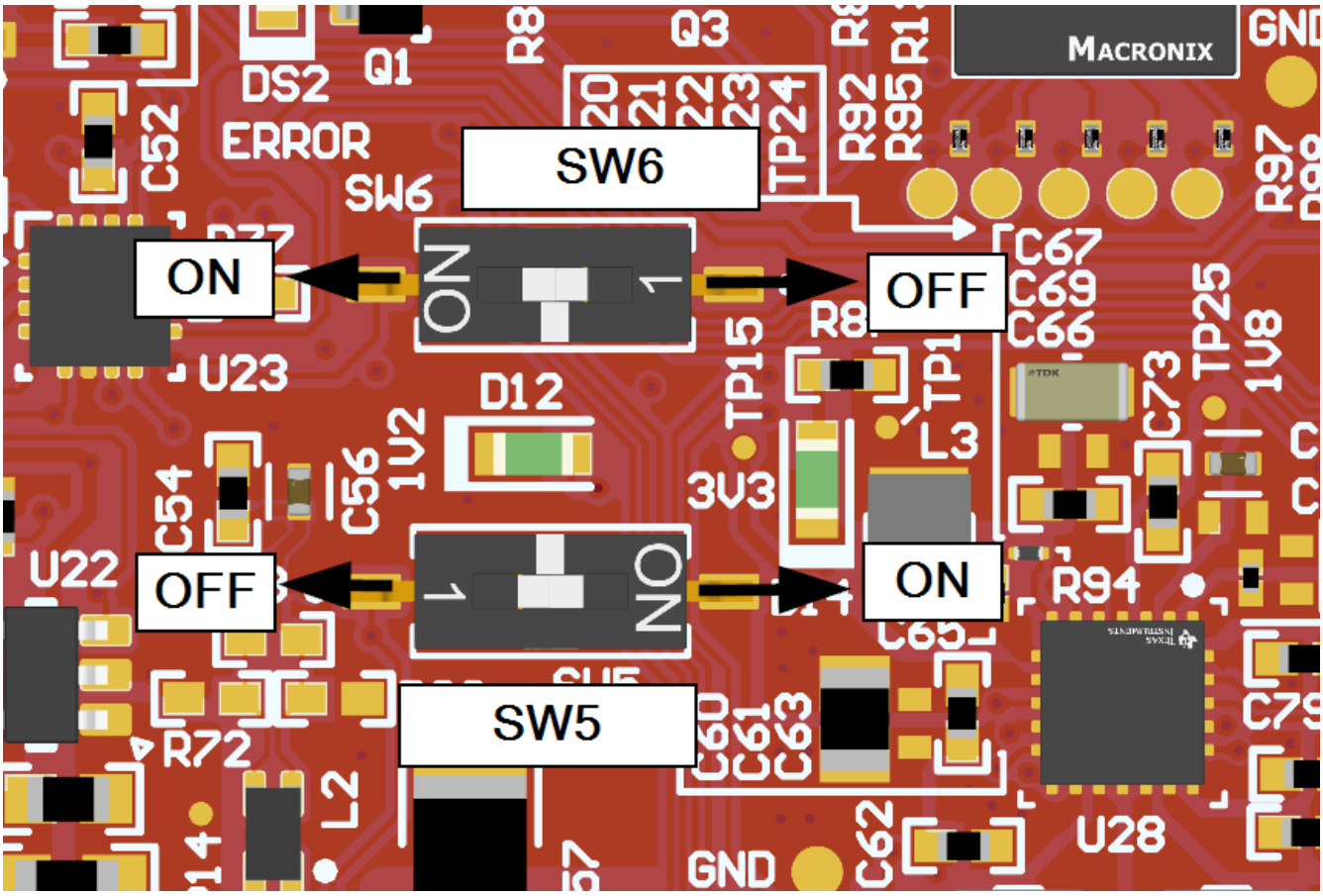


Figure 2-36. USB Mode Switches

USB Device Mode

When using the AM261x device in USB device mode, the VBUS pin of the Micro-USB receptacle is used to detect when voltage has been applied to or removed from the USB connector. Software running on the AM261x manages the internal USB PHY according to the presence of 5V or 0V on the VBUS pin.

USB Host Mode

When using the AM261x device in USB Host mode, 5V on the VBUS pin of the Micro-USB receptacle is required. On the LP-AM261, this supply is generated using a TPS2051B USB Power Distribution switch which sources the main 5V system input and supplies a separate 5V input for the USB bus. As shown in Table 2-47 above, SW6 must be set to ON to enable the TPS2051B USB Power Distribution switch, and SW5 must be ON to indicate that the device is set to USB Host mode. SW6 controls the state of the USB0_DRVVBUS net, which is connected to a dedicated USB0_DRVVBUS pin on the AM261x MCU and drives the enable pin on the TPS2051B. The OC pin of the TPS2051B is an active low, open-drain output that occurs when an overcurrent or overtemperature shutdown condition is detected. The USB0_VBUS_OC net is connected to GPIO64 on the AM261x MCU.

2.11 BoosterPack Headers

Note

This BoosterPack pinout only applies to Revision A of the LP-AM261.

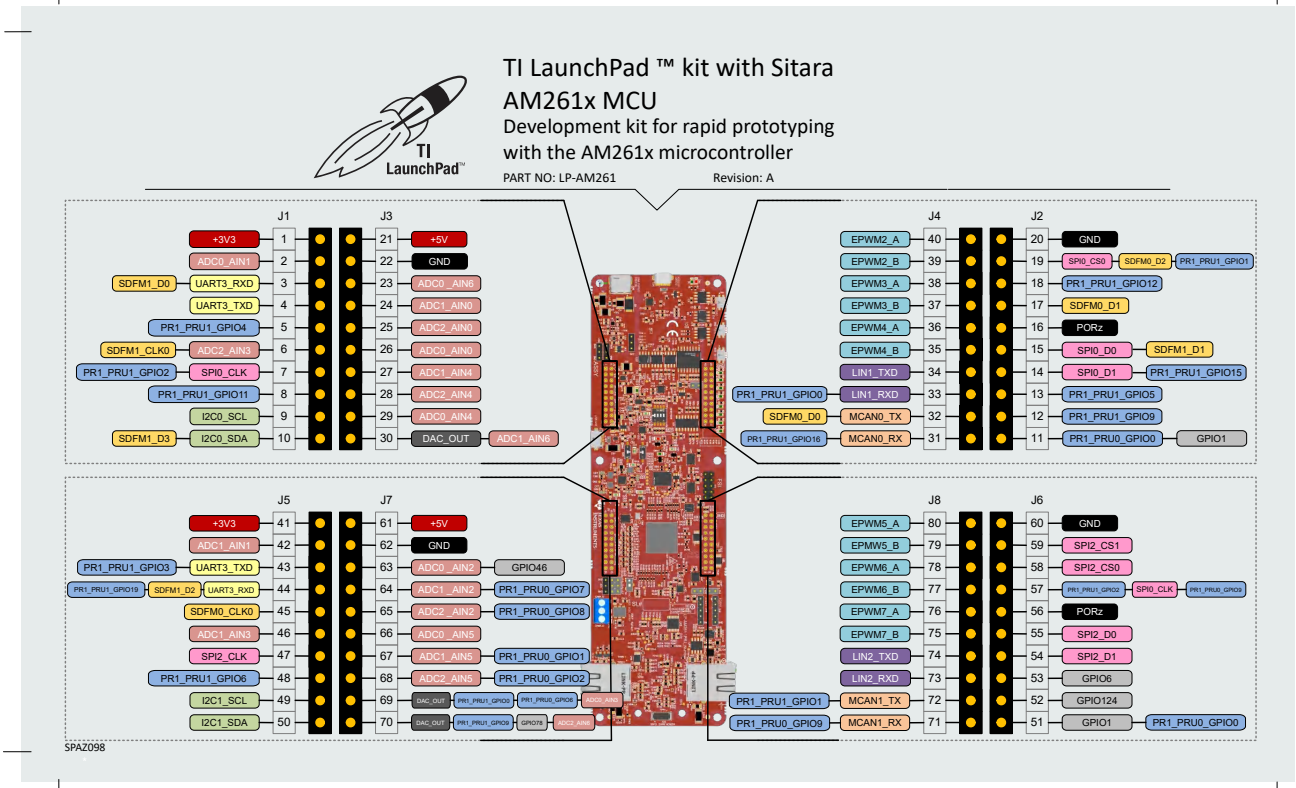


Figure 2-37. AM261x LaunchPad BoosterPack Pinout

Note

This pinout represents the default signals mapped to the BoosterPack Header. Additional signal options for each header are available and detailed in Section 2.12.

The AM261x LaunchPad supports two fully independent BoosterPack XL connectors. BoosterPack site #1 (J1/J3, J2/J4) is located in between the OSPI0 Flash and the micro-B USB Connector. BoosterPack site #2 (J5/J7, J6/J8) is located in between the OSPI0 Flash and the Ethernet add-on board connectors. Each GPIO has multiple functions available through the GPIO mux. The signals connected from the SoC to the BoosterPack headers include:

- Various ADC inputs
- DAC outputs
- UART0 and UART3
- Various GPIO signals
- SPI0 and SPI2
- I2C0 and I2C1
- Various EPWM channels
- LIN1 and LIN2
- MCAN0 and MCAN1
- SDFM0 and SDFM1

BoosterPack Modes

The AM261x LaunchPad is intended to have full compatibility with four Booster Packs, each with differing pinouts.

- Standard LaunchPad Booster Pack as per https://www.ti.com/lit/ml/slat157/slat157.pdf
- Servo Motor Control Booster Packs, such as BOOSTXL-LMG2100-MD and BP-AMC0106-LMG-MD
- BOOSTXL-IOLINKM-8
- Standard C2000 DRVx Booster Packs

The LP-AM261 uses the AM261x MCU pinmux and on-board signal muxes to enable the selection and routing of different AM261x nets to be brought out on the BoosterPack Headers depending on the intended BoosterPack mode.

The modes of the BoosterPack are controlled using select lines with nets BP_MUX_SW_S1 and BP_MUX_SW_S0 as per the schematic. The BoosterPack modes correspond with the following select line combinations:

Table 2-48. LP-AM261 BoosterPack Modes

BP_MUX_SW_S1	BP_MUX_SW_S0	BoosterPack Mode
0	0	Standard LaunchPad/BoosterPack
0	1	Servo Motor Control BoosterPacks
1	0	IO-LINK
1	1	C2000 DRVx BoosterPacks

- BP_MUX_SW_S0 is controlled using the I2C-controlled IO Expander U23 (address 0x20) and is connected to output P7.
- BP_MUX_SW_S1 is controlled using the I2C-controlled IO Expander U23 (address 0x20) and is connected to output P5.

In the following pinout tables, a blank "Selected Net" cell indicates that the BoosterPack pin has no external muxing and the net indicated in the BoosterPack Net Name is always selected.

2.11.1 BoosterPack Mode 00: Standard LaunchPad/BoosterPack Pinout

Mode 00 enables the Standard LaunchPad/BoosterPack pinout. The connections and details are shown in the following tables:

Table 2-49. LP-AM261 BoosterPack Mode 00 Mux Settings

BoosterPack Mux Select Net	State
BP_MUX_SW_S0	0
BP_MUX_SW_S1	0

Table 2-50. Mode 00 : Standard LaunchPad BoosterPack (J1/J3)

Selected net	BoosterPack Net Name	J1	J3	BoosterPack Net Name	Selected net
	VSYS_3V3_BP	1	21	VSYS_5V0_BP_1	
	ADC0_AIN1	2	22	GND	
UART3_RXD	UART3_RXD / SDFM1_D0	3	23	ADC0_AIN6	
	UART3_TXD	4	24	ADC1_AIN0	
	PR1_PRU1_GPIO4	5	25	ADC2_AIN0	
ADC2_AIN3	ADC2_AIN3 / SDFM1_CLK0	6	26	ADC0_AIN0	
SPI0_CLK	SPI0_CLK/PR1_PRU1_GPIO2	7	27	ADC1_AIN4	
	PR1_PRU1_GPIO11	8	28	ADC2_AIN4	
	I2C0_SCL	9	29	ADC0_AIN4	

Table 2-50. Mode 00 : Standard LaunchPad BoosterPack (J1/J3) (continued)

Selected net	BoosterPack Net Name	J1	J3	BoosterPack Net Name	Selected net
	I2C0_SDA	10	30	DAC_OUT / ADC1_AIN6	DAC_OUT

Table 2-51. Mode 00 : Standard LaunchPad BoosterPack (J2/J4)

Selected net	BoosterPack Net Name	J4	J2	BoosterPack Net Name	Selected net
	EPWM2_A	40	20	GND	
	EPWM2_B	39	19	SPI0_CS0 / SDFM0_D2 / PR1_PRU1_GPIO1	SPI0_CS0
	EPWM3_A	38	18	PR1_PRU1_GPIO12	
	EPWM3_B	37	17	SDFM0_D1	
	EPWM4_A	36	16	PORz	
	EPWM4_B	35	15	SPI0_D0 / SDFM1_D1	SPI0_D0
	LIN1_TXD	34	14	SPI0_D1 / PR1_PRU1_GPIO15	SPI0_D1
LIN1_RXD	LIN1_RXD / PR1_PRU1_GPIO0	33	13	PR1_PRU1_GPIO5	
MCAN0_TX	MCAN0_TX / SDFM0_D0	32	12	PR1_PRU1_GPIO9	
MCAN0_RX	MCAN0_RX / PR1_PRU1_GPIO16	31	11	PR1_PRU0_GPIO0/GPIO1	PR1_PRU0_GPIO0

Table 2-52. Mode 00 : Standard LaunchPad BoosterPack (J5/J7)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
	VSYS_3V3_BP	41	61	VSYS_5V0_BP_2	
	ADC1_AIN1	42	62	GND	GND
UART3_TXD	UART3_TXD / PR1_PRU1_GPIO3	43	63	ADC0_AIN2 / GPIO46	ADC0_AIN2
UART3_RXD	UART3_RXD / SDFM1_D2 / PR1_PRU1_GPIO19	44	64	ADC1_AIN2 / PR1_PRU0_GPIO7	ADC1_AIN2
	SDFM0_CLK0	45	65	ADC2_AIN2 / PR1_PRU0_GPIO8	ADC2_AIN2
	ADC1_AIN3	46	66	ADC0_AIN5	
	SPI2_CLK	47	67	ADC1_AIN5 / PR1_PRU0_GPIO1	ADC1_AIN5
	PR1_PRU1_GPIO6	48	68	ADC2_AIN5 / PR1_PRU0_GPIO2	ADC2_AIN5
	I2C1_SCL	49	69	DAC_OUT / PR1_PRU1_GPIO0 / PR1_PRU0_GPIO6 / ADC0_AIN3	DAC_OUT
	I2C1_SDA	50	70	DAC_OUT / PR1_PRU1_GPIO9 / GPIO78 / ADC2_AIN6	DAC_OUT

Table 2-53. Mode 00 : Standard LaunchPad BoosterPack (J6/J8)

Selected net	BoosterPack Net Name	J8	J6	BoosterPack Net Name	Selected net
	EPWM5_A	80	60	GND	
	EPWM5_B	79	59	SPI2_CS1	
	EPWM6_A	78	58	SPI2_CS0	
	EPWM6_B	77	57	PR1_PRU1_GPIO2 / SPI0_CLK / PR1_PRU0_GPIO9	PR1_PRU1_GPIO2
	EPWM7_A	76	56	PORz	
	EPWM7_B	75	55	SPI2_D0	
	LIN2_TXD	74	54	SPI2_D1	

Table 2-53. Mode 00 : Standard LaunchPad BoosterPack (J6/J8) (continued)

Selected net	BoosterPack Net Name	J8	J6	BoosterPack Net Name	Selected net
	LIN2_RXD	73	53	GPIO6	
MCAN1_TX	MCAN1_TX / PR1_PRU1_GPIO1	72	52	GPIO124	
MCAN1_RX	MCAN1_RX / PR1_PRU0_GPIO9	71	51	GPIO1/PR1_PRU0_GPIO0	GPIO1

2.11.2 BoosterPack Mode 01: Servo Motor Control BoosterPacks Mode

Mode 01 enables Servo Motor Control BoosterPack Connections. The connections and details are shown in the following tables:

Note

Additional modifications are required for use with the BP-AMC0106-LMG-MD. See Section 6.3.2 for details.

Table 2-54. LP-AM261 BoosterPack Mode 01 Mux Settings

BoosterPack Mux Select Net	State
BP_MUX_SW_S0	1
BP_MUX_SW_S1	0

Table 2-55. Mode 01: Servo Motor Control BoosterPack (J1/J3)

Selected net	BoosterPack Net Name	J1	J3	BoosterPack Net Name	Selected net
	VSYS_3V3_BP	1	21	VSYS_5V0_BP_1	
	ADC0_AIN1	2	22	GND	
SDFM1_D0	UART3_RXD / SDFM1_D0	3	23	ADC0_AIN6	
	UART3_TXD	4	24	ADC1_AIN0	
	PR1_PRU1_GPIO4	5	25	ADC2_AIN0	
SDFM1_CLK0	ADC2_AIN3 / SDFM1_CLK0	6	26	ADC0_AIN0	
SPI0_CLK	SPI0_CLK/PR1_PRU1_GPIO2	7	27	ADC1_AIN4	
	PR1_PRU1_GPIO11	8	28	ADC2_AIN4	
	I2C0_SCL	9	29	ADC0_AIN4	
	I2C0_SDA	10	30	DAC_OUT / ADC1_AIN6	ADC1_AIN6

Table 2-56. Mode 01: Servo Motor Control BoosterPack (J2/J4)

Selected net	BoosterPack Net Name	J4	J2	BoosterPack Net Name	Selected net
	EPWM2_A	40	20	GND	
	EPWM2_B	39	19	SPI0_CS0 / SDFM0_D2 / PR1_PRU1_GPIO1	SDFM0_D2
	EPWM3_A	38	18	PR1_PRU1_GPIO12	
	EPWM3_B	37	17	SDFM0_D1	
	EPWM4_A	36	16	PORz	
	EPWM4_B	35	15	SPI0_D0 / SDFM1_D1	SDFM1_D1
	LIN1_TXD	34	14	SPI0_D1 / PR1_PRU1_GPIO15	SPI0_D1
LIN1_RXD	LIN1_RXD / PR1_PRU1_GPIO0	33	13	PR1_PRU1_GPIO5	
SDFM0_D0	MCAN0_TX / SDFM0_D0	32	12	PR1_PRU1_GPIO9	

Table 2-56. Mode 01: Servo Motor Control BoosterPack (J2/J4) (continued)

Selected net	BoosterPack Net Name	J4	J2	BoosterPack Net Name	Selected net
PR1_PRU1_GPIO16	MCAN0_RX / PR1_PRU1_GPIO16	31	11	PR1_PRU0_GPIO0/GPIO1	PR1_PRU0_GPIO0

Table 2-57. Mode 01: Servo Motor Control BoosterPack (J5/J7)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
	VSYS_3V3_BP	41	61	VSYS_5V0_BP_2	
	ADC1_AIN1	42	62	GND	
UART3_TXD	UART3_TXD / PR1_PRU1_GPIO3	43	63	ADC0_AIN2 / GPIO46	ADC0_AIN2
UART3_RXD	UART3_RXD / SDFM1_D2 / PR1_PRU1_GPIO19	44	64	ADC1_AIN2 / PR1_PRU0_GPIO7	ADC1_AIN2
	SDFM0_CLK0	45	65	ADC2_AIN2 / PR1_PRU0_GPIO8	ADC2_AIN2
	ADC1_AIN3	46	66	ADC0_AIN5	
	SPI2_CLK	47	67	ADC1_AIN5 / PR1_PRU0_GPIO1	PR1_PRU0_GPIO1
	PR1_PRU1_GPIO6	48	68	ADC2_AIN5 / PR1_PRU0_GPIO2	PR1_PRU0_GPIO2
	I2C1_SCL	49	69	DAC_OUT / PR1_PRU1_GPIO0 / PR1_PRU0_GPIO6 / ADC0_AIN3	PR1_PRU1_GPIO0
	I2C1_SDA	50	70	DAC_OUT / PR1_PRU1_GPIO9 / GPIO78 / ADC2_AIN6	PR1_PRU1_GPIO9

Table 2-58. Mode 01: Servo Motor Control BoosterPack (J6/J8)

Selected net	BoosterPack Net Name	J8	J6	BoosterPack Net Name	Selected net
	EPWM5_A	80	60	GND	
	EPWM5_B	79	59	SPI2_CS1	
	EPWM6_A	78	58	SPI2_CS0	
	EPWM6_B	77	57	PR1_PRU1_GPIO2 / SPI0_CLK / PR1_PRU0_GPIO9	PR1_PRU1_GPIO2
	EPWM7_A	76	56	PORz	
	EPWM7_B	75	55	SPI2_D0	
	LIN2_TXD	74	54	SPI2_D1	
	LIN2_RXD	73	53	GPIO6	
PR1_PRU1_GPIO1	MCAN1_TX / PR1_PRU1_GPIO1	72	52	GPIO5	
PR1_PRU0_GPIO9	MCAN1_RX / PR1_PRU0_GPIO9	71	51	GPIO1/PR1_PRU0_GPIO0	GPIO1

2.11.3 BoosterPack Mode 10: BOOSTXL-IOLINKM-8 Mode

Mode 10 enables BOOSTXL-IOLINKM-8 BoosterPack Connections. The connections and details are shown in the following tables:

Table 2-59. LP-AM261 BoosterPack Mode 10 Mux Settings

BoosterPack Mux Select Net	State
BP_MUX_SW_S0	0
BP_MUX_SW_S1	1

Table 2-60. Mode 10: BOOSTXL-IOLINKM-8 BoosterPack (J1/J3)

Selected net	BoosterPack Net Name	J1	J3	BoosterPack Net Name	Selected net
	VSYS_3V3_BP	1	21	VSYS_5V0_BP_1	
	ADC0_AIN1	2	22	GND	
UART3_RXD	UART3_RXD / SDFM1_D0	3	23	ADC0_AIN6	
	UART3_TXD	4	24	ADC1_AIN0	
	PR1_PRU1_GPIO4	5	25	ADC2_AIN0	
ADC2_AIN3	ADC2_AIN3 / SDFM1_CLK0	6	26	ADC0_AIN0	
PR1_PRU1_GPIO2	SPI0_CLK/PR1_PRU1_GPIO2	7	27	ADC1_AIN4	
	PR1_PRU1_GPIO11	8	28	ADC2_AIN4	
	I2C0_SCL	9	29	ADC0_AIN4	
	I2C0_SDA	10	30	DAC_OUT / ADC1_AIN6	DAC_OUT

Table 2-61. Mode 10: BOOSTXL-IOLINKM-8 BoosterPack (J2/J4)

Selected net	BoosterPack Net Name	J4	J2	BoosterPack Net Name	Selected net
	EPWM2_A	40	20	GND	
	EPWM2_B	39	19	SPI0_CS0 / SDFM0_D2 / PR1_PRU1_GPIO1	PR1_PRU1_GPIO1
	EPWM3_A	38	18	PR1_PRU1_GPIO12	
	EPWM3_B	37	17	SDFM0_D1	
	EPWM4_A	36	16	PORz	
	EPWM4_B	35	15	SPI0_D0 / SDFM1_D1	SDFM1_D1 → PR1_PRU1_GPIO7 via pinmux
	LIN1_TXD	34	14	SPI0_D1 / PR1_PRU1_GPIO15	PR1_PRU1_GPIO15
PR1_PRU1_GPIO0	LIN1_RXD / PR1_PRU1_GPIO0	33	13	PR1_PRU1_GPIO5	
SDFM0_D0 → PR1_PRU1_GPIO10 via pinmux	MCAN0_TX / SDFM0_D0	32	12	PR1_PRU1_GPIO9	
MCAN0_RX → PR1_PRU1_GPIO16 via pinmux	MCAN0_RX / PR1_PRU1_GPIO16	31	11	PR1_PRU0_GPIO0/GPIO1	PR1_PRU0_GPIO0

Table 2-62. Mode 10: BOOSTXL-IOLINKM-8 BoosterPack (J5/J7)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
	VSYS_3V3_BP	41	61	VSYS_5V0_BP_2	
	ADC1_AIN1	42	62	GND	GND
PR1_PRU1_GPIO3	UART3_TXD / PR1_PRU1_GPIO3	43	63	ADC0_AIN2 / GPIO46	GPIO46
PR1_PRU1_GPIO19	UART3_RXD / SDFM1_D2 / PR1_PRU1_GPIO19	44	64	ADC1_AIN2 / PR1_PRU0_GPIO7	PR1_PRU0_GPIO7
	SDFM0_CLK0	45	65	ADC2_AIN2 / PR1_PRU0_GPIO8	PR1_PRU0_GPIO8
	ADC1_AIN3	46	66	ADC0_AIN5	
	SPI2_CLK	47	67	ADC1_AIN5 / PR1_PRU0_GPIO1	PR1_PRU0_GPIO1
	PR1_PRU1_GPIO6	48	68	ADC2_AIN5 / PR1_PRU0_GPIO2	PR1_PRU0_GPIO2

Table 2-62. Mode 10: BOOSTXL-IOLINKM-8 BoosterPack (J5/J7) (continued)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
	I2C1_SCL	49	69	DAC_OUT / PR1_PRU1_GPIO0 / PR1_PRU0_GPIO6 / ADC0_AIN3	PR1_PRU0_GPIO6
	I2C1_SDA	50	70	DAC_OUT / PR1_PRU1_GPIO9 / GPIO78 / ADC2_AIN6	GPIO78

Table 2-63. Mode 10: BOOSTXL-IOLINKM-8 BoosterPack (J6/J8)

Selected net	BoosterPack Net Name	J8	J6	BoosterPack Net Name	Selected net
	EPWM5_A	80	60	GND	
	EPWM5_B	79	59	SPI2_CS1	
	EPWM6_A	78	58	SPI2_CS0	
	EPWM6_B	77	57	PR1_PRU1_GPIO2 / SPI0_CLK / PR1_PRU0_GPIO9	SPI0_CLK → GPIO12 via pinmux
	EPWM7_A	76	56	PORz	
	EPWM7_B	75	55	SPI2_D0	
	LIN2_TXD	74	54	SPI2_D1	
	LIN2_RXD	73	53	GPIO6	
MCAN1_TX	MCAN1_TX / PR1_PRU1_GPIO1	72	52	GPIO124	
PR1_PRU0_GPIO9	MCAN1_RX / PR1_PRU0_GPIO9	71	51	GPIO1/PR1_PRU0_GPIO0	GPIO1

2.11.4 BoosterPack Mode 11: C2000 DRVx BoosterPacks Mode

Mode 11 enables the signal routing for use with C2000™ DRVx BoosterPacks. The connections and details are shown in the following tables:

Table 2-64. LP-AM261 BoosterPack Mode 10 Mux Settings

BoosterPack Mux Select Net	State
BP_MUX_SW_S0	1
BP_MUX_SW_S1	1

Table 2-65. Mode 11: C2000 DRVx BoosterPacks (J1/J3)

Selected net	BoosterPack Net Name	J1	J3	BoosterPack Net Name	Selected net
	VSYS_3V3_BP	1	21	VSYS_5V0_BP_1	
	ADC0_AIN1	2	22	GND	
UART3_RXD	UART3_RXD / SDFM1_D0	3	23	ADC0_AIN6	
	UART3_TXD	4	24	ADC1_AIN0	
	PR1_PRU1_GPIO4	5	25	ADC2_AIN0	
ADC2_AIN3	ADC2_AIN3 / SDFM1_CLK0	6	26	ADC0_AIN0	
SPI0_CLK	SPI0_CLK/PR1_PRU1_GPIO2	7	27	ADC1_AIN4	
	PR1_PRU1_GPIO11	8	28	ADC2_AIN4	
	I2C0_SCL	9	29	ADC0_AIN4	
	I2C0_SDA	10	30	DAC_OUT / ADC1_AIN6	DAC_OUT

Table 2-66. Mode 11: C2000 DRVx BoosterPacks (J2/J4)

Selected net	BoosterPack Net Name	J4	J2	BoosterPack Net Name	Selected net
	EPWM2_A	40	20	GND	
	EPWM2_B	39	19	SPI0_CS0 / SDFM0_D2 / PR1_PRU1_GPIO1	SPI0_CS0
	EPWM3_A	38	18	PR1_PRU1_GPIO12	
	EPWM3_B	37	17	SDFM0_D1	
	EPWM4_A	36	16	PORz	
	EPWM4_B	35	15	SPI0_D0 / SDFM1_D1	SPI0_D0
	LIN1_TXD	34	14	SPI0_D1 / PR1_PRU1_GPIO15	SPI0_D1
LIN1_RXD	LIN1_RXD / PR1_PRU1_GPIO0	33	13	PR1_PRU1_GPIO5	
MCAN0_TX	MCAN0_TX / SDFM0_D0	32	12	PR1_PRU1_GPIO9	
MCAN0_RX	MCAN0_RX / PR1_PRU1_GPIO16	31	11	PR1_PRU0_GPIO0 / GPIO1	PR1_PRU0_GPIO0

Table 2-67. Mode 11: C2000 DRVx BoosterPacks (J5/J7)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
	VSYS_3V3_BP	41	61	VSYS_5V0_BP_2	
	ADC1_AIN1	42	62	GND	GND
PR1_PRU1_GPIO3	UART3_TXD / PR1_PRU1_GPIO3	43	63	ADC0_AIN2 / GPIO46	GPIO46
PR1_PRU1_GPIO19	UART3_RXD / SDFM1_D2 / PR1_PRU1_GPIO19	44	64	ADC1_AIN2 / PR1_PRU0_GPIO7	ADC1_AIN2
	SDFM0_CLK0	45	65	ADC2_AIN2 / PR1_PRU0_GPIO8	ADC2_AIN2
	ADC1_AIN3	46	66	ADC0_AIN5	
	SPI2_CLK	47	67	ADC1_AIN5 / PR1_PRU0_GPIO1	ADC1_AIN5
	PR1_PRU1_GPIO6	48	68	ADC2_AIN5 / PR1_PRU0_GPIO2	ADC2_AIN5
	I2C1_SCL	49	69	DAC_OUT / PR1_PRU1_GPIO0 / PR1_PRU0_GPIO6 / ADC0_AIN3	ADC0_AIN3
	I2C1_SDA	50	70	DAC_OUT / PR1_PRU1_GPIO9 / GPIO78 / ADC2_AIN6	ADC2_AIN6

Table 2-68. Mode 11: C2000 DRVx BoosterPacks (J6/J8)

Selected net	BoosterPack Net Name	J8	J6	BoosterPack Net Name	Selected net
	EPWM5_A	80	60	GND	
	EPWM5_B	79	59	SPI2_CS1	
	EPWM6_A	78	58	SPI2_CS0	
	EPWM6_B	77	57	PR1_PRU1_GPIO2 / SPI0_CLK / PR1_PRU0_GPIO9	PR1_PRU1_GPIO2
	EPWM7_A	76	56	PORz	
	EPWM7_B	75	55	SPI2_D0	
	LIN2_TXD	74	54	SPI2_D1	
	LIN2_RXD	73	53	GPIO6	
MCAN1_TX	MCAN1_TX / PR1_PRU1_GPIO1	72	52	GPIO124	
MCAN1_RX	MCAN1_RX / PR1_PRU0_GPIO9	71	51	GPIO1 / PR1_PRU0_GPIO0	GPIO1

2.12 Pinmux Mapping

The various pinmux options for the BoosterPack connector pins are given below.

Table 2-69. Pinmux Legend

Default signal for BP Header	Muxed alternative signal	External MUX for alternate signal options

Table 2-70. Pinmux Options for J1

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode 10
J1.1	3V3										
J1.2	ADC0_AIN1										
J1.3	PR0_PRU1_GPIO19		UART3_RXD	PR0_IEP0_EDC_SYNC_OUT0			GPMC0_A19	GPIO119	TRC_CLK	EQEP1_A	XBAROUT13
	MMC0_CMD	UART0_TXD	LIN0_TXD	MCAN0_TX	PR1_MDIO0_MDC			GPIO78	SDFM1_D0		
J1.4	PR0_PRU1_GPIO18		UART3_TXD	PR0_IEP0_EDIO_DATA_IN_OUT31			GPMC0_A17	GPIO120	TRC_CTL	EQEP1_B	XBAROUT14
J1.5	SPI1_CS0	EPWM7_A	MMC0_D2	UART4_TXD		PR1_PRU1_GPIO4		GPIO15	GPMC0_WAIT0		ADC_ETCH_XBAROUT4
J1.6	ADC2_AIN3										
	MMC0_CLK	UART0_RXD	LIN0_RXD	MCAN0_RX	PR1_MDIO0_MDIO			GPIO77	SDFM1_CLK0		
J1.7	SPI0_CLK	PR1_PRU0_GPIO9	MMC0_CMD	UART3_TXD		FSITX0_CLK	GPMC0_A7	GPIO12		ADC_ETCH_XBAROUT1	XBAROUT1
	PR1_PRU1_GPIO2		MII1_COL	UART5_TXD			GPMC0_AD2	GPIO73		ADC_ETCH_XBAROUT4	
J1.8	OSPI0_D0	EPWM9_A	PR1_PRU1_GPIO11	UART1_DCDn			GPMC0_AD11	GPIO3			
J1.9	I2C0_SCL							GPIO135		SDFM1_CLK3	
J1.10	I2C0_SDA							GPIO134		SDFM1_CLK2	
	UART2_RTSn	EQEP1_INDEX	LIN0_TXD	UART3_TXD				GPIO137		SDFM1_D3	

Table 2-71. Pinmux Options for J2

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J2.11	MMC0_D2	UART2_TXD	I2C1_SDA		PR1_PRU0_GPIO0			GPIO81	SDFM1_CLK2		
	OSPI0_CSn0	SPI0_CLK	UART3_TXD			UART2_RTSn		GPIO1			XBAROUT0

Table 2-71. Pinmux Options for J2 (continued)

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J2.12	PR1_PRU1_GPIO9		MII1_CRS	UART5_RXD			GPMC0_AD9	GPIO74		ADC_ETCH_XBAROUT5	
J2.13	EPWM5_B		PR1_PRU1_GPIO5	OSPI0_RESET_OUT0			GPMC0_AD5	GPIO54			EPWM8_B
J2.14	SPI0_D1	PR1_PRU0_GPIO1	MMC0_D1	UART3_RTSn		FSITX0_DATA1	GPMC0_BE1n	GPIO14		ADC_ETCH_XBAROUT3	XBAROUT3
	SPI1_D1	EPWM8_B	MMC0_CD	UART5_RXD	OSPI0_RESET_OUT0	PR1_PRU1_GPIO15	FSIRX0_DATA1	GPIO18	GPMC0_WPn	ADC_ETCH_XBAROUT7	XBAROUT4
J2.15	SPI0_D0	PR1_PRU0_GPIO0	MMC0_D0	UART3_CTSn		FSITX0_DATA0	GPMC0_A16	GPIO13		ADC_ETCH_XBAROUT2	XBAROUT2
	I2C2_SCL	PR1_PRU1_GPIO7	UART4_RXD				GPMC0_AD7	GPIO133	EQEP0_IDEX	SDFM1_D1	ADC_ETCH_XBAROUT3
J2.16	PORz										
J2.17	PR0_PRU1_GPIO17	PR1_PRU1_GPIO13	UART2_RXD	PR0_IEP0_EDIO_DATA_IN_OUT30	PR1_UART0_TXD	UART5_CTSn	GPMC0_AD13	GPIO125	SDFM0_D1		
J2.18	OSPI0_D1	EPWM9_B	PR1_PRU1_GPIO12	UART1_RIn			GPMC0_AD12	GPIO4			
J2.19	SPI0_CS0	PR1_PRU0_GPIO2	MMC0_CLK	UART3_RXD			GPMC0_A0	GPIO11		ADC_ETCH_XBAROUT0	XBAROUT0
	UART2_CTSn	PR1_MDIO0_MDC	SPI3_CS1			UART5_RXD	GPMC0_BE0n_CLE	GPIO127	SDFM0_D2		ADC_ETCH_XBAROUT0
	PR1_PRU1_GPIO1	UART1_DSRn		UART4_CTSn			GPMC0_AD1	GPIO72			
J2.20	GND										

Table 2-72. Pinmux Options for J3

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J3.21	5V									
J3.22	GND									
J3.23	ADC0_AIN6									
J3.24	ADC1_AIN0									
J3.25	ADC2_AIN0									
J3.26	ADC0_AIN0									

Table 2-72. Pinmux Options for J3 (continued)

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J3.27	ADC1_AIN4									
J3.28	ADC2_AIN4									
J3.29	ADC0_AIN4									
J3.30	DAC_OUT									
	ADC1_AIN6									

Table 2-73. Pinmux Options for J4

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10	Mode11
J4.31	EPWM8_A	PR1_PRU1_GPIO16	OSPI1_D0	MCAN0_RX	PR0_PRU1_GPIO7	OSPI0_D0	GPMC0_CSn1	GPIO59	UART4_TXD		EPWM8_A	
J4.32	EPWM8_B	PR1_PRU1_GPIO15	OSPI1_CLK	MCAN0_TX		OSPI0_CLK	GPMC0_AD15	GPIO60	UART4_RXD		EPWM9_B	
	PR0_ECAP0_APWM_OUT	PR1_PRU1_GPIO10	UART2_CTSn	PR1_ECAP0_APWM_OUT	OR1_UART0_RTSn		GPMC0_AD10	GPIO123	SDFM0_D0			
J4.33	UART1_RXD	OSPI0_LBCLKO			LIN1_RXD	OSPI1_LBCLKO	GPMC0_CLK	GPIO75				
	PR1_PRU1_GPIO0	UART1_DSRn		UART4_RTSn			GPMC0_AD0	GPIO71				
J4.34	LIN1_TXD	OSPI0_RESET_OUT0	SPI2_CLK	PR1_PRU1_GPIO8	OSPI1_RESET_OUT0	UART1_TXD	GPMC0_AD8	GPIO20			XBAROUT6	EPWM6_A
J4.35	EPWM4_B		PR1_PRU0_GPIO13				GPMC0_A11	GPIO52			EPWM1_B	
J4.36	EPWM4_A		PR1_PRU0_GPIO12				GPMC0_A10	GPIO51			EPWM4_A	
J4.37	EPWM3_B		PR1_PRU0_GPIO11				GPMC0_A9	GPIO50			EPWM6_A	
J4.38	EPWM3_A		PR1_PRU0_GPIO15				GPMC0_A13	GPIO49			EPWM3_A	
J4.39	EPWM2_B		PR1_PRU0_GPIO16		PR1_PRU0_GPIO7		GPMC0_A14	GPIO48			EPWM2_B	
J4.40	EPWM2_A		PR1_PRU0_GPIO3				GPMC0_A1	GPIO47			EPWM2_A	

Table 2-74. Pinmux Options for J5

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J5.41	3V3										
J5.42	ADC1_AIN1										
J5.43	UART2_RTSn	EQEP1_INDEX	LIN0_TXD	UART3_TXD				GPIO137		SDFM1_D3	
	SPI1_CLK	EPWM7_B	MMC0_D3	UART4_RXD		PR1_PRU1_GPIO3	FSIRX0_CLK	GPIO16	GPMC0_OEn_REn	ADC_ETCH_XBAROUT5	XBAROUT2
J5.44	UART1_RTSn	SPI0_CS1	LIN0_RXD	UART3_RXD				GPIO136		SDFM1_D2	
	UART0_RTSn	I2C2_SCL	SPI3_D0	PR1_PRU1_GPIO19	PR1_PRU0_GPIO17	UART3_RXD	GPMC0_WAIT1	GPIO25			XBAROUT9
J5.45	CLKOUT1	PR1_PRU0_GPIO7	UART2_RTSn		PR1_UART0_CTSn		GPMC0_A5	GPIO122	SDFM0_CLK0	EQEP1_STROBE	
J5.46	ADC1_AIN3										
J5.47	SPI2_CLK	PR1_PRU1_GPIO17				UART5_TXD	GPMC0_WEn	GPIO129	SDFM0_D3		ADC_ETCH_XBAROUT1
J5.48	LIN1_RXD	OSPI0_ECC_FAIL	SPI2_CS0	PR1_PRU1_GPIO6	OSPI1_ECC_FAIL	UART1_RXD	GPMC0_AD6	GPIO19	OSPI0_RESET_OUT1	XBAROUT5	EPWM6_B
J5.49	I2C1_SCL		SPI1_CS0	PR1_PRU0_GPIO17			GPMC0_WEn	GPIO23			XBAROUT7
J5.50	I2C1_SDA		SPI3_CLK	PR1_PRU0_GPIO18			GPMC0_OEn_REn	GPIO24			XBAROUT8

Table 2-75. Pinmux Options for J6

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10	Mode11
J6.51	OSPI0_CSn0	SPI0_CLK	UART3_TXD			UART2_RTSn		GPIO1			XBAROUT0	
	MMC0_D2	UART2_TXD	I2C1_SDA		PR1_PRU0_GPIO0			GPIO81	SDFM1_CLK2			
J6.52	PR0_PRU1_GPIO7	CPTS0_TS_SYNC	PR1_PRU0_GPIO10	PR0_IEP0_EDC_SYNC_OUT1	PR1_UART0_RXD		GPMC0_A8	GPIO124	SDFM0_CLK1	SDFM1_D0	UART2_TXD	UART5_RTSn
J6.53	OSPI0_D3	SPI0_D1	OSPI0_D4					GPIO6				
J6.54	SPI2_D1	PR1_PRU1_GPIO14				UART5_RXD	GPMC0_AD14	GPIO128	SDFM0_CLK3	SDFM1_D2	ADC_ETCH_XBAROUT9	
J6.55	SPI2_D0	PR1_PRU1_GPIO18	UART4_RTSn	PR1_IEP0_ED_SYNC_OUT0	I2C1_SDA	MCAN1_RX	GPMC0_OEn_REn	GPIO130		SDFM1_CLK0		

Table 2-75. Pinmux Options for J6 (continued)

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10	Mode11
J6.56	PORZ											
J6.57	PR1_PRU1_GPIO2		MII1_COL	UART5_TXD			GPMC0_AD2	GPIO73		ADC_ETCH_XBAROUT4		
	SPI0_CLK	PR1_PRU0_GPIO9	MMC0_CMD	UART3_TXD		FSITX0_CLK	GPMC0_A7	GPIO12		ADC_ETCH_XBAROUT1	XBAROUT1	
J6.58	CLKOUT0	LIN1_RXD	OSPI0_ECC_FAIL	UART1_RXD	SPI2_CS0	OSPI1_ECC_FAIL	USB0_DRVVBUS	GPIO138	SAFETY_ERRORn			
J6.59	UART1_CTSn	PR1_MDIO0_MDIO	SPI2_CS1	PR1_IEP0_EDC_SYNC_OUT1	UART5_CTSn	UART5_TXD	GPMC0_CLKLB	GPIO126	SDFM0_CLK2	SDFM1_D1		
J6.60	GND											

Table 2-76. Pinmux Options for J7

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J7.61	5V										
J7.62	GND										
J7.63	ADC0_AIN2										
	EPWM1_B		PR1_PRU0_GPIO4				GPMC0_A4	GPIO46			EPWM4_B
J7.64	ADC1_AIN2										
	UART0_CTSn	I2C2_SDA	SPI3_D1	SPI0_CS1	PR1_PRU0_GPIO7	UART3_TXD		GPIO26			XBAROUT10
J7.65	ADC2_AIN2										
	EPWM0_B		PR1_PRU0_GPIO8				GPMC0_A6	GPIO44			EPWM0_B
J7.66	ADC0_AIN5										
J7.67	ADC1_AIN5										
	MMC0_D3	UART3_RTSn			PR1_PRU0_GPIO1			GPIO82	SDFM1_D2		
J7.68	ADC2_AIN5										
	MMC0_WP	UART0_RTSn	I2C2_SCL		PR1_PRU0_GPIO2			GPIO83	SDFM1_CLK3		
J7.69	DAC_OUT										
	PR1_PRU1_GPIO0	UART1_DSRn		UART4_RTSn			GPMC0_AD0	GPIO71			
	EPWM1_A		PR1_PRU0_GPIO6				GPMC0_A4	GPIO45			EPWM1_A
	ADC0_AIN3										

Table 2-76. Pinmux Options for J7 (continued)

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J7.70	DAC_OUT										
	PR1_PRU1_GPIO9		MII1_CRS	UART5_RXD			GPMC0_AD9	GPIO74		ADC_ETCH_XBAR OUT5	
	MMC0_CMD	UART0_TXD	LIN0_TXD	MCAN0_TX	PR1_MDIO0_MDC			GPIO78	SDFM1_D0		
	ADC2_AIN6										

Table 2-77. Pinmux Options for J8

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J8.71	MMC0_D0	UART2_RXD	I2C1_SCL	MCAN1_RX	PR1_PRU0_G PIO10			GPIO79	SDFM1_CLK1		
	MMC0_D1			MCAN1_TX	PR1_PRU0_G PIO9			GPIO80	SDFM1_D1		
J8.72	SPI2_CS0	PR1_PRU0_GPIO19	UART4_CTSn	PR1_IEP0_EDIO_DATA_IN_O UT31	I2C1_SCL	MCAN1_TX	GPMC0_CSn0	GPIO131	EQEP0_B	SDFM1_D0	
	PR1_PRU1_GPIO1		MII1_RX_ER	UART4_CTSn			GPMC0_AD1	GPIO72			
J8.73	LIN2_RXD	UART2_RXD	SPI2_D0	USB0_DRVVBUS	OSPI1_RESE T_OUT1	OSPI0_RESET_ OUT1		GPIO21	GPMC0_CSn0		
J8.74	LIN2_TXD	UART2_TXD	SPI2_D1					GPIO22	GPMC0_ADVn_ALE		
J8.75	LIN0_RXD	UART1_CTSn		I2C0_SDA	UART2_TXD			GPIO63			EPWM7_B
J8.76	EPWM7_A	PR1_PRU1_GPIO4	OSPI0_CSn1			OSPI1_CSn1	GPMC0_AD4	GPIO57			EPWM7_A
J8.77	EPWM6_B	PR1_PRU1_GPIO6		UART2_RTSn			GPMC0_A20	GPIO56			EPWM6_B
J8.78	EPWM6_A	PR1_PRU1_GPIO8	CLKOUT0				GPMC0_AD8	GPIO55			EPWM3_B
J8.79	EPWM7_B	PR1_PRU1_GPIO3	OSPI1_D1			OSPI0_D1	GPMC0_AD3	GPIO58			EPWM5_B
J8.80	EPWM5_A		PR1_PRU0_G PIO13				GPMC0_A11	GPIO52			EPWM51_B

Table 2-78. Pinmux Legend

Default signal for BP Header	Muxed alternative signal	External MUX for alternate signal options

2.13 Test Points

The AM261x LaunchPad includes multiple test points to aid in hardware debug. Table 2-79 includes a list of the test points available on the LaunchPad.

Table 2-79. LP-AM261 Test Points

Test Point Designator	Test Point Net Name	Description
TP1	VUSB_5V0	USB Type-C 5V Input
TP2	VDD_XDS3V3	XDS110 3.3V supply
TP3	GND_XDS	XDS110 isolated GND
TP4	TUSB_ADDR	USB Type-C Logic Controller (U6) ADDR input
TP5	TUSB_ID	USB Type-C Logic Controller (U6) ID pin
TP6	TM4C129_TCK	XDS110 TCK pin
TP7	TM4C129_TMS	XDS110 TMS pin
TP8	TA_RESETz_XDS	Test Automation reset signal to XDS110
TP9	-	XDS110 PM3 pin
TP10	TM4C129_TDI	XDS110 TDI pin
TP11	TM4C129_TDO	XDS110 TDO pin
TP12	VBUS_XDS_5V0	XDS110 5.0V supply
TP13	GND_XDS	XDS110 isolated GND
TP14	VBUS_MICRO_AB_5V0	USB2.0 micro-AB port 5.0V VBUS supply
TP15	VREG	PMIC (U28) VREG output
TP16	VSYS_3V3	PMIC (U28) BUCK1 3.3V output - system IO rail
TP17	OSPI0_CSN0	OSPI0 chip select 0
TP18	OSPI0_CLK	OSPI0 clock
TP19	VCORE_1V25	PMIC (U28) BUCK3 1.25V output - AM261x core voltage
TP20	OSPI0_D7	OSPI0 data bit 7
TP21	OSPI0_D6	OSPI0 data bit 6
TP22	OSPI0_D1	OSPI0 data bit 1
TP23	OSPI0_D5	OSPI0 data bit 5
TP24	OSPI0_D0	OSPI0 data bit 0
TP25	VDD_1P8	PMIC (U28) VDD_1P8 pin
TP26	OSPI0_ECC_FAIL	OSPI0 ECC Fail
TP27	VSYS_2V5	PMIC (U28) BUCK2 2.5V output
TP28	OSPI0_D3	OSPI0 data bit 3
TP29	OSPI0_D2	OSPI0 data bit 2
TP30	AM261_OSPI0_DQS	OSPI0 DQS
TP31	VSYS_1V8	PMIC (U28) 1.8V LDO output
TP32	OSPI0_D4	OSPI0 data bit 4
TP33	OSPI1_D7	OSPI1 data bit 7
TP34	OSPI1_DQS	OSPI1 DQS
TP35	OSPI1_D6	OSPI1 data bit 6
TP36	OSPI1_D5	OSPI1 data bit 5
TP37	OSPI1_D0	OSPI1 data bit 0
TP38	OSPI1_D3	OSPI1 data bit 3
TP39	OSPI1_D4	OSPI1 data bit 4
TP40	OSPI1_D1	OSPI1 data bit 1
TP41	OSPI1_CSN0	OSPI1 chip select 0

Table 2-79. LP-AM261 Test Points (continued)

Test Point Designator	Test Point Net Name	Description
TP42	OSPI1_D2	OSPI1 data bit 2
TP43	OSPI1_ECC_FAIL	OSPI1 ECC Fail
TP44	OSPI1_CLK	OSPI1 clock
TP45	EXT1_VMON2	Ethernet Connector 0 voltage monitor
TP46	AM261_PORZ	PORZ
TP47	MII1_CRS	MII1 Carrier Sense
TP48	VDDA_ETH1_1V8	PHY1 1.8V supply input
TP49	ETH1_CLKOUT	PHY1 CLK_OUT pin
TP50	VDDA_ETH0_1V8	PHY0 1.8V supply input
TP51	ETH0_CLKOUT	PHY0 CLK_OUT pin
TP52	VSYS_5V0	USB 5.0V input power load switch (U14) output
TP53	RJ45_0_VCC	PHY0 RJ-45 VCC input
TP54	RJ45_1_VCC	PHY1 RJ-45 VCC input
TP55	GND	GND
TP56	GND	GND
TP57	TA_GPIO2	Test Automation GPIO2
TP58	AM261_SAFETY_ERRORN	Safety Error output signal
TP59	AM261_WARMRSTN	Warm Reset
TP60	AM261_GPIO33	GPIO33
TP61	AM261_GPIO40	GPIO40
TP62	AM261_SPI2_D0	SPI2 data bit 0
TP63	AM261_MII2_COL	MII2 collision detect
TP64	AM261_UART3_RXD	UART3 receive
TP65	AM261_INT_PB_GPIO124	User interrupt push button input
TP66	AM261_SPI2_CS1	SPI2 chip select 1
TP67	GND	GND
TP68	GND	GND
TP69	GND	GND
TP70	GND	GND
TP71	GND	GND
TP72	GND	GND
TP73	GND	GND

2.14 Best Practices

Electrostatic Discharge (ESD) Compliance

Components installed on the product are sensitive to electrostatic discharge (ESD). TI recommends this product be used in ESD controlled environment. This includes a temperature or humidity controlled environment to limit the buildup of ESD. TI recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

Assumed Operating Conditions

This kit is assumed to run at standard room conditions. Standard ambient temperature and pressure (SATP) with moderate-to-low humidity is assumed.

3 Software

The AM261x MCU+ Software Development Kit (MCU-PLUS-SDK-AM261X) is a unified software platform for embedded processors providing easy setup and fast out-of-the-box access to examples, benchmarks and demonstrations. This software accelerates application development schedules by eliminating creating basic system software functions from scratch.

The AM261x MCU+ Academy provides a Getting Started Guide for first-time software development using the LP-AM261. Follow the steps in this guide to begin development.

4 Hardware Design Files

The LP-AM261 hardware design files can be downloaded from the EVM Tool Page, or by clicking this link.

5 Compliance

All components selected meet RoHS compliance.

6 Additional Information

6.1 Revision E1 Appendix

The below issues were identified in LP-AM261 RevE1. The details of modifications needed for all these issues are also captured. **All these modifications are already made on all the LP-AM261 RevE1 boards ordered from ti.com**.

6.1.1 TA_POWERDOWNz pulled up by VSYS_TA_3V3 which is powered by VSYS_3V3

The TA_POWERDOWNz which enables the input power load switch to enable the system VSYS_5V0 power is pulled up using VSYS_3V3. Since VSYS_3V3 is itself derived from VSYS_5V0, the LP-AM261 RevE1 does not power on in default configuration.

Modification: The VSYS_TA_3V3 needs to be powered from power source other than that from PMIC. Hence an LDO is soldered which generates 3.3V from VSYS_5V0 and pulls up TA_POWERDOWNz to 3.3V.

6.1.2 USB2.0_MUX_SEL0 pulled up by R355

The USB2.0_MUX_SEL0 net is pulled up by R355, which makes the USB signals from AM261x to be routed to USB-C connecter by default, than as intended to USB Micro-AB.

Modification: The resistor R355 is unmounted or made DNI.

6.1.3 MDIO and MDC of PRU0-ICSS0 needs to be routed to both Ethernet PHYs

The nets AM261_PR0_MDIO0_MDIO and AM261_PR0_MDIO0_MDC need to be connected to both Ethernet PHYs. In the current configuration

- Ethernet Phy 0 has muxed AM261_MDIO0_MDC, AM261_MDIO0_MDIO with AM261_PR**0**_MDIO0_MDC, AM261_PR**0**_MDIO0_MDIO connected.
- Ethernet Phy 1 has muxed AM261_MDIO0_MDC, AM261_MDIO0_MDIO with AM261_PR**1**_MDIO0_MDC, AM261_PR**1**_MDIO0_MDIO connected.

But the needed configuration is

- Both Ethernet Phy 0 and 1 should get muxed AM261_MDIO0_MDC, AM261_MDIO0_MDIO with AM261_PR**0**_MDIO0_MDC, AM261_PR**0**_MDIO0_MDIO nets.

Modification: For the above changes,

- R135 in series with AM261_PR1_MDIO0_MDIO – Unmount(DNP) R135
- R137 in series with AM261_PR1_MDIO0_MDC – Unmount(DNP) R137
- A blue wire from R167 Pin1 to R137 Pin1 should be connected.
- A blue wire from R180 Pin1 to R135 Pin1 should be connected.

6.1.4 AM261_RGMII1_RXLINK and AM261_RGMII2_RXLINK to be connected to GPIO

The pin 43 of both the Ethernet headers bring out AM261_RGMII1_RXLINK and AM261_RGMII2_RXLINK, which in the current implementation of LP-AM261x RevE1, this is just made a Test point. But these need to be connected to RX_LINK pins of respective PRU of AM261x.

Modification: For the above changes,

- PR0_PRU0_GPIO8(GPIO90) - pr0_mii0_rxlink - should connect to RX_LINK of Ethernet connector 0 (TP52).
- PR0_PRU1_GPIO8(GPIO106) - pr0_mii1_rxlink - should connect to RX_LINK of Ethernet connector 1 (TP46).

6.2 Revision E2 Appendix

The following sections detail changes made on the LP-AM261 from Revision E1 to E2 and identified limitations of Revision E2.

6.2.1 Revision E2 Changes from E1

The following EVM updates were made for LP-AM261 Rev E2.

- BoosterPack pinout
  - The BoosterPack header pinout was overhauled to accommodate for the four BoosterPack modes. Refer to Section 2.11 for pinout and BoosterPack mode details.
- Test Automation power (VSYS_TA_3V3) added to test automation interface power tree
- OSPI Interfaces
  - OSPI0 device changed to MX25UW6445GXDQ00 NOR Flash
  - OSPI1 device changed to APS12808L-OBMX-BA PSRAM
- PMIC part number updated to TPS65036501RAYRQ1
- VCORE_1V2 power changed to VCORE_1V25 to match core voltage requirement for 500MHz AM261x MCU
- Added active low mux for SOP pins. Mux's enable is controlled by SOP_DRIVER_OEN and BP_BO_MUX_EN_N
- AM261x part number updated to XAM2612AOFFHIZFG

All Revision E1 modifications detailed in Section 6.1 are now implemented in the PCB hardware, and are not required on Revision E2.

6.2.2 Revision E2 Known Limitations

OSPI Boot - Silicon Errata

AM261x devices have a silicon errata (errata i2479) associated with the OSPI Reset signal when the device is in OSPI boot mode. In OSPI boot mode, GPIO61 is configured by the AM261x Boot ROM as OSPI0_RESET_OUT0 to drive low at power-on in order to reset an external OSPI flash device. However, due to a reset signal management issue in the OSPI controller, this pin does not de-assert and drive high after the flash device resets. The flash device remains in reset which causes the boot to fail. The LP-AM261 showcases one workaround to this issue. The implementation details are below:

- GPIO61/OSPI0_RESET_OUT0 is routed from the AM261x to a level translator. The level translator is **disabled** by default. The pull-down resistor **R90** on the enable signal prevents the OSPI0_RESET_OUT0 from propagating to the OSPI0 reset logic at boot. **This resistor should not be removed unless OSPI boot functionality is not desired.**
- At the OSPI0 reset logic circuit, the OSPI0_RESET_OUT0 net is held HIGH through pull-up resistor **R344** to hold the net high at boot. The OSPI0 reset is triggered by the WARMRSTn signal, which drives LOW at boot and goes HIGH once power supplies are stable. The output of AND gate U27 connects to the OSPI0 flash device reset input.
- Once boot is complete, the level translator U25 can be enabled by configuring the BP_BO_MUX_EN signal HIGH via the I2C-controlled IO Expander U23. This allows OSPI_RESET_OUT0 to be configured in software to reset the flash during an application.

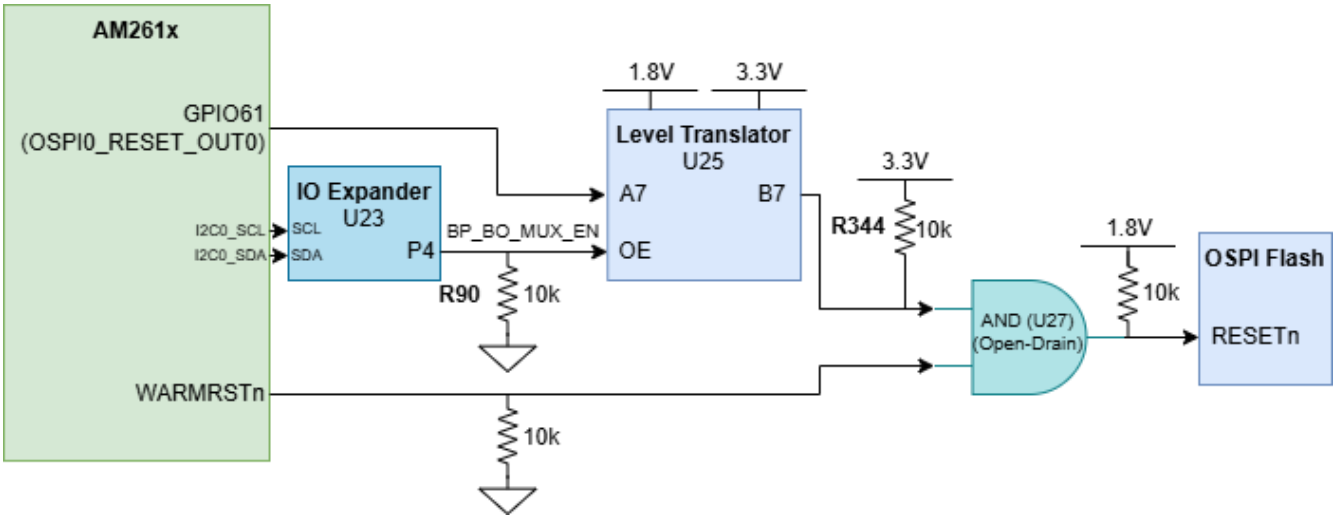


Figure 6-1. LP-AM261 OSPI Reset Scheme

For more details on this silicon errata, see the AM261x Errata Document.

For more details on hardware workarounds for this issue, see the *AM261x OSPI/QSPI Boot Pin Requirements* section in the AM26x Hardware Design Guidelines document.

RMII Ethernet

When running RMII Ethernet on LP-AM261 Rev E2 (and E1), 10% of packets experience RX CRC or RX AlignCode errors due to signal trace length matching rules for RMII being violated on the PCB. This issue will be fixed in the next revision of the EVM with proper data and clock trace length matching.

All other Ethernet modes and protocols do not experience this issue and are expected to function without error.

6.3 Revision A Appendix

The following section details changes made to LP-AM261 from Revision E2 to Revision A.

6.3.1 Revision A Changes from E2

The following EVM updates were made for LP-AM261 Revision A.

- Ethernet
  - **On-board DP83869 Gigabit PHYs:** Revision A of the LP-AM261 removes the Ethernet add-on board ecosystem support and now comes with 2x DP83869 gigabit Ethernet PHYs assembled on-board, each with an RJ-45 connector.
- PMIC
  - **Watchdog Disable:** The OTP configuration on the TPS65036601 PMIC enables the watchdog timer by default. This timer triggers a reset signal to the AM261x device if left idle for >12 minutes. On Rev A, the watchdog timer is disabled at power-on by connecting the PMIC's GPIO pin (13) to the internal voltage reference VDD_1P8 pin (3) via jumper SH-J1 on J1 pins 1-2, which comes assembled on the EVM by default. This connection sets an internal bit on the PMIC to disable the watchdog timer before the PMIC ramps. To enable the watchdog at power-on, simply remove the jumper on J1 pins 1-2 before applying 5V/3A to the LP-AM261.
  - **nINT and GPIO Pin Assignments**: The net assignments for PMIC pins 13 (GPIO) and 21 (nINT) have been corrected in Rev A to their intended use case nets. The GPIO pin (13) is connected to the SAFETY_ERRORn pin on the AM261x MCU when SH-J1 is installed on J1 pins 2-3, and the nINT pin (21) is assigned to PMIC_INTn_GPIO0, which connects to GPIO0 on the AM261x MCU. On previous LP-AM261 revisions, these nets were swapped.
- BoosterPack Pinout Changes
  - **Servo Motor Control BoosterPacks:** Revision A now supports a wider array of servo motor control BoosterPacks. These pinout changes are shown in Section 2.11.2.

  - **BoosterPack Power Supply Pins:** The 3V3 supply on pins J1-1 and J5-41, and the 5V0 supply on pins J3-21 and J7-61 are now enabled by default via jumpers installed at PCB assembly on pins 1-2 of J13, J26, and J27.
  - GPIO124 is routed to J6-52 in order to have the CPTS0_TS_SYNC signal accessible on a header.
- General
  - The GPIO Interrupt Pushbutton is connected to GPIO5 (changed from GPIO124).
  - The IO Expanders can now be reset using PORz.

6.3.2 Revision A Errata

BP-AMC0106-LMG-MD Servo Motor Control Demo with SDFM Current Feedback

The following section details known errata related to Revision A of the LP-AM261.

Hardware modifications to the LP-AM261 are required for this demo:

1. Bend or remove the following pins on the LaunchPad: J1-4, J1-9, J3-27, J4-33, J2-14
2. Add a shunt between J1-6 and J1-7
3. Remove R219 and populate R218
4. Set the ADC VREF switches to Internal VREF (see Figure 2-32)

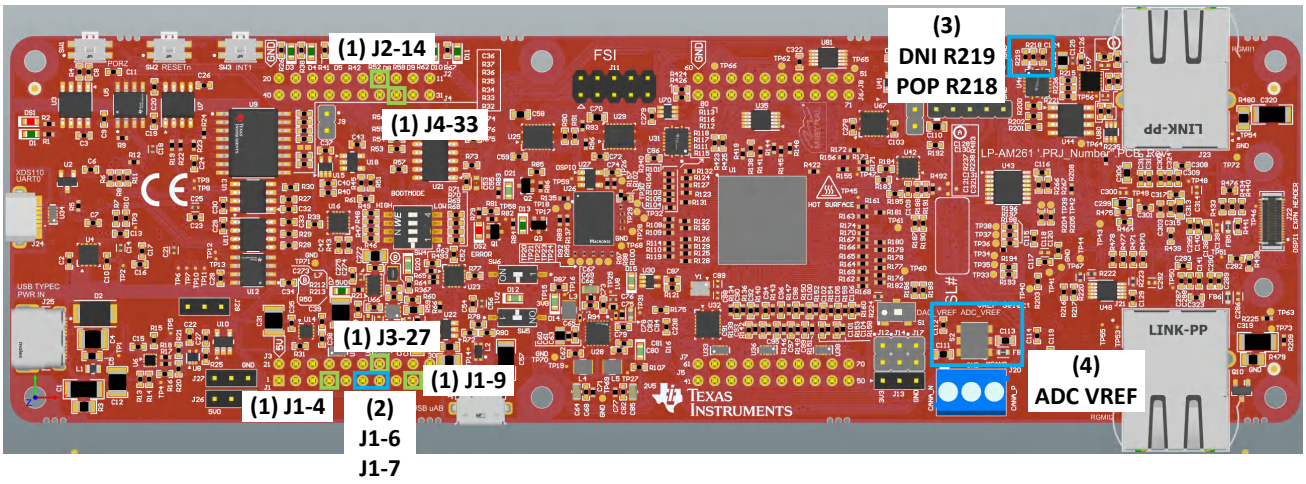


Figure 6-2. LP-AM261 Modifications for BP-AMC0106-LMG-MD Demo

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7 References

7.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- Texas Instruments, AM2612 Microcontroller, webpage
- Texas Instruments, AM261x Sitara™ Microcontrollers, data sheet
- Texas Instruments, AM261x Technical Reference Manual
- Texas Instruments, AM261x Register Addendum, technical reference manual

- *Texas Instruments Code Composer Studio*
- *Updating XDS110 Firmware*
  - To find the serial number, only follow steps 1 and 2 of updating XDS110 firmware

7.2 Other TI Components Used in This Design

This LaunchPad uses various other TI components for its functions. A consolidated list of these components with links to their TI data sheets is shown below.

- *TUSB320USB Type-C Configuration Channel Logic and Port Controller*
- *TPD4E02B04 4-Channel ESD Protection Diode for USB Type-C*
- *TPS22965x-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch*
- *TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter*
- *TPS748 1.5-A Low-Dropout Linear Regulator*
- *TCA6408A Low-Voltage 8-Bit I 2C and SMBus I/O Expander*
- *SN74AVC4T245 Dual-Bit Bus Transceiver with Configurable Voltage Translation*
- *TPS22918-Q1, 5.5-V, 2-A, 52-mΩ On-Resistance Load Switch*
- *TPD6E001 Low-Capacitance 6-Channel ESD-Protection for High-Speed Data Interfaces*
- *XDS110 JTAG Debug Probe*
- *TS5A23159 1-Ω 2-Channel SPDT Analog Switch*
- *TCAN1044V-Q1 Automotive Fault-Protected CAN FD Transceiver*
- *DP83869HM High Immunity 10/100/1000 Ethernet Physical Layer Transceiver*
- *TS3DDR3812 12-Channel, 1:2 MUX/DEMUX Switch for DDR3 Applications*
- *TCA9617B Level-Translating I2C Bus Repeater*
- *SN74CB3Q3257 4-Bit 1-of-2 FET Multiplexer/Demultiplexer*
- *TPIC2810 8-Bit LED Driver with I2C Interface*
- *TPS796xx 1-A Low-Dropout Linear Regulators*
- *TXB0108 8-Bit Bidirectional Voltage-Level Translator with Auto-Direction Sensing*
- TCA6408ARGTR 8-bit translating 1.65- to 5.5-V I2C/SMBus I/O expander

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 5, 2025 to December 31, 2025 (from Revision B (November 2025) to Revision C (December 2025)) **Page**

- Changed J1-3 to J1-4. J1-3 is needed and should not be bent/removed. Image updated to reflect the text... 76

Changes from May 30, 2025 to November 5, 2025 (from Revision A (May 2025) to Revision B (November 2025)) **Page**

- Feature List updated for Rev A.....1
- Updated functional block diagram to reflect Rev A.....4
- Setup topic revised to remove information on Ethernet add-on boards..... 6
- Updated diagram and tables to reflect Rev A addition of signal on U42 P0.....21
- [UART] Updated for Rev A - two UART3 pinned out.....36

- Diagrams and table updated for Rev A..... 46

Changes from August 31, 2024 to May 30, 2025 (from Revision * (August 2024) to Revision A (May 2025)) **Page**

- Feature List updated for Rev E2.....1
- Updated kit contents list to include USB Type-C cable..... 2
- Updated System Architecture diagram to include USB2.0 interface..... 3
- Updated Component ID diagrams with Rev E2 PCB images.....3
- Updated functional block diagram to reflect Rev E2.....4
- Initial Creation.....4
- Updated link to BoosterPack Pinmux section.....5
- Setup topic revised to include information on both EVM setup configurations.....6
- Updated core voltage to 1.25V in power tree diagram..... 10
- Added power status LED diagram..... 11
- Initial Creation..... 11
- Updated push button figure to reflect LP-AM261..... 13
- Updated block diagrams for Rev E2 and corrected reset signal association for PORz and Warm Reset.....15
- Updated boot mode tables for clarity between SOP pins and on-board switch settings..... 19
- Added GPIO tables to IO Expander topic to show active status and IO usage. Updated block diagram to show reference designator and I2C address..... 21
- Updated OSPI Interface to reflect Rev E2 changes - OSPI0 is Macronix flash, OSPI1 is AP Memory PSRAM. Updated block diagram to reflect part numbers and pin naming. Added table for resistor mods to enable OSPI1 expansion connector. Added PCB images to show resistor modifications..... 23
- Added mux tables and updated diagrams for SPI.....34
- Added mux tables and new diagram for MCAN..... 38
- Updated FSI diagram and added mux select table..... 43
- Updated Mux tables and revised diagram for LIN..... 45
- Updated ADC interface block diagram. Added PCB image for ADC/DAC VREF switches. 46
- Updated EQEP diagram..... 50
- Updated USB block diagram. Added micro-USB mode switch settings and PCB image. Added information on USB Host and Device modes.....51
- Updated BoosterPack pinout diagram for Rev E2.....54
- Updating Reference Documents section to match other AM261 EVMs.....77

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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