TMCS1236-Q1 AEC-Q100, Precision 4MHz Hall-Effect Current Sensor With Reinforced Isolation, Enhanced EMI Rejection, and 75ns Fast Overcurrent Detection

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- High continuous current capability: $80A_{RMS}$
- Robust isolation with $1.3kV_{DC}$ reinforced working voltage
- Fast Response
  - Overcurrent detection response: 75ns
  - -3dB signal bandwidth: 4MHz
  - Response time: 200ns
  - Propagation delay: 100ns
- High immunity to external magnetic fields
- Operating supply range: 3V to 5.5V
- Bidirectional and unidirectional current sensing
- High accuracy
  - Offset thermal drift: ±15µV/°C (30.8mV/A variant)
  - Non-linearity: ±0.1%
- Over Current Threshold Voltage
- Multiple sensitivity options:
  - Refer to *Device Comparison Table*
- Safety related certifications
  - UL 1577 Component Recognition Program
  - IEC/CB 62368-1

2 Applications

- Onboard charger
- DC/DC converter
- Rotor excitation
- HVAC compressor
- High-voltage PDU

3 Description

The TMCS1236-Q1 is a galvanically isolated Hall-effect current sensor with industry leading isolation, high signal bandwidth and fast detection response time. An output voltage proportional to the input current is provided with excellent linearity, minimal signal tracking delay, and low drift. Precision signal conditioning circuitry with robust full chip regulation is optimized for switching applications.

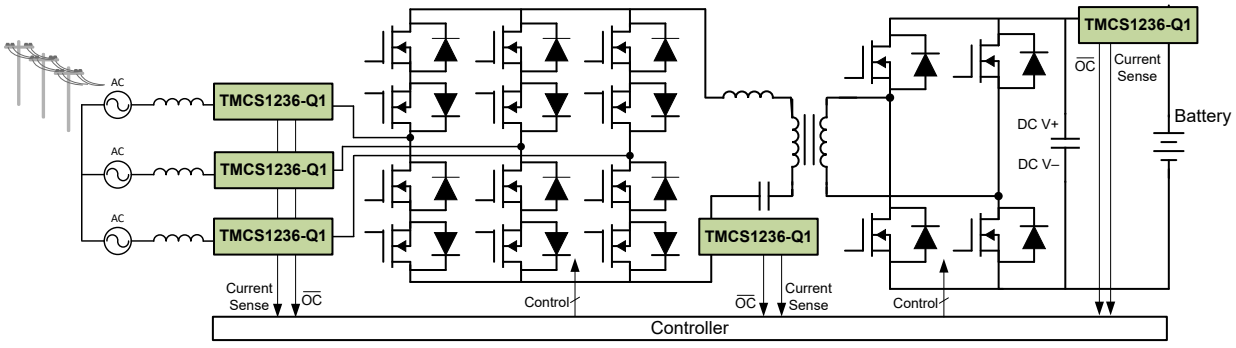
AC or DC input current flows through an internal conductor generating a magnetic field measured by integrated Hall-effect sensors. Core-less construction eliminates the need for magnetic concentrators. Differential Hall sensors reject interference from stray external magnetic fields. Low conductor resistance increases linear current ranges while minimizing power loss. Shuntless isolated current measurement eliminates the requirement for the primary side power supply and complex PCB layout for Kelvin connection. Insulation capable of withstanding $5kV_{RMS}$, coupled with a minimum of 8mm creepage and clearance, provides high levels of reliable lifetime reinforced working voltage.

Integrated shielding enables excellent common-mode rejection, EMI rejection, and transient immunity. Fixed sensitivity allows the device to operate from a single 3V to 5.5V power supply, eliminating ratiometry errors and improving supply noise rejection.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMCS1236-Q1	DVG (SOIC, 10)	10.3mm × 10.3mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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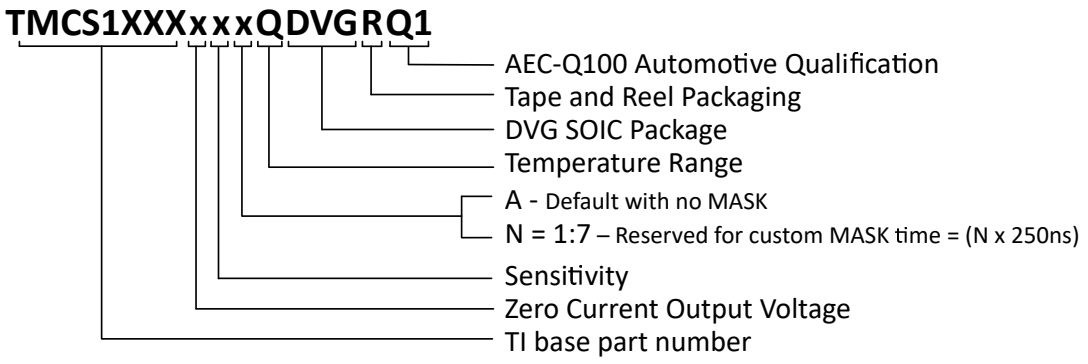
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4 Device Comparison

Table 4-1. Device Comparison

PRODUCT(3)	SENSITIVITY	ZERO CURRENT OUTPUT VOLTAGE	I_{IN} LINEAR MEASUREMENT RANGE(1)	
			V_S = 5V	V_S = 3.3V
TMCS1236AGx-Q1	30.8mV/A	2.5V	±77.9A(2)	–77.9A to 22.7A(2)

(1) Linear range limited by the maximum output swing to power supply (3V to 5.5V) and ground, not by thermal limitations.
(2) Current levels must remain below both allowable continuous DC/RMS and transient peak current safe operating areas to not exceed device thermal limits. See the *Safe Operating Area* section.
(3) Device Comparison table is for reference and includes both released and prospective options. Device options are subject to change and continuously expanding based on demand. Refer to Section PACKAGE OPTION ADDENDUM at end of this document for current orderable part numbers (OPNs), or contact your TI sales representative for custom configurations.



Note

MASK time is NOT user programmable. Factory-trimmed options available in 250ns steps increment above default overcurrent comparator response time. Refer to PACKAGE OPTION ADDENDUM for current OPNs, or contact your TI sales representative for custom configurations.

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5 Pin Configuration and Functions

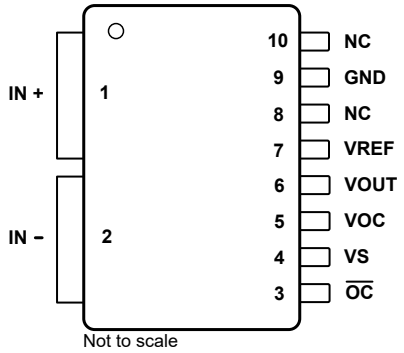


Figure 5-1. DVG Package 10-Pin SOIC Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN+	Analog Input	Input current positive pin
2	IN–	Analog Input	Input current negative pin
3	$\overline{OC}$	Digital Output	Overcurrent output, open-drain active low. Connect pin to GND if not used.
4	VS	Analog	Power supply
5	VOC	Analog Input	Overcurrent threshold. Sets overcurrent threshold. Connect pin to VS if not used.
6	VOUT	Analog Output	Output voltage
7	VREF	Analog Output	Zero current output voltage reference
8	NC	-	Reserved. Pin can be connected to GND or left floating.
9	GND	Analog	Ground
10	NC	-	Reserved. Pin can be connected to GND or left floating.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage		GND – 0.3	6	V
	Analog input	VOC	GND – 0.3	(V_S) + 0.3	V
	Analog output	VOUT, VREF			
	Digital output	$\overline{OC}$			
	No Connect	NC			
T_J	Junction temperature		–65	165	°C
V	Storage temperature		–65	165	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Operating supply voltage	3	5	5.5	V
T_A(1)	Operating free-air temperature	–40		125	°C

(1) Input current safe operating area is constrained by junction temperature. Recommended condition based on use with the *TMCS-ADAPTER-EVM*. Input current rating is derated for elevated ambient temperatures.

6.4 Thermal Information

THERMAL METRIC (1)		TMCS1236 (2) DVG (SOIC-W-10) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	10.1	
Ψ_{JT}	Junction-to-top characterization parameter	4.4	
Ψ_{JB}	Junction-to-board characterization parameter	8.3	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Applies when device is mounted on the *TMCS-ADAPTER-EVM* with 40A input current. For more details, see the *Safe Operating Area* section.

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6.5 Power Ratings

V_S = 5.5V, T_A = 125°C, T_J = 165°C, device soldered on the *TMCS-ADAPTER-EVM*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)				2.0	W
P_{D1}	Maximum power dissipation (current input, side-1)	I_{IN} = 44A			1.9	W
P_{D2}	Maximum power dissipation by (side-2)	V_S = 5.5V, I_Q = 14.5mA, no loads			0.1	W

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	≥ 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	≥ 8	mm
CTI	Comparative tracking index	DIN EN 60112; IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V_{RMS}	I-IV	
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1697	V_{PK}
V_{IOWM}	Maximum reinforced isolation working voltage	AC voltage (sine wave); Time Dependent Dielectric Breakdown (TDDB) test, < 1ppm fail rate, see the *Input Isolation* section.	950	V_{RMS}
			1343	V_{DC}
	Maximum basic isolation working voltage	AC voltage (sine wave); Time Dependent Dielectric Breakdown (TDDB) test, < 1000ppm fail rate, see the *Input Isolation* section.	1200	V_{RMS}
			1697	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = √2 x V_{ISO}, t = 60s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 62368-1, 1.2/50µs waveform, V_{TEST} = 1.3 × V_{IOSM} (qualification)	10000	V_{PK}
q_{pd}	Apparent charge(3)	Method b1: At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1s, $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1s	≤5	pC
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 sin (2πft), f = 1MHz	0.6	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500V, T_A = 25°C	>10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	>10^{11}	Ω
		V_{IO} = 500V at T_S = 150°C	>10^9	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO}, t = 60s (qualification); V_{TEST} = 1.2 × V_{ISO}, t = 1s (100% production)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Take care to maintain the creepage and clearance distance of the board design to make sure that the mounting pads of the isolator on the printed circuit board do not reduce this distance. Creepage and clearance on a printed circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

UL	
UL 1577 Component Recognition Program	Certified according to IEC 62368-1 CB
File number: E181974	Certificate number: US-43893-M1-UL

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6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input current (side 1)(1)	T_J = 165°C, T_A = 25°C, see *Thermal Derating Curve, Side 1*.			80	A_{RMS}
I_S	Safety input, output, or supply current (side 2)(1)	V_I = 5V, T_J = 165°C, T_A = 25°C, see *Thermal Derating Curve, Side 2*.			1.35	
P_S	Safety input, output, or total power(1)	T_J = 165°C, T_A = 25°C, see *Thermal Derating Curve, Both Sides*.			6.8	W
T_S	Safety temperature(1)				165	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S must not be exceeded. These limits vary with the ambient temperature, T_A as shown in the *Safe Operating Area* section when used in the *TMCS-ADAPTER-EVM*.

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6.9 Electrical Characteristics

at T_A = 25°C, V_S = 5V on TMCS1236Axx, V_S = 3.3V on (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
R_{IN}	Input Conductor Resistance	IN+ to IN–		0.7		mΩ
R_{IN}	Input Conductor Resistance Temperature Drift	T_A= –40ºC to 125ºC		2.1		µΩ/°C
$I_{IN,MAX}$	Maximum Continuous Input Current(1)	T_A= 25ºC		80		A_{RMS}
		T_A= 125ºC		44		
Sensitivity: 30.8mV/A						
S_G	Sensitivity			30.8		mV/A
$S_{driftG,therm}$	Sensitivity Error Over Temperature (7)(10)	0.05V ≤ V_{OUT} ≤ V_S − 0.2V, T_A = 25°C to 125°C		±1	±2.6	%
	Sensitivity Error Over Temperature ±3σ (6)(7)				±1.5	
	Sensitivity Error Over Temperature (7)(10)	0.05V ≤ V_{OUT} ≤ V_S − 0.2V, T_A = −40°C to 25°C		±1	±2.6	
	Sensitivity Error Over Temperature ±3σ (6)(7)				±1.5	
$V_{OEG,\ drift\ therm}$	Output Voltage Offset Thermal Drift (7)	$V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±15	±30	µV/°C
V_{OEG}	Output Voltage Offset Error	$V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A		±0.2	±1.5	mV
$PSRR_{G,\ mA}$	Power Supply Rejection Ratio	Input Referred, V_S = 3V to 5.5V, T_A= –40ºC to 125ºC		±6	±42	mA/V
OC_{HYSG}	Over Current Hysteresis			3.6		A
OUTPUT						
e_{NL}	Nonlinearity Error	V_{OUT} = 0.1V to V_S – 0.1V		±0.1		%
$S_{drift,\ life}$	Sensitivity Lifetime Drift(2)	0.05V ≤ V_{OUT} ≤ V_S − 0.2V		±0.7	±1	%
	Sensitivity Lifetime Drift ±3σ (6)				±0.8	
$V_{OUT,0A}$	Zero Current Output Voltage	TMCS1236Axx, I_{IN} = 0A		2.5		V
$I_{OS,\ drift,\ life}$	Offset Lifetime Drift(2)	Input Referred, ($V_{OUT,0A}$ − V_{REF}) / S, I_{IN} = 0A		±10	±43	mA
	Offset Lifetime Drift ±3σ (6)				±23	
CMTI	Common Mode Transient Immunity (3)(7)	Step V_{CM} = 1000V, ΔV_{OUT} < 200mV, 1µs		150		kV/µs
CMRR	Common Mode Rejection Ratio	Input Referred, DC to 60Hz		13		µA/V
CMFR	Common Mode Field Rejection (7)	Uniform External Magnetic Field, Input Referred, DC to 1kHz		3		mA/mT
	Input Noise Density (11)	Input Referred, Full Bandwidth		86		µA/√Hz
$C_{L,MAX}$	Maximum Capacitive Load	VOUT to GND		4.7		nF
	Short Circuit Output Current	VOUT short to GND, short to V_S		50		mA
$Swing_{VS}$	Swing to V_S Power Supply Rail	R_L = 10kΩ to GND, T_A= –40ºC to 125ºC		V_S – 0.02	V_S – 0.05	V
$Swing_{GND}$	Swing to GND			5	10	mV
BANDWIDTH & RESPONSE						
BW	Analog Bandwidth	- 3dB Gain		4		MHz
SR	Slew Rate(4)(7)	Output rate of change between reaching 10% and 90% of final value as shown in *Figure 7-3* with a 100ns input step and >1.5V output transition	2	5		V/µs
t_r	Response Time(4)(7)	Time between input and output reaching 90% of final values, as shown in *Figure 7-3* with a 100ns input step and a 1V output transition		200	350	ns
t_{pd}	Propagation Delay(4)(7)	Time between input and output reaching 10% of final values as shown in *Figure 7-3* with a 100ns input step and a 1V output transition		100	150	ns
	Current Overload Recovery Time			300		ns
INTEGRATED REFERENCE						
V_{REF}	Reference Output Voltage	TMCS1236Axx	2.49	2.5	2.51	V
	Reference Output Thermal Drift(7)	TMCS1236Axx		18	76	µV/°C
	Reference Output Lifetime Drift(2)			±3.6	±12.2	mV
	Maximum Reference Output Capacitive Load			6		nF

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at T_A = 25°C, V_S = 5V on TMCS1236Axx, V_S = 3.3V on (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Reference Output Voltage Load Regulation	V_{REF} load = -5mA, 0mA, 5mA		0.25		mV/mA
OVER CURRENT DETECTION						
V_{OC}	Over Current Detection Threshold Voltage	V_{OC} = S x I_{OC} / 2	0.3		V_S	V
R_{OC}	Over Current Input Impedance		120			kΩ
	Over Current Threshold Error (7)(8)	T_A = –40°C to 125°C		±2	±10	%
	Over Current Detection Response Time (8)(9)	I_{IN} step = 120% of I_{OC}. OC Default MASK Time = 0		75	200	ns
t_{MASK}	Over Current Detection MASK Time (5)	TMCS1236xxN, I_{IN} step = 120% of I_{OC}, MASK Time = N x 0.25µs		0.25		µs
I_{OC_sink}	Over Current Pin Sink Current (7)	OC fault asserted		3	10	mA
$\overline{OC}_{,OL}$	$\overline{OC}$ Pin Pull-down Voltage	I_{OL} = 3mA. T_A = –40°C to 125°C	GND	0.07	0.2	V
POWER SUPPLY						
V_S	Supply Voltage	T_A = –40ºC to 125ºC	3.0		5.5	V
I_Q	Quiescent Current	T_A = 25ºC		12	16	mA
		T_A = –40ºC to 125ºC			16.5	mA
	Power On Time	Time from V_S > 3V to valid output (internal OTP is loading before 1ms)		1		ms
OC Ready	Power on Over Current Comparator Ready Time	Time from V_S > 3V to ready for OC detection		2		ms

(1) Thermally limited by junction temperature, see *Absolute Maximum Ratings*. Applies when device mounted on *TMCS-ADAPTER-EVM*. For more details, see the *Safe Operating Area* section.
(2) Lifetime and environmental drift specifications based on AEC-Q100 qualification stress test results. Typical values are population mean +1σ from worst case stress test condition. Maximum values are tested device population mean ±6σ. Devices tested in AEC-Q100 qualification stayed within maximum limits after TC, HTOL, uHAST and HTSL stress.
(3) Refer to the *Common-Mode Transient Immunity* section for details on common-mode transient response.
(4) Refer to the *Transient Response Parameters* section for details on transient response of the device.
(5) Refer to the *Overcurrent Detection MASK Time* section for details on the overcurrent response time with MASK.
(6) Informational mean ± 3σ values represent 99.73% of the device population based on initial characterization.
(7) Guaranteed by characterization.
(8) Over current threshold are bench characterized with step DC current input.
(9) Excluding magnetic coupling from layout deviation from recommended layout. See the *Layout* section for more information.
(10) Sensitivity error over temperature are characterized at 4A.
(11) Refer to the *Optional Filter* section for details on bandwidth vs noise RMS.

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6.10 Typical Characteristics

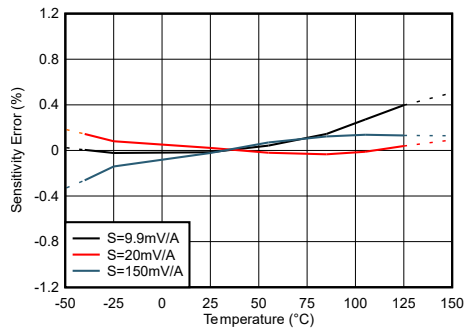


Figure 6-1. Sensitivity Error vs Temperature

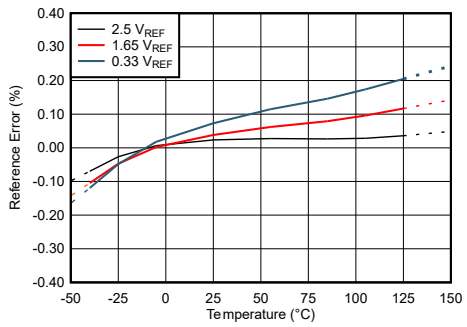


Figure 6-2. Reference Error vs Temperature

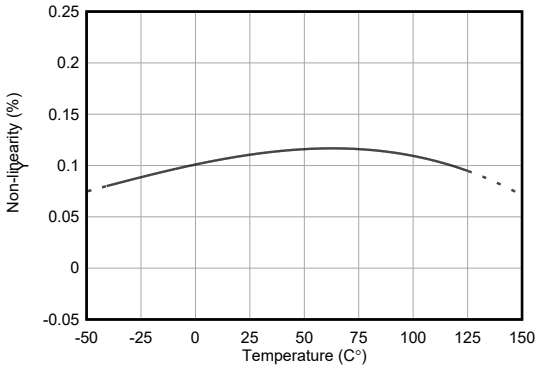


Figure 6-3. Non-Linearity vs Temperature

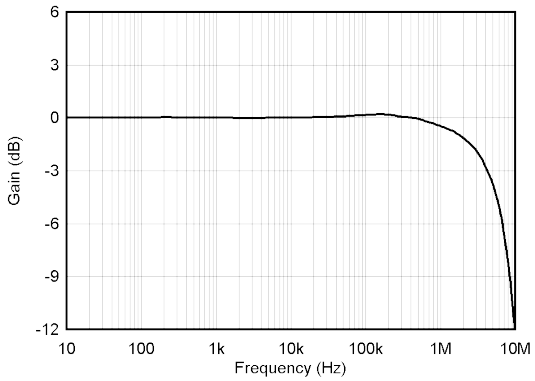


Figure 6-4. Sensitivity vs Frequency, All Gains Normalized to 1Hz

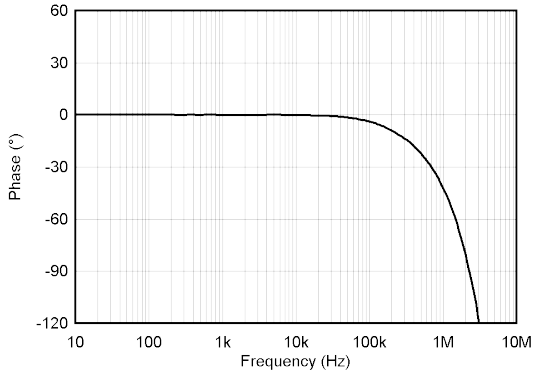


Figure 6-5. Phase vs Frequency, All Gains

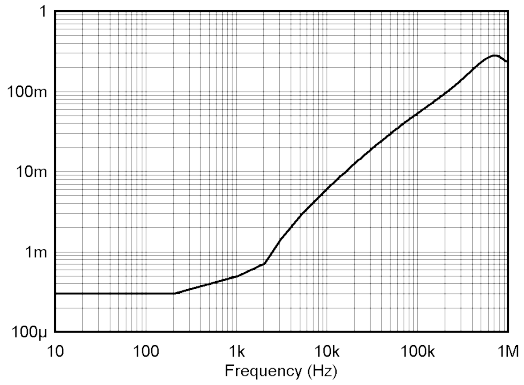


Figure 6-6. PSRR vs Frequency

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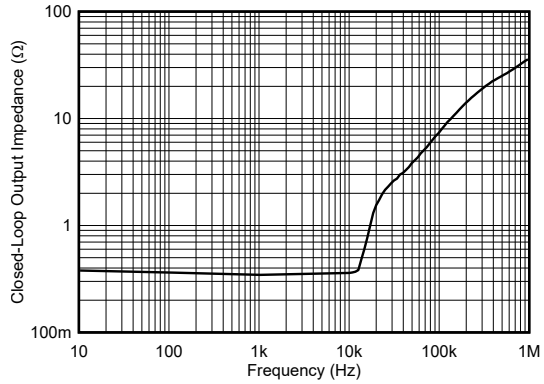


Figure 6-7. Output Impedance vs Frequency

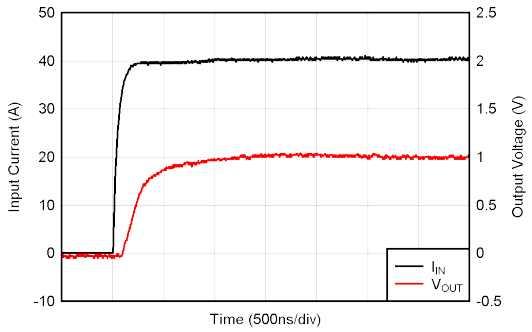


Figure 6-8. Voltage Output Step Response, Rising

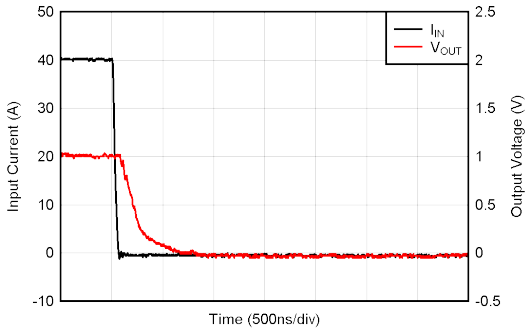


Figure 6-9. Voltage Output Step Response, Falling

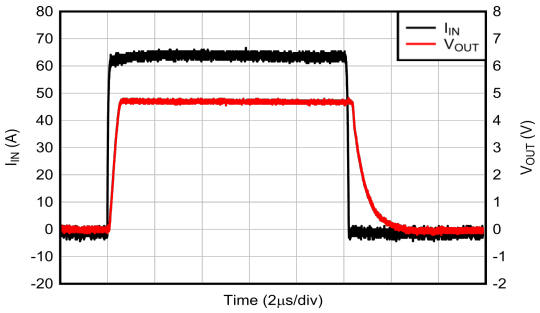


Figure 6-10. Current Overload Response

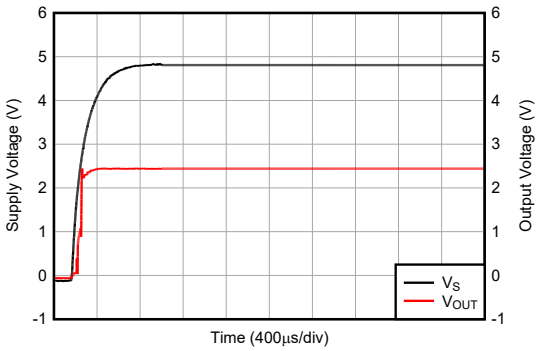


Figure 6-11. Startup Transient Response

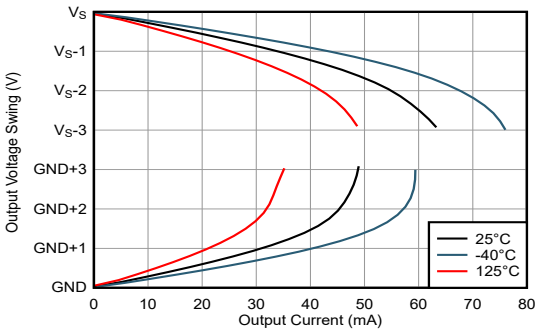


Figure 6-12. Output Swing vs Output Current

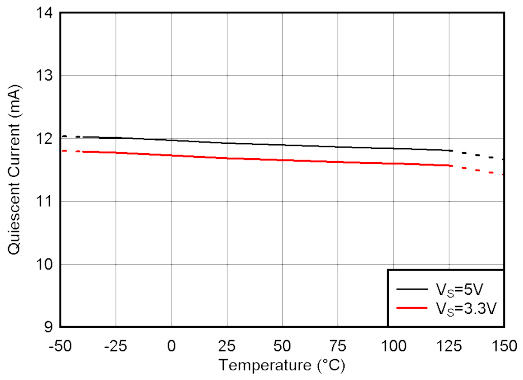


Figure 6-13. Quiescent Current vs Temperature

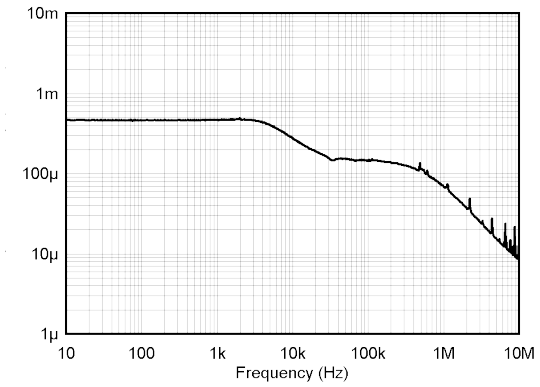


Figure 6-14. Input-Referred Noise Density vs Frequency

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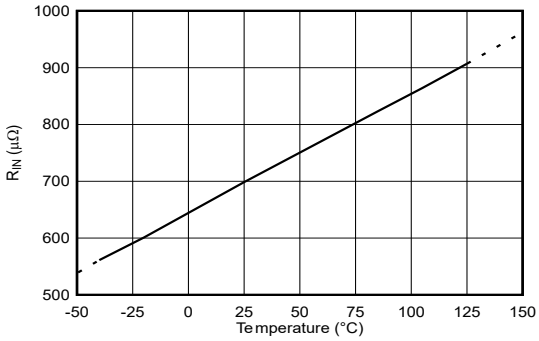


Figure 6-15. Input Conductor Resistance vs Temperature

6.10.1 Insulation Characteristics Curves

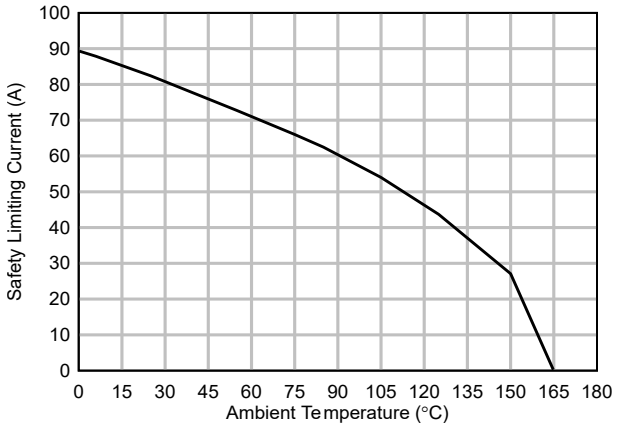


Figure 6-16. Thermal Derating Curve for Safety-Limiting Current, Side 1

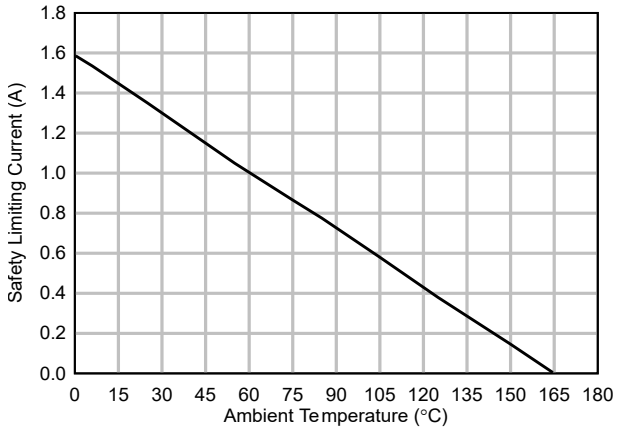


Figure 6-17. Thermal Derating Curve for Safety-Limiting Current, Side 2

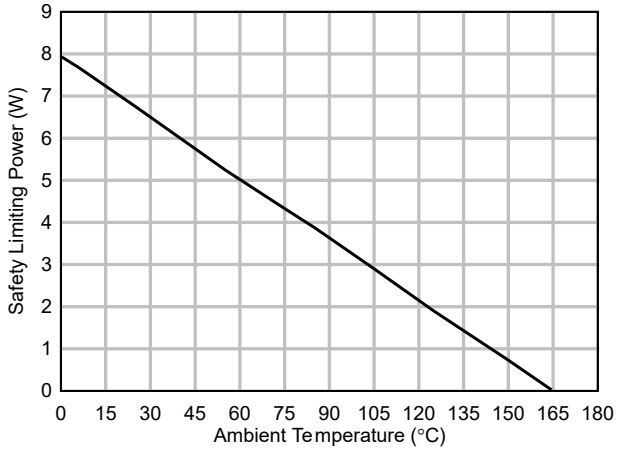


Figure 6-18. Thermal Derating Curve for Safety-Limiting Power

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7 Parameter Measurement Information

7.1 Accuracy Parameters

The ideal first-order transfer function of the TMCS1236-Q1 is given by Equation 1, where the output voltage is a linear function of input current. The accuracy of the device is quantified both by the error terms in the transfer function parameters, as well as by nonidealities that introduce additional error terms not in the simplified linear model.

$$V_{OUT} = (I_{IN} \times S) + V_{REF} \quad (1)$$

where

- V_{OUT} is the analog output voltage.
- I_{IN} is the isolated input current.
- S is the sensitivity of the device.
- V_{REF} is the zero current reference output voltage for the device variant.

7.1.1 Sensitivity Error

Sensitivity is the proportional change in the sensor output voltage due to a change in the input conductor current. This sensitivity is the slope of the first-order transfer function of the sensor (see Figure 7-1). The sensitivity of the TMCS1236-Q1 is tested and calibrated at the factory for high accuracy.

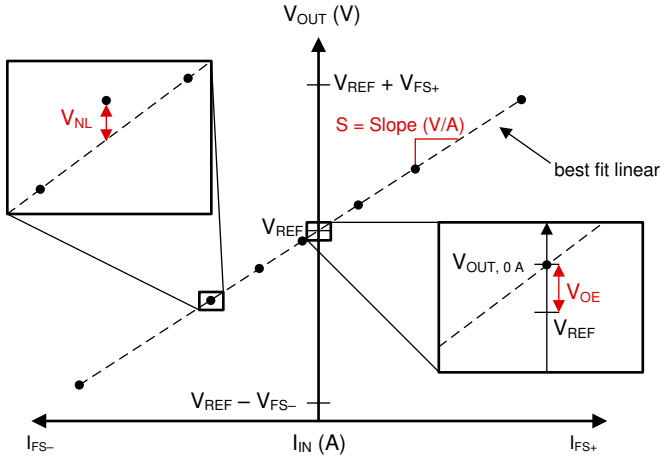


Figure 7-1. Sensitivity, Offset, and Nonlinearity Error

Sensitivity error e_S is the deviation from ideal sensitivity and is defined in Equation 2 as the variation of the best-fit measured sensitivity from the ideal sensitivity.

$$e_S = \frac{(S_{fit} - S_{ideal})}{S_{ideal}} \quad (2)$$

where

- e_S is the sensitivity error.
- S_{fit} is the best fit sensitivity.
- S_{Ideal} is the ideal sensitivity.

Sensitivity thermal drift $S_{drift,therm}$ is the change in sensitivity with temperature and is reported in percentage.

Sensitivity lifetime drift $S_{drift,life}$ is the change in sensitivity due to operational and environmental stresses over the entire lifetime of the device, and is reported as a worst-case percentage change in sensitivity over lifetime at 25°C.

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7.1.2 Offset Error and Offset Error Drift

Offset error is the deviation from the ideal output with zero input current and most often limits measurement accuracy at low input current levels. Offset error can be referred to the output as offset voltage error or referred to the input as offset current error. When divided by device sensitivity, S, output voltage offset error V_{OE} is input referred as input current offset error I_{OS} (see Equation 3). Offset error referred to the input (RTI) allows for more direct comparisons or offset error with input current. Regardless of whether offset error is referred to the input as current offset error I_{OS}, or to the output as voltage offset error V_{OE}, offset error is a single error source and must only be included once in either input-referred or output-referred error calculations.

$$I_{OS} = \frac{V_{OE}}{S} \tag{3}$$

As shown in Figure 7-1, the output voltage offset error V_{OE} of the TMCS1236-Q1 is the difference between the zero current output voltage $V_{OUT,0A}$ and the zero current output reference voltage V_{REF} (see Equation 4).

$$V_{OE} = V_{OUT,\,0A} - V_{REF} \tag{4}$$

The output offset error V_{OE} includes magnetic offset error in the Hall sensor and offset voltage error in the signal chain. The internal zero current output reference voltage is brought out to pin VREF so that errors in the internal reference voltage as well as errors introduced at the system level can be removed.

Offset drift is the change in the offset as a function of temperature T. Output offset drift is reported in µV/°C. To calculate offset error at any given temperature, multiply the offset drift by the change in temperature and add that value to the offset error at 25°C (see Equation 5).

$$V_{OE,\,\Delta T} = V_{OE,\,25°C} + \left(V_{OE,\,drift} \times \Delta T\right) \tag{5}$$

where

- $V_{OE,drift}$ is the output voltage offset drift with temperature in µV/°C.
- ΔT is the change in device temperature from 25°C.

7.1.3 Nonlinearity Error

Nonlinearity is the deviation of the output voltage from a linear relationship to the input current. Nonlinearity voltage, as shown in Figure 7-1, is the maximum voltage deviation from the best-fit line based on measured parameters (see Equation 6).

$$V_{NL} = V_{OUT,\,meas} - \left[\left(I_{meas} \times S_{fit}\right) + V_{OUT,\,0A}\right] \tag{6}$$

where

- $V_{OUT,meas}$ is the voltage output at maximum deviation from best fit.
- I_{meas} is the input current at maximum deviation from best fit.
- S_{fit} is the best-fit sensitivity of the device.
- $V_{OUT,0A}$ is the device zero current output voltage.

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Nonlinearity error for the TMCS1236-Q1 is specified as a percentage of the full-scale output range, V_{FS} (see Equation 7).

$$e_{NL} = \frac{V_{NL}}{V_{FS}} \quad (7)$$

7.1.4 Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) is the change in device offset due to variations in supply voltage. Use Equation 8 to calculate input referred offset errors caused by supply variations on 5V or 3.3V variant.

$$e_{PSRR,\,A} = \text{PSRR} \times (V_S - 5V) \quad (8)$$

$$e_{PSRR,\,B} = e_{PSRR,\,C} = \text{PSRR} \times (V_S - 3.3V) \quad (9)$$

where

- PSRR is the input referred power supply rejection ratio in mA/V.
- V_S is the operational supply voltage.

7.1.5 Common-Mode Rejection Ratio

Common-mode rejection ratio (CMRR) quantifies the effective input current error due to varying voltage on the isolated input of the device. Due to magnetic coupling and galvanic isolation of the current signal, the TMCS1236-Q1 has very high rejection of input common-mode voltage. Use Equation 10 to calculate the error contribution from the input common-mode voltage V_{CM}.

$$e_{CMRR} = \text{CMRR} \times V_{CM} \quad (10)$$

where

- CMRR is the input-referred common-mode rejection in µA/V.
- V_{CM} is the operational AC or DC voltage on the input of the device.

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7.1.6 Optional Filter for Reduced Bandwidth and Noise

An optional RC filter at the sensor output can reduce the effective signal bandwidth and high-frequency noise. The filter RC component values and corresponding input-referred noise (IRN) reduction are list in Table 7-1. The filter configuration is shown in Figure 7-2. Select the appropriate RC values based on the required system bandwidth and noise performance.

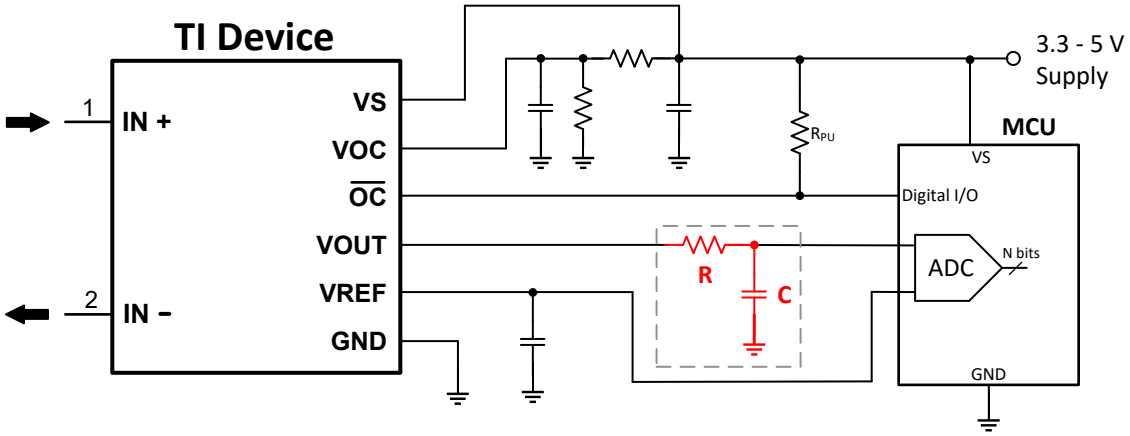


Figure 7-2. Application Diagram

Table 7-1. Example Application Design Requirements

Bandwidth [Hz]	R [Ohm]	C [nF]	IRN [mArms]
4M	N/A	N/A	217
1M	100	1.5	175
500k	220	1.5	145
250k	220	3.3	113
100k	470	3.3	79

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7.2 Transient Response Parameters

Critical TMCS1236-Q1 transient step response parameters are shown in Figure 7-3. Propagation delay, t_{pd}, is the time period between the input current waveform reaching 10% of the final value and the output voltage, V_{OUT}, reaching 10% of the final value. Response time, t_r, is the time period between the input current reaching 90% of the final value and the output voltage reaching 90% of the final value, for an input current step sufficient to cause a 1V change in the output voltage. Slew rate, SR, is defined as the rate of change between the output voltage reaching 10% and 90% of the final value during the sufficiently fast input current step.

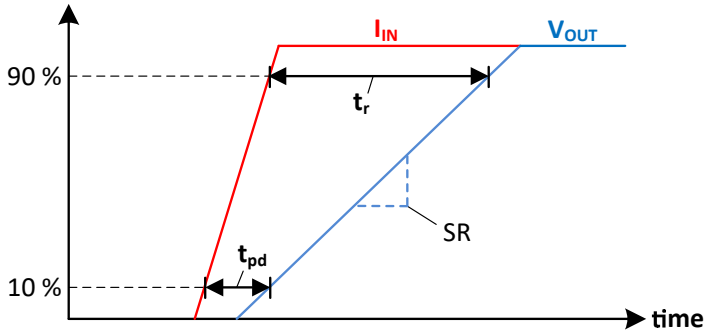


Figure 7-3. Transient Step Response

7.2.1 CMTI, Common-Mode Transient Immunity

CMTI is the capability of the device to tolerate a rising or falling voltage step on the input without coupling significant disturbance on the output signal. The device is specified for the maximum common-mode transition rate when the output signal does not experience a disturbance greater than 200mV lasting longer than 1µs, as shown in Figure 7-4 with a 150kV/µs common-mode input step. Higher edge rates than the specified CMTI can be supported with sufficient filtering or blanking time after common-mode transitions. For signal routing of the VREF and VOUT pins, use an 0402, X7R, 3.3nF capacitor from VOUT to GND and an 0402, X7R, 4.7nF capacitor from VREF to GND for rejecting CMTI disturbances.

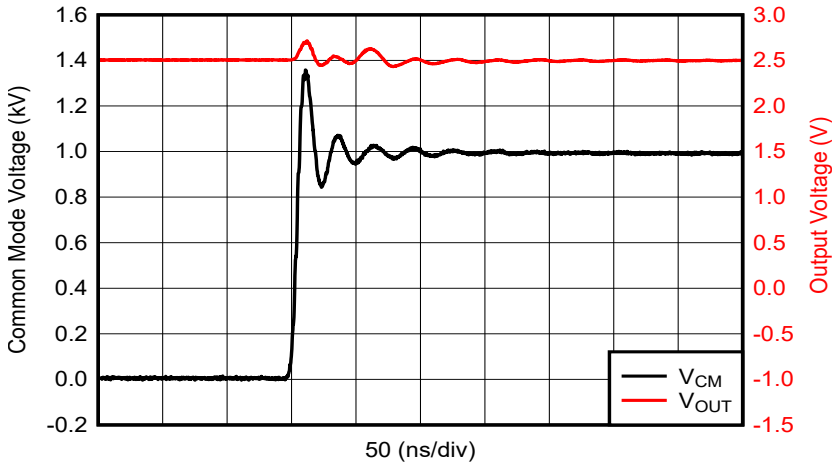


Figure 7-4. Common-Mode Transient Response

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7.3 Safe Operating Area

The isolated input current safe operating area (SOA) of the TMCS1236-Q1 is constrained by self-heating due to power dissipation in the input conductor. Depending upon the use case, the SOA is constrained by multiple conditions, including exceeding maximum junction temperature, Joule heating in the leadframe, or leadframe fusing under extremely high currents. These mechanisms depend greatly on input current amplitude and duration, along with ambient thermal conditions.

Current SOA strongly depends on the thermal environment and design of the system-level printed circuit board (PCB). Multiple thermal variables control the transfer of heat from the device to the surrounding environment, including air flow, ambient temperature, and PCB construction and design. All ratings are for a single TMCS1236-Q1 device mounted on the *TMCS-Adapter-EVM*, or equivalent PCB design with no air flow under specified ambient temperature conditions. Device use profiles must satisfy continuous current conduction SOA capabilities for the thermal environment planned for system operation.

7.3.1 Continuous DC or Sinusoidal AC Current

The longest thermal time constants of device packaging and PCBs are in the order of seconds; therefore, any continuous DC or sinusoidal AC periodic waveform with a frequency higher than 1Hz can be evaluated based on the RMS continuous-current levels. The continuous-current capability has a strong dependence upon the operating ambient temperature range expected in operation. Figure 7-5 shows the maximum continuous current-handling capability of the device when mounted on the *TMCS-Adapter-EVM*. Current capability falls off at higher ambient temperatures because of the reduced thermal transfer from junction-to-ambient and increased power dissipation in the leadframe. By improving the thermal design of an application, the SOA can be extended to higher currents at elevated temperatures see *PCB Thermal Analysis of In-Package Magnetic Current*. Using larger and heavier copper power planes, providing air flow over the board, or adding heat sinking structures to the area of the device can all improve thermal performance.

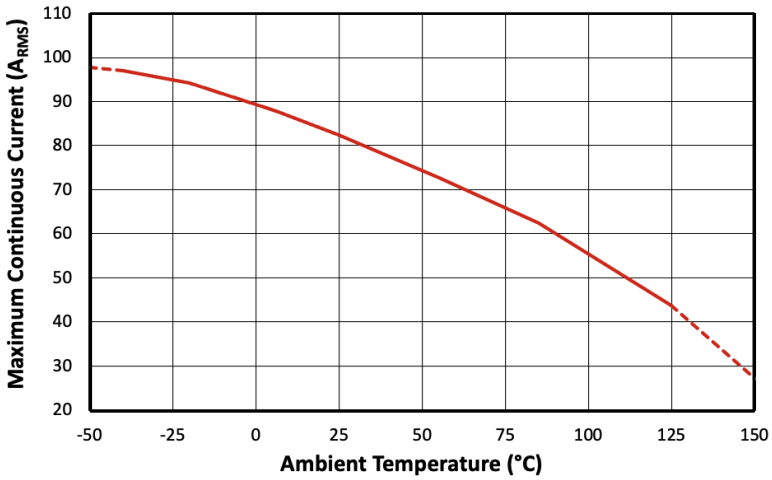


Figure 7-5. Maximum Continuous RMS Current vs Ambient Temperature

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7.3.2 Repetitive Pulsed Current SOA

For applications where current is pulsed between a high current and no current, the allowable capabilities are limited by short-duration heating of the leadframe. The TMCS1236-Q1 can tolerate higher current ranges under some conditions, however, for repetitive pulsed events, the current levels must satisfy both the pulsed current SOA and the RMS continuous current constraint. Pulse duration, duty cycle, and ambient temperature all impact the SOA for repetitive pulsed events. Figure 7-6, Figure 7-7, Figure 7-8, and Figure 7-9 illustrate repetitive stress levels based on test results from the *TMCS-Adapter-EVM* under which parametric performance and isolation integrity is not impacted post-stress for multiple ambient temperatures. At high duty cycles or long pulse durations, this limit approaches the continuous current SOA for a RMS value defined by Equation 11.

$$I_{IN,\ RMS} = I_{IN,\ P} \times \sqrt{D} \quad (11)$$

where

- $I_{IN,RMS}$ is the RMS input current level
- $I_{IN,P}$ is the pulse peak input current
- D is the pulse duty cycle

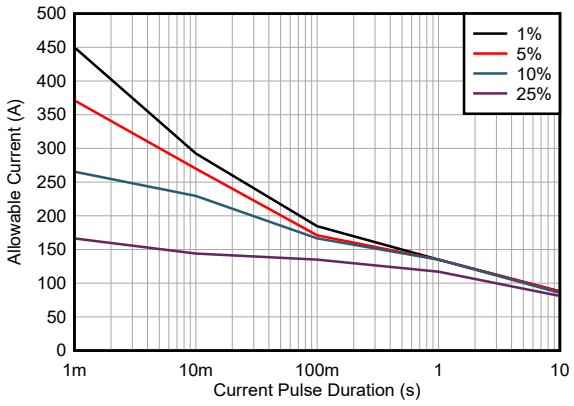


Figure 7-6. Maximum Repetitive Pulsed Current vs. Pulse Duration

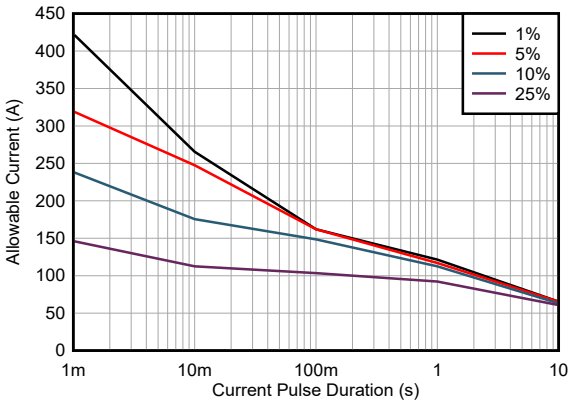


Figure 7-7. Maximum Repetitive Pulsed Current vs. Pulse Duration

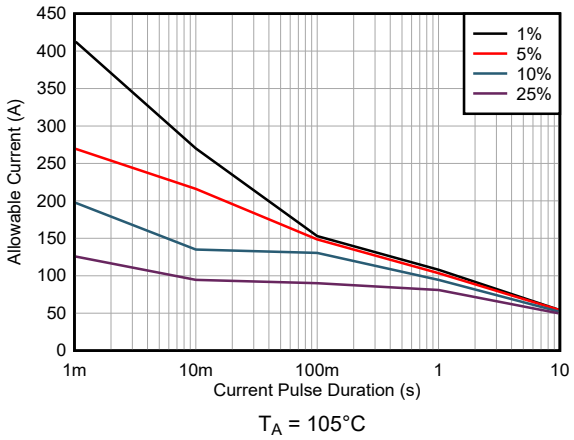


Figure 7-8. Maximum Repetitive Pulsed Current vs. Pulse Duration

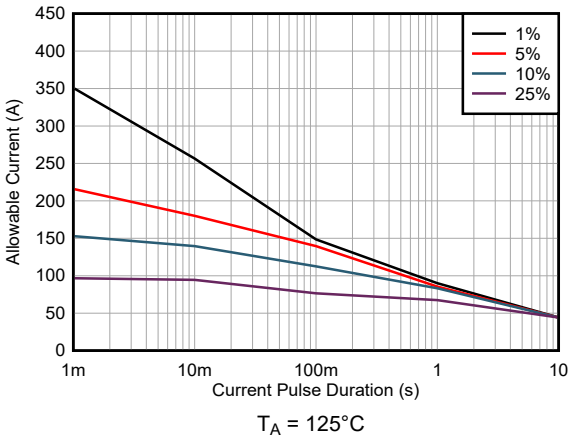


Figure 7-9. Maximum Repetitive Pulsed Current vs. Pulse Duration

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7.3.3 Single Event Current Capability

Single higher-current events that are shorter duration can be tolerated by the TMCS1236-Q1, because the junction temperature does not reach thermal equilibrium within the pulse duration. Figure 7-10 shows the short-circuit duration curve for the device for single current-pulse events, where the leadframe resistance changes after stress. This level is reached before a leadframe fusing event, but must be considered an upper limit for short duration SOA. For long-duration pulses, the current capability approaches the continuous RMS limit at the given ambient temperature.

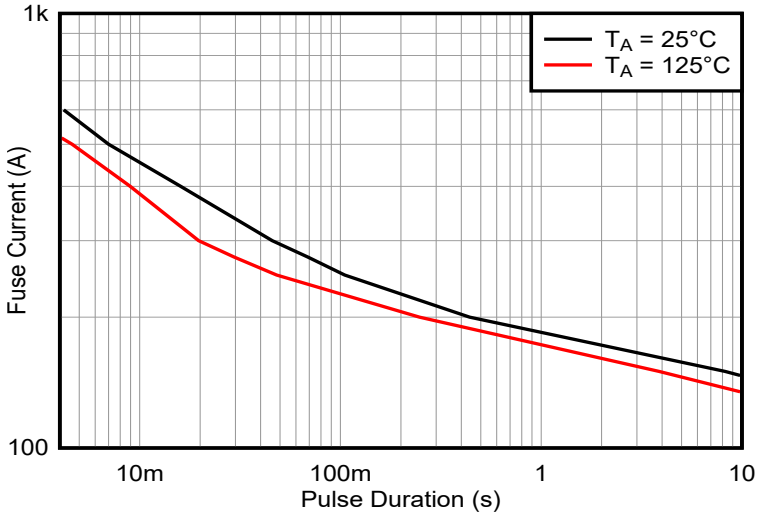


Figure 7-10. Single-Pulse Leadframe Capability

8 Detailed Description

8.1 Overview

The TMCS1236-Q1 is a precision Hall-effect current sensor, providing high levels of reliable reinforced isolation working voltage, ambient field rejection, and high current carrying capability. The input current flows through a conductor between the isolated input current pins. The conductor has a 0.7mΩ resistance at room temperature and accommodates up to 44A_{RMS} of continuous current at 125°C ambient temperature when used with printed circuit boards of comparable thermal design, such as the TMCS-Adapter-EVM. The low-ohmic leadframe path reduces power dissipation compared to alternative current measurement methodologies, and does not require any external passive components, isolated supplies, or control signals on the high-voltage side. The magnetic field generated by the input current is sensed by a Hall sensor and amplified by a precision signal chain. The device can be used for both AC and DC current measurements and has a high bandwidth of 4MHz. The TMCS1236-Q1 can operate with a low voltage supply ranging from 3V to 5.5V, and is optimized for switching systems.

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8.2 Functional Block Diagram

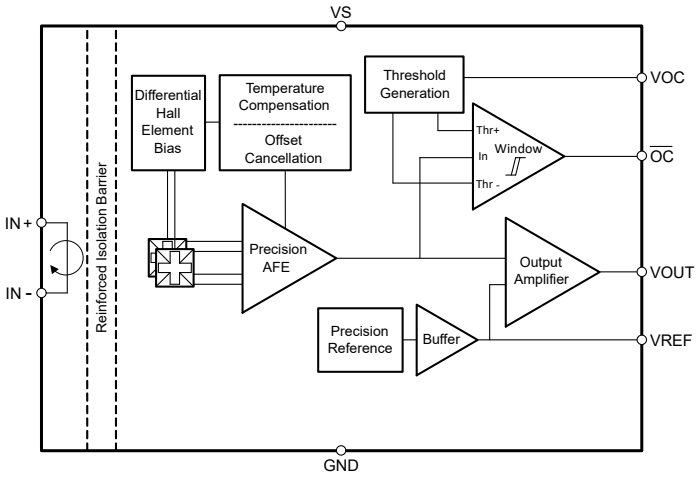


Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Current Input

Input current to the TMCS1236-Q1 passes through the isolated high-voltage side of the package leadframe into and out of the IN+ and IN– pins. The current flowing through the package generates a magnetic field that is proportional to the input current, which is measured by an integrated on-chip galvanically-isolated, precision Hall sensor. As a result of the electrostatic shielding on the Hall sensor die, only the magnetic field generated by the input current is measured, thus limiting input voltage switching pass-through to the circuitry. This configuration allows for direct measurement of currents with high-voltage transients without signal distortion on the current-sensor output. The leadframe conductor has a low resistance and a positive temperature coefficient as defined in the *Specifications*.

8.3.2 Input Isolation

The separation between the input conductor and the Hall sensor die due to the TMCS1236-Q1 construction provides inherent galvanic isolation between package pins 1 and 2 on the high-voltage input side, and package pins 3 through 10 on the low-voltage output side. Insulation capability is defined according to certification agency definitions and using industry-standard test methods as defined in *Insulation Specifications*. Assessment of device lifetime working voltages follow the IEC 60747-17 standard for basic and reinforced insulation, requiring time-dependent dielectric breakdown (TDDB) data-projection are based on projected failure rates of less than 1 part per million (ppm) for reinforced insulation and less than 1000ppm for basic insulation, and a minimum insulation lifetime of 30 years. For reinforced insulation, the IEC 60747-17 standard also requires additional safety margins of 20% for working voltage, and 50% for insulation lifetime, translating into a minimum required lifetime of 30 years at $800V_{RMS}$ for the TMCS1236-Q1.

Specifications shows the intrinsic capability of the isolation barrier to withstand high-voltage stress over the lifetime of the device. Based on the TDDB data, the intrinsic capability of these devices is $670V_{RMS}$ with a lifetime > 20 years. Other factors such as operating environment and pollution degree can further limit the working voltage of the component in an end system.

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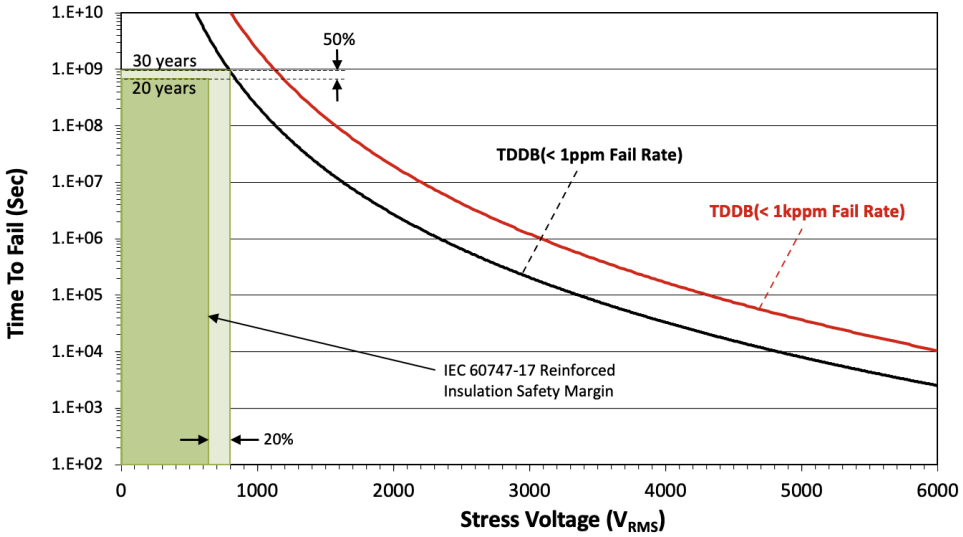


Figure 8-2. Insulation Lifetime

8.3.3 Ambient Field Rejection

The TMCS1236-Q1 is designed to provide high levels of current measurement accuracy in harsh environments. Immunity to interference from stray magnetic fields allows for use in close proximity to high current carrying traces, motor windings, inductors, or any other erroneous source of stray magnetic fields. The TMCS1236-Q1 incorporates differential Hall sensors that are strategically located and configured to reject interference from stray external magnetic fields. Ambient Field Rejection (AFR) limited only by Hall element matching and package leadframe coupling reduces errors from stray magnetic fields.

8.3.4 High-Precision Signal Chain

The TMCS1236-Q1 uses a precision, low-drift signal chain with proprietary sensor linearization techniques to provide a highly accurate and stable current measurement across the full temperature range and lifetime of the device. The device is fully tested and calibrated at the factory to account for any variations in either silicon processing, assembly, or packaging of the device. The full signal chain provides a fixed sensitivity voltage output that is proportional to the current flowing through the leadframe of the isolated input.

8.3.4.1 Temperature Stability

The TMCS1236-Q1 includes a proprietary temperature compensation technique which results in significantly improved parametric drift across the full temperature range. This compensation technique accounts for changes in ambient temperature change. A zero-drift signal chain architecture along with Hall sensor temperature compensation methods enable stable sensitivity while minimizing offset errors across temperature. System-level performance is drastically improved across required operating conditions.

8.3.5 Internal Reference Voltage

The TMCS1236-Q1 has a precision internal reference that determines the zero current output voltage, $V_{OUT,0A}$. Overall current sensing dynamic range can be optimized by choosing either of the three different zero current output voltage options listed in the *Device Comparison* table. These extremely low-drift precision zero current reference options are listed in Equation 12, Equation 13, and Equation 14. These equations are for precise bidirectional or unidirectional current measurements using various supply voltages ranging between 3.0V to 5.5V.

TMCS11xxAxx-Q1 ➔ $V_{OUT,0A} = V_{REF} = 2.5V$ (12)

TMCS11xxBxx-Q1 ➔ $V_{OUT,0A} = V_{REF} = 1.65V$ (13)

TMCS11xxCxx-Q1 ➔ $V_{OUT,0A} = V_{REF} = 0.33V$ (14)

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8.3.6 Current-Sensing Measurable Ranges

The zero current reference voltage, V_{REF}, along with device sensitivity, S, and supply voltage, V_S, determine the TMCS1236-Q1 linear input current measurement ranges listed in the *Device Comparison* table. The maximum linear output voltage, $V_{OUT,max}$, is limited to 100mV less than the supply voltage as shown in Equation 15. The minimum linear output voltage, $V_{OUT,min}$, is limited to 100mV above ground as shown in Equation 16.

$$V_{OUT,\,max} = V_S - 100mV \tag{15}$$

$$V_{OUT,\,min} = 100mV \tag{16}$$

Overall maximum dynamic range can be optimized with proper device selection by referring minimum and maximum linear output voltage swing to minimum and maximum linear input current range by dividing output voltage by sensitivity, S (see Equation 17 and Equation 18).

$$I_{IN,\,max+} = \frac{(V_{OUT,\,max} - V_{OUT,\,0A})}{S} \tag{17}$$

$$I_{IN,\,max-} = \frac{(V_{OUT,\,0A} - V_{OUT,\,min})}{S} \tag{18}$$

where

- $I_{IN,max+}$ is the maximum linear measurable positive input current.
- $I_{IN,max-}$ is the maximum linear measurable negative input current.
- S is the sensitivity of the device variant.
- $V_{OUT,0A}$ is the appropriate zero current output voltage.

8.3.7 Overcurrent Detection

In addition to the precision analog signal, the TMCS1236-Q1 also offers a fast digital overcurrent detection response. The Overcurrent Detection (OCD) circuit provides an open-drain comparator output that can be used to trigger a warning or initiate a system shutdown to prevent damage from excessive current flow caused by short circuits, motor stalls, or other unintended system conditions. This fast digital response can be configured on both bidirectional and unidirectional devices to assert based on a signal that is anywhere from half to over twice the full-scale analog measurement range.

Use of this fast digital output $\overline{OC}$ instead of the precision analog output VOUT to detect overcurrent events outside the nominal operating current range allows for higher dynamic range with higher sensitivity optimized for the nominal operating current range. Use of this fast digital output $\overline{OC}$ also allows for lower overall signal noise from lower analog signal bandwidth than often needed when using the analog signal chain to detect fast overcurrent events.

8.3.7.1 Setting The User Configurable Overcurrent Threshold

The desired overcurrent threshold, I_{OC}, is set by applying an external voltage, V_{OC}, to the VOC pin according to the following equation.

$$V_{OC} = \frac{S \times I_{OC}}{2} \tag{19}$$

where

- S is the device sensitivity in V/A.
- I_{OC} is the desired overcurrent threshold in A.
- V_{OC} is the voltage applied that sets the overcurrent threshold in V.

An example of how to set the desired overcurrent threshold, I_{OC}, is shown in Section 8.3.7.1.2. Regardless of which TMCS1236-Q1 sensitivity variant is chosen or which zero current output voltage option is selected, the above equation applies when calculating overcurrent threshold voltage V_{OC}. A digital-to-analog converter (DAC)

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can be used to set the desired overcurrent threshold I_{OC}, or a simple external resistor divider circuit can be used as shown in Section 8.3.7.1.1.

8.3.7.1.1 Setting Overcurrent Threshold Using Power Supply Voltage

A simple external resistor divider driven from the power supply as shown in Figure 8-3 can be used to generate the external overcurrent voltage V_{OC} applied to the VOC pin to set the desired overcurrent threshold I_{OC} according to the equation in Section 8.3.7.1.

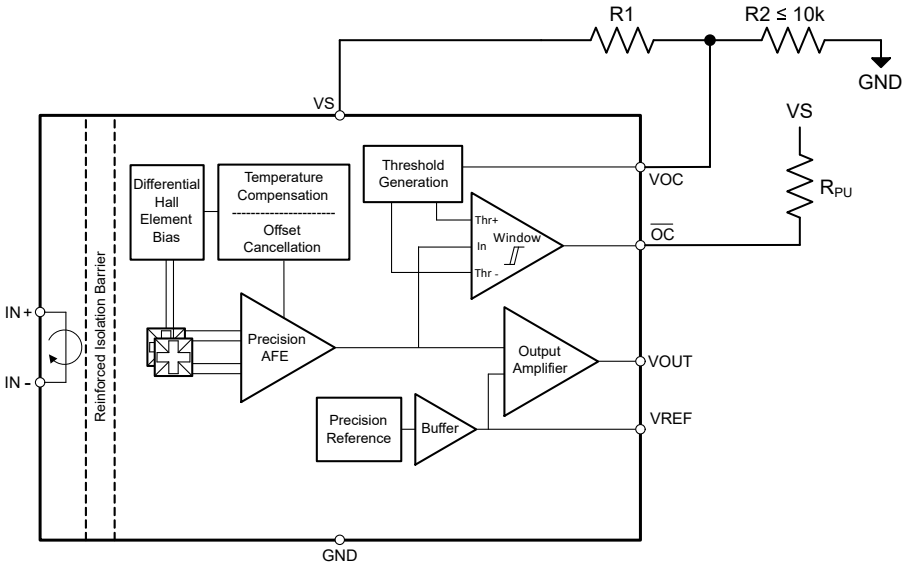


Figure 8-3. User Configurable Overcurrent Threshold Using Power Supply Voltage

When using a resistor divider as shown in Figure 8-3, R2 must be less than 10kΩ to mitigate the impact of the VOC input impedance on overcurrent threshold accuracy.

8.3.7.1.2 Setting Overcurrent Threshold Example

For example, to set a desired overcurrent threshold to I_{OC} = ±50A on a bidirectional devices with ±32A linear measurement range, as well as on the unidirectional device, size the resistors R1 and R2 to apply a voltage V_{OC} = 1.875V to the VOC pin according to the equation in Section 8.3.7.1.

with

- Assume device with sensitivity S = 0.075V/A.
- Desired overcurrent threshold, I_{OC} = ±50A.
- Applied overcurrent threshold voltage V_{OC} = 1.875V.

8.3.7.2 Overcurrent Output Response

Figure 8-4 shows the active-low overcurrent digital output $\overline{OC}$ response to bidirectional overcurrent events. When the input current exceeds $|\pm I_{OC}|$ on a bidirectional device, the fast $\overline{OC}$ pin is pulled low. The input current must return to within $\pm I_{OC}$ by more than a hysteresis current I_{Hys} before the $\overline{OC}$ pin resets back to the normal high-state.

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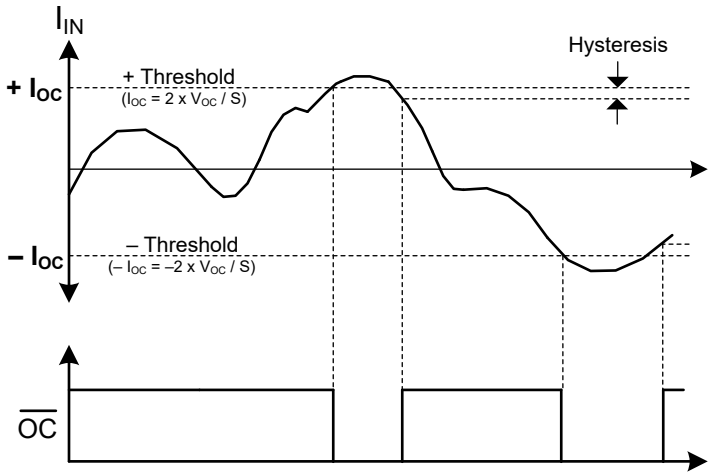


Figure 8-4. Overcurrent Output Response

8.3.7.3 Overcurrent Detection MASK Time

8.4 Device Functional Modes

8.4.1 Power-Down Behavior

As a result of the inherent galvanic isolation of the device, very little consideration must be paid to powering down the device, as long as the limits in the *Specifications* table are not exceeded on any pins. The isolated current input and the low-voltage signal chain can be decoupled in operational behavior, as either can be energized with the other shutdown, as long as the isolation barrier capabilities are not exceeded. The low-voltage power supply can be powered down while the isolated input is still connected to an active high-voltage signal or system.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The key feature sets of the TMCS1236-Q1 provide significant advantages in any application where an isolated current measurement is required.

- Galvanic isolation provides a high isolated working voltage and excellent immunity to input voltage transients.
- Hall-based measurement simplifies system level designs without the need for a power supply on the high-voltage (HV) side.
- An input current path through the low impedance conductor minimizes power dissipation.
- Excellent accuracy and low temperature drift eliminate the need for multipoint calibrations without sacrificing system performance.
- A wide operating supply range enables a single device to function across a wide range of voltage levels.

These advantages increase system-level performance while minimizing complexity for any application where precision current measurements must be made on isolated currents. Specific examples and design requirements are detailed in the following section.

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9.2 Typical Application

In many applications, power must be converted from AC sources for use in DC circuitry. Some type of controlled power factor correction (PFC) stage is typically needed to improve power transfer efficiency. Faster and faster power switches are being used in modern PFC stages to reduce overall size and to improve power transfer efficiency. Often, the PFC stage of AC to DC converters is connected directly to AC power grids. A primary challenge to sensing in PFC stages is that the current sensor is subjected to large voltage spikes coming from the high-voltage (HV) power grid along with large transients coming from high speed power switches during charge transfer. Inherent isolation in the TMCS1236-Q1 construction helps overcome these challenges by providing high levels of isolation between the HV current sensing nodes and low-voltage control circuitry, with high common-mode transient immunity (CMTI). Figure 9-1 shows the use of the TMCS1236-Q1 measuring phase currents in a common AC to DC converter stage.

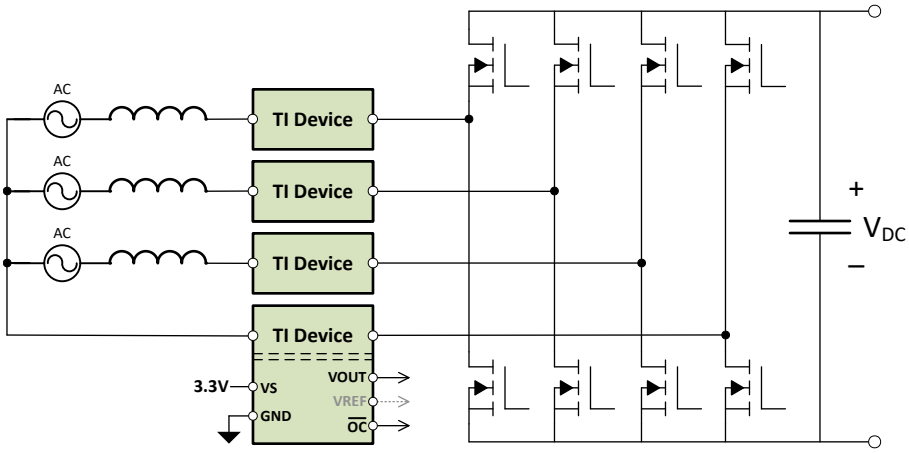


Figure 9-1. AC to DC Converter Current Sensing

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9.2.1 Design Consideration

Intermodulation distortion is a distortion product that arises when signals are applied to the input of a non-linear circuit utilizing a chopping topology, creating undesired frequency products that can interfere with the desired signal. The switching frequency of the chopping clock can interact with the frequency content of the input signal. To minimize this effect, in the TMCS1236-Q1 the internal oscillator frequency is increased to 1.1MHz, to enable operation with higher switching frequencies.

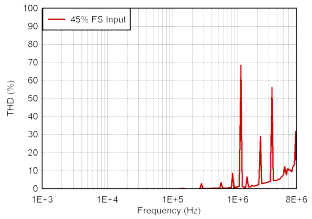


Figure 9-2. Distortion Over Frequency

The TMCS1236-Q1 employs a chopping signal chain to achieve low offset. A well-known characteristic of chopped architectures is that the periodic switching action of the internal chopper introduces intermodulation between the clock frequency (f_{CLK}) and the spectral content of the input signal. When the input current contains spectral energy near the chopper frequency or clock harmonics, mixing products are generated at frequencies $|n \times f_{CLK} +/- f_{IN}|$ for integer n. These tones can appear within the measurement band if not accounted for in the system frequency plan. To place the dominant intermodulation tones well above the signal frequencies of typical power-conversion applications, the internal oscillator is designed to operate at 1.1MHz. For distoration-sensitive application, Figure 9-2 characterizes THD versus input frequency for the 132mV/A device variant at 45% full-scale input. System designers should select an operating frequency plan that maintains adequate spectral separation and design margin between the input signal and the clock frequency and its harmonics. Additionally, the internal oscillator frequency is subject to normal process, voltage, and temperature variation.

9.2.2 Application Curve

To illustrate high levels of isolation achievable between noisy high-voltage current sensing nodes and low-voltage precision current measurement and control circuitry, Figure 9-3 shows the output signal from the TMCS1236-Q1 in a noisy in-phase PWM motor control example. In this example with a large induction motor under no load, no PWM edge interference is seen on the current sensor output with high-voltage PWM switching on the current sensor input, as is often pronounced on many current sensors.

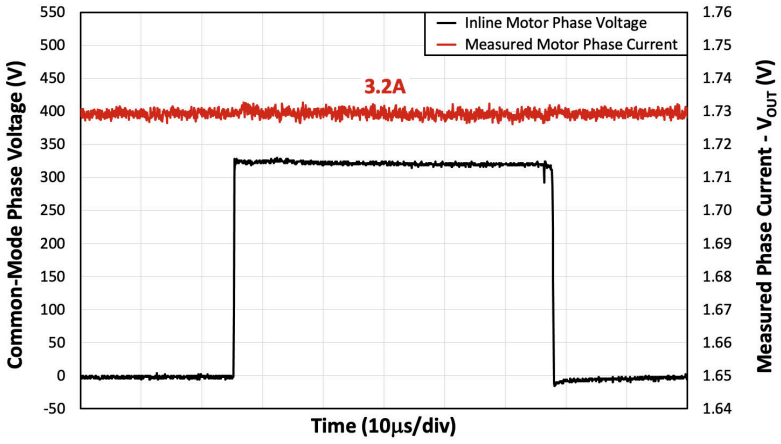


Figure 9-3. Inline Motor Current-Sense Input and Output Signals

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9.3 Power Supply Recommendations

The TMCS1236-Q1 only requires a power supply (V_S) on the low-voltage isolated side, which powers the analog circuitry independent of the isolated current input. V_S determines the full-scale output range of the analog output V_{OUT}, and can be supplied with any voltage between 3V and 5.5V. To filter noise in the power-supply path, place a low-ESR decoupling capacitor of 0.1µF between V_S and GND pins as close as possible to the supply and ground pins of the device. More decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. When used in extremely noisy environments, ferrite beads can be added close to the supply pin as shown in Figure 9-4 to target and suppress high-frequency noise coupled on to system supply.

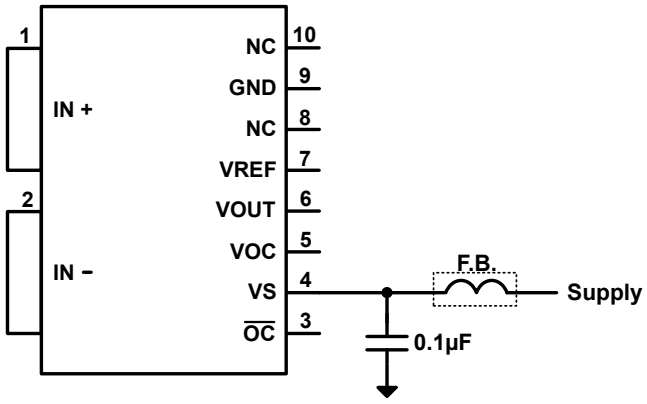


Figure 9-4. Power Supply Noise Filtering

The TMCS1236-Q1 power supply V_S can be sequenced independently of current flowing through the input. However, there is a power-on delay between V_S reaching the recommended operating voltage and the analog output validation. During this power-on time, the output voltage V_{OUT} can transition between GND and V_S as the output transfers from a high impedance reset state to the active drive state. If this behavior must be avoided, then provide a stable supply voltage V_S for longer than the power-on time prior to applying input current.

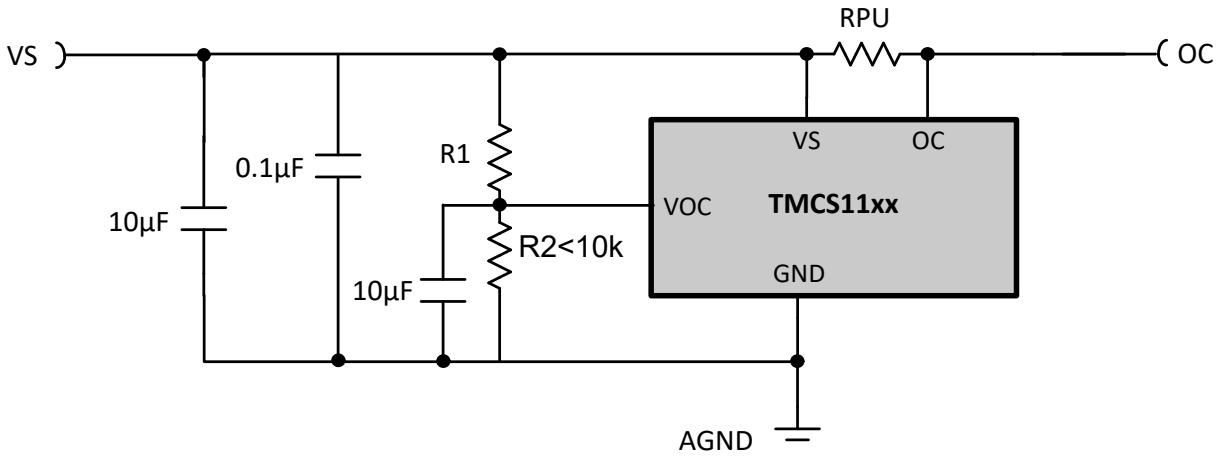


Figure 9-5. TMCS11xx Overcurrent Threshold Stability

9.4 Layout

9.4.1 Layout Guidelines

The TMCS1236-Q1 is specified for a continuous current handling capability on the *TMCS-Adapter-EVM* which uses 4oz copper planes. This current capability is fundamentally limited by the maximum device junction temperature and the thermal environment, primarily the PCB layout and design. To maximize current-handling capability and thermal stability of the device, take care with PCB layout and construction to optimize the

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thermal capability. Efforts to improve the thermal performance beyond the design and construction of the *TMCS-Adapter-EVM* can result in increased continuous-current capability due to higher heat transfer to the ambient environment. Keys to improving thermal performance of the PCB include:

- Use large copper planes for both input current path and isolated power planes and signals.
- Use heavier copper PCB construction.
- Place thermal via *farms* around the isolated current input.
- Provide airflow across the surface of the PCB.

9.4.2 Layout Example

An example layout, shown in Figure 9-6, is from the *TMCS-Adapter-EVM User's Guide*. Device performance is targeted for thermal and magnetic characteristics of this layout, which provides optimal current flow from the terminal connectors to the device input pins while large copper planes enhance thermal performance.

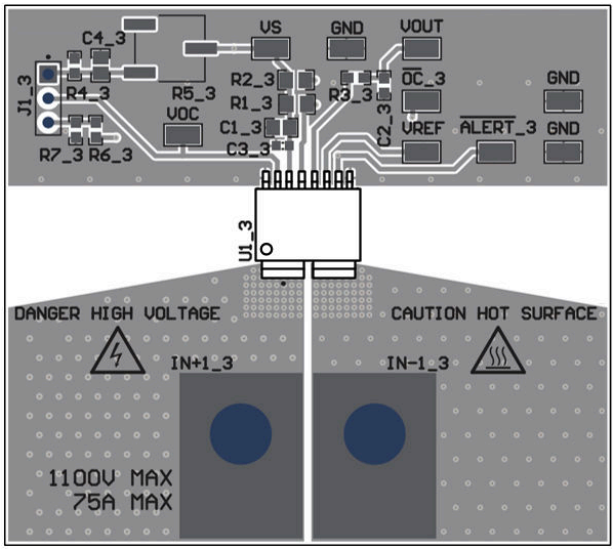


Figure 9-6. Recommended Board Layout

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
TMCS1236AGAQDVGRQ1	PROD	SOIC	DVG | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1236AGAQ1

(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

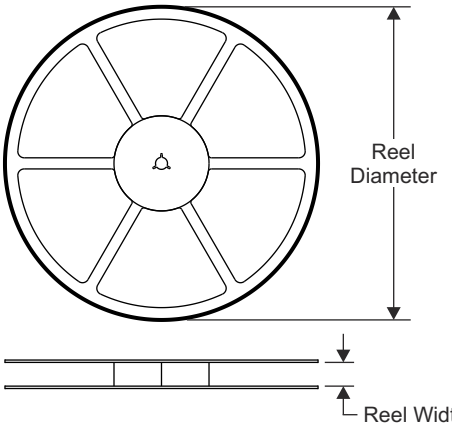
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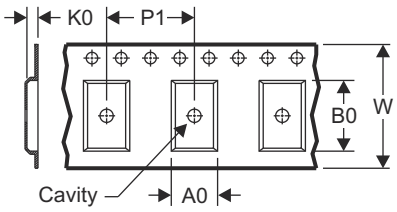
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11.1 Tape and Reel Information

REEL DIMENSIONS

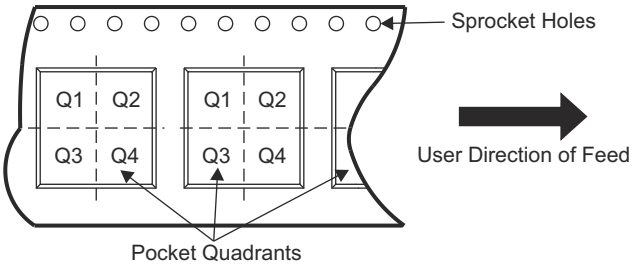


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

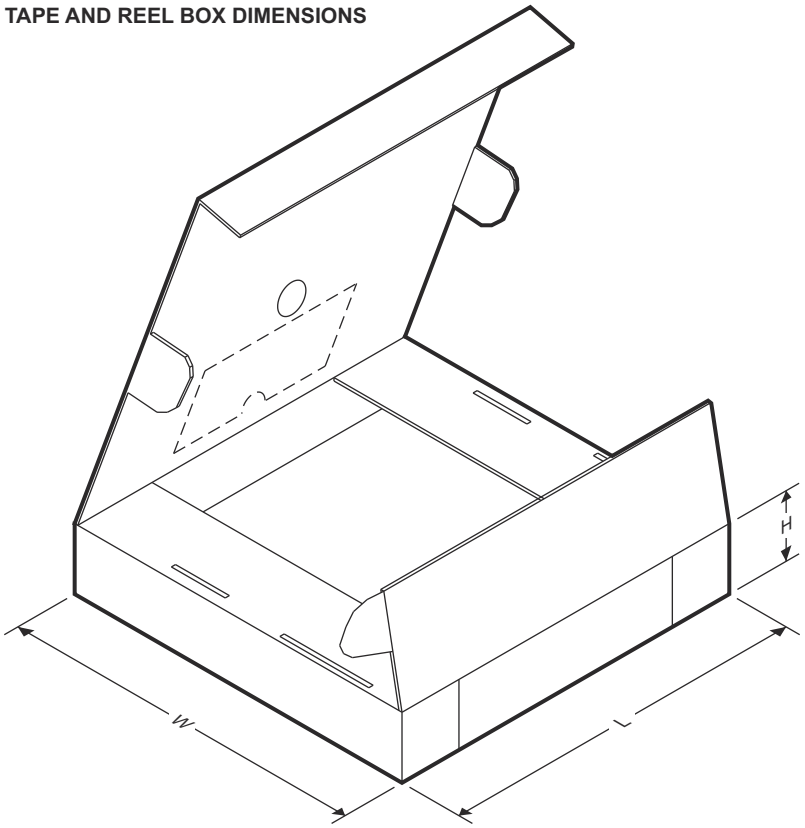
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMCS1236AGAQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	1236AGAQ1

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMCS1236AGAQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0

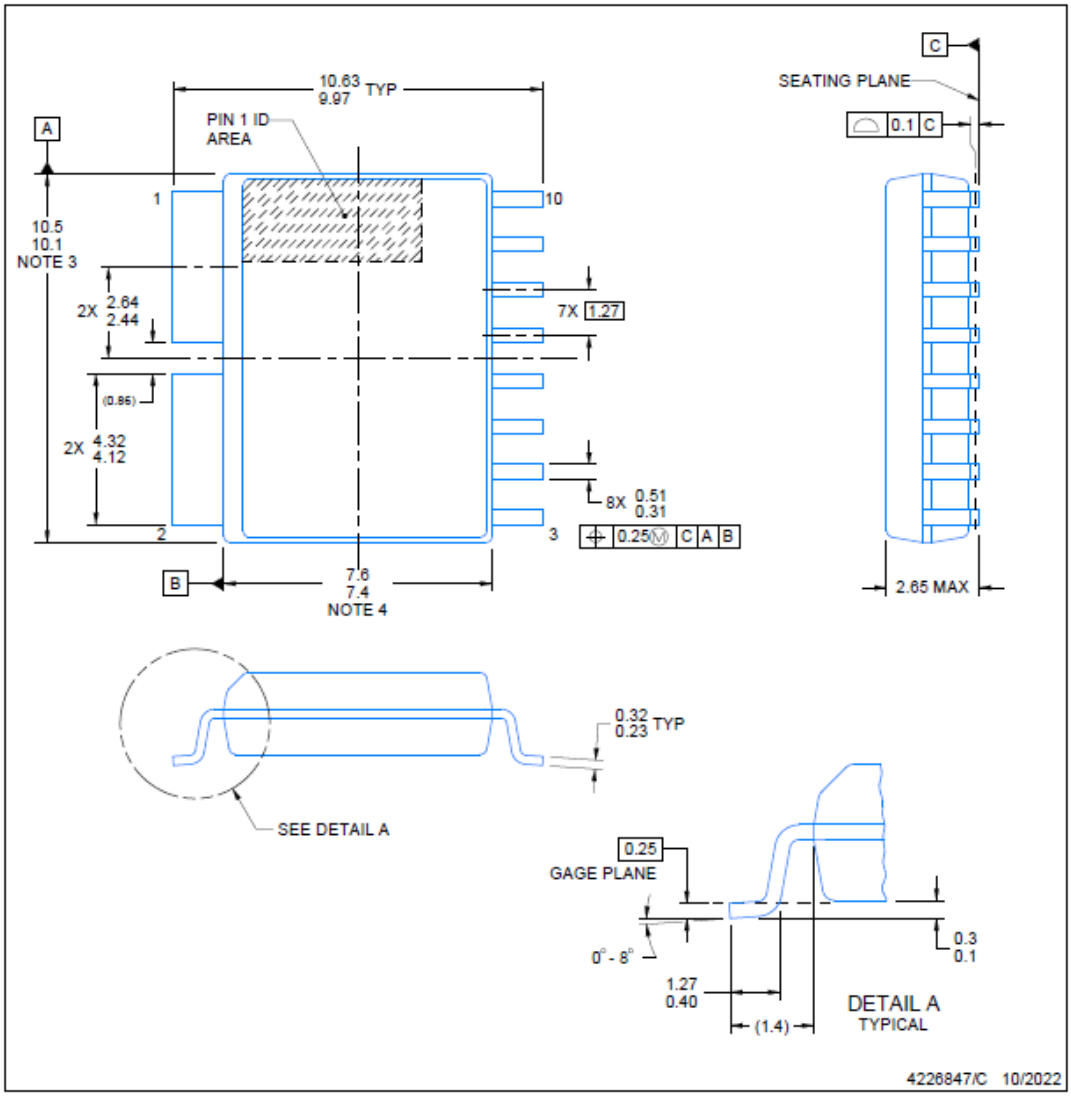
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11.2 Mechanical Data

PACKAGE OUTLINE

DVG0010A — **SOIC - 2.65 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

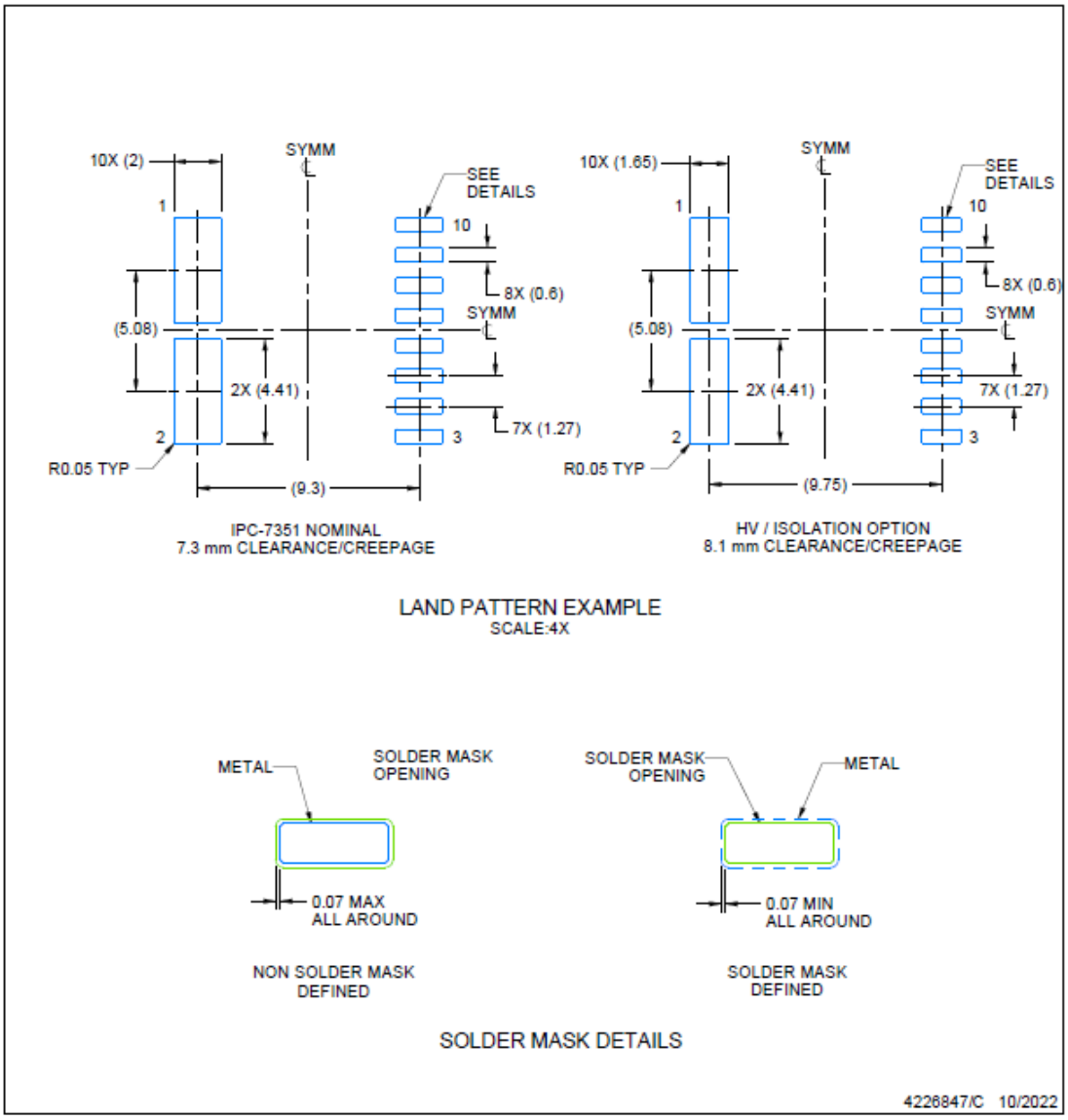
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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EXAMPLE BOARD LAYOUT

DVG0010A — **SOIC - 2.65 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

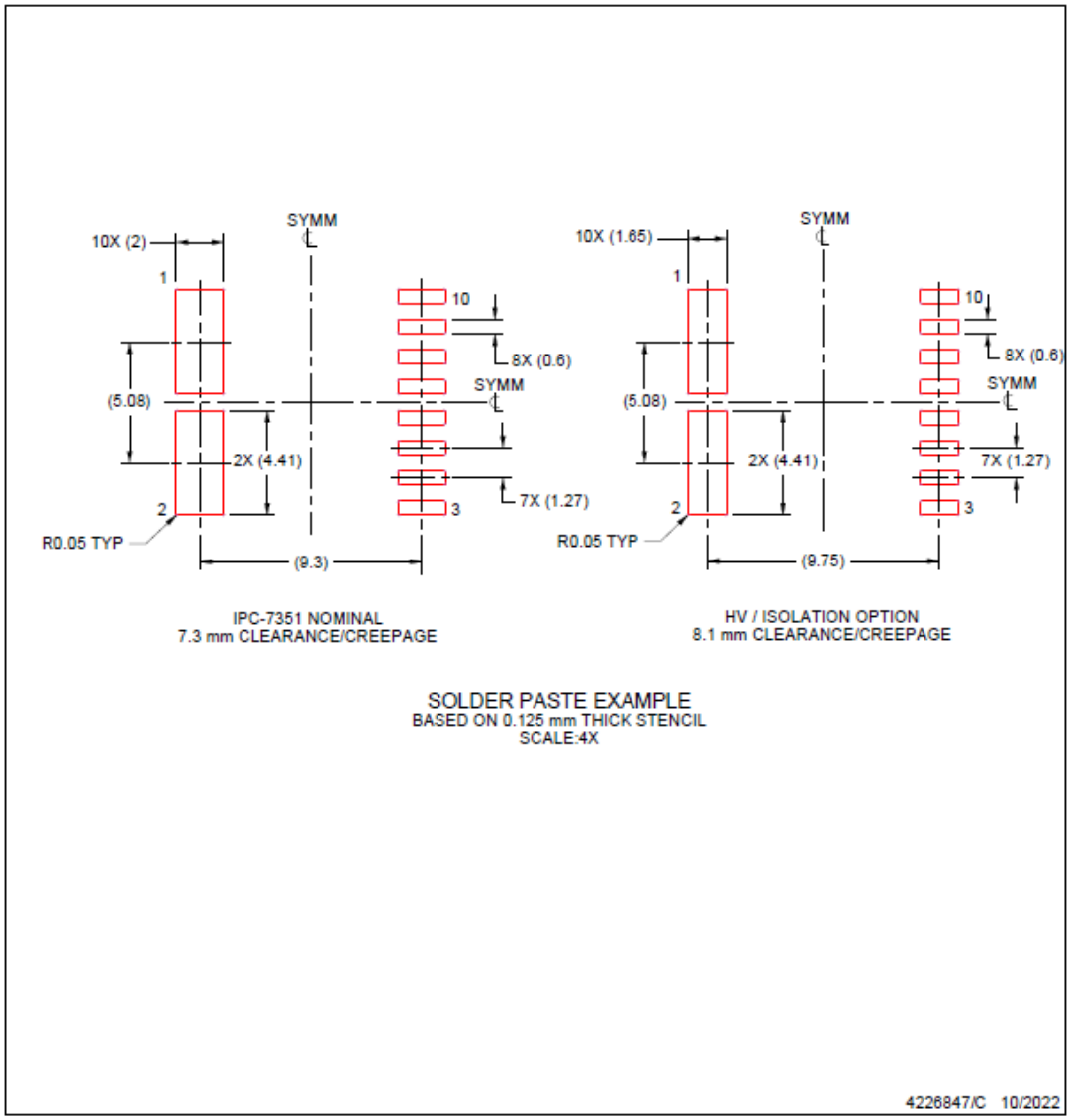
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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EXAMPLE STENCIL DESIGN

DVG0010A — **SOIC - 2.65 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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