PCA9518 Expandable Five-Channel I²C HUB

1 Features

- Expandable Five-Channel Bidirectional Buffer
- 400-kHz Fast I²C Bus
- Operating V_{CC} Range of 3 V to 3.6 V
- 5-V Tolerant I²C and Enable Input Pins to Support Mixed-Mode Signal Operation
- Active-High Individual Repeater Enable Inputs
- Open-Drain Input/Outputs
- Lockup-Free Operation
- Supports Multiple Masters
- Powered-Off High-Impedance I²C Pins
- I²C Bus and SMBus Compatible
- Latchup Performance Exceeds 100 mA Per JESD 78
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Description

The PCA9518 is an expandable five-channel bidirectional buffer for I²C and SMBus applications. The I²C protocol requires a maximum bus capacitance of 400 pF, which is derived from the number of devices on the I²C bus and the bus length. The PCA9518 overcomes this restriction by separating and buffering the I²C data (SDA) and clock (SCL) lines into multiple groups of 400-pF segments. Any segment-to-segment transition sees only one repeater delay. Each PCA9518 can communicate with other PCA9518 hubs through a 4-wire inter-hub expansion bus. Using multiple PCA9518 parts, any width hub (in multiples of five) can be implemented using the expansion pins, with only one repeater delay and no functional degradation of the system performance.

The PCA9518 does not support clock stretching across the repeater.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9518	SSOP (20)	7.20 mm × 5.30 mm
	SOIC (20)	12.80 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

DB, DBQ, DW, OR PW PACKAGE
(TOP VIEW)

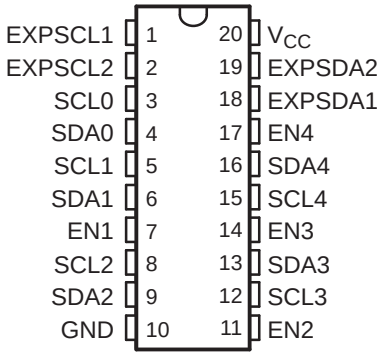


Table of Contents

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2010) to Revision C	Page
• Added Clock Stretching Errata section.	10

Changes from Revision A (June 2010) to Revision B	Page
• Deleted any references to clock stretching in the data sheet. This does not effect min/max specifications.	1

4 Description (Continued)

The device is designed for 3-V to 3.6-V V_{CC} operation, but it has 5-V tolerant I^2C and enable (EN) input pins. This feature allows for translation from 3 V to 5 V between a master and slave. The enable pin also can be used to electrically isolate a repeater segment from the I^2C bus. This is useful in cases where one segment needs to run at 100 kHz while the rest of the system is at 400 kHz. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz, because of the delays added by the repeater.

The output low levels for each internal buffer are approximately 0.5 V, but the input voltage of each internal buffer must be 70 mV or more below the output low level, when the output internally is driven low. This prevents a lockup condition from occurring when the input low condition is released.

A PCA9518 cluster cannot be put in series with a repeater such as the PCA9515 or another PCA9518 cluster, as the design does not allow this configuration. Multiple PCA9518 devices can be grouped with other PCA9518 devices into any size cluster using the EXPxxxx pins that allow the I^2C signals to be sent or received from one PCA9518 to another PCA9518 within the cluster. Because there is no direction pin, slightly different valid low voltage levels are used to avoid lockup conditions between the input and the output of individual repeaters in the cluster. A valid low applied at the input of any of the PCA9518 devices is propagated as a buffered low, with a slightly higher value, to all enabled outputs in the PCA9518 cluster. When this buffered low is applied to another repeater or separate PCA9518 cluster (not connected via the EXPxxxx pins) in series, the second repeater or PCA9518 cluster does not recognize it as a regular low and does not propagate it as a buffered low again. For this reason, the PCA9518 should not be put in series with other repeater or PCA9518 clusters.

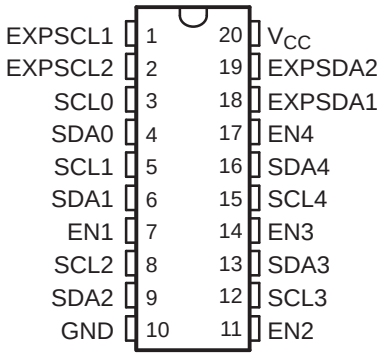
The PCA9518 has five multidirectional open-drain buffers designed to support the standard low-level-contention arbitration of the I^2C bus. Except during arbitration, the PCA9518 acts like a pair of noninverting open-drain buffers, one for SDA and one for SCL.

There is an internal power-on-reset circuit (V_{POR}) that allows for an initial condition and the ramping of V_{CC} to set the internal logic.

As with the standard I^2C system, pullup resistors are required on each SDAn and SCLn to provide the logic high levels on the buffered bus. The size of these pullup resistors depends on the system, but it is essential that each side of the repeater have a pullup resistor. The device is designed to work with standard-mode and fast-mode I^2C devices in addition to SMBus devices. Standard-mode I^2C devices only specify 3 mA in a generic I^2C system where standard-mode devices and multiple masters are possible.

5 Pin Configuration and Functions

DB, DBQ, DW, OR PW PACKAGE
(TOP VIEW)



Pin Functions

SOIC, SSOP, TSSOP, OR QSOP PIN NO.	NAME	DESCRIPTION
1	EXPSCL1	Expandable serial clock pin 1. Connect to V_{CC} through a pullup resistor.
2	EXPSCL2	Expandable serial clock pin 2. Connect to V_{CC} through a pullup resistor.
3	SCL0	Serial clock bus 0. Connect to V_{CC} through a pullup resistor.
4	SDA0	Serial data bus 0. Connect to V_{CC} through a pullup resistor.
5	SCL1	Serial clock bus 1. Connect to V_{CC} through a pullup resistor.
6	SDA1	Serial data bus 1. Connect to V_{CC} through a pullup resistor.
7	EN1	Active-high bus enable 1
8	SCL2	Serial clock bus 2. Connect to V_{CC} through a pullup resistor.
9	SDA2	Serial data bus 2. Connect to V_{CC} through a pullup resistor.
10	GND	Ground
11	EN2	Active-high bus enable 2
12	SCL3	Serial clock bus 3. Connect to V_{CC} through a pullup resistor.
13	SDA3	Serial data bus 3. Connect to V_{CC} through a pullup resistor.
14	EN3	Active-high bus enable 3
15	SCL4	Serial clock bus 4. Connect to V_{CC} through a pullup resistor.
16	SDA4	Serial data bus 4. Connect to V_{CC} through a pullup resistor.
17	EN4	Active-high bus enable 4
18	EXPSDA1	Expandable serial data pin 1. Connect to V_{CC} through a pullup resistor.
19	EXPSDA2	Expandable serial data pin 2. Connect to V_{CC} through a pullup resistor.
20	V_{CC}	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Enable input voltage range(2)		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(3)	DB package		63	°C/W
		DBQ package		61	
		DW package		46	
		PW package		88	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	125	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}		5.5	V
		EN	2		5.5	
		EXPSDA, EXPSCL	0.55 × V_{CC}		5.5	
V_{IL} (1)	Low-level input voltage	SCL, SDA	–0.5		0.3 × V_{CC}	V
		EN	–0.5		0.8	
		EXPSDA, EXPSCL	–0.5		0.45 × V_{CC}	
V_{ILc} (1)	Low-level input voltage contention	SCL, SDA	–0.5		0.4	V
T_A	Operating free-air temperature		–40		85	°C

(1) V_{IL} specification is for the first low level seen by SDA/SCL. V_{ILc} is for the second and subsequent low levels seen by SDA/SCL. V_{ILc} must be at least 70 mV below V_{OL}.

6.4 Electrical Characteristics

over recommended operating free-air temperature range, V_{CC} = 3 V to 3.6 V, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP (1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = −18 mA		3 V to 3.6 V			–1.2	V
V_{OL}	SCLn, SDAn	I_{OL} = 0 (2) or 6 mA		3 V to 3.6 V	0.45	0.52	0.7	V
	EXPSCL, EXPSDA	I_{OL} = 12 mA		3 V to 3.6 V			0.5	
V_{OL} – V_{ILc}	Low-level input voltage below low-level output voltage	SCL, SDA		3 V to 3.6 V			70	mV
I_I	SCLn, SDAn	V_I = 3.6 V		3 V to 3.6 V			±1	µA
		V_I = 0.2 V					1	
	EN1, EN2, EN3, EN4	V_I = V_{CC}					±1	
		V_I = 0.2 V (input current LOW)				10	20	
	EXPSCL, EXPSDA	V_I = 0.2 V					2	
I_{CC}	Quiescent supply current, Both channels high	SDAn = SCLn = V_{CC}, EXPSCLn = EXPSDAn = V_{CC}		3.6 V		1.75	6	mA
	Quiescent supply current, Both channels low	One SDA and one SCL are at GND, while other SDA and SCL are open.				2.5	9	
	Quiescent supply current, In contention	SDAn = SCLn = GND, EXPSCLn = EXPSDAn = V_{CC}				9	11	
I_{off}	SDAx, SCLx power-off condition with static V_{CC}	V_I = 3.6 V	EN = L or H	0 V			1	µA
		VI = GND					1	
$I_{I(ramp)}$	SDAx, SCLx power-off condition with V_{CC} ramping up or down	V_I = 3.6 V,	EN = L or H	0 V to 3 V			1	µA
C_I	SCLn, SDAn	V_I = 3 V or GND		3 V to 3.6 V		8	9.5	pF
	EN1, EN2, EN3, EN4					3	7	
	EXPSCL, EXPSDA					6	8	

(1) All typical values are at 3.3-V supply voltage and T_A = 25°C.
(2) Test performed with I_{OL} = 10 µA

6.5 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{su}	Setup time, EN↑ before Start condition	300		ns
t_h	Hold time, EN↓ after Stop condition	300		ns

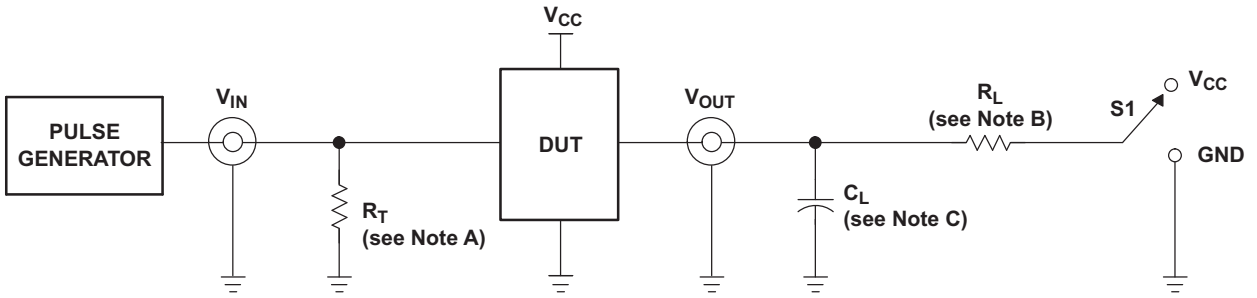
6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 1)(1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PHLs} (2)	Propagation delay	SDA or SCL	SDAn or SCLn	105	202	389	ns
t_{PLHs} (3)				105	259	265	ns
t_{PHLE1s}		EXPSDA1 or EXPSCL1	SDA or SCL	109	193	327	ns
t_{PLHE1s}				120	153	200	ns
t_{PLHE2s}		EXPSDA2 or EXPSCL2	SDA or SCL	120	234	279	ns
t_{THLs}	Output transition time, SDAn, SCLn	70%	30%	48	110	187	ns
t_{TLHs}		30%	70%		0.85RC		ns

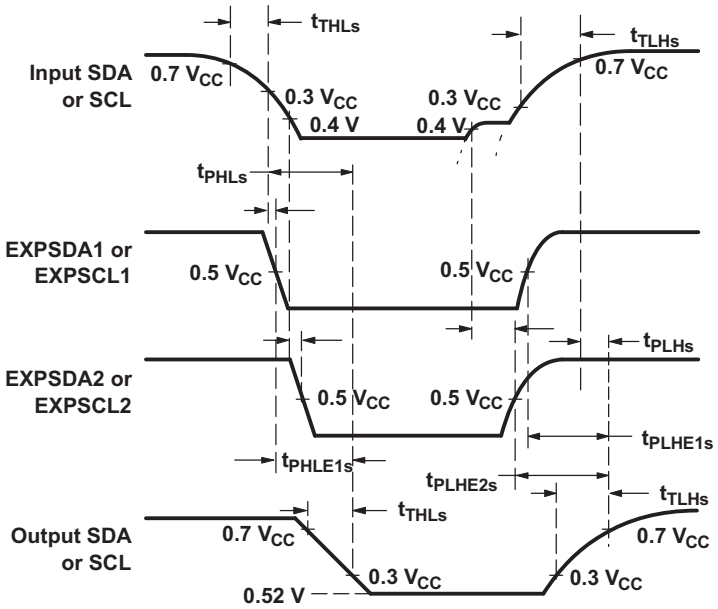
(1) The SDA and SCL propagation delays are dominated by rise times or fall times. The fall times mostly are internally controlled and are sensitive only to load capacitance. The rise times are RC time-constant controlled and, therefore, a specific numerical value can be given only for fixed RC time constants.
(2) The SDA high-to-low propagation delay, t_{PHLs}, includes the fall time from V_{CC} to 0.5 V_{CC} of EXPSDA1 or EXPSCL1 and the SDA or SCL fall time from the quiescent high (usually V_{CC}) to below 0.3 V_{CC}. The SDA and SCL outputs have edge-rate-control circuits included that make the fall time almost independent of load capacitance.
(3) The SDA or SCL low-to-high propagation delay, t_{PLHs}, includes the rise-time constant from the quiescent low to 0.5 V_{CC} for EXPSDA1 or EXPSCL2, the rise-time constant for the quiescent low to 0.5 V_{CC} for EXPSDA1 or EXPSCL1, and the rise time constant from the quiescent externally driven low to 0.7 V_{CC} for SDA or SCL.

7 Parameter Measurement Information



TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

TEST	S1
t_{PLH}/t_{PHL}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

A. Termination resistance, R_T, should be equal to the Z_{OUT} of the pulse generators.

B. Load resistor, R_L = 1.1 kΩ for I^2C and 500 Ω for EXP

C. Load capacitance, C_L, includes jig and probe capacitance; 100 pF for I^2C and EXP.

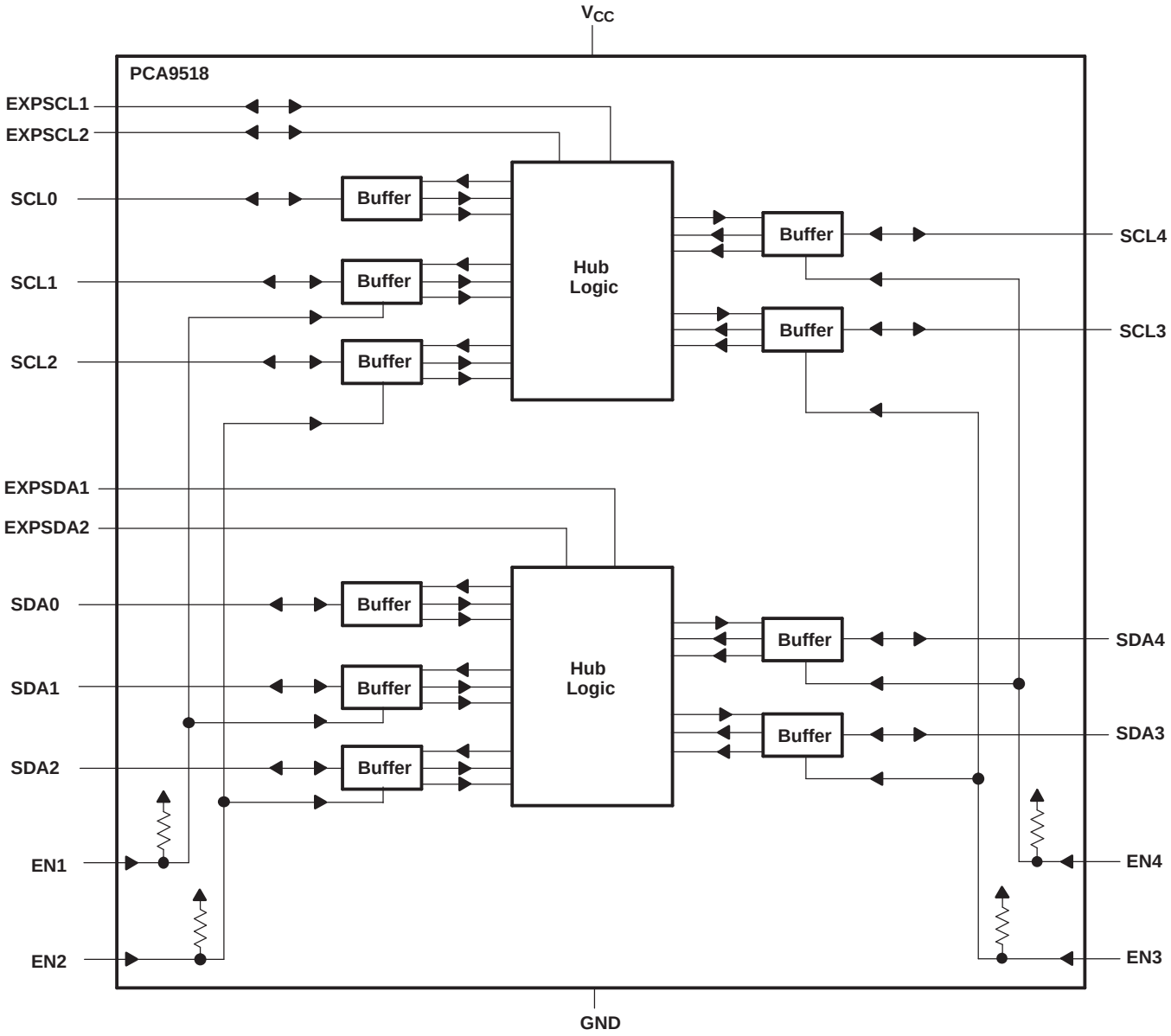
D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

E. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Functional Block Diagram



A more detailed view of each buffer in the functional block diagram is shown in Figure 2.

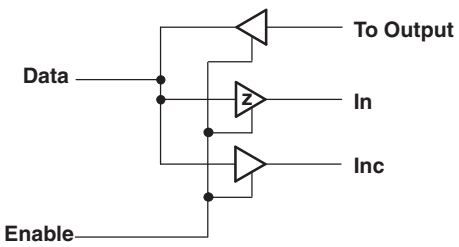


Figure 2. Buffer Details

8.2 Feature Description

8.2.1 Enable

EN1–EN4 are active-high enable pins and have internal pullup resistors. Each enable pin, ENn, controls its associated SDAn and SCLn ports. When ENn is low, it isolates its corresponding SDAn and SCLn from the system by blocking the inputs from SDAn and SCLn and disabling the output drivers on the SDAn and SCLn pins. It is essential that the ENn change state only when both the global bus and the local port are in an idle state to prevent system failures. EN1–EN4 also allow the use of open-drain drivers that can be wire-ORed to create a distributed enable where either centralized control signal (master) or spoke signal (submaster) can enable the channel when it is idle.

8.2.2 Expansion

The PCA9518 has four open-drain I/O pins used for expansion. The internal state of the serial data within each hub is communicated to other hubs through two expansion pins, EXPSDA1 and EXPSDA2. The EXPSDA1 pins of all hubs are connected together to form an open-drain bus. Similarly, all EXPSDA2 pins, EXPSCL1 pins, and EXPSCL2 pins are connected together, forming a 4-wire bus between hubs. When it is necessary to be able to deselect every port, each expansion device contributes only four ports that can be enabled or disabled; the fifth port does not have an enable pin. Pullup resistors are required on the EXPxxxx pins, even if only one PCA9518 is used.

8.2.3 Clock Stretching Errata

Description

Due to the static offset on both sides of the buffer (SCLx & SDAx) and the possibility of an overshoot above 500 mV during events like clock stretching, the device should not be used with rise time accelerators.

System Impact

An incorrect logic state will be transferred to circuits, creating an I^2C communication failure on the bus.

System Workaround

There are two possible workarounds to avoid an I^2C communication failure:

- Removing rise-time accelerators from the B-side bus.
- Adding a larger capacitive load to the bus will limit the overshoot.

8.3 Device Functional Modes

Table 1. Function Table(1)(2)(3)

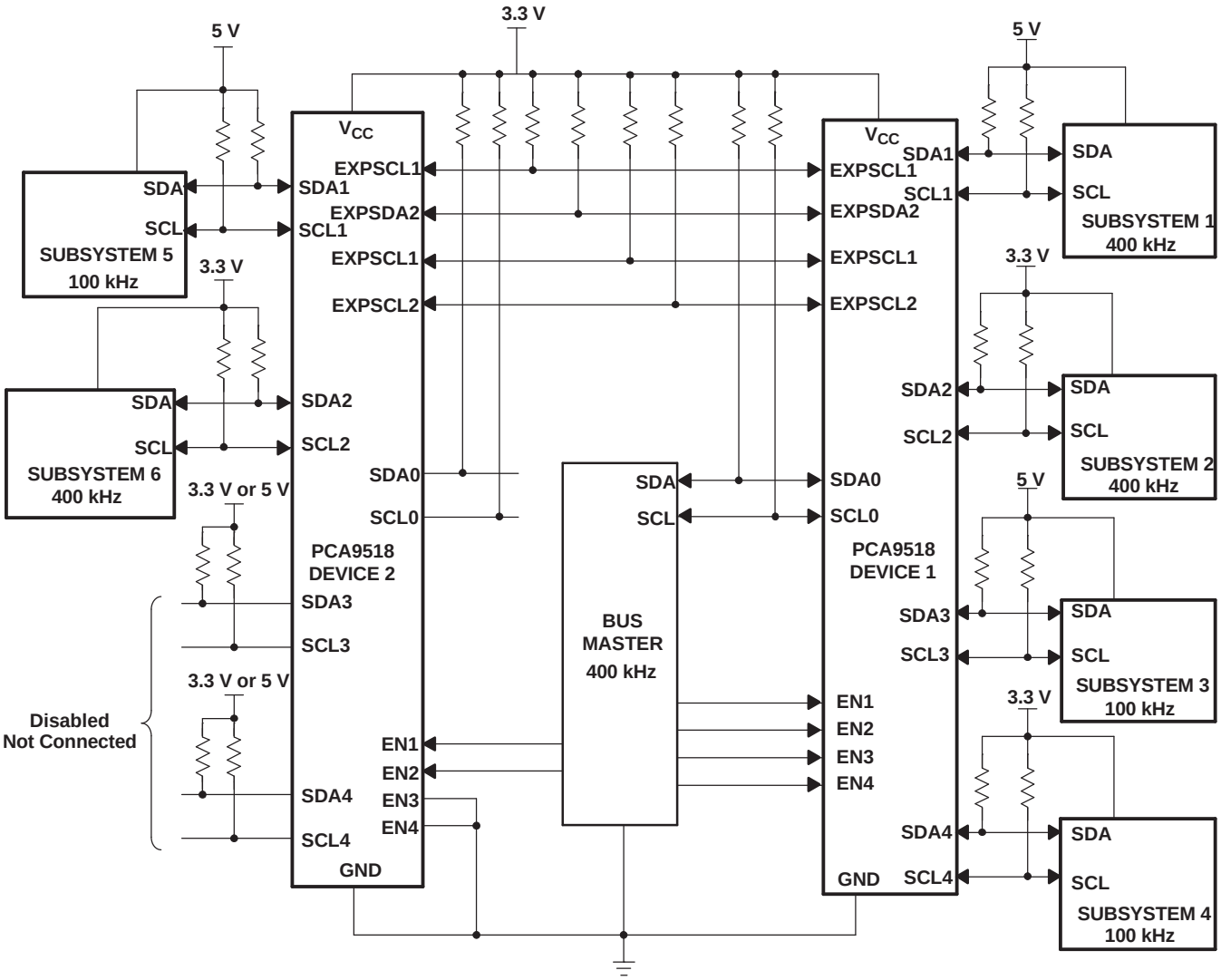
INPUTS				FUNCTION							
EN1	EN2	EN3	EN4	SCL1	SCL2	SCL3	SCL4	SDA1	SDA2	SDA3	SDA4
L	L	L	L	Disconnect	Disconnect	Disconnect	Disconnect	Disconnect	Disconnect	Disconnect	Disconnect
L	L	L	H	Disconnect	Disconnect	Disconnect	SCL0	Disconnect	Disconnect	Disconnect	SDA0
L	L	H	L	Disconnect	Disconnect	SCL0	Disconnect	Disconnect	Disconnect	SDA0	Disconnect
L	L	H	H	Disconnect	Disconnect	SCL0	SCL0	Disconnect	Disconnect	SDA0	SDA0
L	H	L	L	Disconnect	SCL0	Disconnect	Disconnect	Disconnect	SDA0	Disconnect	Disconnect
L	H	L	H	Disconnect	SCL0	Disconnect	SCL0	Disconnect	SDA0	Disconnect	SDA0
L	H	H	L	Disconnect	SCL0	SCL0	Disconnect	Disconnect	SDA0	SDA0	Disconnect
L	H	H	H	Disconnect	SCL0	SCL0	SCL0	Disconnect	SDA0	SDA0	SDA0
H	L	L	L	SCL0	Disconnect	Disconnect	Disconnect	SDA0	Disconnect	Disconnect	Disconnect
H	L	L	H	SCL0	Disconnect	Disconnect	SCL0	SDA0	Disconnect	Disconnect	SDA0
H	L	H	L	SCL0	Disconnect	SCL0	Disconnect	SDA0	Disconnect	SDA0	Disconnect
H	L	H	H	SCL0	Disconnect	SCL0	SCL0	SDA0	Disconnect	SDA0	SDA0
H	H	L	L	SCL0	SCL0	Disconnect	Disconnect	SDA0	SDA0	Disconnect	Disconnect
H	H	L	H	SCL0	SCL0	Disconnect	SCL0	SDA0	SDA0	Disconnect	SDA0
H	H	H	L	SCL0	SCL0	SCL0	Disconnect	SDA0	SDA0	SDA0	Disconnect
H	H	H	H	SCL0	SCL0	SCL0	SCL0	SDA0	SDA0	SDA0	SDA0

(1) SCL from master = SCL0
(2) SDA from master = SDA0
(3) See *Description* and *Application Information* for information on EXPxxx1 and EXPxxx2 behavior.

9 Application and Implementation

9.1 Typical Application

Figure 3 shows an application in which the PCA9518 can be used.



A. Only two of the five channels of the PCA9518 device 2 are being used. EN3 and EN4 are connected to GND to disable channels 3 and 4, or SDA3/SCL3 and SDA4/SCL4 are pulled up to V_{CC}. SDA0 and SCL0 can be used as a normal I^2C port, but they must be pulled up to V_{CC} if unused, because there is no enable pin.

Figure 3. Multiple Expandable Five-Channel I^2C Hubs

Typical Application (continued)

9.1.1 Design Requirements

Here, the system master is running on a 3.3-V I^2C bus, while the slaves are connected to a 3.3-V or 5-V bus. The PCA9518 is 5-V tolerant, so it does not require any additional circuitry to translate between the different bus voltages.

All buses run at 100 kHz, unless slaves 3, 4, and 5 are isolated from the bus. If the master bus and slaves 1, 2, and 6 need to run at 400 kHz, slaves 3, 4, and 5 can be isolated through the bus master. In this case, the bus master will change the state on the corresponding EN pin (for slaves 3, 4, and 5) to low.

Any segment of the hub can talk to any other segment of the hub. Bus masters and slaves can be located on any segment with 400-pF load allowed on each segment.

9.1.2 Detailed Design Procedure

When one port of the PCA9518 is pulled low by a device on the I^2C bus, a CMOS hysteresis-type input detects the falling edge and drives the EXPxxx1 line low; when the EXPxxx1 voltage is less than 0.5-V V_{CC}, the other ports are pulled down to the V_{OL} of the PCA9518, which is typically 0.5 V.

If the bus master in Figure 3 were to write to the slave through the PCA9518, the waveform shown in Figure 4 would be created.

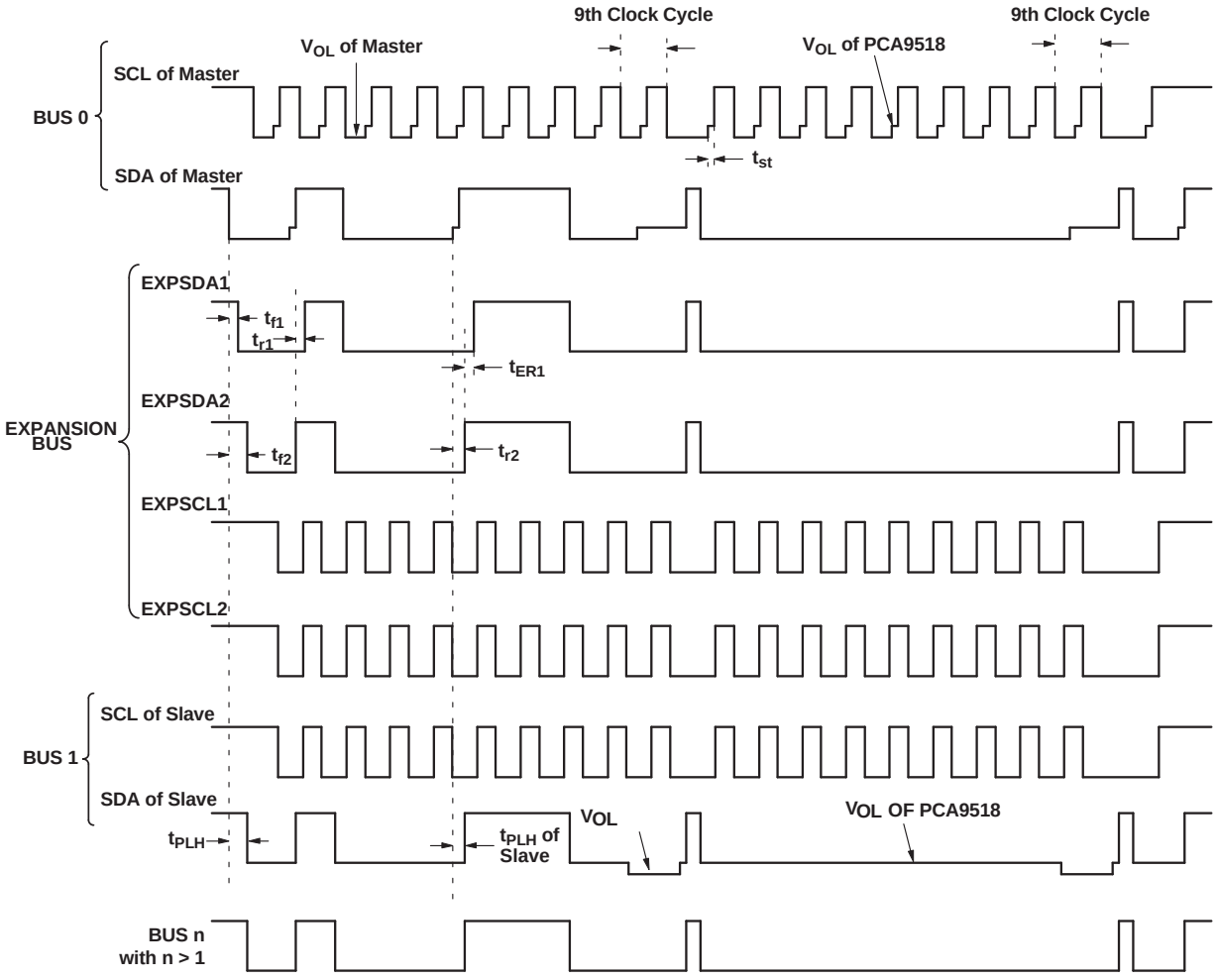


Figure 4. Bus Waveforms

Note that any arbitration on bus 1 require that the V_{OL} of the devices on bus 1 be 70 mV below the V_{OL} of the PCA9518 (see $V_{OL} – V_{ILc}$ in electrical characteristics) to be recognized by the PCA9518 and transmitted to bus 0.

Typical Application (continued)

This looks like a normal I^2C transmission, except for the small step preceding each clock low-to-high transition and proceeding each data low-to-high transition for the master. The step height is the difference between the low level driven by the master and the higher-voltage low level driven by the PCA9518 repeater. That same magnitude of delay is seen on the rising edge of the data. The step on the rising edge of the data is extended through the ninth clock pulse as the PCA9518 repeats the acknowledge from the slave to the master. The clock of the slave looks normal, except that the V_{OL} is the 0.5-V level generated by the PCA9518. The SDA at the slave has a particularly interesting shape during the ninth clock cycle, when the slave pulls the line below the value driven by the PCA9518 during the ACK and then returns to the PCA9518 level, creating a foot before it completes the low-to-high transition. SDA lines, other than the one with the master and the one with the slave, have a uniform low level driven by the PCA9518 repeater.

The expansion bus signals shown in Figure 4 are included primarily for timing reference points.

All timing on the expansion bus is with respect to 0.5 V_{CC}. EXPSDA1 is driven low whenever any SDA pin falls below 0.3-V V_{CC} and EXPSDA2 is driven low when any pin is ≤0.4 V. EXPSCL1 is driven LOW whenever any SCL pin falls below 0.3-V V_{CC} and EXPSCL2 is driven LOW when any SCL pin is ≤0.4 V. EXPSDA2 returns high after the SDA pin that was the last one being held below 0.4 V by an external driver starts to rise. The last SDA to rise above 0.4 V is held down by the PCA9518 to 0.5 V until after the delay of the circuit that determines that it was the last to rise; then, it is allowed to rise above the 0.5-V level driven by the PCA9518.

Considering the bus 0 SDA to be the last one to go above 0.4 V, then EXPSDA1 returns to high after EXPSDA2 is high and either bus 0 SDA rise time is 1 µs or bus 0 SDA reaches 0.7-V V_{CC}, whichever occurs first. After both EXPSDA2 and EXPSDA1 are high, the rest of the SDA lines are allowed to rise. The same description applies to the EXPSCL1, EXPSCL2, and SCL pins.

Any arbitration events on bus 1 requires that the V_{OL} of the devices on bus 1 be 70 mV below the V_{OL} of the PCA9518 (see $V_{OL} – V_{ILc}$ in electrical characteristics) to be recognized by the PCA9518 and then transmitted to bus 0.

10 Device and Documentation Support

10.1 Trademarks

All trademarks are the property of their respective owners.

10.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCA9518DBQR	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCA9518
PCA9518DBQR.A	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCA9518
PCA9518DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD518
PCA9518DBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD518
PCA9518DBT	Active	Production	SSOP (DB) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD518
PCA9518DBT.A	Active	Production	SSOP (DB) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD518
PCA9518DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9518
PCA9518DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9518
PCA9518DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9518
PCA9518DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9518
PCA9518DWT	Active	Production	SOIC (DW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9518
PCA9518DWT.A	Active	Production	SOIC (DW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9518
PCA9518PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	PD518
PCA9518PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD518
PCA9518PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD518
PCA9518PWT	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	PD518

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

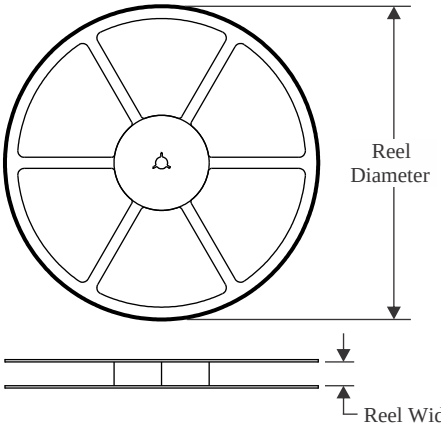
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

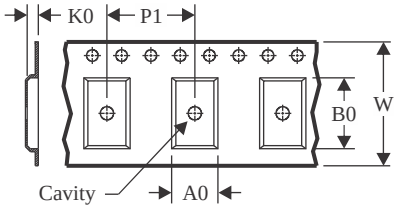
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

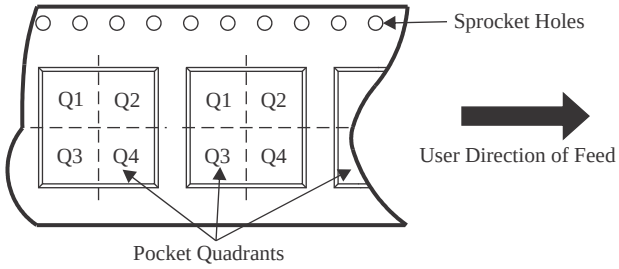


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

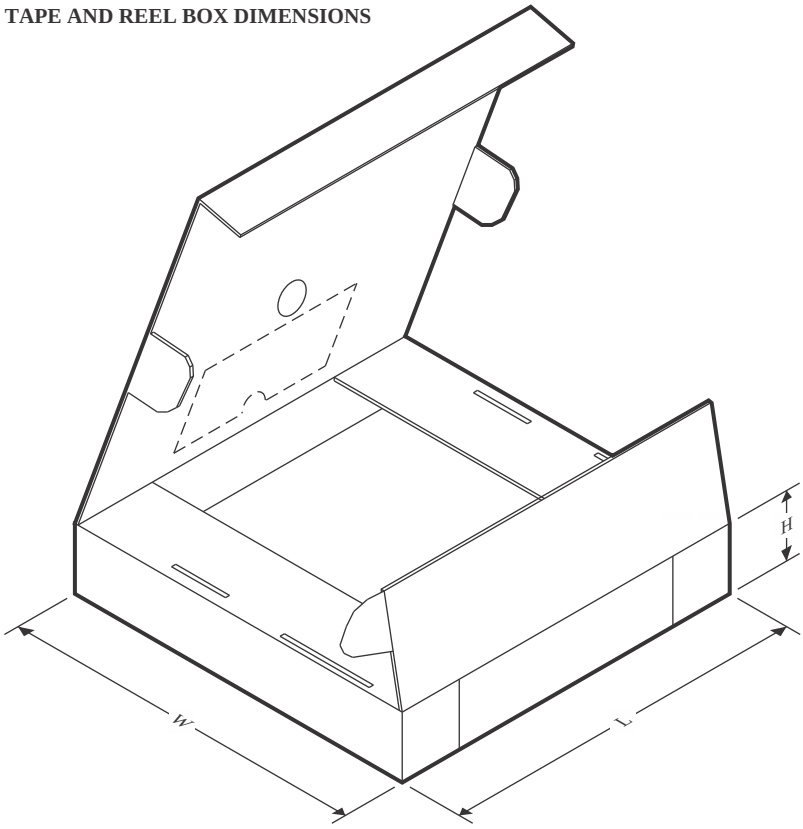
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9518DBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCA9518DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
PCA9518DBT	SSOP	DB	20	250	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
PCA9518DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
PCA9518DWT	SOIC	DW	20	250	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
PCA9518PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

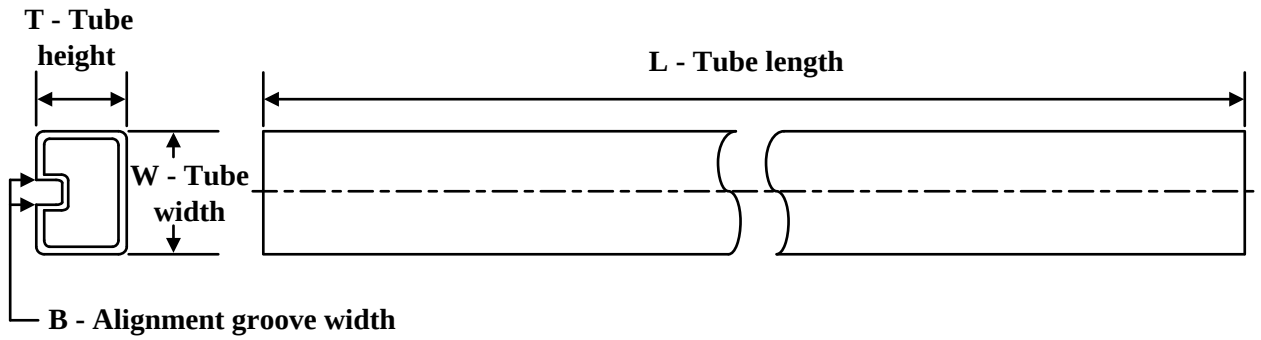
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9518DBQR	SSOP	DBQ	20	2500	353.0	353.0	32.0
PCA9518DBR	SSOP	DB	20	2000	353.0	353.0	32.0
PCA9518DBT	SSOP	DB	20	250	353.0	353.0	32.0
PCA9518DWR	SOIC	DW	20	2000	356.0	356.0	45.0
PCA9518DWT	SOIC	DW	20	250	356.0	356.0	45.0
PCA9518PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

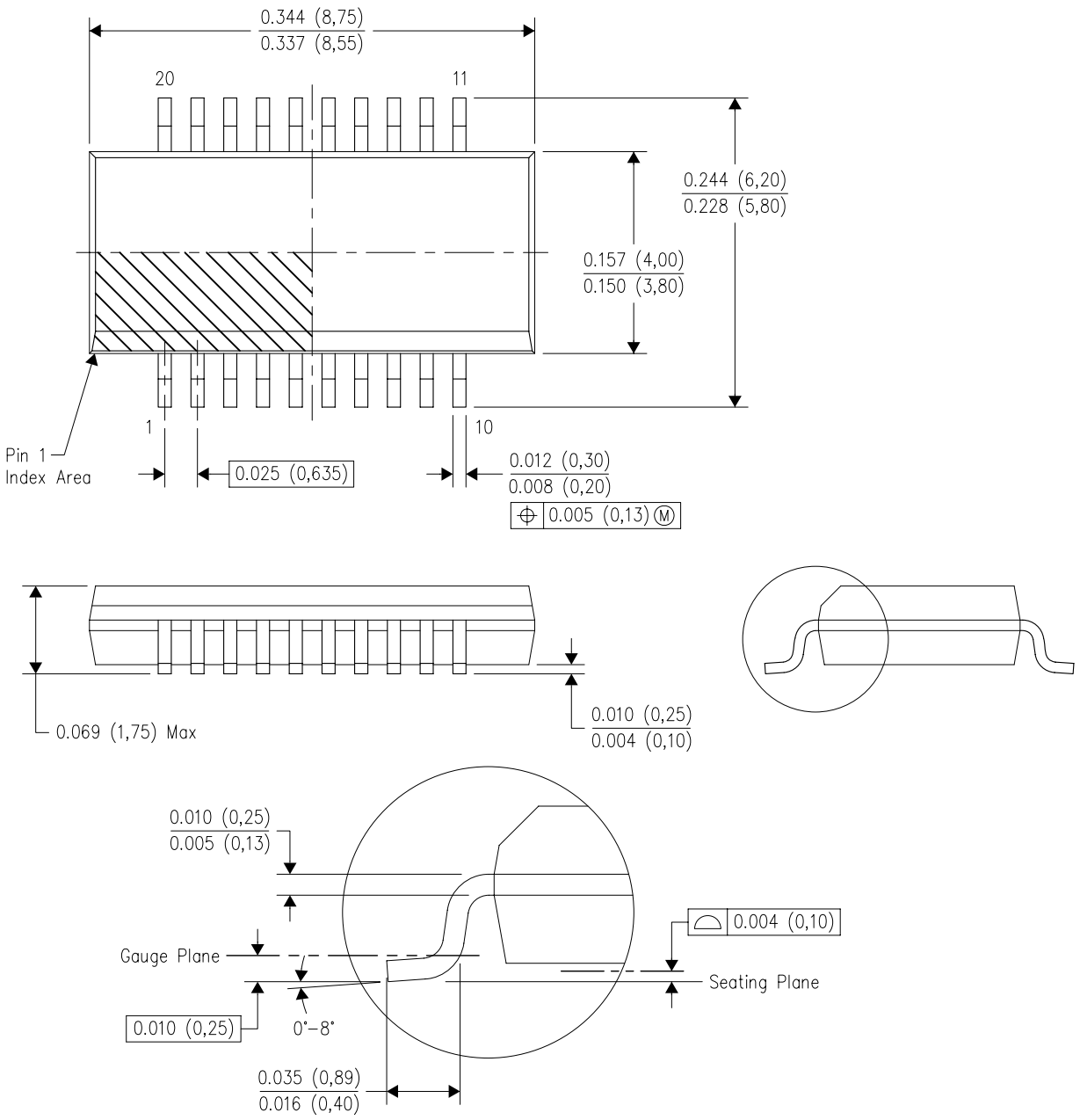
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCA9518DW	DW	SOIC	20	25	507	12.83	5080	6.6
PCA9518DW.A	DW	SOIC	20	25	507	12.83	5080	6.6

DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



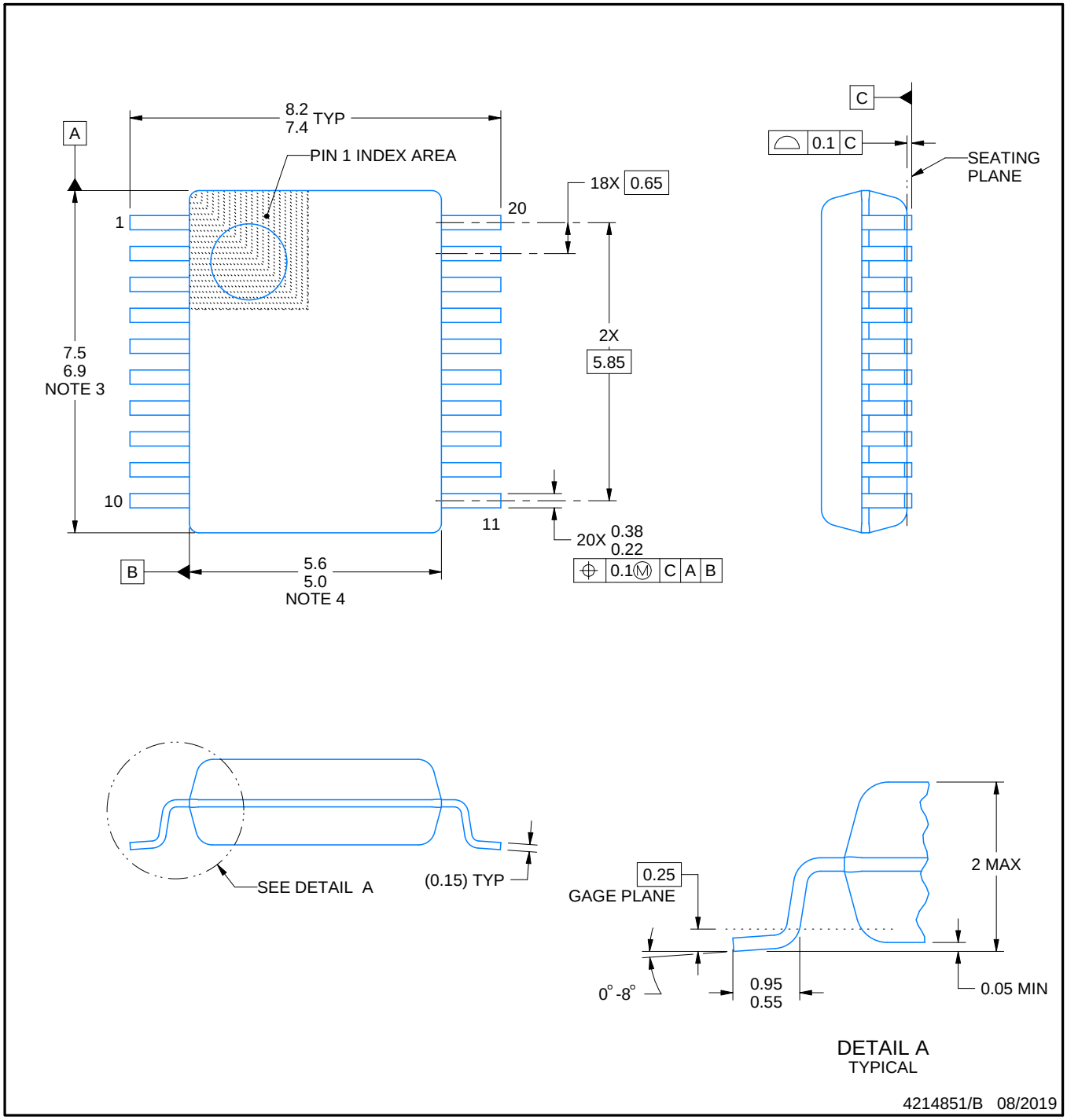
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

PACKAGE OUTLINE

DB0020A

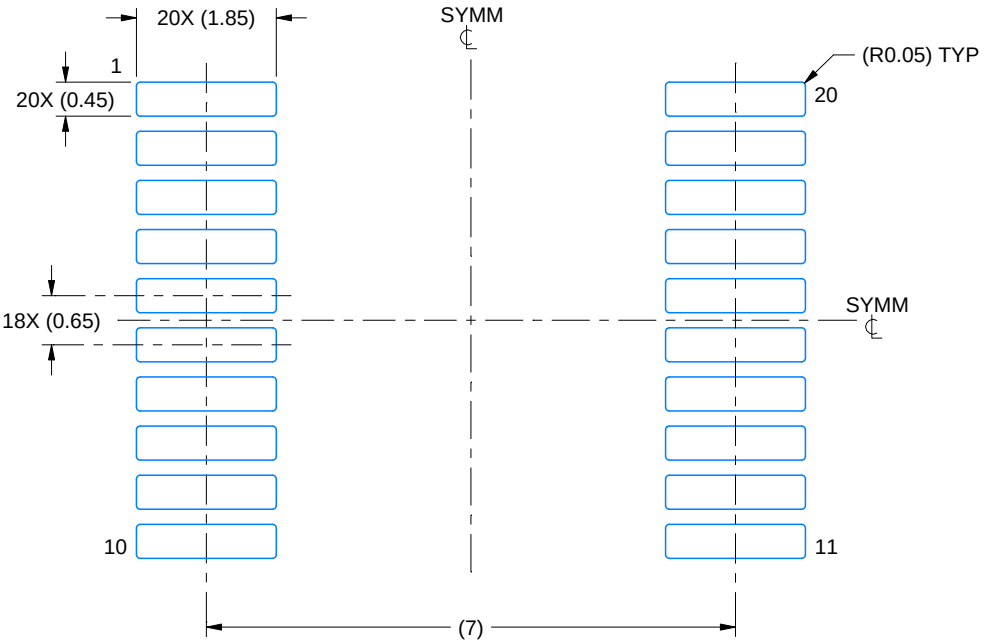
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

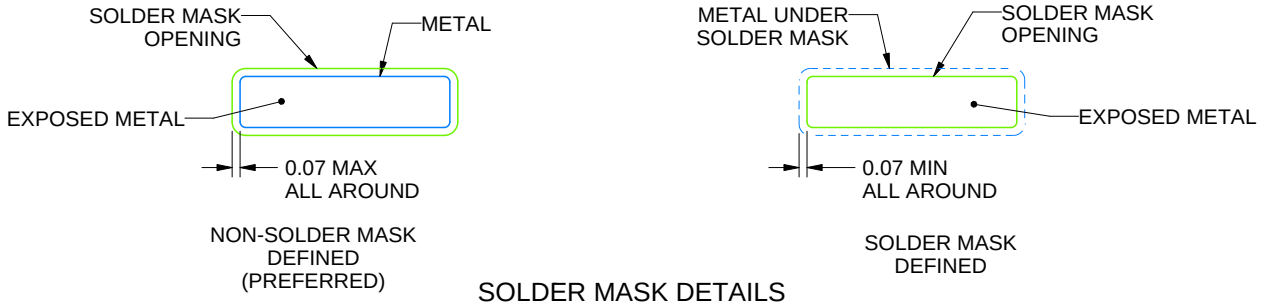


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

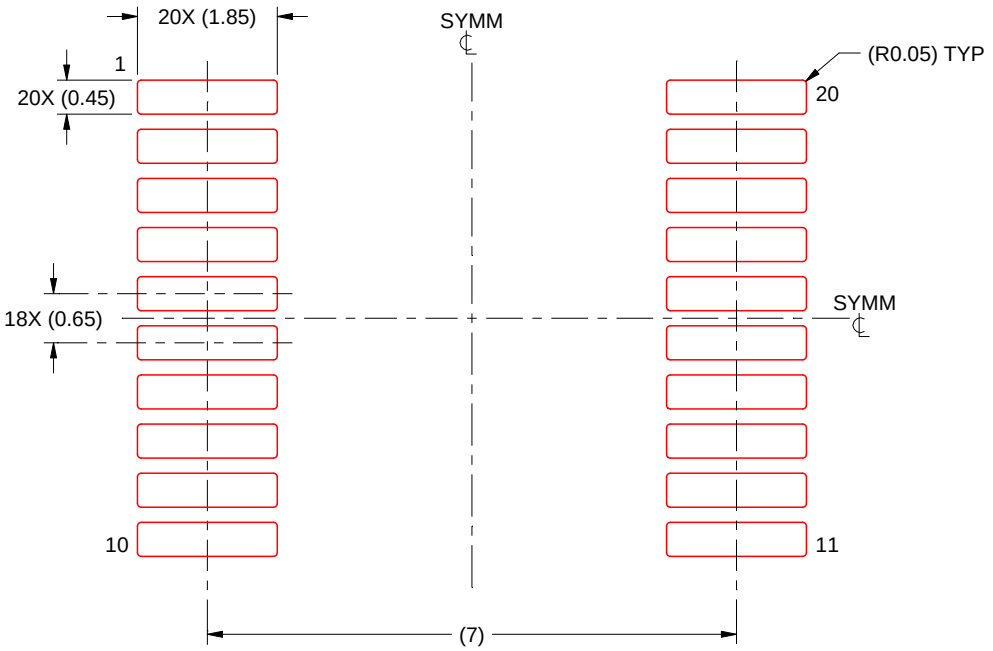
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

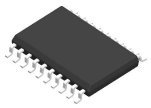


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

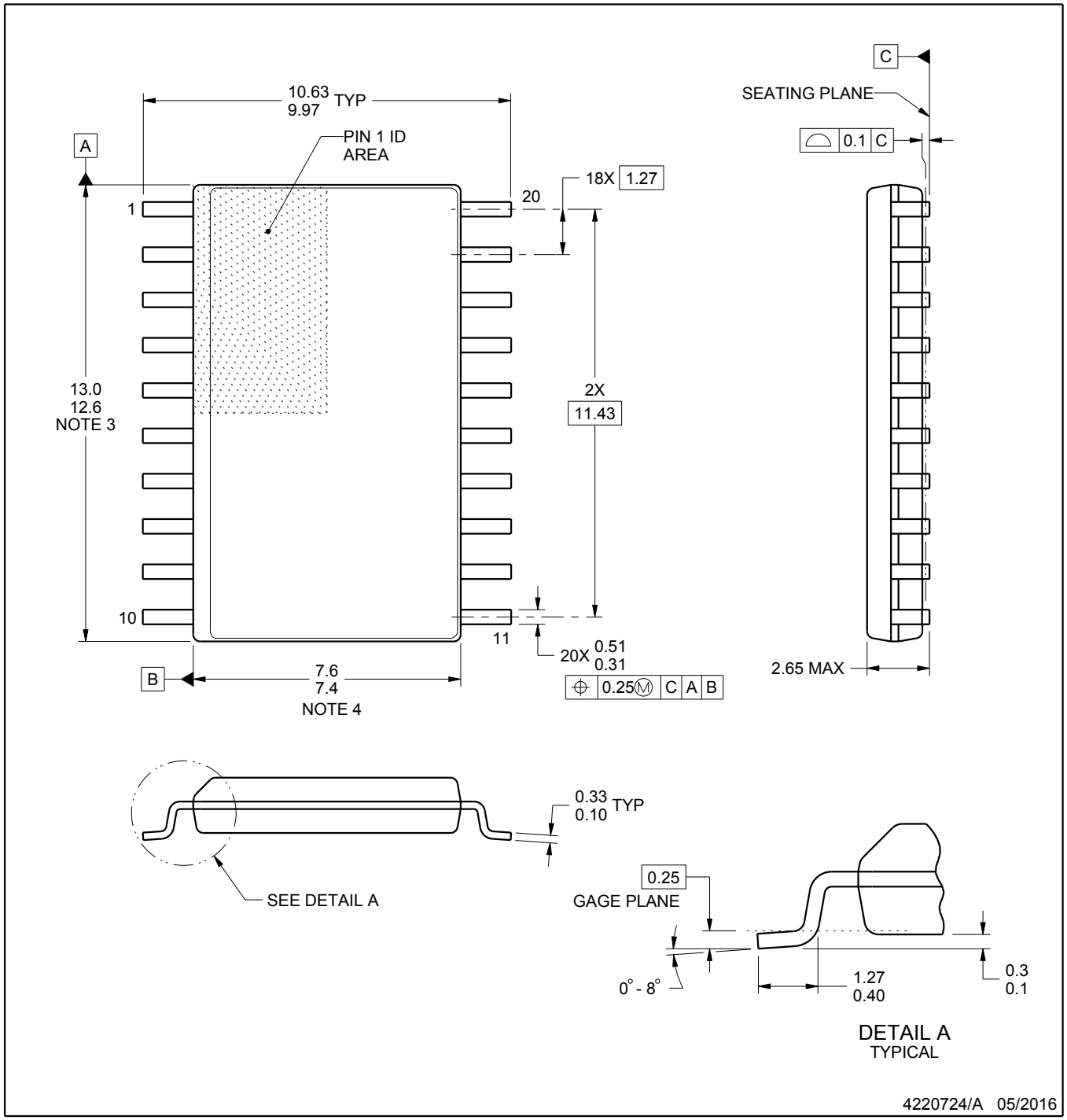


PACKAGE OUTLINE

DW0020A

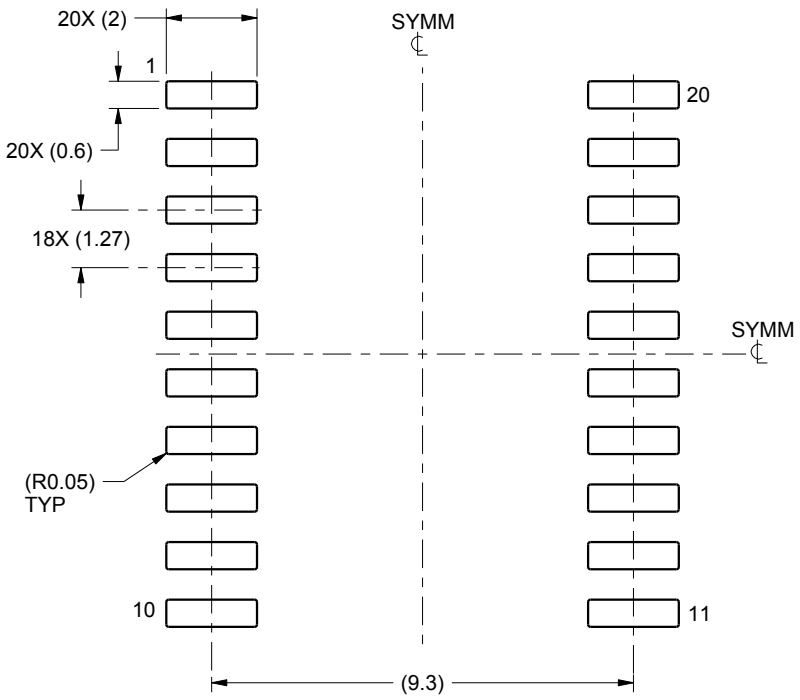
SOIC - 2.65 mm max height

SOIC

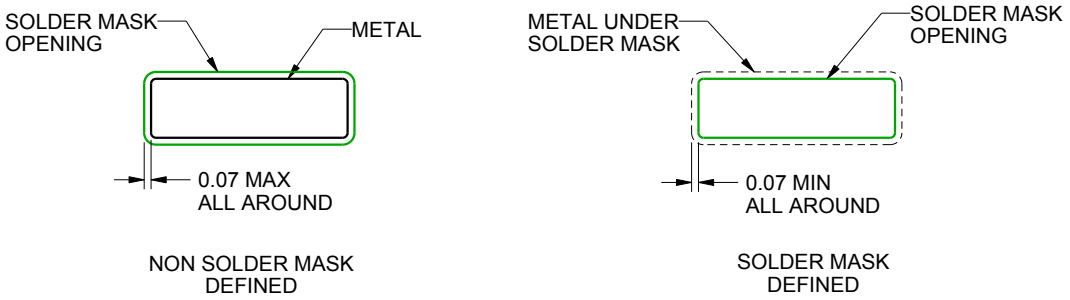


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

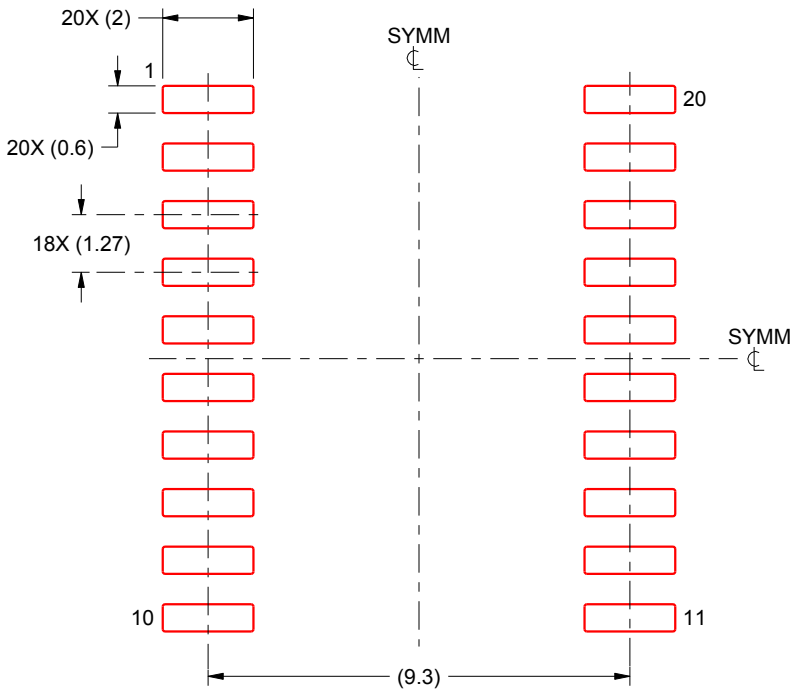


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

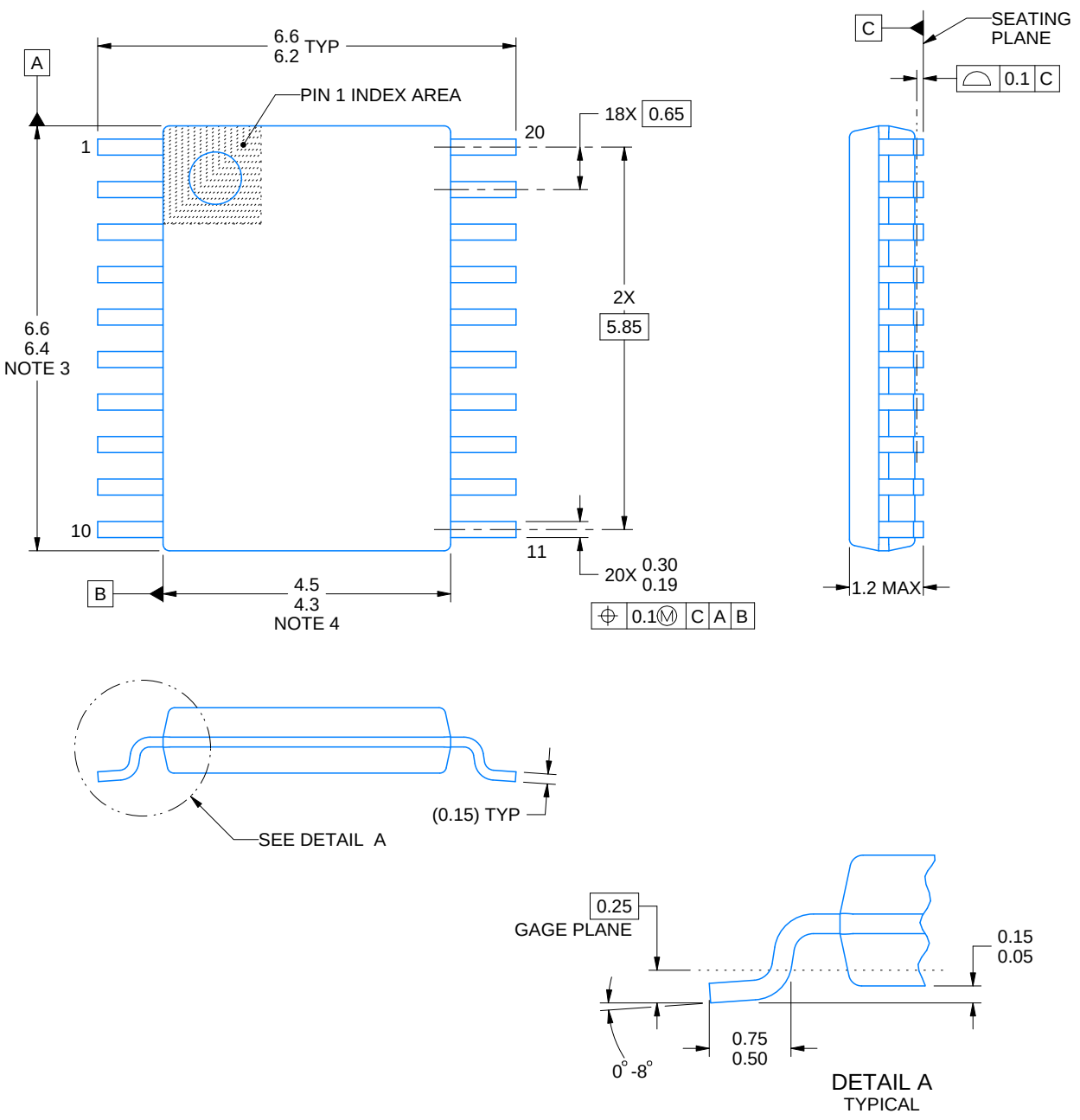
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

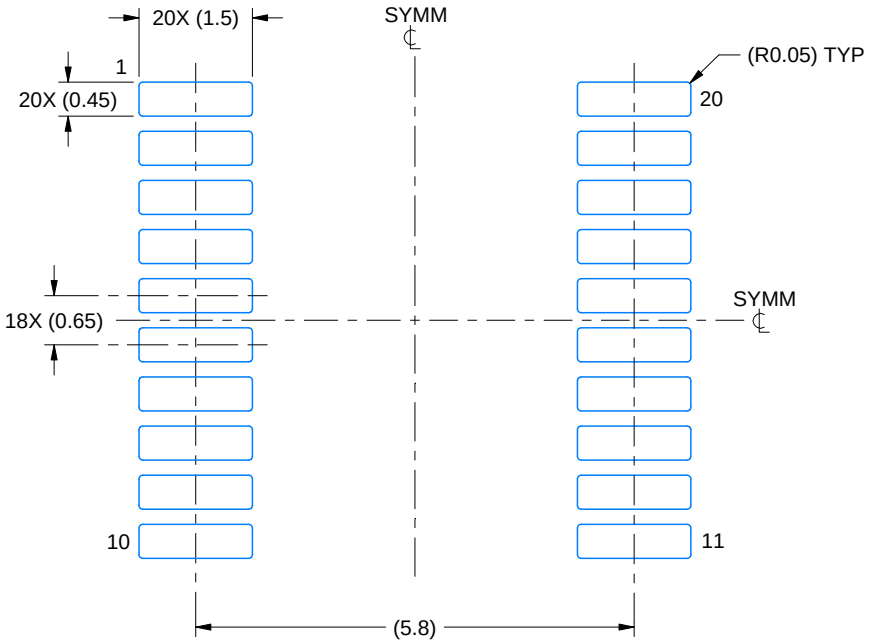
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



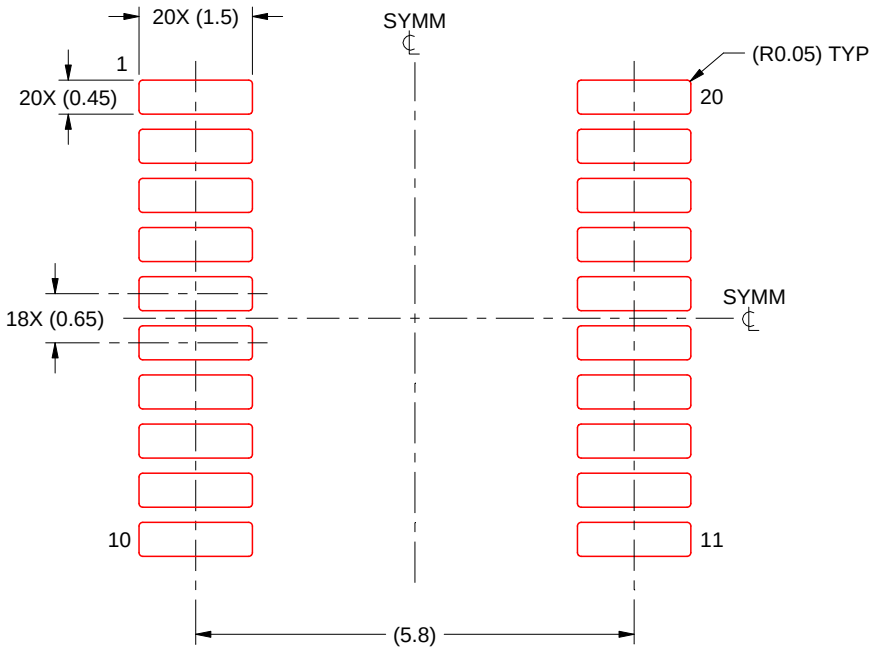
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025