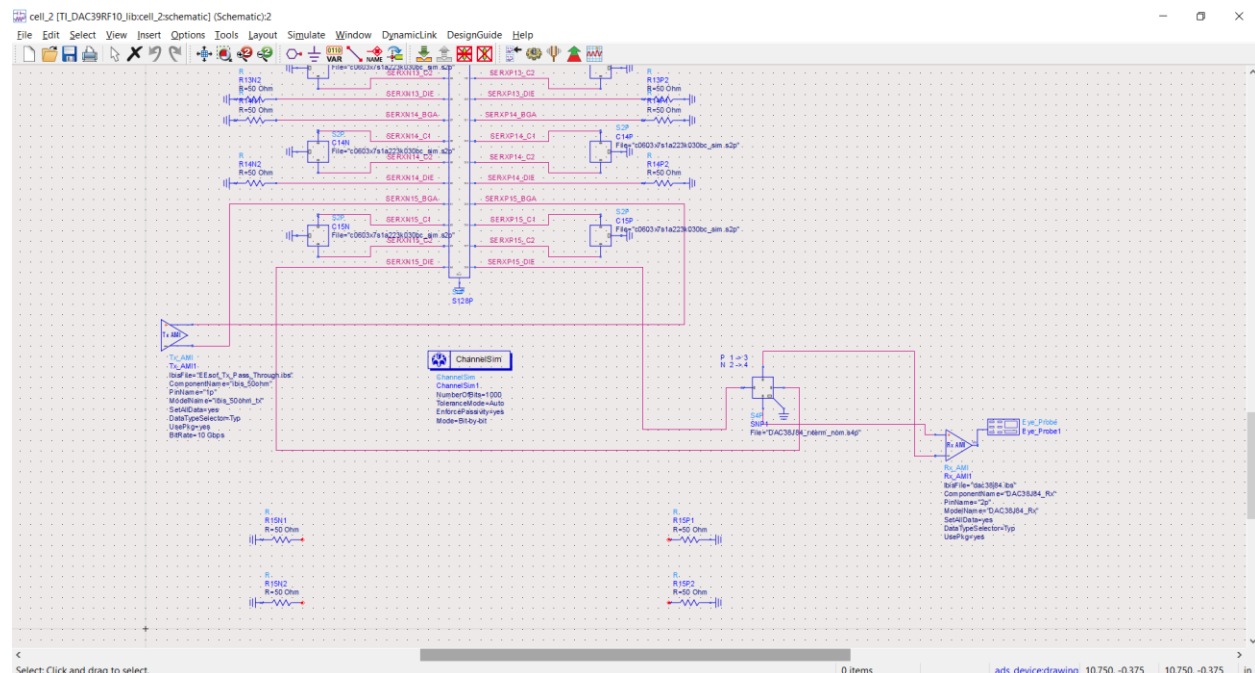


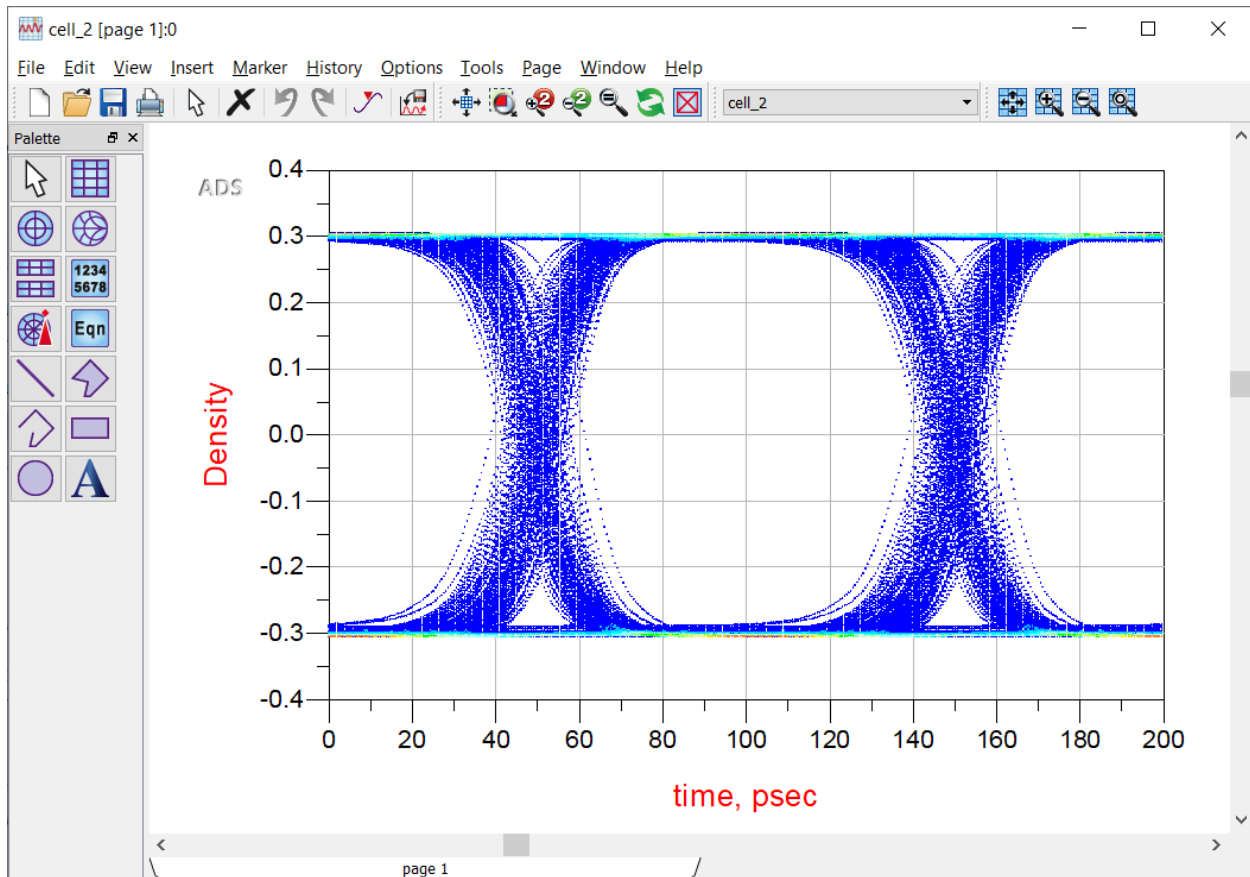
The package model consists of a 128 port s-parameter file which includes routing of the ball to in package capacitor (32 traces x 2 ports = 64 ports) and capacitor to die (32 traces x 2 ports = 64 ports). In addition, an s2p model is included for the in package capacitors to include in the simulation.

Port Name	Description
SERXN#_DIE	Die port for Serdes #SRX- (negative terminal)
SERXN#_C1	Capacitor port 1 for Serdes #SRX- (negative terminal)
SERXN#_C2	Capacitor port 2 for Serdes #SRX- (negative terminal)
SERXN#_BGA	BGA ball port for Serdes #SRX- (negative terminal)
SERXP#_DIE	Die port for Serdes #SRX+ (positive terminal)
SERXP#_C1	Capacitor port 1 for Serdes #SRX+ (positive terminal)
SERXP#_C2	Capacitor port 2 for Serdes #SRX+ (positive terminal)
SERXP#_BGA	BGA ball port for Serdes #SRX+ (positive terminal)

The TI\_DAC39RF10\_IBIS\_AMI\_ADS\_17NOV21.7z package includes an Keysight ADS workspace for running simulations (an ideal TX model is used and no PCB channel is included). Extract .7z file. The schematic cell\_2 shows how to connect the s-parameter files for on Serdes lane (the other lanes are terminated). The screenshot below shows the model connections.



The simulation output should look like

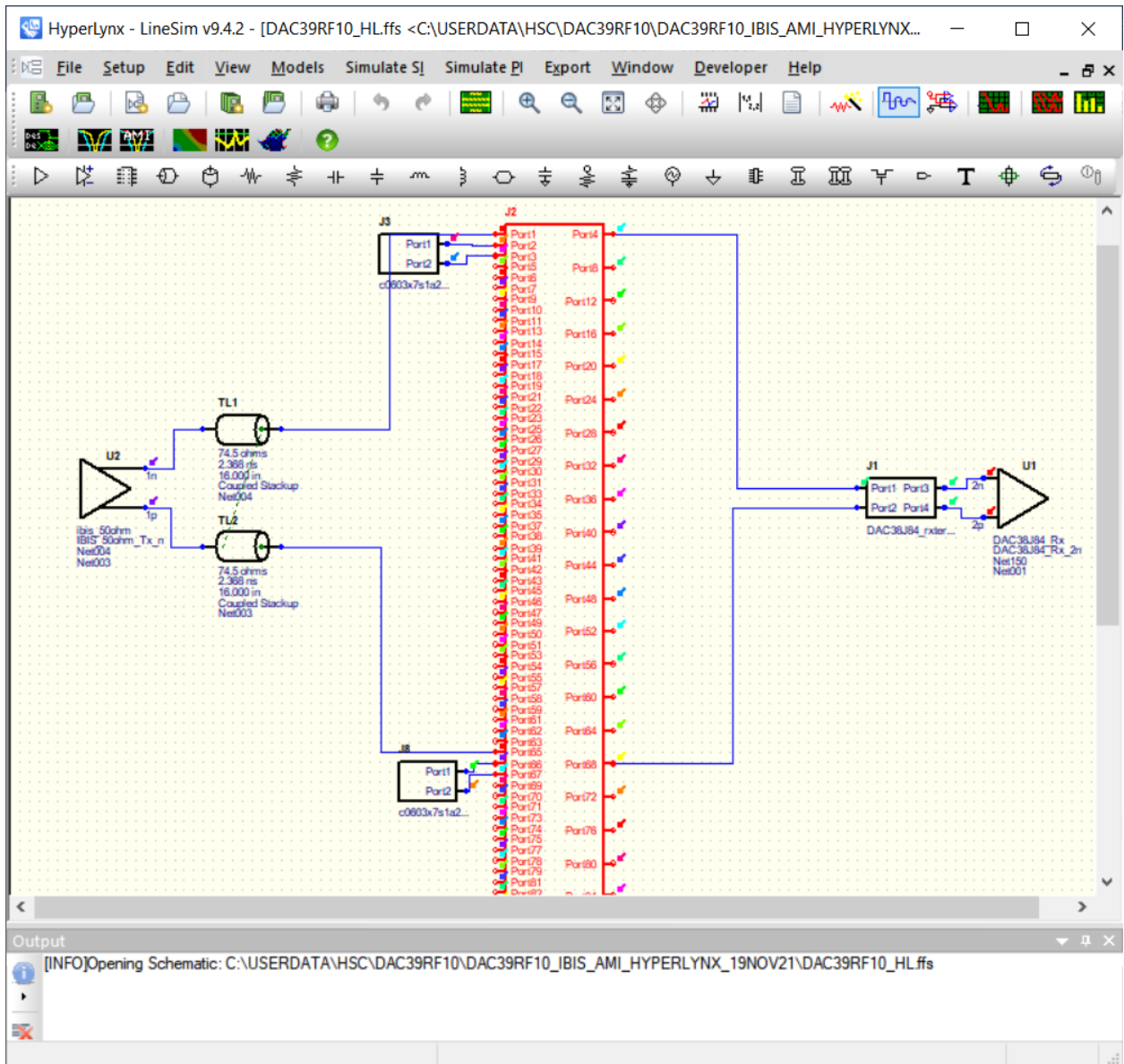


The IBIS AMI files are available in the /data folder and can be used for simulation in another tool.

#### Running in Hyperlynx

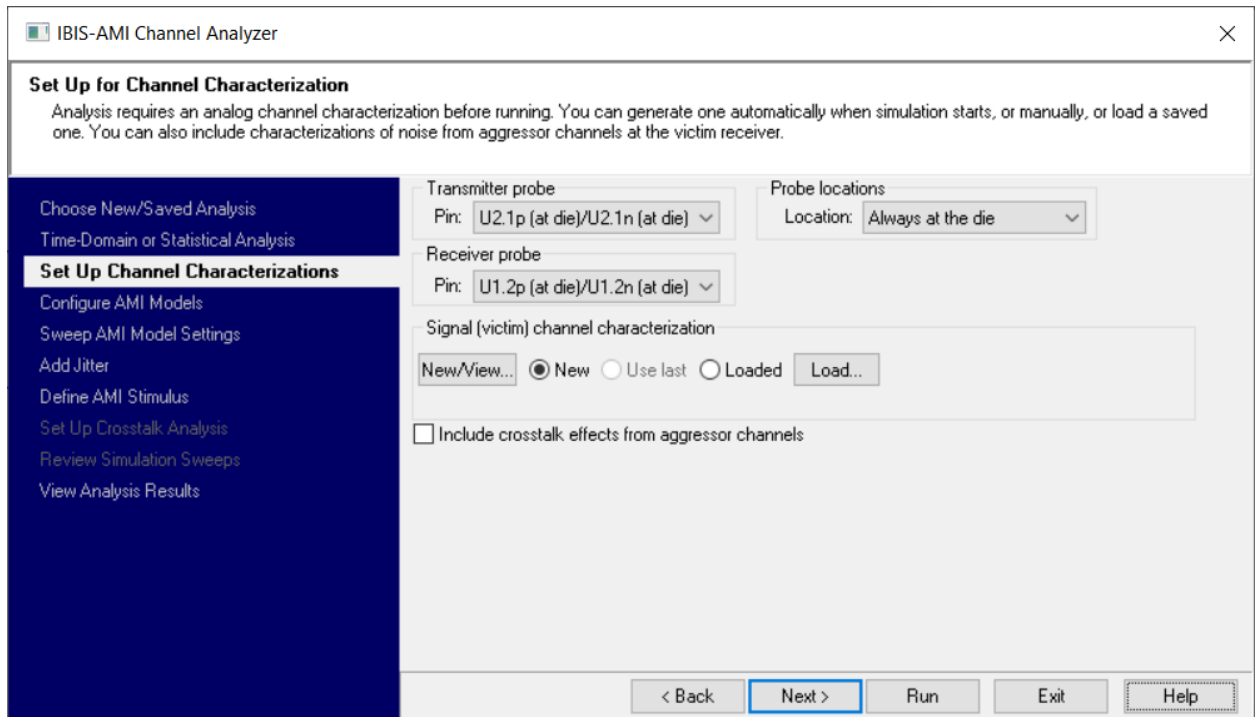
The TI\_DAC39RF10\_IBIS\_AMI\_HYPERLYNX\_19NOV21.zip package includes an Hyperlynx project for running simulations (an ideal TX model is used and no PCB channel is included). Extract .7z file.

1. Open DAC39RF10\_HL.ffs

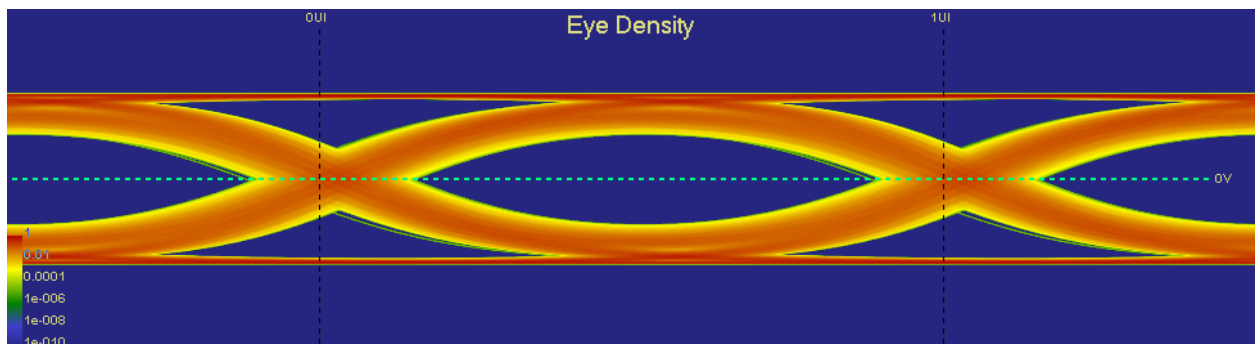


2. Run Simulate SI>Run IBIS AMI Channel Analysis...
3. New configuration NEXT>
4. Time domain NEXT>

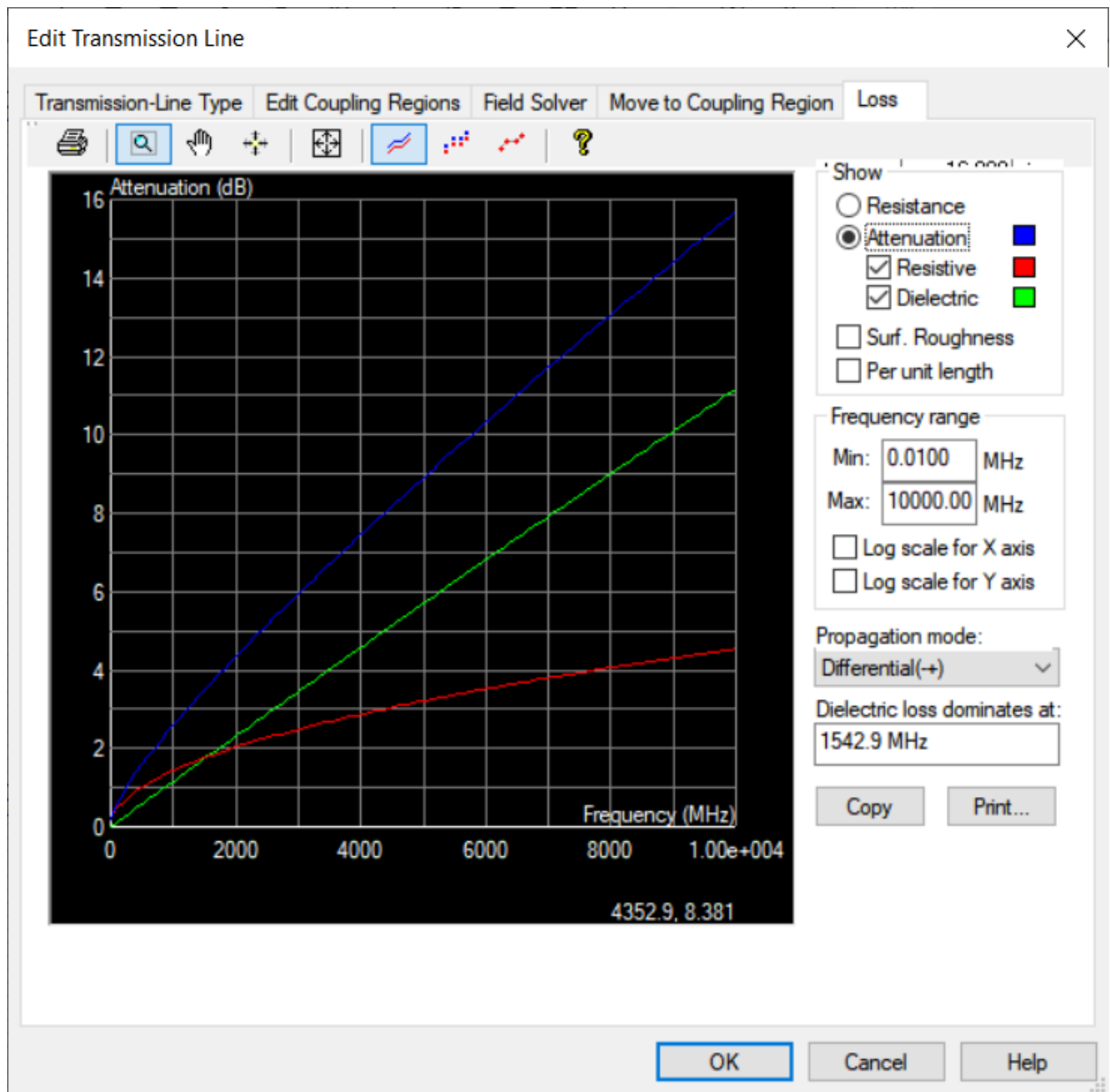
- Select receiver probe pin: U1.2p for CTLE output, J1.port 3/J1.port 4 for CTLE input



- Configure RX AMI>
- Change CDR Threshold to 4 for default setting. Gaincode = -1 for adaptive equalizer. NEXT>
- Optional Sweep Parameters NEXT>
- Add Jitter NEXT>
- Define stimulus – change bit rate to desired bit rate (12.8Gbps maximum) NEXT>
- View Analysis – check BER plots RUN>
- Results for the default 16" PCB traces:



PCB Channel loss:



13. DAC38J48.adapt (misspelled) shows the AEQ\_Zero and AEQ\_Gain adapted parameters over time in the 4st 2 columns:

```
0 , 2, 0, 0, 200, -18, 0
0 , 2, 0, 0, 200, 2, 1
0 , 2, 0, 0, 200, 3, 0
0 , 2, 0, 0, 200, -15, 0
0 , 2, 0, 0, 200, 18, 0
0 , 2, 0, 0, 200, -14, 0
```