Design Guide: TIDA-060031

Precision DAC Reference Design for Premium Audio in Hi-Fi Applications

Description

The DAC11001 audio reference design is a unique and comprehensive audio design featuring the DAC11001A and DAC11001B. The DAC11001 is a 20-bit, low-noise, ultra-high performance precision R-2R digital-to-analog converter (DAC). Delta-sigma type modulators are the most common DACs used in audio applications. Precision R-2R based DACs are generally not used in audio applications due to the additional design considerations for specific audio requirements. This reference design demonstrates the strengths and limitations of precision R-2R DACs for dynamic signal generation in the context of high-fidelity audio as an application.

Features

- 20-bit precision R-2R DAC for audio generation
- 2.1V_{RMS} line-level outputs with 108dB total harmonic distortion plus noise (THD+N)
- Low-noise output buffer
- High-bandwidth reference buffer
- USB and TOSLINK® optical input
- I2S to serial peripheral interface (SPI) conversion

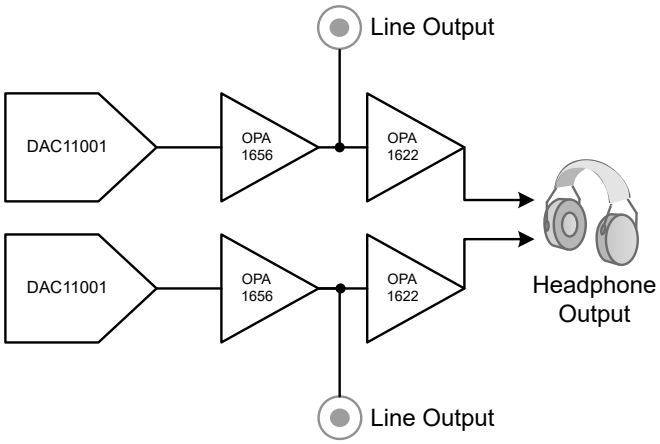
Applications

- AV receiver
- Streaming media player
- Soundbar
- Automotive head unit

Resources

TIDA-060031	Design Folder
DAC11001A	Product Folder
DAC11001B	Product Folder
OPA1656	Product Folder
OPA1622	Product Folder

Ask our TI E2E™ support experts



1 System Description

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	DAC11001A	DAC11001B	DETAILS
THD+N	108dB	111dB	Section 3.3.2
Dynamic range	119dB	119dB	Section 3.3.4
SNR	121dB	121dB	Section 3.3.6
Noise at idle	1.9μV_{RMS}	1.9μV_{RMS}	Section 3.3.6
Line-out amplitude	2.1V_{RMS}	2.1V_{RMS}	Section 3.3.6
Headphone output amplitude	480mV_{RMS}	480mV_{RMS}	Section 3.3.2

2 System Overview

2.1 Block Diagram

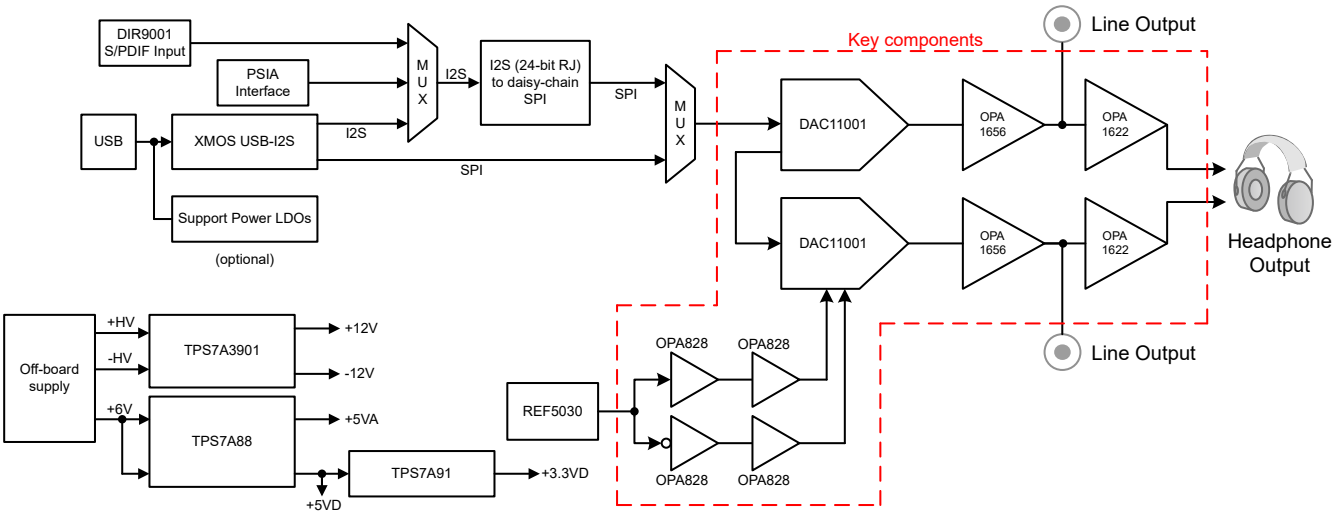


Figure 2-1. TIDA-060031 Block Diagram

2.2 Design Considerations

2.2.1 Differences Between Audio DACs and Precision DACs

There are many types of digital-to-analog converters (DACs) in the marketplace. These include general-purpose voltage-output DACs, highly specialized DACs such as audio DACs, and high-precision DACs like the DAC11001A. There are various architectures for these DACs. Most DACs use a precision resistor architecture like a string divider or R-2R ladder. More specialized DACs feature high-frequency switching architecture like a pulse-width modulator (PWM) or a delta-sigma modulator.

Early audio DACs primarily featured R-2R ladders, but as digital processes improved, multi-segmented delta-sigma architectures began to replace R-2R designs in most products.

There are positive and negative aspects to both of these architectures. For example, R-2R resistor ladders require very precise resistors to be integrated into the design, which can add cost. In addition, most resistor ladder type designs have code-to-code dependent errors, such as glitch, that can impact AC performance.

Delta-sigma designs integrate many forms of error averaging to reduce the impact of errors, reducing the need for precise analog components. However, these DACs require a higher frequency main clock to drive the over-sampling circuit. This clock results in noise at higher frequencies, while R-2R architectures have a flat noise profile.

Practically speaking, using a precision DAC in an audio DAC application can present some difficulties. First, precision DACs require a low-noise and precise reference voltage. Next, precision DACs lack digital features like

volume attenuation with zero-crossing detection. And finally, precision DACs do not accept standard I2S inputs. This means that some digital logic must be added to the design to convert I2S to SPI.

This reference design compares the performance of the DAC11001A and DAC11001B. The DAC11001B features better THD+N performance at higher frequencies compared to the DAC11001A through a more advanced track-and-hold circuit. This circuit, along with the benefits and limitations, are described in Section 2.4.1 *Output Glitch*.

2.2.2 Right-Justified I2S to Daisy-Chained SPI Conversion

Audio devices primarily use the Inter-Integrated Circuit Sound (I2S) protocol for communication. I2S features a bit clock (BCLK), a left-right clock (LRCLK), and a data line. For ease of use, the TIDA-060031 features onboard digital logic to convert a 24-bit, right-justified I2S input into a two-frame daisy-chained SPI output. The DACs are set up in a daisy-chain configuration. This output is latched by the two DAC11001 devices. Figure 2-2 shows the I2S input overlaid with the desired SPI output.

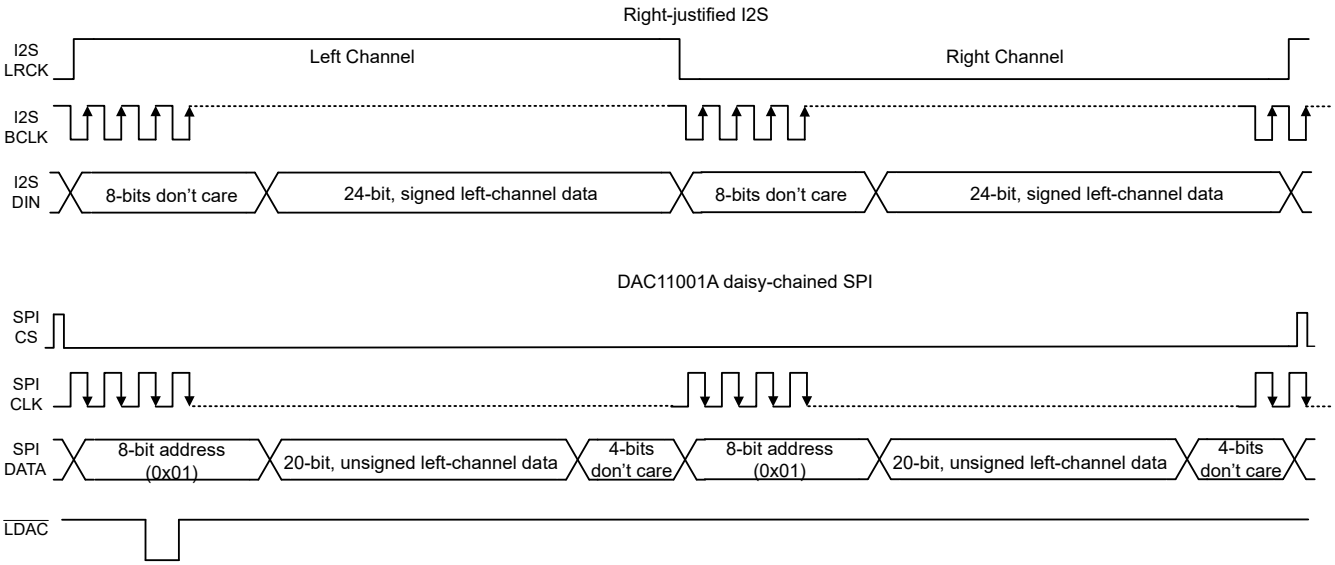


Figure 2-2. I2S to Daisy-Chained SPI

There are some key design challenges to overcome when creating the I2S-to-SPI digital logic.

- The SPI clock is inverted compared to the I2S clock.
- The 8 most-significant bits in the I2S frame are *don't-cares* while the DAC11001 requires this to be the DAC address, 0x01. This is accomplished with the SN74LV165APW, an 8-bit parallel load shift register.
- The four least significant bits (LSBs) for the DAC11001 are *don't-cares*. This is not a major issue as 24-bit data is common in I2S, so no shifting is necessary.
- The LRCK is 50% duty-cycle signal, while the DAC11001 requires an active-low chip select line. The LRCLK is delayed and inverted, and then ANDed with the original LRCLK to produce the CS-high pulse required by the DAC11001s.
- An LDAC signal must be generated for the DACs to latch the data at same time.
- The data value in I2S is a signed 24-bit integer, while the DAC11001A requires an unsigned integer. This means the most-significant bit of the data value must be inverted.

The TIDA-060031 implemented I2S-to-SPI conversion using the logic shown in Figure 2-3.

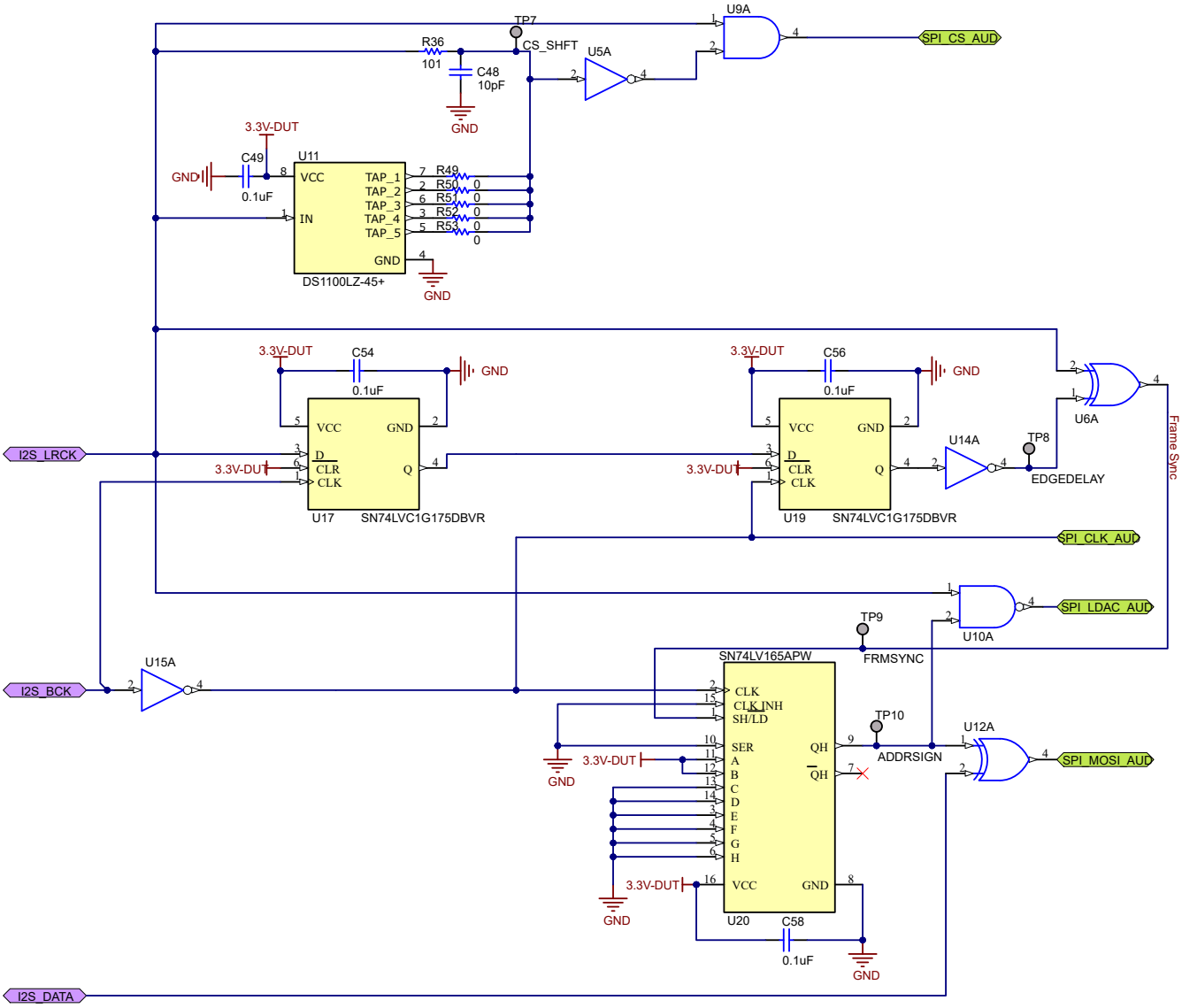


Figure 2-3. Digital Logic for I2S-to-SPI Conversion

2.3 Highlighted Products

2.3.1 DAC11001

The 20-bit DAC11001 is a highly accurate, low-noise, voltage-output, single-channel, digital-to-analog converter. The DAC11001 is specified monotonic by design and offers excellent linearity across all output ranges.

The unbuffered voltage output offers low noise performance (7nV/$\sqrt{Hz}$) in combination with a fast settling time (1µs), making this device an excellent choice for low-noise, fast control-loop, and waveform generation applications. The DAC11001 integrates an enhanced de-glitch circuit with code-independent ultra-low glitch (1nV-s) to enable clean waveform ramps with ultra-low total harmonic distortion (THD).

The DAC11001 incorporates a power-on-reset circuit so that the DAC powers with known values in the registers. With external references, DAC output ranges from V_{REFPF} to V_{REFNF} can be achieved, including asymmetric output ranges.

The DAC11001 features a versatile 4-wire serial interface that operates at clock rates of up to 50MHz. The DAC11001 is specified over the industrial temperature range of –40°C to +125°C.

2.3.2 OPA1656

The OPA1656 is a Burr-Brown™ operational amplifier (op amp) designed specifically for audio and industrial applications where maintaining signal fidelity is crucial. The FET-input architecture achieves a low 2.9nV/√Hz voltage noise density and 6fA/√Hz current noise density, allowing for very low noise performance in a wide variety of circuits. The high bandwidth and high open-loop-gain design of the OPA1656 delivers a low distortion of 0.000035% (–129dB) at 20kHz and improves audio signal fidelity across the full audio bandwidth. This device also features excellent output current drive capability, offering rail-to-rail output swing to within 250mV of the power supplies with a 2kΩ load, and can deliver 100mA of output current.

The OPA1656 operates over a very wide supply range of ±2.25V to ±18V or 4.5V to 36V on 3.9mA of supply current to accommodate the power supply constraints of many types of audio products. The temperature range is specified from –40°C to +125°C. The device is offered in an 8-pin SOIC package.

2.3.3 OPA1622

The OPA1622, dual, bipolar-input, SoundPlus™ audio operational amplifier achieves a very low, 2.8nV/√Hz noise density with an ultra-low THD+N of –119.2dB at 1kHz, while driving a 32Ω load at 100mW output power. The OPA1622 offers extremely high ac PSRR and CMRR specifications that eliminate noise from power supplies, making the OPA1622 an excellent choice for portable-audio applications. This device also has a high output-drive capability of +145mA per –130mA.

The OPA1622 operates over a very wide supply range of ±2V to ±18V, on only 2.6mA of supply current per channel. The OPA1622 op amp is unity-gain stable and provides excellent dynamic behavior over a wide range of load conditions. The OPA1622 includes a shutdown mode, allowing the amplifiers to be switched from normal operation to a standby current that is typically less than 5µA. This shutdown feature is specifically designed to eliminate click and pop noise when transitioning into or out of shutdown mode.

The OPA1622 features a unique internal layout for lowest crosstalk, and freedom from interactions between channels, even when over-driven or overloaded. This device is specified from –40°C to +125°C.

2.3.4 OPA2828

The OPA828 and OPA2828 (OPAx828) JFET input operational amplifiers are the next generation OPA627 and OPA827, combining high speed with high dc precision and ac performance. These op amps supply low offset voltage, low drift over temperature, low bias current, and low noise with only 60nV_{RMS} 0.1Hz to 10Hz noise. The OPAx828 operate over a wide supply-voltage range of ±4V to ±18V and a supply current of 5.5mA/channel, typical.

AC characteristics, including a 45MHz gain bandwidth product (GBW), a slew rate of 150V/µs, and precision dc characteristics, make the OPAx828 family an excellent choice for a variety of systems. These include high-speed and high-resolution data-acquisition systems, such as 16-bit to 18-bit mixed signal systems, trans-impedance (I/V-conversion) amplifiers, filters, precision ±10V front ends, and high-impedance sensor-interface applications.

The OPAx828 are available in an 8-pin SOIC package and a thermally enhanced, 8-pin HVSSOP PowerPAD™ integrated circuit package.

2.4 System Design Theory

2.4.1 Output Glitch

Glitch is a major contributing factor in THD performance. Minimizing glitch is therefore required for high-fidelity audio performance. The main contributor of glitch in R-2R DACs comes from the R-2R switch network.

Typically, R-2R DAC architectures have each bit of resolution comprised of two resistors (R and 2R) and a switch that connects the resistor pair to the DAC positive reference or negative reference voltage. Figure 2-4 shows a simplified example. This architecture acts as a binary-weighted voltage divider. When the relative bit is *high*, the switch connects the R-2R pair to the positive reference. When the bit is *low*, the pair is connected to the negative reference.

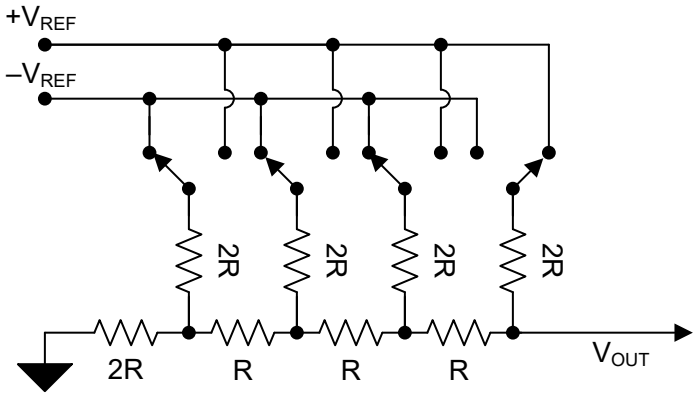


Figure 2-4. R-2R Switch Architecture

DAC glitch is defined as the energy associated with the overshoot or undershoot created by a code transition of a DAC. This glitch can occur even when just transitioning one code. Glitch energy is the result of charge injection from the R-2R switches. In R-2R DACs, code update glitches are large due to each switch representing a bit. The code-to-code glitch is dependent on the number of switches in the resistor ladder changing during a code transition. More individual bits changing results in higher glitch. The worst case code-to-code glitch is found at the mid-scale code transition at code 0x7FFFF and 0x80000 in a 20-bit device. In addition, the R-2R ladder commonly requires the use of larger switches which have larger capacitance. The higher capacitance increases the charge injection of each of the switches. Most R-2R DACs feature a *two-lobe* glitch output, where the output has a small overshoot into a large undershoot when the DAC output increases. This over- and undershoot is characteristic of the R-2R switches opening and then closing. Figure 2-6 shows an example of two-lobe glitch. The code-dependent glitch energy is detectable in the output spectrum as increases in higher-order harmonics or as additional spurs at non-harmonic frequencies.

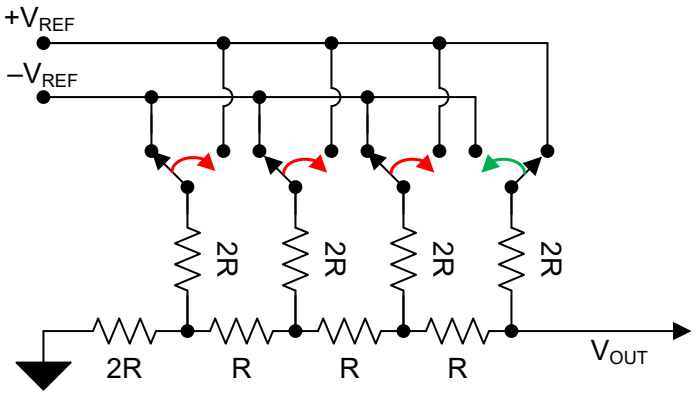


Figure 2-5. R-2R Switches Mid-Scale Code Transition

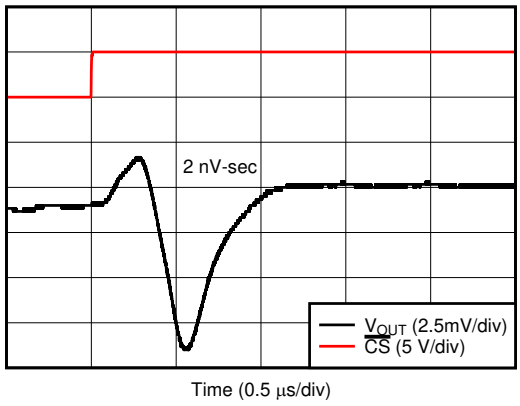


Figure 2-6. R-2R Output Glitch

The DAC11001 devices feature a complex and high-performing track-and-hold (TnH) circuit to reduce the code-to-code glitch impacts of the 20-bit, R-2R resistor ladder used in the device. Figure 2-7 shows this circuit. The circuit features a switch and a sample capacitor on the output of the R-2R ladder. When the DAC code updates, the track-and-hold switch opens before the R-2R ladder changes. The sample capacitor holds the voltage stable at the initial voltage, shown as $V_{POST-TnH}$. After the R-2R ladder has finished updating, the track-and-hold switch closes, updating the output voltage. The track-and-hold circuit significantly reduces the glitch when the DAC changes at the expense of the DAC update rate. Figure 2-8 shows a comparison of the output glitch with the track-and-hold enabled and disabled.

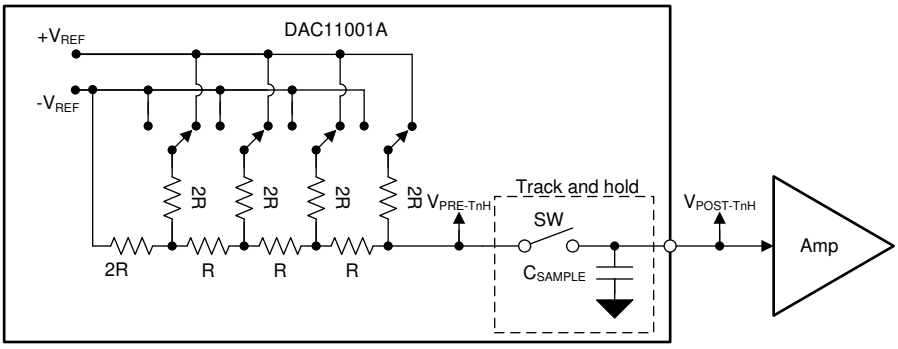


Figure 2-7. DAC11001 Track-and-Hold Diagram

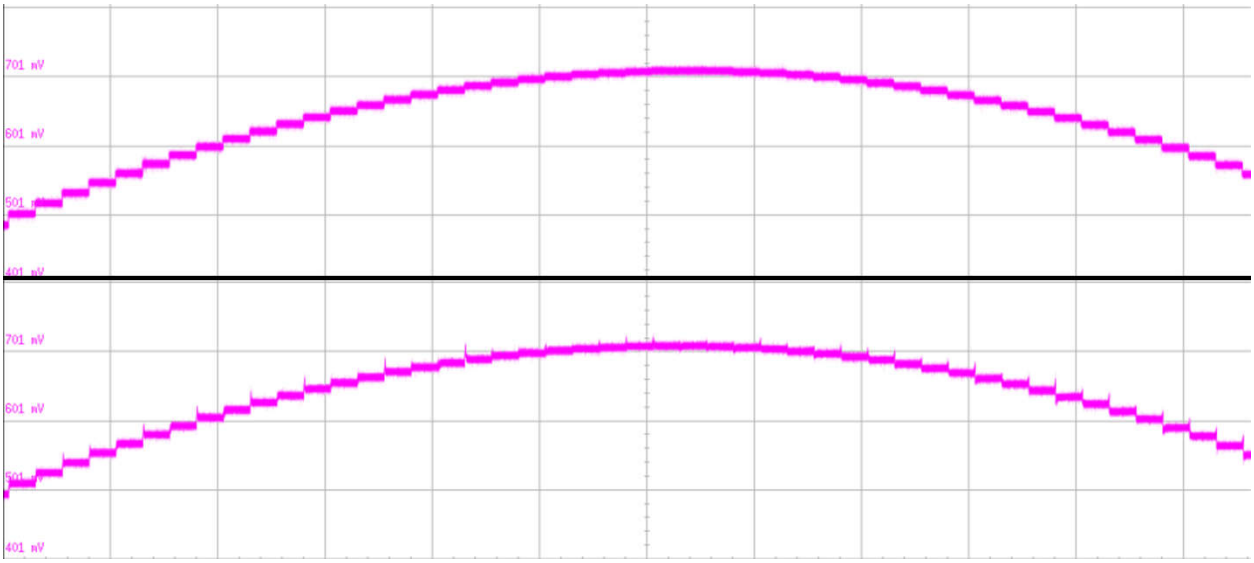


Figure 2-8. DAC11001 Track-and-Hold Enabled vs Disabled

The effectiveness of the TnH circuit is tested by measuring THD+N with the circuit on and off using a 1kHz tone at a sample rate of 192kSPS. With the TnH circuit on, the THD+N measurement is –107dB. With the circuit off, the THD+N measurement is –73dB. This is a difference of 34dB, or roughly 50 times worse performance.

Additionally, whenever the R-2R switches change position, the reference input impedance changes. Figure 2-9 shows the code-to-code change effect on the reference. This sudden impedance change causes a small glitch on the reference in the form of a voltage droop. While the track-and-hold circuit helps mitigate this glitch, it is important that the reference settles before the track-and-hold switch opens. Fast-settling reference buffers are required to minimize the glitch from the reference.

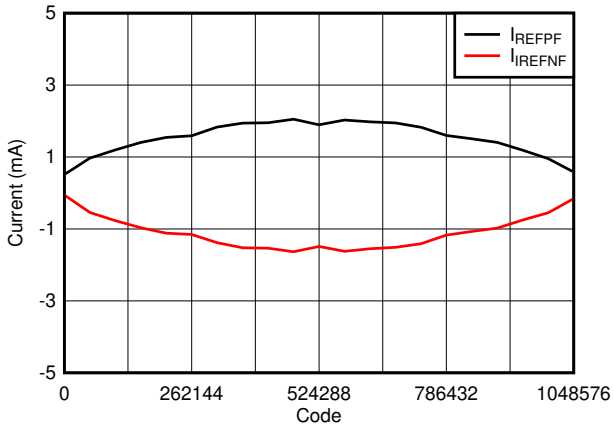


Figure 2-9. Reference Current vs DAC Code

2.4.2 Sample Rate Dependence in Precision DACs

A higher sample rate decreases DAC output distortion by reducing quantization noise. Precision DACs, unlike high-speed DACs and audio DACs, have low sample rates of typically less than 1MSPS. Precision DACs have a threshold where sample rate is limited by the output settling time. The output buffer must be able to settle within each DAC code update to prevent output signal distortion.

Devices that feature a track-and-hold circuit have additional barriers to high sample rates. The track-and-hold circuit has a set amount of time for the switch to remain open after each DAC update. The output distorts if the sample rate exceeds the track-and-hold sample period.

Delta-sigma designs feature other forms of error averaging, so these DACs do not have this track-and-hold limitation.

2.4.3 System Noise

In noise-sensitive applications, the goal is to minimize the DAC noise as much as possible to achieve the best possible performance. There are multiple sources of noise to consider when designing a system with an unbuffered R-2R precision DAC. Major sources of noise include the power supply, the DAC reference, the reference buffers, the DAC output amplifier, and the DAC R-2R resistor network. Intentional component selection helps reduce the noise.

A noisy supply can have a detrimental effect on system noise performance. Supply noise can be suppressed through input filters and through decoupling and bypass capacitors. Decoupling capacitors reduce the effects of voltage sags. Bypass capacitors act as a low-pass filter to reduce the effects of high-frequency noise from the power supply. Selecting devices with high power supply rejection ratio (PSRR) performance also helps reduce the effect of a noisy supply. AC PSRR is the ability of a device to reject noise and oscillations from the supply. Table 2-1 shows the devices selected in the reference design and the data sheet PSRR values.

Table 2-1. PSRR of Reference Design Devices

DEVICE	PSRR (1kHz)
DAC11001	95dB
REF5030	130dB
TPS7A39	69dB
TPS7A88	70dB
TPS7A90	60dB

Reference noise has a direct effect on the DAC THD+N performance, as any noise from the reference feeds through to the DAC output. Reference noise can be minimized by selecting a reference with good noise performance. Certain reference devices, such as the REF5030, have a dedicated Trim pin or Noise pin that can be used to improve noise performance. Additional methods of noise reduction include adding low-pass filters and selecting a low-noise output buffer. A buffer for the reference must contend with the need for fast settling, as stated in the output glitch section. Finding a compromise between fast settling and low noise represents the best approach.

Unbuffered R-2R DACs like the DAC11001 often feature higher output impedance due to the R-2R resistor network. When selecting an output buffer, the higher DAC output impedance can make current noise more of a concern than voltage noise. Table 2-2 shows the noise performance of different op amp input architectures. Op amps with bipolar inputs feature very low voltage noise, but have higher current noise. CMOS op amps, such as the OPA1656, favor low current noise at the expense of slightly higher voltage noise. Figure 2-10 shows the noise simulation that is created in TINA-TI™ to compare different op amps tied to a high-impedance output. Figure 2-11 shows the results of this noise simulation. The two CMOS op amps perform better than the bipolar OPA1612. With an R-2R DAC, the CMOS op amp results in better noise performance overall because of the reduction of current noise.

Table 2-2. Op Amp Noise Comparison

OP AMP	INPUT STAGE	VOLTAGE NOISE AT 1kHz	CURRENT NOISE AT 1kHz
OPA1612	Bipolar	1.1nV/√Hz	1700fA/√Hz
OPA1656	CMOS	4.3nV/√Hz	6fA/√Hz
OPA1678	CMOS	4.5nV/√Hz	3fA/√Hz

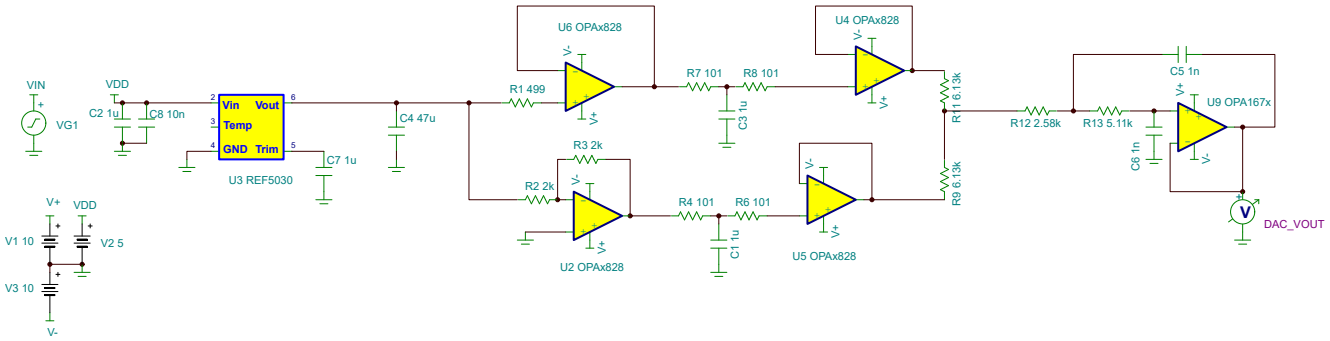


Figure 2-10. TINA-TI™ Noise Simulation

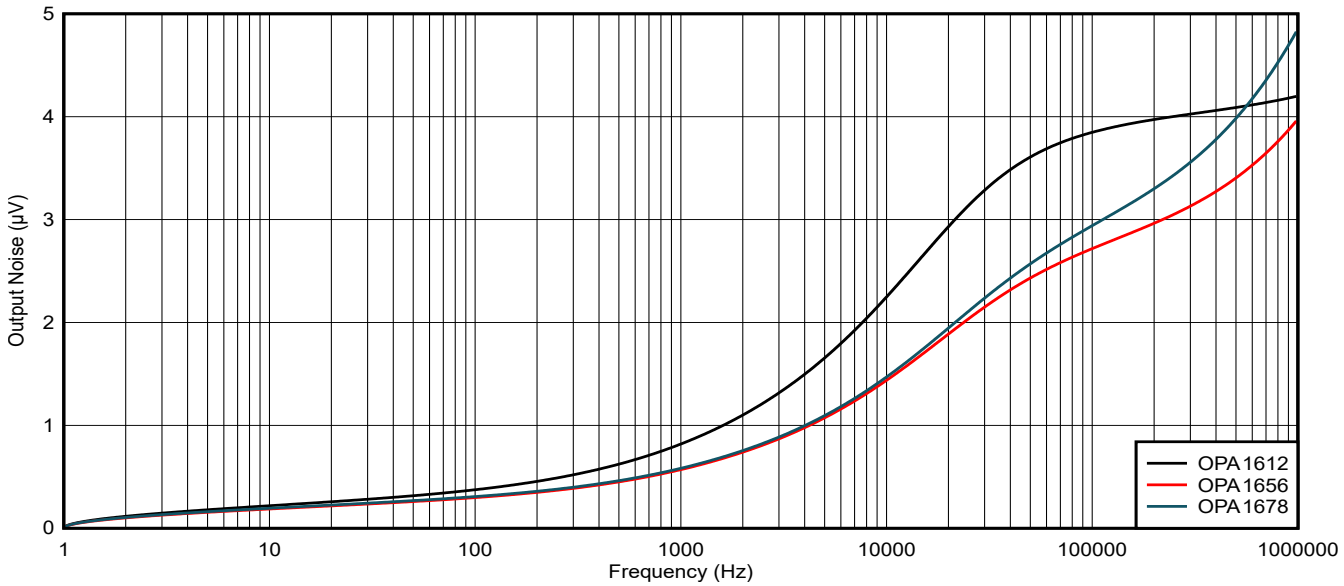


Figure 2-11. Op Amp Noise Simulation Comparison

2.4.4 DAC11001A vs DAC11001B

The DAC11001B is an enhanced version of the DAC11001A. These enhancements include lower integral nonlinearity (INL) and an improved track-and-hold circuit (TnH).

INL, also called relative accuracy, measures the difference between the actual DAC output and the expected theoretical output for each code. This parameter is commonly noted in least significant bits, or LSBs. Mathematically, INL is the sum of each individual code-to-code error of previous codes. The DAC11001A has a maximum 4LSB error, this means an individual code has the potential of being up to four LSBs away from the best possible output, not including offset and gain error. The DAC11001B has maximum 1LSB error, providing a significantly more accurate output. Figure 2-12 and Figure 2-13 show the INL comparison from the two datasheets.

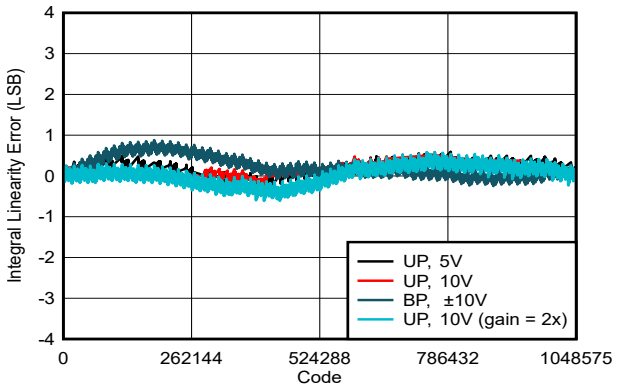


Figure 2-12. DAC11001A INL

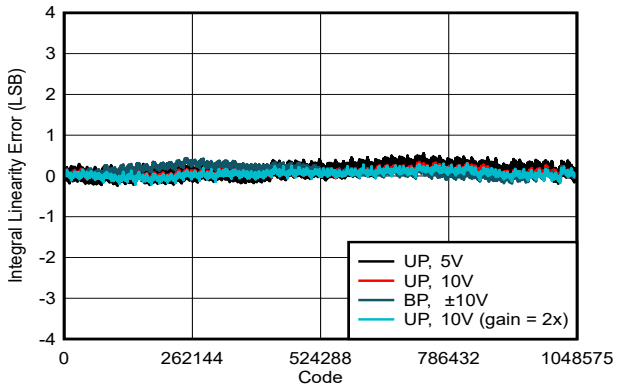


Figure 2-13. DAC11001B INL

The DAC11001A and DAC1001B both implement track-and-hold subcircuits to reduce the impact of code-to-code glitch. As described in the *Output Glitch* section, the TnH circuit separates the output from the R-2R ladder during a DAC update with a switch. This switch is a complementary PMOS or NMOS structure. These MOSFETs can turn into parasitic diodes when the voltage across the switch is higher than some threshold. In the DAC11001A, Figure 2-14 shows that the TnH causes the output to slew when the differential voltage is greater than around 1V. This limitation is improved on the DAC11001B, as shown in Figure 2-15.

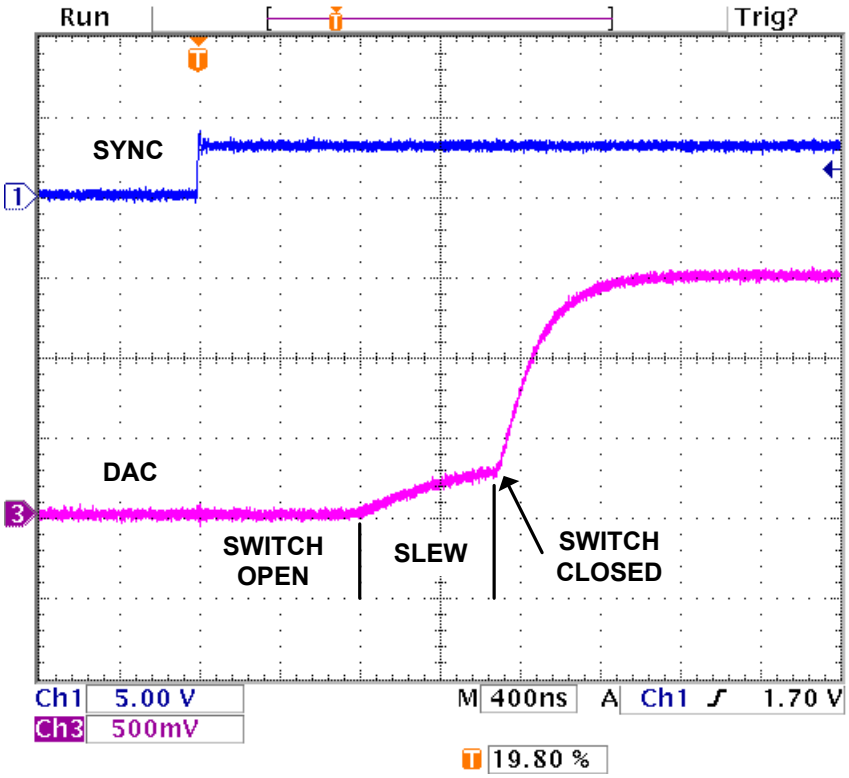


Figure 2-14. DAC11001A Track-and-Hold Voltage Feedthrough

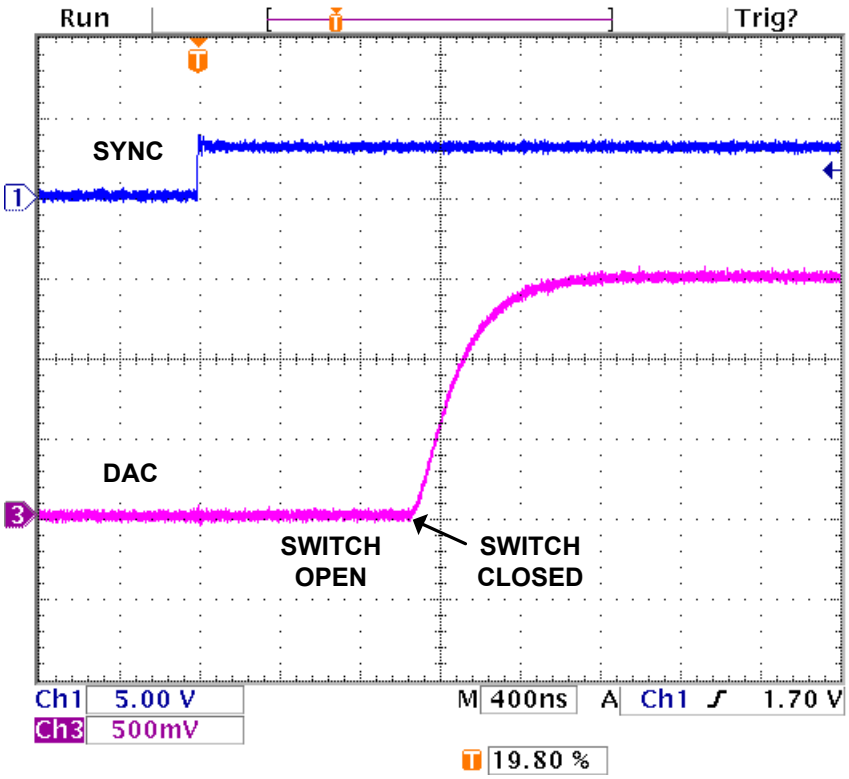


Figure 2-15. DAC11001B Track-and-Hold No Voltage Feedthrough

This TnH issue directly impacts THD+N through output distortion. Three parameters effect the DAC11001A TnH circuit: sample rate, output amplitude, and tone frequency. A low sample rate increases the time between output updates, potentially resulting in larger voltage steps between DAC updates. A larger DAC output range directly

increases the voltage change amplitude. With a constant sample rate, increasing the tone frequency can cause the output to require larger voltage changes. Any of these affected parameters can be addressed by giving sufficient headroom in the other parameters. For example, a high output range is less likely to cause an issue if the sample rate is sufficiently high.

Figure 2-16 shows how these different parameters affect the THD+N of the DAC11001A and DAC11001B across the frequency spectrum. The figure compares the 0dB and –30dB amplitudes of the two DACs. The 0dB output range of the reference design is ±3V. All four data sets are measured with a constant sample rate of 192kSPS. At 0dB, DAC11001A starts degrading in THD+N at 1kHz. As the frequency increases, the voltage change amplitude with each update increases, and this causes the track-and-hold circuit to produce more distortion. The DAC11001B does not start degrading until 5kHz due to the improved TnH circuit. In the –30dB DACs, the THD+N measurements do not degrade until 10kHz. The lower amplitude reduces the maximum amplitude of the voltage update changes, and in turn prevents the additional TnH distortion. While the TnH circuit does not produce distortion, the overall THD+N measurements are worse with the –30dB amplitude because the DAC output amplitude is closer to the noise floor.

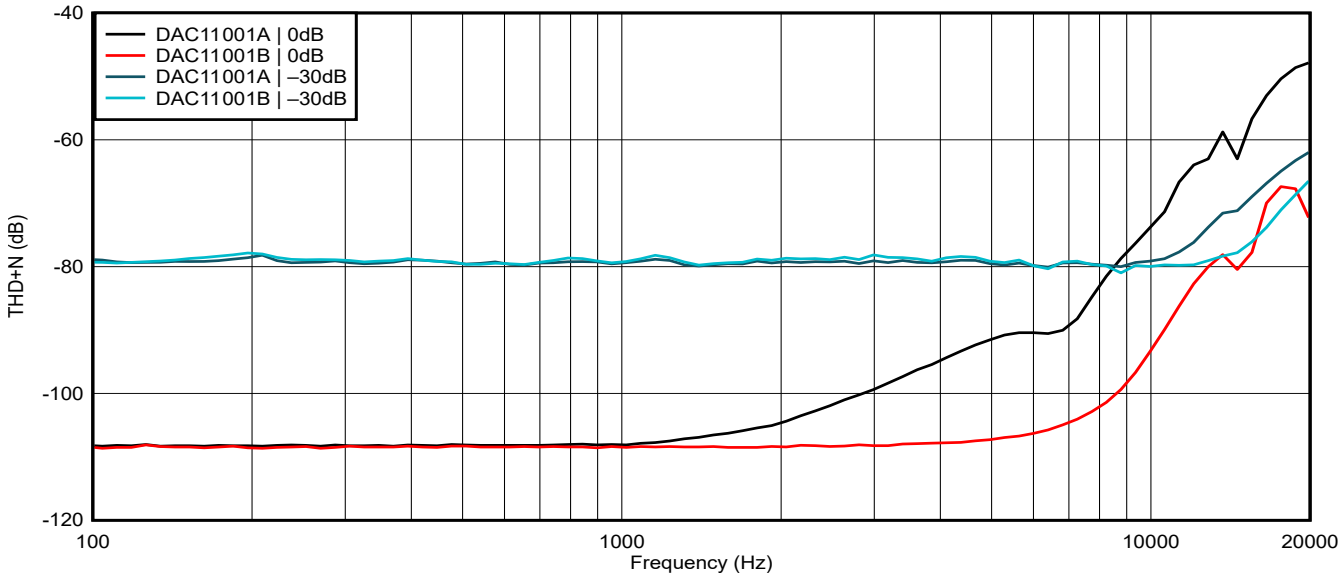


Figure 2-16. Track-and-Hold Circuit Comparison

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

3.1.1 Required External Power Supplies

The TIDA-060031 requires two power supply sources. The left side of the design primarily features support circuitry for the digital input and USB interface. Figure 3-1 shows that the circuitry can be supplied by the USB input or from the external supplies through the power bridge.

The right side of the board features the critical analog circuitry, specifically the DAC, DAC reference and reference buffers, and the DAC output buffers. This side also features some digital control circuitry used to manage the SPI data-path and to convert the incoming RJ I2S data to a daisy-chained SPI format. This side of the board requires external power.

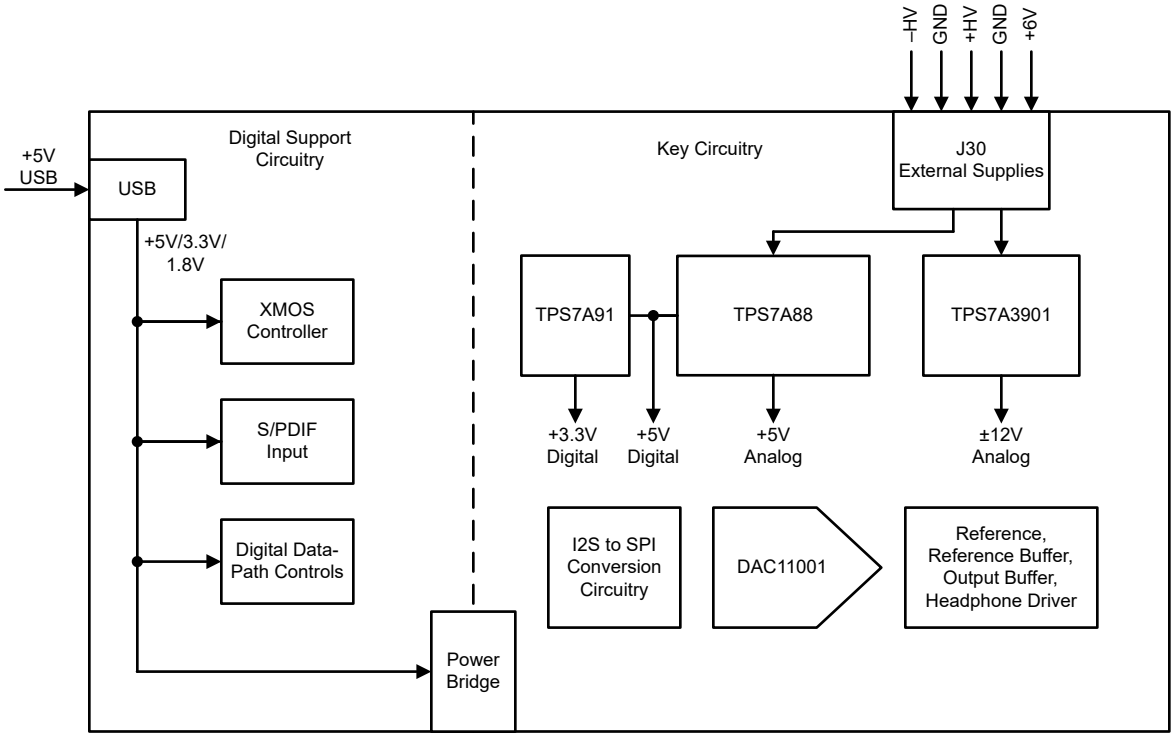


Figure 3-1. Power Supply Configuration

Figure 3-1 shows the power inputs for the TIDA-060031 design. The terminal block, J30, is used for an external supply for the key circuitry. Table 3-1 shows the J30 definitions.

Table 3-1. Power Supply Inputs

J30 PIN	DESCRIPTION	VALUE AND LIMITS
J30.1	Low-voltage supply +6V. This supply is used for the 5V analog, 5V digital, and 3.3V digital supplies for the key circuitry.	+6V input, 300mA limit
J30.2	Ground	Ground
J30.3	Positive high-voltage supply input. This is used for the +12V supply for the key circuitry.	+12.5 to +15V, 200mA limit
J30.4	Ground	Ground
J30.5	Negative high-voltage supply input. This is used for the –12V supply for the key circuitry.	–12.5V to –15V, 200mA limit

If the USB input is not being used (I2S is provided by the S/PDIF input or connected directly to the design), then the USB supply is not needed. The +3.3V supply from the key circuitry side can be used to power the minimal support circuitry from the left side of the board. This can be accomplished by connecting the 3.3V supply on the power bridge (J29, position 1-2).

3.1.2 Jumper Definitions

Table 3-2 details the jumper definitions.

Table 3-2. Jumper Definitions

JUMPER	NAME	DESCRIPTION
J1, J2	S/PDIF Format Selection	FMT1 SHORT, FMT0 SHORT: 16-bit, MSB-first, right-justified FMT1 SHORT, FMT0 OPEN: 24-bit, MSB-first, right-justified. **DEFAULT**, this is the only supported format from the TIDA-060031. FMT1 OPEN, FMT0 SHORT: 24-bit MSB-first, left-justified FMT1 OPEN, FMT0 OPEN: 24-bit, MSB-first, I2S
J10	External LDAC Selection	**SHORT**: Short LDAC to ground. **OPEN**: LDAC is pulled up to 3.3V.
J11	USB Power Selection	**SHORT 1-2** (5V-IN): J12 is used as the +5V input to the left side of board. **SHORT 2-3** (5V-USB): Recommended, the USB input is used to source the left side of board.
J13	BCLK Selection	**SHORT 2-3**: The USB or S/PDIF BCLK input is selected as the I2S Source. **External connection to 1-2**: Pin 1 is ground. This allows an external I2S BCLK source (such as a PSIA) to be connected to the EVM.
J14	MCLK Selection	**SHORT 2-3**: The USB or S/PDIF MCLK input is selected as the I2S Source. This is not needed on the TIDA-060031 as no MCLK signal is used. **External connection to 1-2**: Pin 1 is ground. This allows an external I2S source (such as a PSIA) to be connected to the EVM.
J15	DIN Selection	**SHORT 2-3**: The USB or S/PDIF DIN input is selected as the I2S source. **External connection to 1-2**: Pin 1 is ground. This allows an external I2S DIN source (such as a PSIA) to be connected to the EVM.
J16	LRCK Selection	**SHORT 2-3**: The USB or S/PDIF LRCK input is selected as the I2S Source. **External connection to 1-2**: Pin 1 is ground. This allows an external I2S LRCK source (such as a PSIA) to be connected to the EVM.
J17	DIR9001 (S/PDIF) Input Select	**SHORT**: Connects the DIR9001 input to the I2S data path. **OPEN**: Connects the USB I2S source to the I2S data path.
J19	I2S Target Select	Not supported on the TIDA-060031, leave open.
J20	I2S TDM Mode Select	Not supported on the TIDA-060031, leave open.
J21	XMOS High-Speed USB	**SHORT**: Allows the TIDA-060031 to be detected as a USB2.0 device and to support 192kHz sample rates.
J22	JTAG Input	This header allows for JTAG inputs.
J24	SPI Source Select	**SHORT**: The SPI output of the I2S to SPI conversion circuit is connected to the DAC11001A devices. **OPEN**: The SPI input from the SPI input bridge (J25) is connected to the DAC11001A devices.

Table 3-3. Input and Output Connectors

JUMPER	NAME	DESCRIPTION
J5	Headphone Output	Headphone output. Combines the left and right DAC output.
J6	Left-Side Phonograph Jack	Left-side line output.
J7	Right-Side Phonograph Jack	Right-side line output.
J12	5V Digital Input	5V DC power jack for the digital side.
J23	USB Input	USB input. Leave unplugged if not required.

Table 3-4. I2S, SPI, GPO, and Power Bridge

JUMPER	NAME	DESCRIPTION
J8	I2S Connection Bridge	This connection allows I2S inputs to be connected to the DAC and support circuitry. The TIDA-060031 reference design only requires LRCK, BCLK, and DIN.
J9	I2C Connection Bridge	The TIDA-060031 reference design does not use I2C.
J18	I2S to Ground	This header connects the I2S signals to ground. These connections can be left unpopulated.
J25	SPI Connection Bridge	This connection allows the XMOS controller to generate SPI for configuration of the DAC11001A devices. By default, the reference design does not require configuration. Specialized software is needed to operate the SPI. By default, these connections can be left unpopulated.
J26	GPO Connection Bridge	This connection allows the XMOS controller to set a few control lines in use with SPI. By default, these can be left unpopulated.
J27	SPI Input	This connection can be used to bypass the I2S circuitry if SPI is used instead.
J28	PICO-LDAC to GND	This connection shorts SPI PICO and LDAC to ground.
J29	Power Connection Bridge	This connection allows power to be shared between the reference design and the USB controller. By default, this connection can be left unpopulated. A jumper can be placed on J29.1-2 (3.3V) to power the 3.3V circuitry on the left side of the board. This is useful if an external or S/PDIF input is being used, as the USB input is undesired.

3.1.3 Selecting I2S Source

This section describes the various input configurations which can be used with TIDA-060031 reference design.

3.1.3.1 USB I2S Source

The easiest method for evaluating the DAC11001A for audio performance is to use the USB input. Figure 3-2 shows the jumper configurations for selecting the USB input.

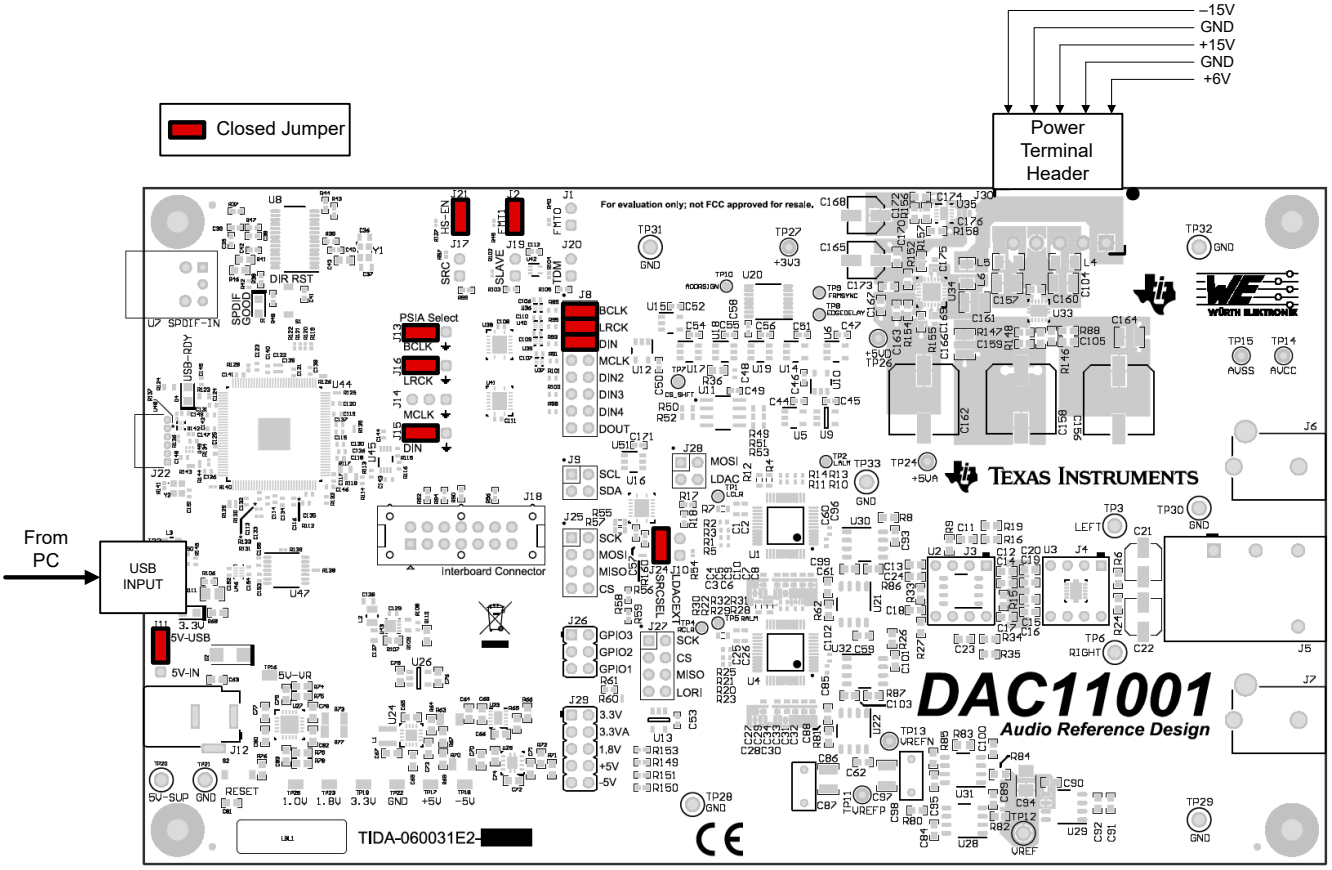


Figure 3-2. USB I2S Input Configuration

3.1.3.2 SPDIF I2S Source

Figure 3-3 shows the jumper configurations for using an optical SPDIF input as the audio source in the TIDA-060031 reference design. This only supports 48kSPS inputs.

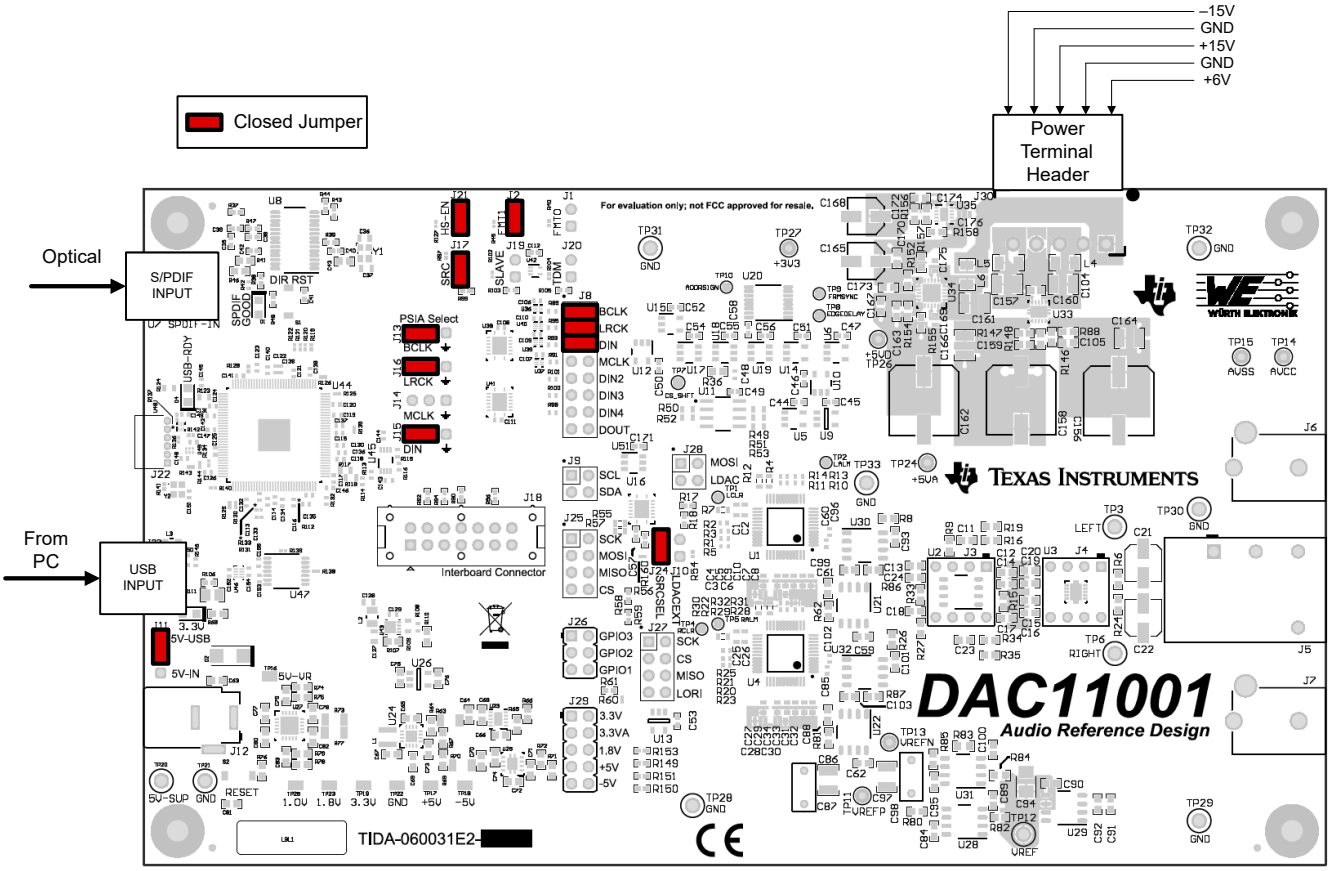


Figure 3-3. S/PDIF I2S Input Configuration

3.1.3.3 External PSIA I2S Source

An external I2S input can provided to the TIDA-060031 by using the PSIA input headers J13-J16. Accomplish this by removing the jumpers on J13-J16 and connecting the I2S input to the headers in the 1-2 position. Pin 1 on the header is connected to ground for a cleaner digital connection. The I2S input must be configured in 24-bit right-justified mode.

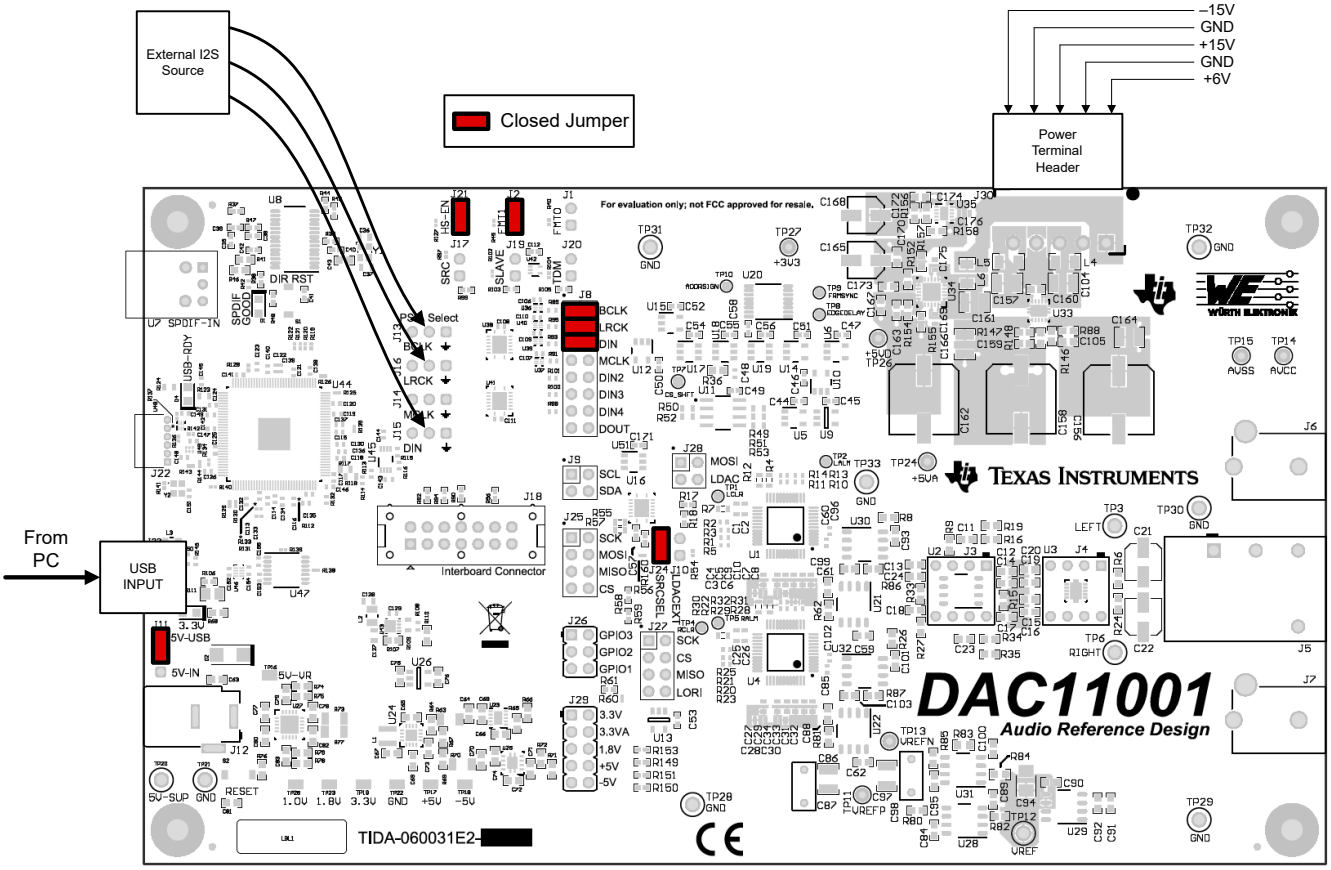


Figure 3-4. External I2S Input Configuration

3.2 Software Requirements

The TIDA-060031 reference design does not require any control software. A driver is required for the USB interface. The easiest method to install the driver is to install PurePath™ Console Software.

3.2.1 Installing the XMOS USB 2.0 Driver

The PurePath Console Software is accessible by requesting access at the landing page: PurePath Console. Once access has been granted, download the software from ti.com/secureresources.

Once the driver is successfully installed, the TIDA-060031 is detected by the PC as *TUSBAudio Eval UAC2.0 (BB04)*.

3.2.2 Setting USB Sample Rate

The sample rate of the USB input is determined by the sample rate settings for the audio device in the settings of the PC. Access the device properties to set the sample rate. Figure 3-5 shows the use of 24-bit, 190000Hz for testing. Microsoft® Windows® requires restarting any software that plays an audio source after changing the rate.

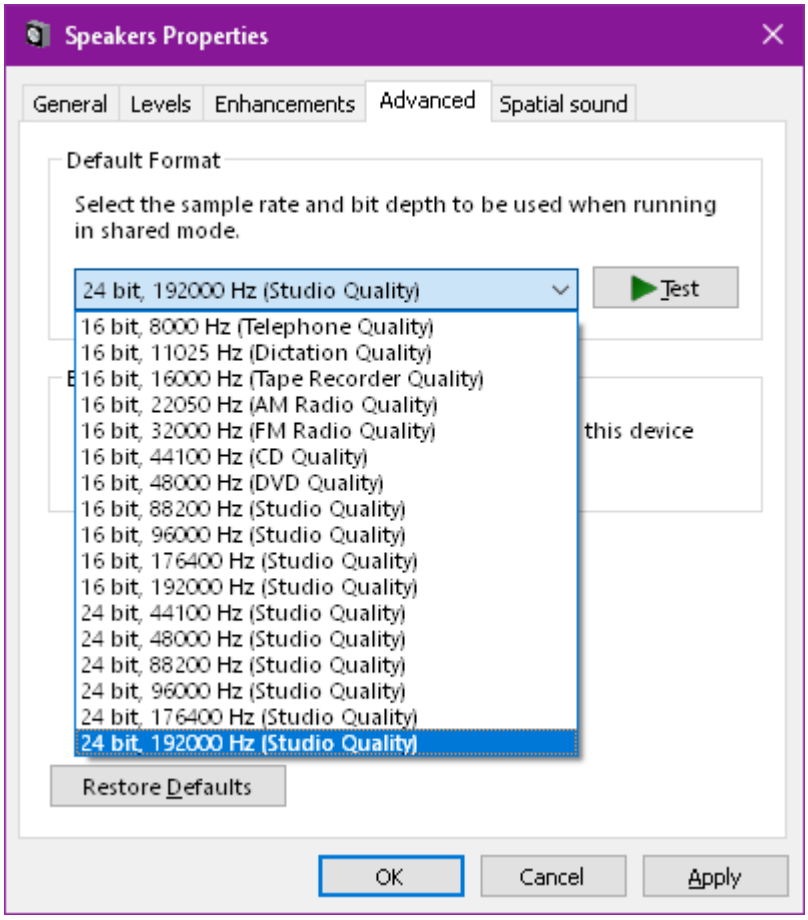


Figure 3-5. Speaker Properties Menu for Selecting Sample Rate

3.3 Testing and Results

3.3.1 Measuring Total Harmonic Distortion and Noise

The THD+N is measured using an Audio Precision System 2 (AP2). The AP2 is provided an external I2S source, configured for 24-bit data in a right-justified output pattern. The I2S signals are connected to the I2S input connectors J13-J16 on the TIDA-060031 design.

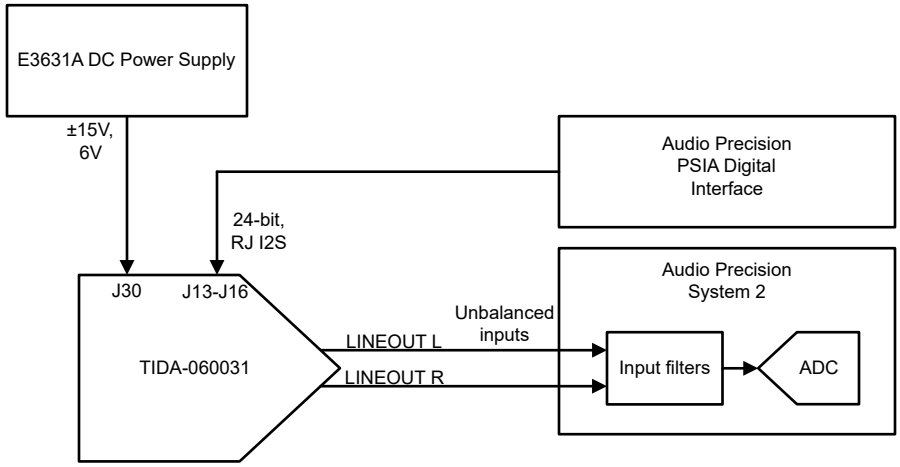


Figure 3-6. THD+N Measurement Setup

Table 3-5. THD+N Input Filters

SAMPLE RATE	FILTER
48kSPS	22Hz high-pass filter, 20kHz AES17 low-pass filter
96kSPS	22Hz high-pass filter, 40kHz AES17 low-pass filter
192kSPS	22Hz high-pass filter, 40kHz AES17 low-pass filter

3.3.2 THD and THD+N Results

Table 3-6 and Table 3-7 show the THD+N measurement results across various amplitudes, tones, and sample rates.

Table 3-6. DAC11001A THD+N Measurement Results

INPUT AMPLITUDE	TONE FREQUENCY	SAMPLE RATE		
		48kSPS	96kSPS	192kSPS
0dBFS	1kHz	–107dB	–107dB	–108dB
	2kHz	–94dB	–101dB	–106dB
	5kHz	–56dB	–74dB	–92dB
	10kHz	–49dB	–45dB	–73dB
–60dBFS	1kHz	–55dB	–51dB	–50dB
	2kHz	–54dB	–50dB	–49dB
	5kHz	–56dB	–50dB	–49dB
	10kHz	–57dB	–50dB	–50dB

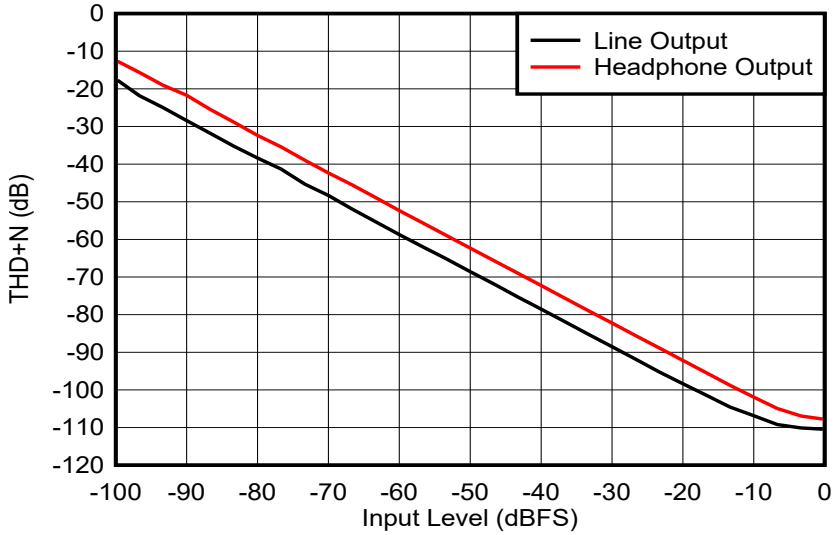
Table 3-7. DAC11001B THD+N Measurement Results

INPUT AMPLITUDE	TONE FREQUENCY	SAMPLE RATE		
		48kSPS	96kSPS	192kSPS
0dBFS	1kHz	–111dB	–108dB	–108dB
	2kHz	–110dB	–108dB	–108dB
	5kHz	–75dB	–97dB	–106dB
	10kHz	–47dB	–69dB	–92dB

Table 3-7. DAC11001B THD+N Measurement Results (continued)

INPUT AMPLITUDE	TONE FREQUENCY	SAMPLE RATE		
		48kSPS	96kSPS	192kSPS
–60dBFS	1kHz	–55dB	–51dB	–50dB
	2kHz	–53dB	–50dB	–49dB
	5kHz	–55dB	–50dB	–40dB
	10kHz	–57dB	–50dB	–50dB

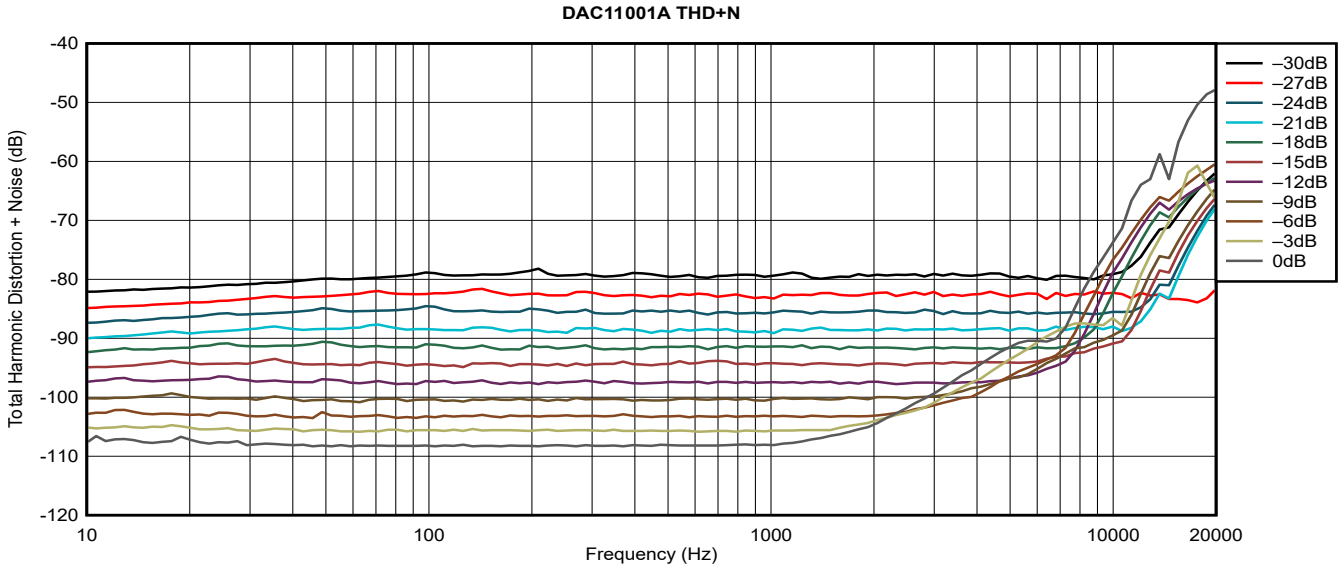
Figure 3-7 shows the THD+N improving as the input level magnitude increases. This is because the magnitude of the DAC output is increasing as the noise level stays the same. The linear decline of the THD+N value shows that the THD+N is dominated by noise. The headphone amplitude is around 12dB lower than the line amplitude, which is reflected in the slightly worse THD+N results.



500Hz sine-wave input, sampling frequency = 192kSPS

Figure 3-7. Line and Headphone Output THD+N vs Input Level

The behavior shown in Figure 3-8 demonstrates the enhanced performance of the DAC11001B track-and-hold design compared to the DAC11001A. The DAC11001B maintains a flatter THD+N profile across higher frequencies.



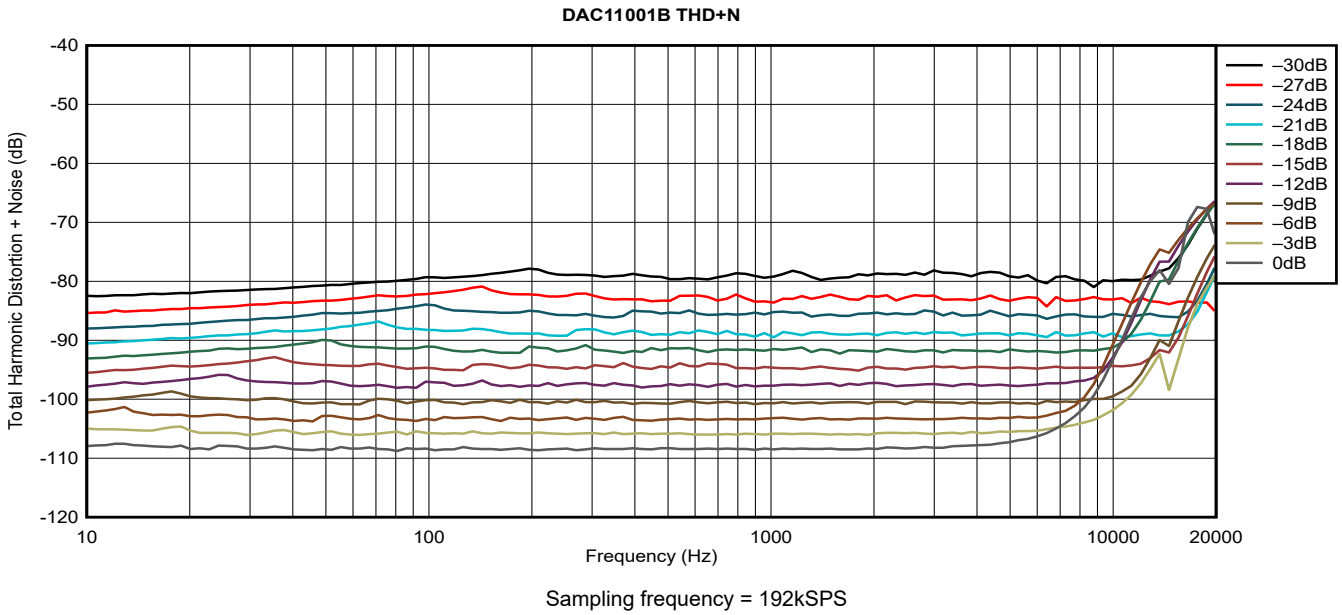


Figure 3-8. Line Output THD+N vs Frequency and Amplitude

Figure 3-9 shows the noise and harmonic performance of the DAC11001 with a 10k tone.

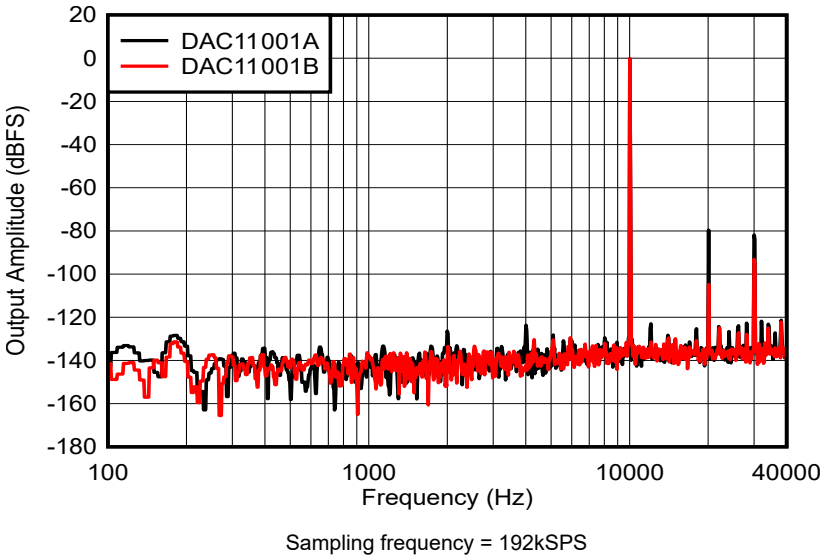


Figure 3-9. FFT of Audible Range With 10kHz Sine Wave

3.3.3 Measuring Dynamic Range

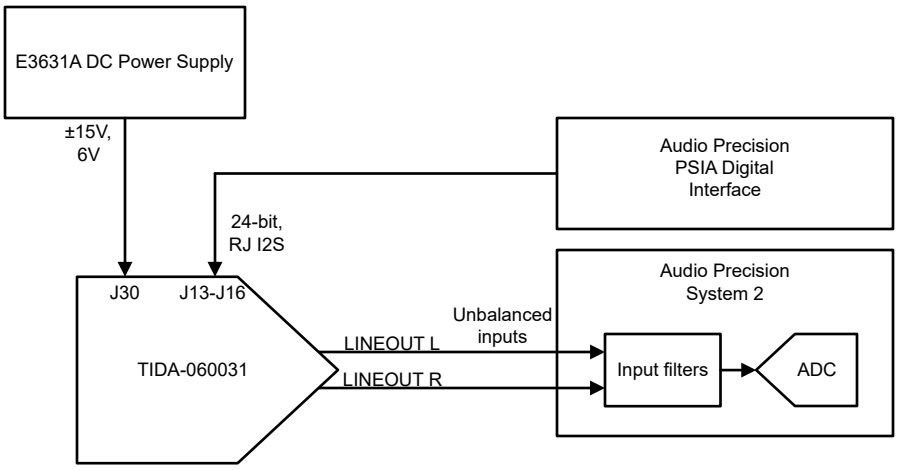


Figure 3-10. Dynamic Range Measurement Setup

Table 3-8. Dynamic Range Input Filters

SAMPLE RATE	FILTER
48kSPS	22Hz high-pass filter, 20kHz AES17 low-pass filter, A-weighted
96kSPS	22Hz high-pass filter, 40kHz AES17 low-pass filter, A-weighted
192kSPS	22Hz high-pass filter, 40kHz AES17 low-pass filter, A-weighted

3.3.4 Dynamic Range Results

Table 3-9 shows the dynamic range of the DAC11001.

Table 3-9. Dynamic Range Measurement Results

INPUT AMPLITUDE	TONE FREQUENCY	SAMPLE RATE		
		48kSPS	96kSPS	192kSPS
–60dBFS	1kHz	–117dB (THD+N: –57dB)	–117dB (THD+N: –57dB)	–115dB (THD+N: –55dB)
	2kHz	–118dB (THD+N: –58dB)	–117dB (THD+N: –57dB)	–115dB (THD+N: –55dB)
	10kHz	–113dB (THD+N: –53dB)	–118dB (THD+N: –58dB)	–119dB (THD+N: –59dB)

3.3.5 Measuring Signal-to-Noise Ratio

Figure 3-11 shows the SNR measurement setup.

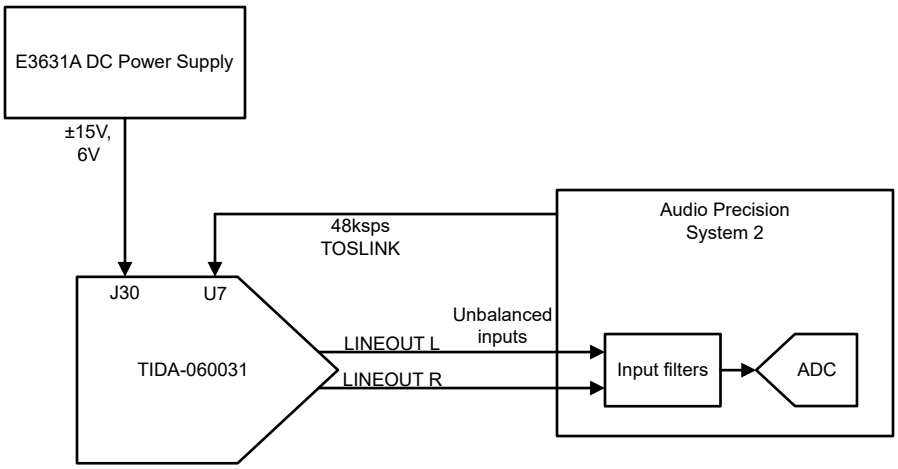


Figure 3-11. SNR Measurement Setup

Table 3-10. SNR Input Filter

SAMPLE RATE	FILTER
48kSPS	22Hz high-pass filter, 20kHz AES17 low-pass filter, A-weighted
96kSPS	22Hz high-pass filter, 40kHz AES17 low-pass filter, A-weighted
192kSPS	22Hz high-pass filter, 40kHz AES17 low-pass filter, A-weighted

3.3.6 SNR Results

Table 3-11 and Table 3-12 show the SNR results of the DAC11001A and DAC11001B. Some noise is generated from the digital transmitter, resulting in a slightly worse SNR. The SNR with the digital transmitter turned off is shown in Table 3-13.

Table 3-11. DAC11001A Signal-to-Noise Ratio Measurements

INPUT AMPLITUDE	TONE FREQUENCY	SAMPLE RATE		
		48kSPS	96kSPS	192kSPS
100% Full-scale	1kHz	2.115V_{RMS}	2.112V_{RMS}	2.112V_{RMS}
0% Full-scale, no dither	N/A	1.893μV_{RMS}	2.038μV_{RMS}	2.29μV_{RMS}
Calculated SNR		120.9dB	120.3dB	119.3dB

Table 3-12. DAC11001B Signal-to-Noise Ratio Measurements

INPUT AMPLITUDE	TONE FREQUENCY	SAMPLE RATE		
		48kSPS	96kSPS	192kSPS
100% Full-scale	1kHz	2.115V_{RMS}	2.112V_{RMS}	2.112V_{RMS}
0% Full-scale, no dither	N/A	1.858μV_{RMS}	2.039μV_{RMS}	2.325μV_{RMS}
Calculated SNR		121.1dB	120.3dB	119.2dB

Table 3-13. DAC11001 Signal-to-Noise Ratio with no Digital

INPUT AMPLITUDE	TONE FREQUENCY	RESULT
100% Full-scale	1kHz	2.115V_{RMS}
0% Full-scale, no TX	N/A	1.732μV_{RMS}
Calculated SNR		121.7dB

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-060031.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-060031.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-060031.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-060031.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-060031.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-060031.

5 Related Documentation

1. Texas Instruments, *DACx1001 20-Bit, 18-Bit, and 16-Bit, Low-Noise, Ultra-Low Harmonic Distortion, Fast-Settling, High-Voltage Output, Digital-to-Analog Converters (DACs) Data Sheet*
2. Texas Instruments, *DAC11001B 20-Bit, Low-Noise, Ultra-Low Harmonic Distortion, Fast-Settling, High-Voltage-Output, Digital-to-Analog Converter (DAC) Data Sheet*
3. Texas Instruments, *Understanding Op Amp Noise in Audio Circuits Application Report*
4. Texas Instruments, *Tips and Tricks for Designing with Voltage References E-Book*

5.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Last updated 10/2025