Application Note

Throughput Characterization of OSPI and QSPI Serial NOR/NAND Flash Operations on MCU+ SDK

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ABSTRACT

This application note provides a comprehensive Flash memory performance profiling for TI's Sitara™ MPU family (AM243x, AM62x, AM62Ax, AM64x, AM62Px, AM62Dx, AM275x processors), addressing the critical need for optimizing Flash memory throughput across different operational modes and configurations. The target audience for this is embedded engineers and developers working on industrial and automotive applications.

This document benchmarks NOR OSPI, NOR QSPI, and NAND OSPI Flash parts under various settings including DMA, PHY, clock frequencies, and protocols. The profiling data enables engineers to select configurations that maximize read/write throughput with key findings presented in this document.

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1 Introduction

Flash memory performance is critical for achieving system responsiveness in embedded applications. As Sitara™ Sitara MPU-based designs handle increasingly complex, data-intensive operations, selecting the right Flash memory configuration directly impacts overall application performance. Different Flash interfaces (OSPI, QSPI), protocols (8D-8D-8D, 4S-4D-4D, 1S-8S-8S), and operational modes (DMA/PHY enabled or disabled) can significantly affect read/write throughput.

This application note presents comprehensive profiling data for Flash read and write operations on OSPI and QSPI Flash interfaces within bare-metal environments using the MCU+ SDK of the Texas Instruments Sitara MPU family, including AM243x, AM62x, AM62A, AM64x, AM62P, AM62D, AM275x devices. The profiling covers Flash parts tested on various EVMs using both ARM Cortex-A53 and Cortex-R5F cores.

By understanding performance characteristics across configurations, developers can optimize systems for maximum throughput, power efficiency, or application-specific requirements. The data tables and performance graphs provide clear comparisons to identify settings for specific use cases.

2 Terminology

PHY: Refers to the PHY mode of the OSPI and QSPI Drivers

QSPI: Quad Serial Peripheral Interface

OSPI: Octal Serial Peripheral Interface

DDR: Dual Data Rate

SDR: Single Data Rate

DAC: Direct Access Controller

INDAC: Indirect Access Controller

MiBps: Mebibytes per second

PHY:

PHY mode uses a specialized timing circuit to manage memory data transfers. In this mode, each reference clock cycle generates one complete memory clock cycle for standard transfers or half a cycle for double-speed transfers. The system offers four different timing configurations, using either internal signals or external feedback from the memory chip.

When PHY is enabled, the input clock divider is bypassed. As a result, the effective frequency is the input clock frequency. The PHY tuning algorithm calculates the tuning point by varying rxDLL, txDLL, and Read Delay. To learn more about this, see the following FAQ.

TAP:

TAP mode uses an internal reference clock to time data transfers with the memory device. This divides this reference clock by four for standard transfers or by eight for double data rate transfers. This mode only supports a direct (non-loopback) configuration, using the reference clock for data capture timing.

When TAP Mode is enabled, the input clock divider is not bypassed. As a result, the effective frequency is the input clock frequency divided by the input clock divider.

QSPI:

Quad Serial Peripheral Interface - an enhanced SPI variant using four data lines (DQ0-DQ3) for serial data transfer. Supports single/dual/quad modes for different transfer phases, achieving up to 4x bandwidth improvement over standard SPI while maintaining backward compatibility.

OSPI:

Octal Serial Peripheral Interface - an advanced SPI variant using eight data lines (DQ0-DQ7) for serial data transfer. Supports all QSPI modes plus octal mode, enabling even higher bandwidth. Can operate with or without DQS (Data Strobe) signal for source-synchronous data capture.

SDR:

SDR mode transfers data on a single edge of the clock signal, sending one bit per clock cycle per data line. This is the simpler and more traditional clocking scheme that provides good reliability at moderate speeds. In octal SDR mode with eight data lines, the theoretical maximum data rate is eight bits per clock cycle.

DDR:

DDR mode transfers data on both rising and falling edges of the clock signal, effectively doubling the data throughput compared to SDR mode. In octal DDR mode with eight data lines, data is transferred 16 bits per clock cycle (eight bits per edge × two edges).

Protocol (Command-Address-Data):

The protocol mode format is WR-WR-WR, where the first WR represents the command bit width and rate, the second WR represents the command modifier bit width and rate, and the third WR represents the data bit width

and rate. The bit width (W) can be one or eight bits. The rate (R) is either S for SDR or D for DDR. SDR transfers the same value on both rising and falling clock edges, while DDR may transfer different values on each edge.

For example, 1S-1S-1S means all phases use 1-bit wide SDR. The notation 8D-8D-8D means all phases use 8-bit wide DDR.

DAC:

Direct access refers to the operation where data interface accesses directly trigger a read or write to Flash memory. It is memory mapped and can be used to both access and directly execute code from external Flash memory.

INDAC:

The aim of the indirect mode of operation is to read significant numbers of bytes from Flash memory without requiring a data interface access to trigger it. Instead indirect operations are controlled and triggered by software via specific control/configuration Indirect Read Transfer registers. The read data is placed into the local SRAM module ready for fast and low latency delivery to any external controller.

3 Methodology

The following numbers are validated for MCU+ SDK release 11.01/11.02.

OSPI Flash IO example was used as a reference for profiling the Flash operations.

The profiling was done in ambient and room temperature, across approximately 20MHz to 166MHz frequencies.

Each Flash operation was profiled 100 times, across the following configurations:

DMA, PHY, TAP, DAC, INDAC, Data Sizes used: 1KiB, 10KiB, 256KiB, 512KiB, 1MiB, 5MiB, 10MiB

Table 3-1. Flash Parts Available by Default on TI EVM

Sitara MPU Board	Flash Parts on TI EVM			
	NOR OSPI (S28HS512T)	NAND OSPI (W35N01JWTBAG)	NOR QSPI(S25HL512T)	NAND QSPI(W25N01JWTBAG)
LP-AM243	No	No	Yes	No
TMDS243EVM	Yes	No	No	No
AUDIO-AM275-EVM	Yes	No	No	No
SK-AM62B-P1	Yes	No	No	No
SK-AM62A-LP	No	Yes	No	No
AUDIO-AM62D-EVM	Yes	No	No	No
TMDS62LEVM	Yes	No	No	Yes (supported only in Processor Linux SDK)
SK-AM62P-LP	Yes	No	No	No
TMDS64EVM	Yes	No	No	No

The profiling done is much more exhaustive than the existing performance numbers present in the MCU+ SDK datasheet. The existing numbers can be found here:

- Serial NOR OSPI Flash
- Serial NAND OSPI Flash

The datasheet for the available Flash parts is mentioned in the References.

Table 3-2. Configurations Used for Profiling on MCU+ SDK 11.01/11.02

SOC	Flash	INDAC[1] [2] Writes	DAC Writes	DAC* Reads	INDAC Reads	Protocol Used
AM243x AM275x AM62x AM62Dx AM62Lx AM62Px AM64x	Serial NOR OSPI	Yes	No[3]	Yes	Yes[4](PHY and DMA are not supported)	8D-8D-8D
AM243x	Serial NOR QSPI	Yes	No	Yes	Yes (PHY and DMA are not supported)	4S-4D-4D[5]
AM62Ax	Serial NAND OSPI	No	Yes	Yes	No	1S-8S-8S8D-8D-8D[6]

The following are the limitations on MCU+ SDK 11.01/11.02:

1. INDAC writes happen in TAP mode. In TAP mode, the effective frequency is input clock frequency divided by the input clock divider. In PHY mode, the effective frequency is the input clock frequency, because the input clock divider gets bypassed.
2. PHY enabled Writes are not supported for Serial NOR and NAND Flash in the MCU+ SDK. This is a software limitation.
3. Direct writes are supported for Serial NAND Flash but not for Serial NOR Flash. Serial NOR Flash requires indirect writes because in DTR mode, it expects a 4-byte dummy address (all zeros) with the read status register command. This is a functionality the controller does not support when polling for write completion.
4. INDAC Reads currently do not have PHY and DMA support in the MCU+ SDK. This is a software limitation.
5. Serial NOR QSPI Flash (S25HL512T) does not support 4D-4D-4D Protocol. This is a limitation coming from the on-board QSPI NOR Flash, but the driver is capable of supporting 4D-4D-4D.

6. For Serial NAND Flash, PHY Tuning is not supported for DDR mode. This is a software limitation.

* DAC Reads with OTP Validation: When PHY-enabled DAC Reads are performed, the tuning point is validated through a diagonal check. If any point fails this check, a new tuning point is automatically identified and implemented to verify performance.

Note

Refer to the latest MCU+ SDK for supported features with respect to PHY, DAC and INDAC software support.

Throughput is calculated as:

Throughput (in MiBps) = Data size used in Bytes / Time taken in microseconds

The theoretical throughput is calculated as:

For DDR,

Theoretical Throughput (MiBps) = (Effective clock frequency x 2 x Number of bits per transfer) / 8

For SDR,

Theoretical Throughput (MiBps) = (Effective clock frequency x 1 x Number of bits per transfer) / 8

Effective Clock Frequency is calculated as:

Effective Clock Frequency = Input Clock Frequency / Input Clock Divider

Time taken for each Flash operation is calculated as:

Time Taken (in µs) = Data size used in Bytes / Throughput in MiBps

4 Benchmarking Flash Operations

The graphs below illustrate the throughput performance when both PHY and DMA are enabled. However, for the 8D-8D-8D configuration on Serial NAND OSPI Flash, the graphs show throughput with only DMA enabled and PHY not supported (refer to Table 3-2). The labels on the data points of the graphs represent the size of the data profiled and the corresponding time taken to profile each operation.

The accompanying tables summarize all the results of an exhaustive profiling exercise, covering all possible permutations and combinations of the supported configurations, including TAP, PHY, DAC, INDAC, and DMA.

The average observed throughput was calculated by taking the mean of the throughput values for data sizes between 256 KiB and 10 MiB, with DMA and PHY enabled. The observed throughputs are summarized in the tables below.

*The values highlighted in **bold** represent the highest throughput achieved for different configurations.*

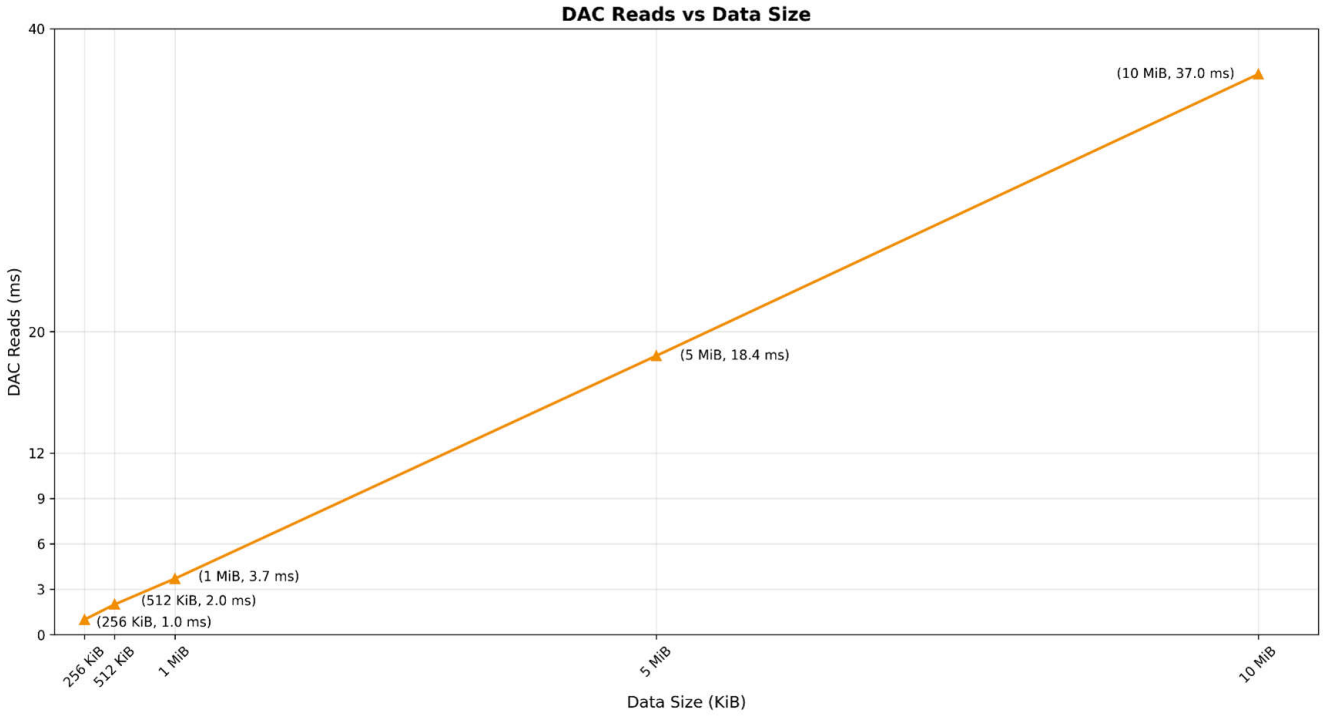
4.1 Processor - AM243x / AM64x

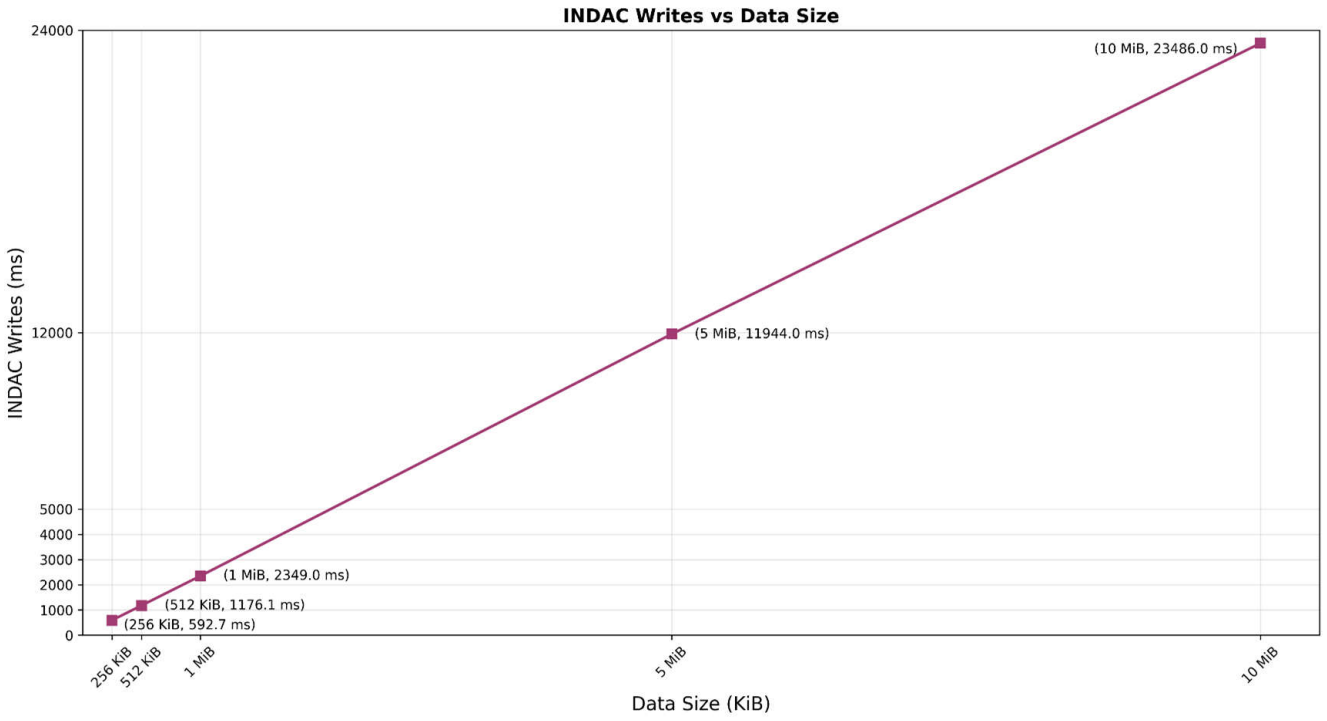
4.1.1 TMDS243EVM / TMDS64EVM

Core	R5F
Board	TMDS243EVM
Flash	NOR OSPI S28HS512T
Input Clock Frequency	166 MHz
Input Clock Divider	8
Protocol	8D-8D-8D

Theoretical throughput for DAC Reads: 332MiBps

Average throughput observed for DAC Reads: 282.86MiBps





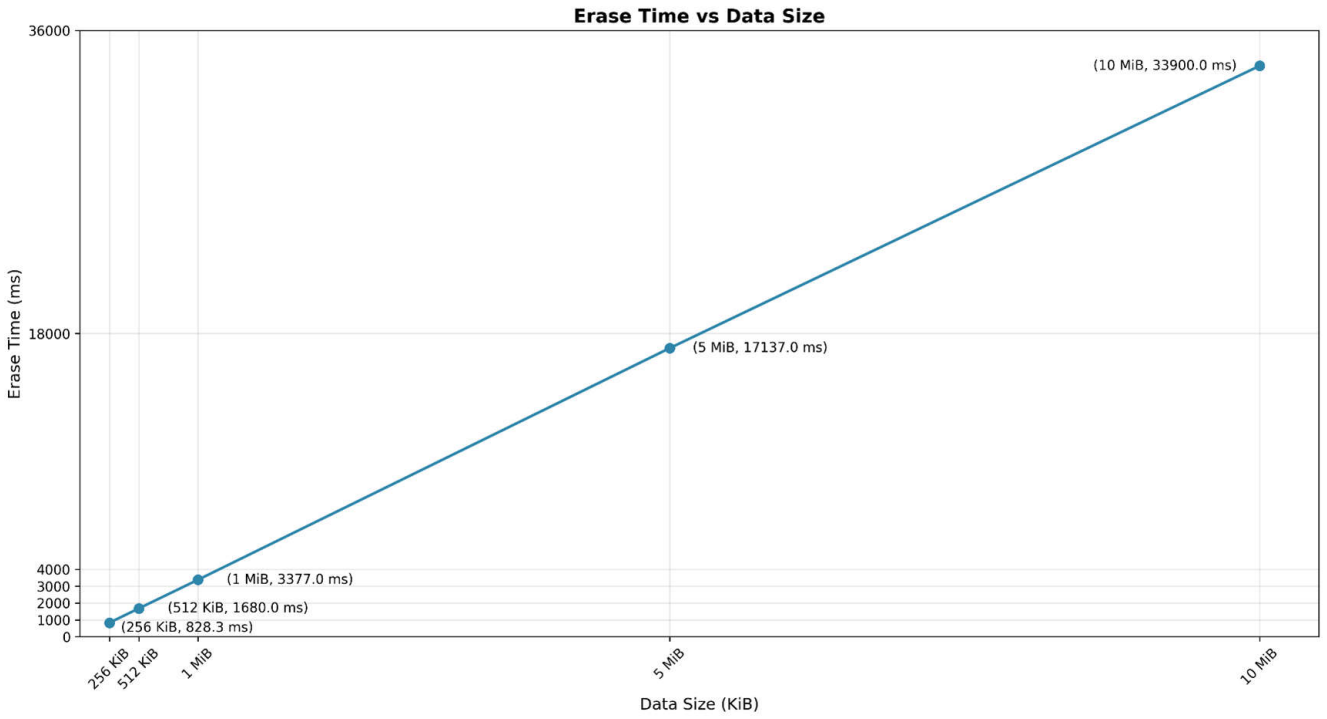


Table 4-1. 8D-8D-8D on R5F Core

Frequency	Divider	Data Size Used	DMA	PHY	Throughput (MiBps)				
					INDAC Writes	DAC Reads	DAC Reads with failed OTP Validation	INDAC Reads	Erase
166 MHz	4	1 KiB	No	No	**0.41**	1.12	N/A	**23.27**	0.001
			No	Yes	0.41	2.35	0.04	N/A	0.001
			Yes	No	0.41	1.12	N/A	N/A	0.001
			Yes	Yes	0.41	**2.35**	**0.04**	N/A	0.001
		10 KiB	No	No	**0.43**	1.12	N/A	**25.75**	0.01
			No	Yes	0.43	2.38	0.40	N/A	0.01
			Yes	No	0.43	26.39	N/A	N/A	0.01
			Yes	Yes	0.43	**200**	**0.40**	N/A	0.01
		256 KiB	No	No	**0.43**	1.12	N/A	**22.21**	0.32
			No	Yes	0.43	2.36	9.55	N/A	0.32
			Yes	No	0.43	27.08	N/A	N/A	0.32
			Yes	Yes	0.43	**279.41**	**9.55**	N/A	0.32
		512 KiB	No	No	**0.41**	1.12	N/A	**22.22**	0.31
			No	Yes	0.41	2.36	18.50	N/A	0.31
			Yes	No	0.41	27.10	N/A	N/A	0.31
			Yes	Yes	0.41	**282.18**	**18.50**	N/A	0.31
		1 MiB	No	No	**0.41**	1.12	N/A	**22.23**	0.31
			No	Yes	0.41	2.34	34.72	N/A	0.31
			Yes	No	0.41	27.10	N/A	N/A	0.31
			Yes	Yes	0.41	**283.51**	**34.72**	N/A	0.31
		5 MiB	No	No	**0.45**	1.12	N/A	**22.24**	0.31
			No	Yes	0.45	2.34	116.73	N/A	0.31
			Yes	No	0.45	27.11	N/A	N/A	0.31
			Yes	Yes	0.45	**284.74**	**116.73**	N/A	0.31
		10 MiB	No	No	**0.41**	1.12	N/A	**22.24**	0.31
			No	Yes	0.41	2.34	165.63	N/A	0.31
			Yes	No	0.41	27.11	N/A	N/A	0.31
			Yes	Yes	0.41	**284.87**	**165.63**	N/A	0.31

Table 4-2. 8D-8D-8D on R5F Core

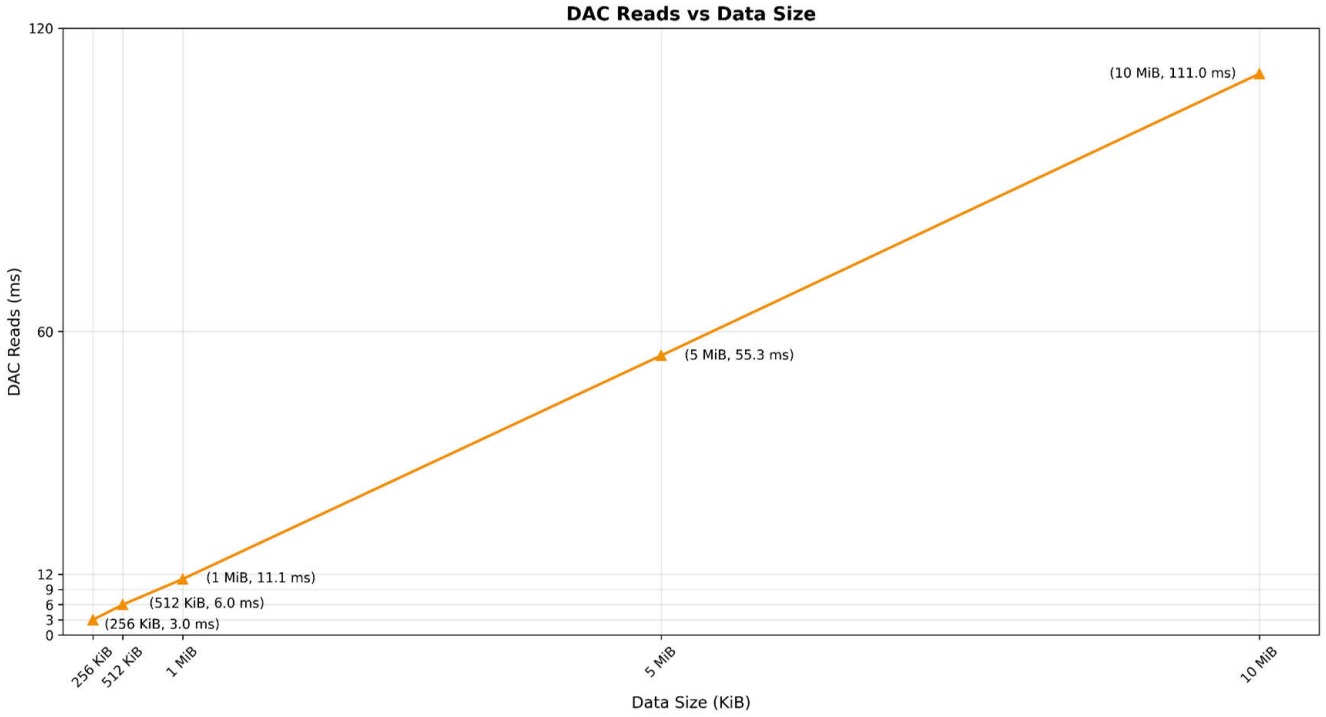
Frequency	Divider	Data Size Used	DMA	PHY	Throughput (MiBps)				
					INDAC Writes	DAC Reads	DAC Reads with failed OTP Validation	INDAC Reads	Erase
166 MHz	8	1 KiB	No	No	**0.45**	0.65	N/A	**22.65**	0.001
			No	Yes	0.45	2.35	0.04	N/A	0.001
			Yes	No	0.45	0.65	N/A	N/A	0.001
			Yes	Yes	0.45	**2.34**	**0.04**	N/A	0.001
		10 KiB	No	No	**0.46**	0.65	N/A	**25.69**	0.01
			No	Yes	0.46	2.37	0.40	N/A	0.01
			Yes	No	0.46	37.87	N/A	N/A	0.01
			Yes	Yes	0.46	**180.92**	**0.40**	N/A	0.01
		256 KiB	No	No	**0.44**	0.65	N/A	**22.13**	0.32
			No	Yes	0.44	2.34	9.57	N/A	0.32
			Yes	No	0.44	40.68	N/A	N/A	0.32
			Yes	Yes	0.44	**279.11**	**9.57**	N/A	0.32
		512 KiB	No	No	**0.44**	0.65	N/A	**22.19**	0.31
			No	Yes	0.44	2.37	18.51	N/A	0.31
			Yes	No	0.44	40.74	N/A	N/A	0.31
			Yes	Yes	0.44	**282.09**	**18.51**	N/A	0.31
		1 MiB	No	No	**0.44**	0.65	N/A	**22.23**	0.31
			No	Yes	0.44	2.34	34.77	N/A	0.31
			Yes	No	0.44	40.77	N/A	N/A	0.31
			Yes	Yes	0.44	**283.55**	**34.77**	N/A	0.31
		5 MiB	No	No	**0.44**	0.65	N/A	**22.22**	0.31
			No	Yes	0.44	2.34	116.83	N/A	0.31
			Yes	No	0.44	40.80	N/A	N/A	0.31
			Yes	Yes	0.44	**284.72**	**116.83**	N/A	0.31
		10 MiB	No	No	**0.45**	0.65	N/A	**22.23**	0.31
			No	Yes	0.45	2.34	165.73	N/A	0.31
			Yes	No	0.45	40.80	N/A	N/A	0.31
			Yes	Yes	0.45	**284.87**	**165.73**	N/A	0.31

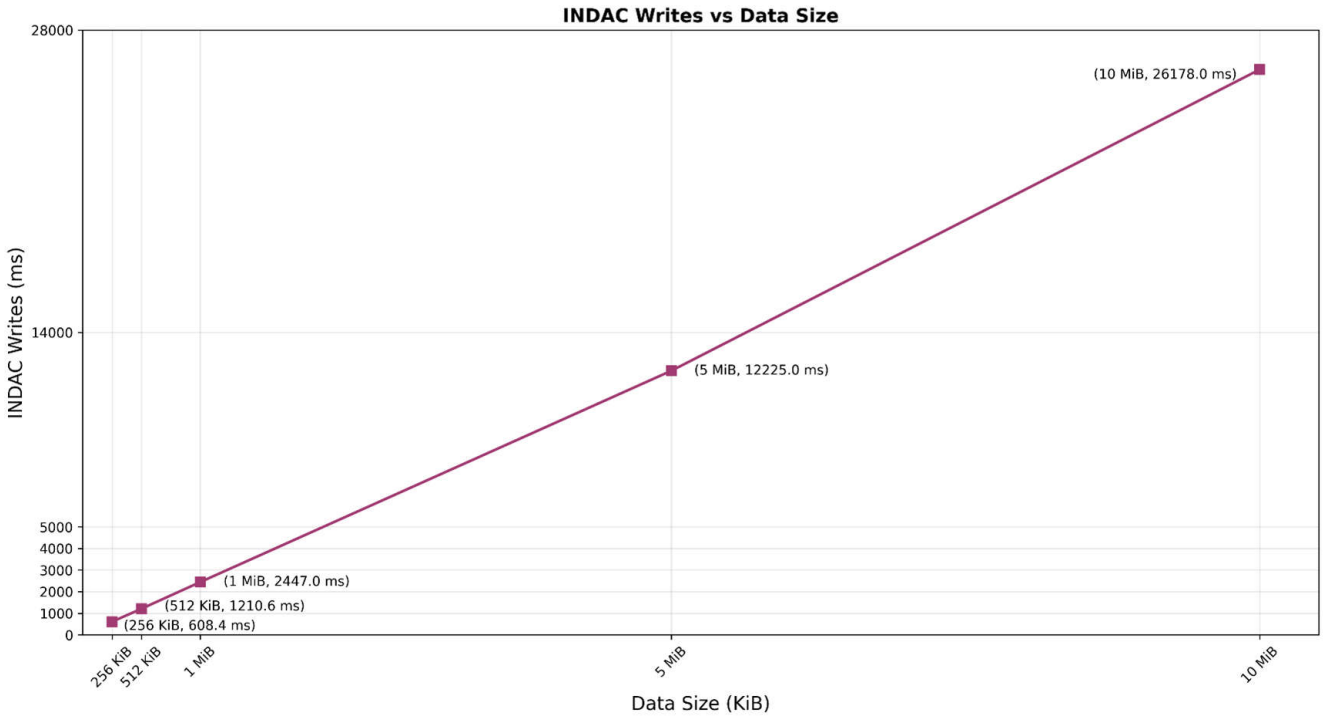
4.1.2 LP-AM243

Core	R5F
Board	LP-AM243
Flash	NOR QSPI S25HL512T
Input Clock Frequency	100 MHz
Input Clock Divider	4
Protocol	4S-4D-4D

Theoretical throughput for DAC Reads: 100MiBps

Average throughput observed for DAC Reads: 94.78MiBps





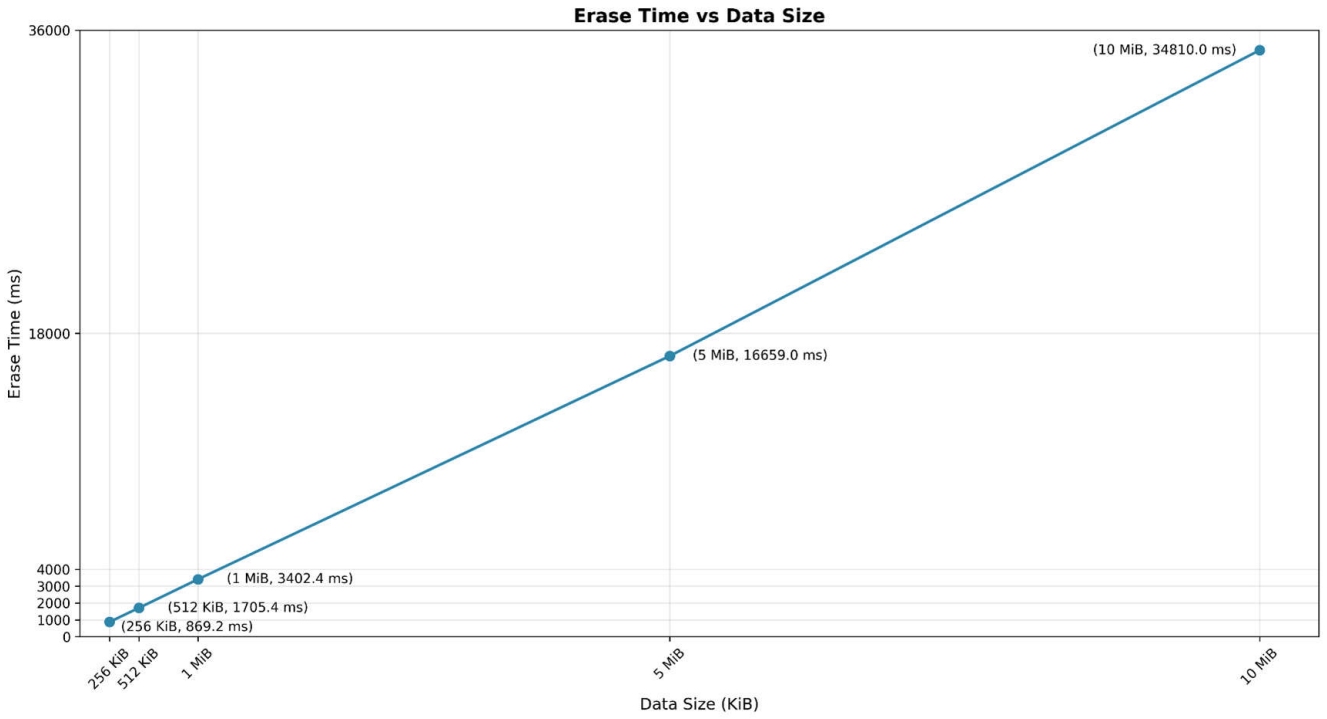


Table 4-3. 4S-4D-4D on R5F Core

Frequency	Divider	Data Size Used	DMA	PHY	Throughput (MiBps)				
					INDAC Writes	DAC Reads	DAC Reads with failed OTP Validation	INDAC Reads	Erase
100MHz	4	1KiB	No	No	0.40	0.67	N/A	21.07	0.001
			No	Yes	0.40	1.57	0.002	N/A	0.001
			Yes	No	0.40	0.67	N/A	N/A	0.001
			Yes	Yes	0.40	1.57	0.002	N/A	0.001
		10KiB	No	No	0.43	0.67	N/A	24.50	0.01
			No	Yes	0.43	1.58	0.02	N/A	0.01
			Yes	No	0.43	23.86	N/A	N/A	0.01
			Yes	Yes	0.43	82.85	0.02	N/A	0.01
		256KiB	No	No	0.43	0.67	N/A	24.66	0.30
			No	Yes	0.43	1.58	0.40	N/A	0.30
			Yes	No	0.43	24.65	N/A	N/A	0.30
			Yes	Yes	0.43	94.50	0.40	N/A	0.30
		512KiB	No	No	0.43	0.67	N/A	24.67	0.31
			No	Yes	0.43	1.58	0.78	N/A	0.31
			Yes	No	0.43	24.67	N/A	N/A	0.31
			Yes	Yes	0.43	94.83	0.78	N/A	0.31
		1MiB	No	No	0.43	0.67	N/A	24.67	0.31
			No	Yes	0.43	1.58	1.56	N/A	0.31
			Yes	No	0.43	24.67	N/A	N/A	0.31
			Yes	Yes	0.43	94.86	1.56	N/A	0.31
		5MiB	No	No	0.43	0.67	N/A	24.67	0.31
			No	Yes	0.43	1.58	7.30	N/A	0.31
			Yes	No	0.43	24.67	N/A	N/A	0.31
			Yes	Yes	0.43	94.86	7.30	N/A	0.31
		10MiB	No	No	0.40	0.67	N/A	24.67	0.31
			No	Yes	0.40	1.58	13.56	N/A	0.31
			Yes	No	0.40	24.67	N/A	N/A	0.31
			Yes	Yes	0.40	94.87	13.56	N/A	0.31

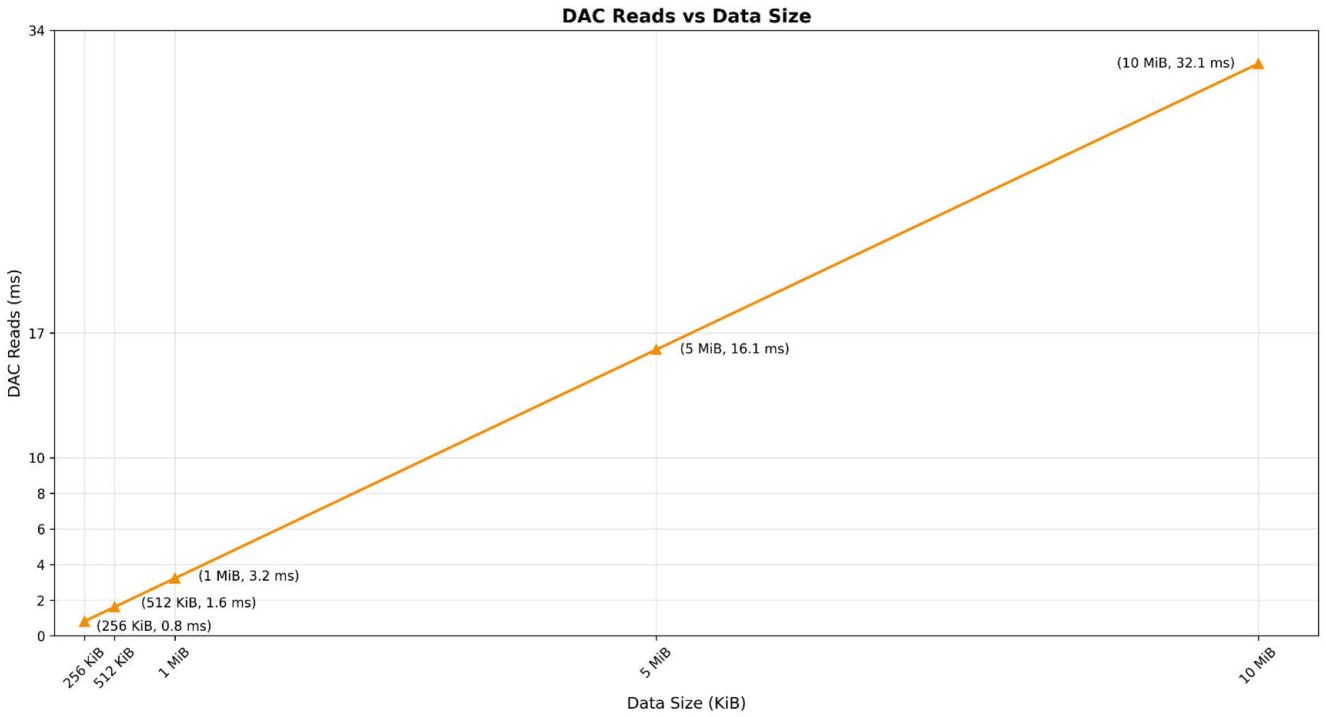
4.2 Processor - AM62Lx

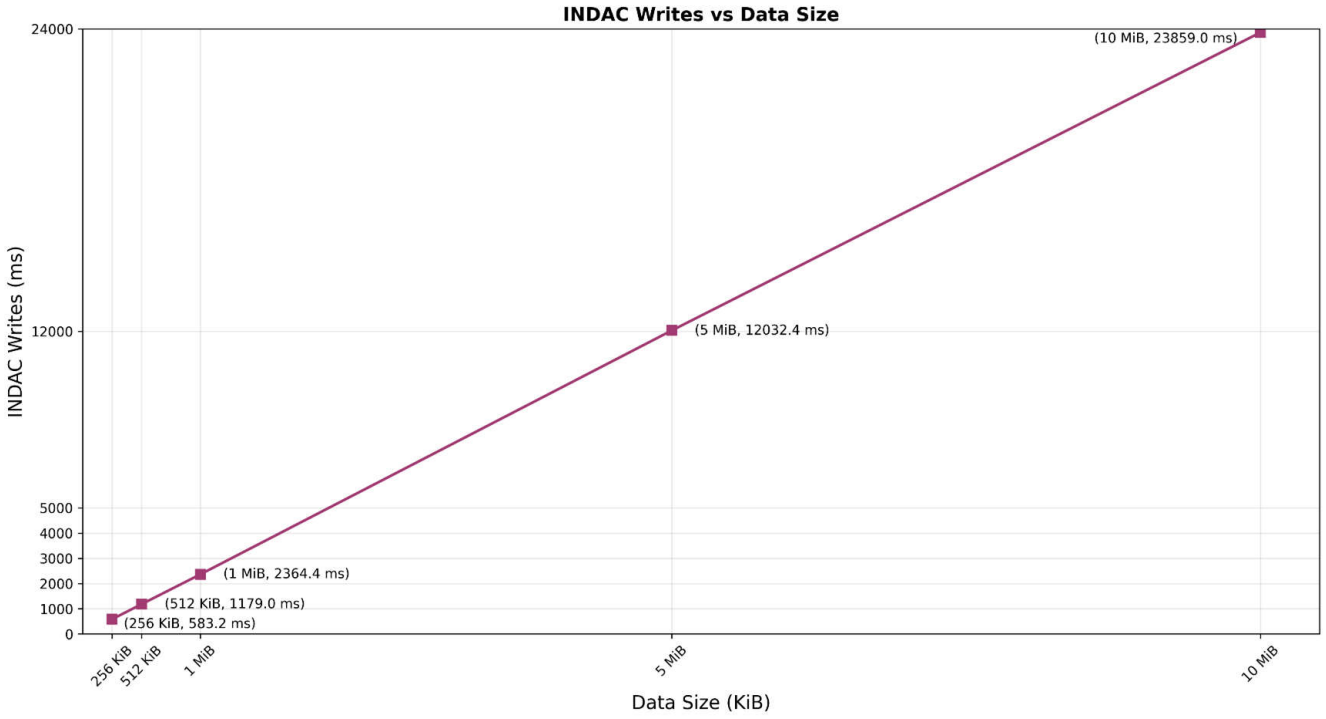
4.2.1 TMDS62LEVM

Core	A53
Board	TMDS62LEVM
Flash	NOR OSPI S28HS512T
Input Clock Frequency	166MHz
Input Clock Divider	8
Protocol	8D-8D-8D

Theoretical throughput for DAC Reads: 332MiBps

Average throughput observed for DAC Reads: 323.86MiBps





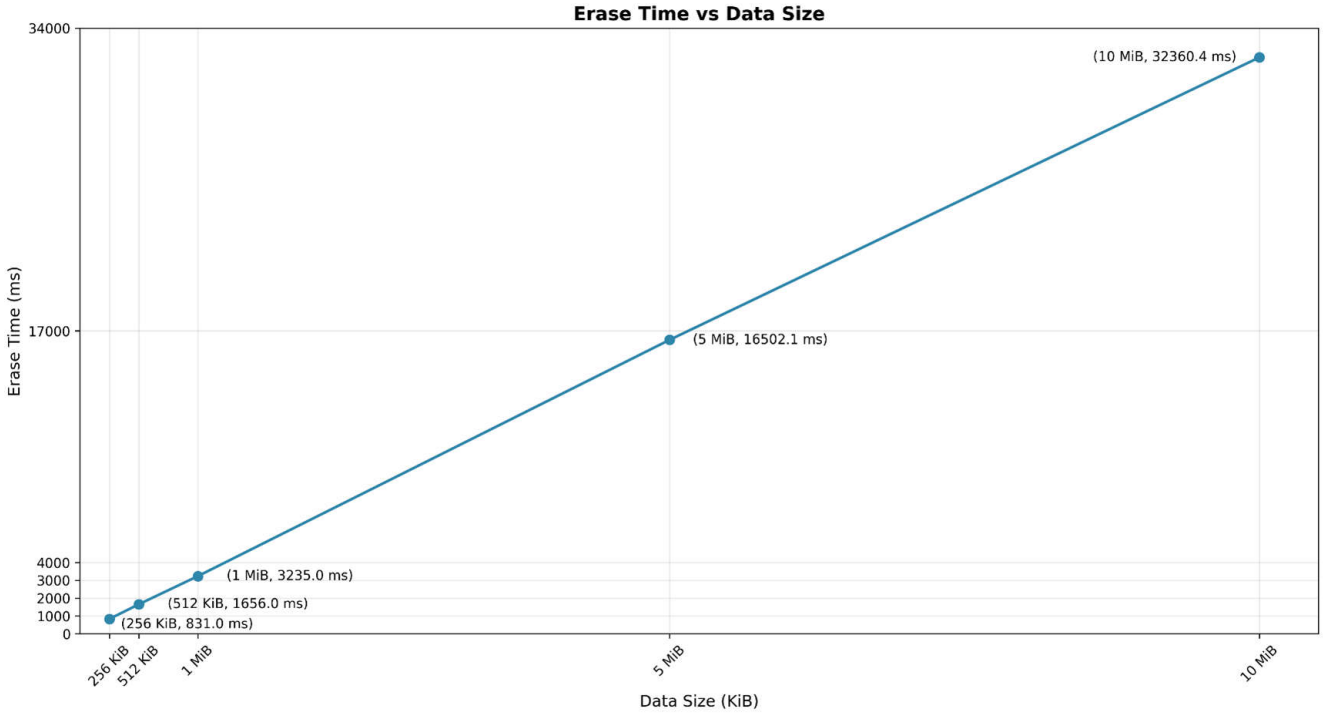


Table 4-4. 8D-8D-8D on A53 Core

Frequency	Divider	Data Size Used	DMA	PHY	Throughput (MiBps)			
					INDAC Writes	DAC Reads	INDAC Reads	Erase
166MHz	8	1 KiB	No	No	**0.43**	0.65	**27.83**	0.001
			No	Yes	0.43	2.48	N/A	0.001
			Yes	No	0.43	0.65	N/A	0.001
			Yes	Yes	0.43	**2.48**	N/A	0.001
		10 KiB	No	No	**0.45**	0.65	**30.70**	0.01
			No	Yes	0.45	2.52	N/A	0.01
			Yes	No	0.45	39.38	N/A	0.01
			Yes	Yes	0.45	**231.67**	N/A	0.01
		256 KiB	No	No	**0.45**	0.65	**31.29**	0.31
			No	Yes	0.45	2.50	N/A	0.31
			Yes	No	0.45	41.44	N/A	0.31
			Yes	Yes	0.45	**319.14**	N/A	0.31
		512 KiB	No	No	**0.44**	0.65	**31.29**	0.32
			No	Yes	0.44	2.52	N/A	0.32
			Yes	No	0.44	41.50	N/A	0.32
			Yes	Yes	0.44	**322.96**	N/A	0.32
		1 MiB	No	No	**0.44**	0.65	**31.29**	0.32
			No	Yes	0.44	2.52	N/A	0.32
			Yes	No	0.44	41.53	N/A	0.32
			Yes	Yes	0.44	**324.74**	N/A	0.32
		5 MiB	No	No	**0.43**	0.65	**31.11**	0.32
			No	Yes	0.43	2.50	N/A	0.32
			Yes	No	0.43	41.56	N/A	0.32
			Yes	Yes	0.43	**326.15**	N/A	0.32
		10 MiB	No	No	**0.44**	0.65	**31.30**	0.32
			No	Yes	0.44	2.50	N/A	0.32
			Yes	No	0.44	41.56	N/A	0.32
			Yes	Yes	0.44	**326.34**	N/A	0.32

4.3 Processor - AM62Ax

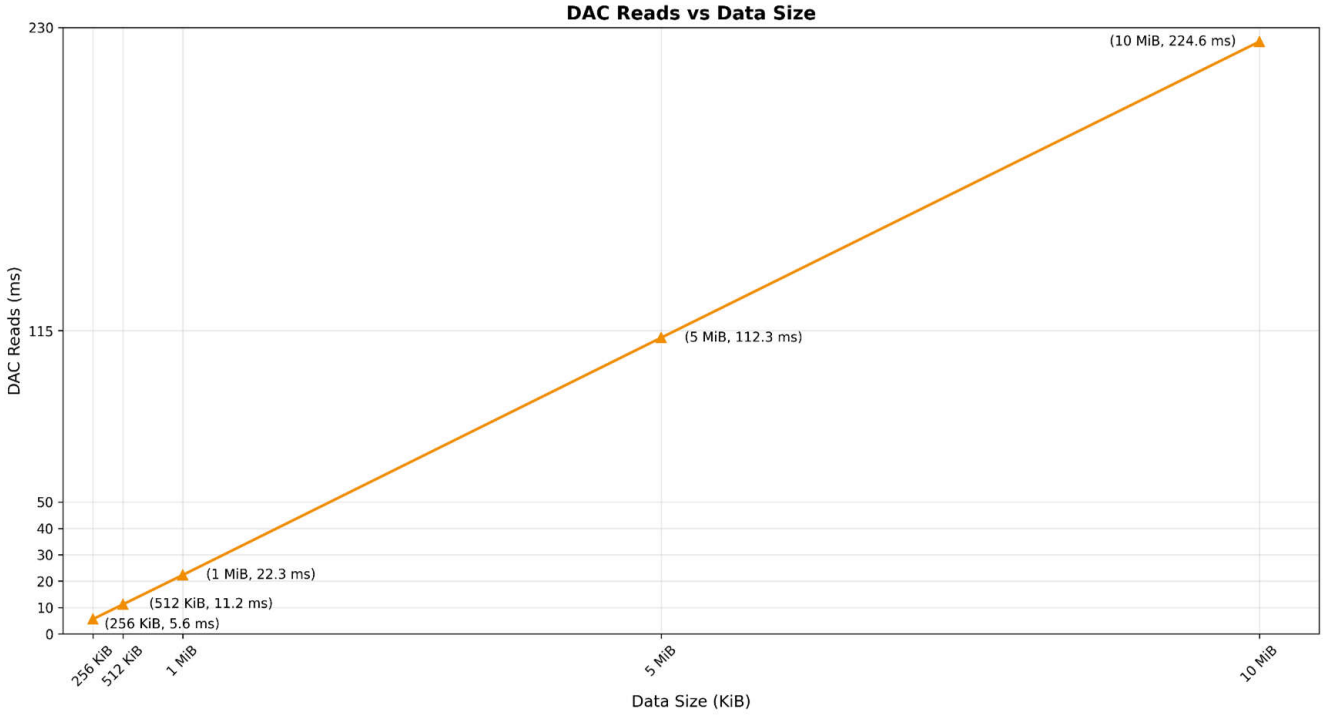
4.3.1 SK-AM62A-LP

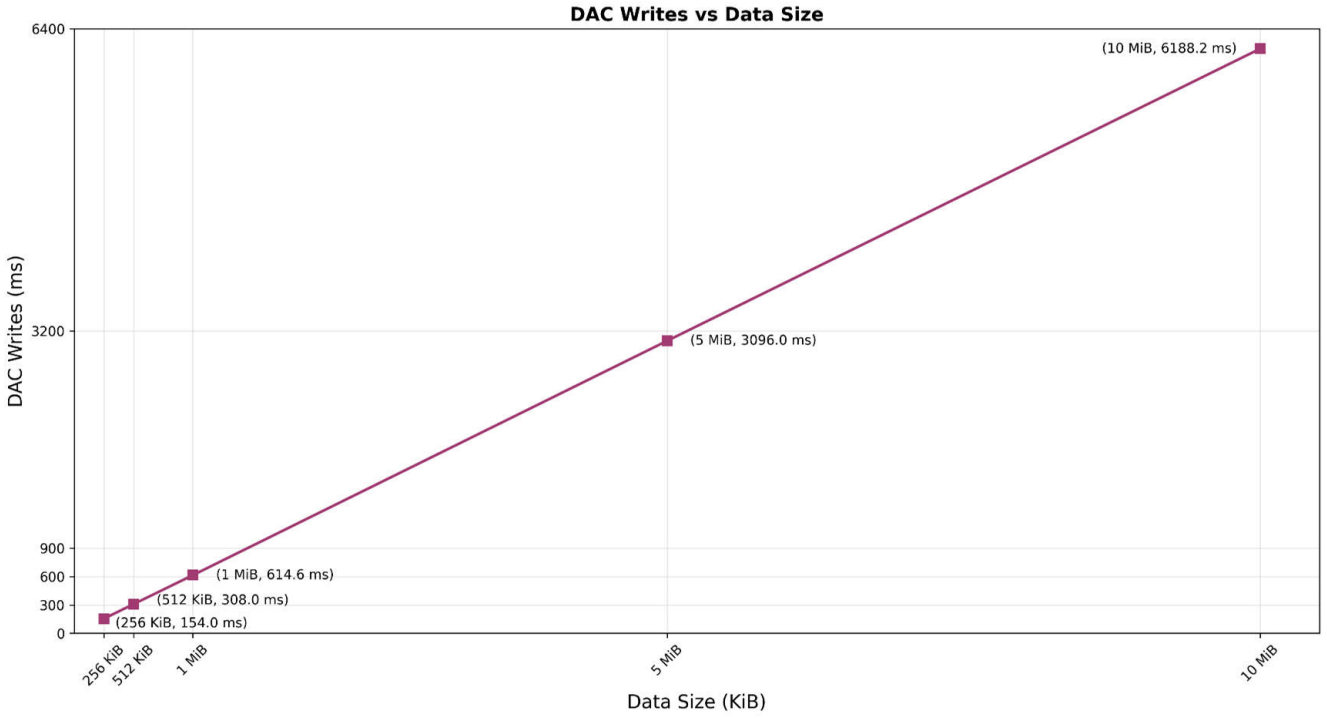
Core	R5F
Board	SK-AM62A-LP
Flash	NAND OSPI W35N01JWTBAG
Input Clock Frequency	166MHz
Input Clock Divider	8
Protocol	1S-8S-8S

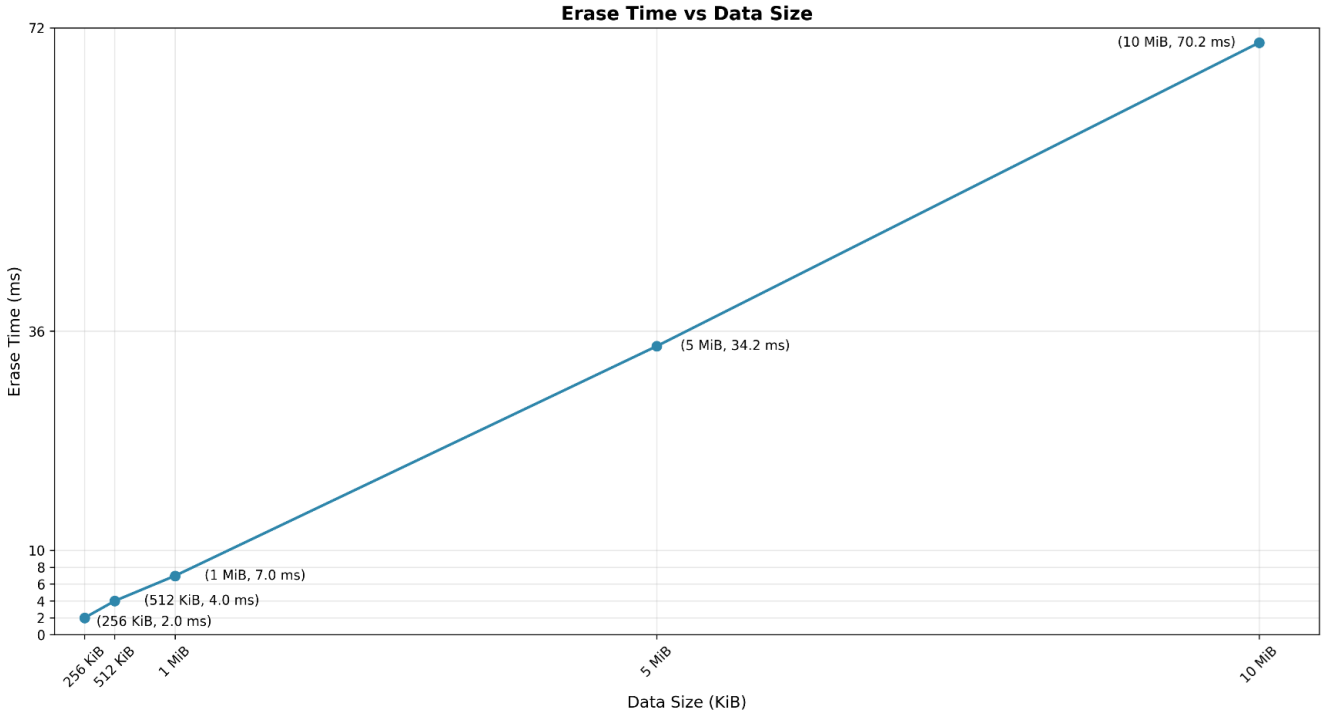
Theoretical throughput for DAC Reads: 240 MiBps

(Serial NAND OSPI Flash W35N01JWTBAG supports a maximum clock frequency of 166 MHz (166 MiBps) and 120 MHz DDR (240 MiBps), refer to the datasheet)

Average throughput observed for DAC Reads: 46.86 MiBps





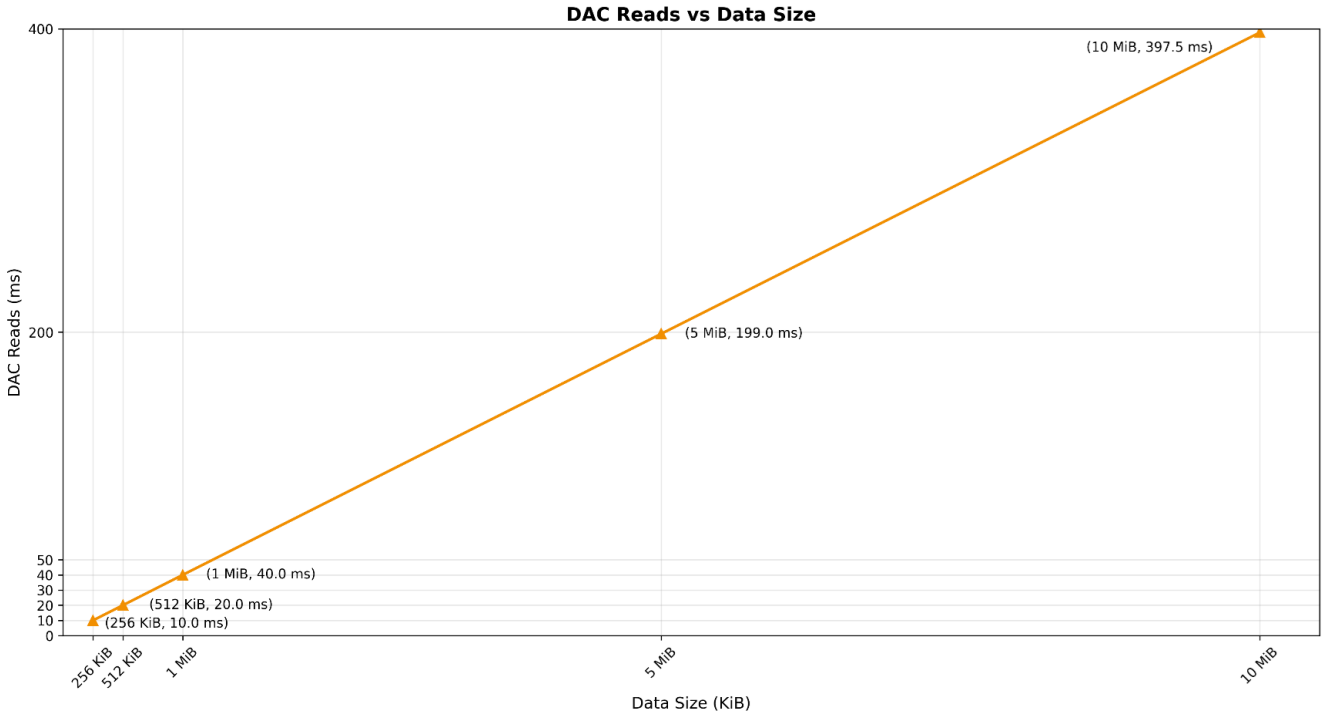


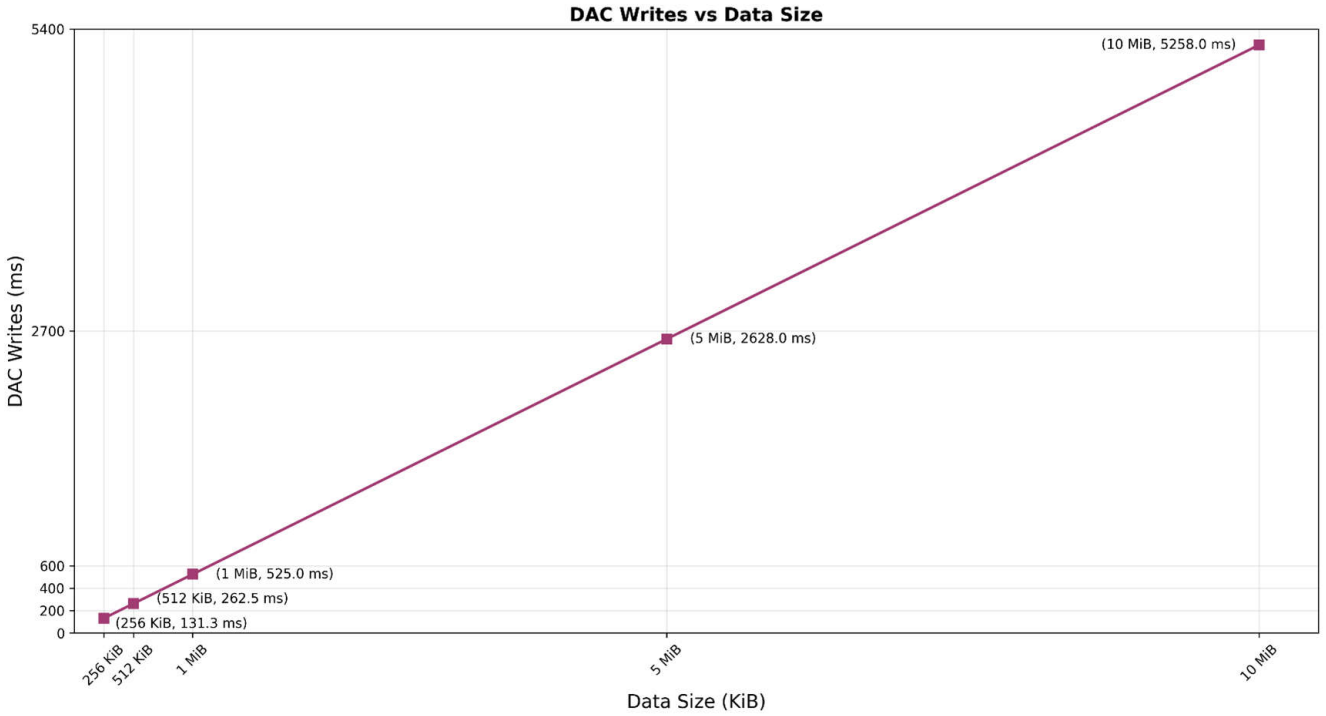
Core	R5F
Board	SK-AM62A-LP
Flash	NAND OSPI W35N01JWTBAG
Input Clock Frequency	166MHz
Input Clock Divider	8
Protocol	8D-8D-8D

Theoretical throughput for DAC Reads: 41.5MiBps

(Serial NAND OSPI Flash W35N01JWTBAG supports a maximum clock frequency of 166MHz (166MiBps) and 120MHz DDR (240MiBps), see the datasheet)

Average throughput observed for DAC Reads: 26.37MiBps





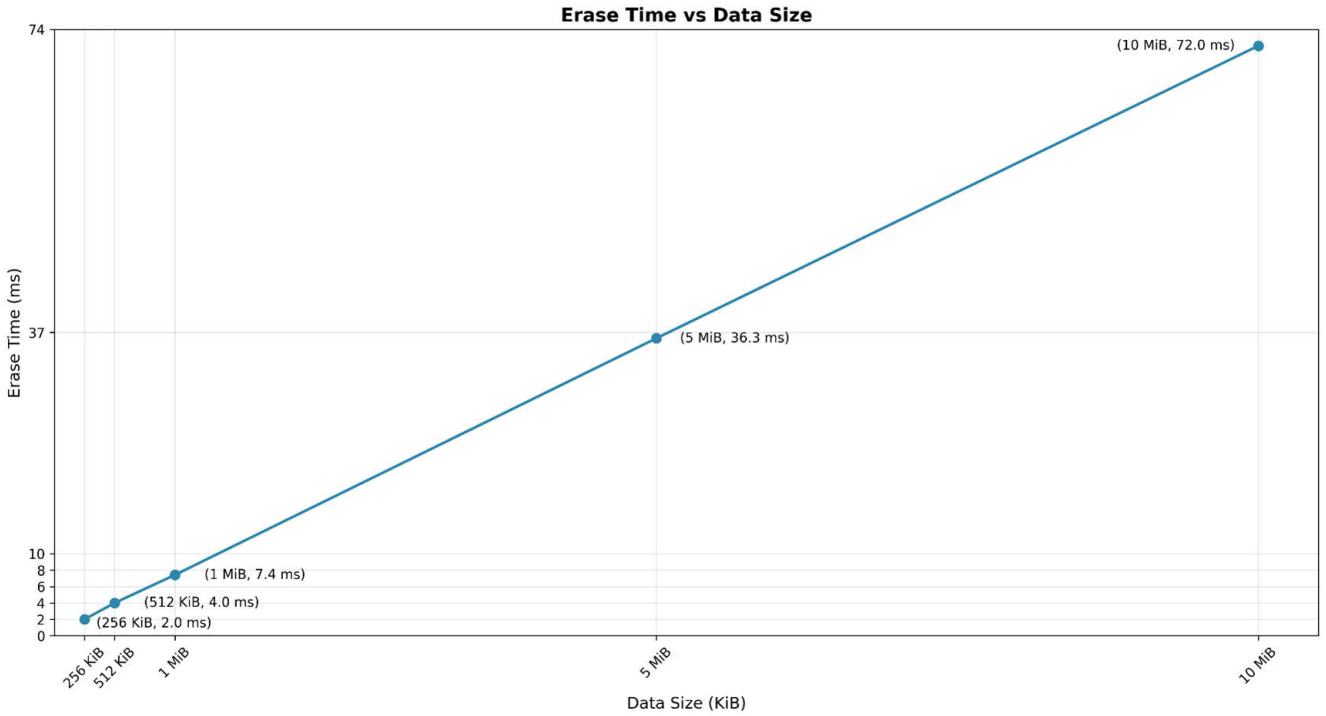


Table 4-5. 1S-8S-8S on R5F Core

Frequency	Divider	Data Size Used	DMA	PHY	Throughput (MiBps)		
					INDAC Writes	DAC Reads	Erase
166MHz	8	1KiB	No	No	**1.13**	1.76	0.88
			No	Yes	1.13	4.58	1.03
			Yes	No	1.13	9.21	0.88
			Yes	Yes	1.13	**14.55**	0.95
		10KiB	No	No	**1.67**	1.87	7.61
			No	Yes	1.67	5.44	7.13
			Yes	No	1.67	15.01	7.13
			Yes	Yes	1.67	**39.69**	7.13
		256KiB	No	No	**1.70**	1.85	140.56
			No	Yes	1.70	5.36	140.71
			Yes	No	1.70	15.94	140.47
			Yes	Yes	1.70	**46.97**	140.66
		512KiB	No	No	**1.70**	1.85	159.76
			No	Yes	1.70	5.37	160.05
			Yes	No	1.70	15.94	148.20
			Yes	Yes	1.70	**46.98**	141.17
		1MiB	No	No	**1.70**	1.85	159.95
			No	Yes	1.70	5.37	150.30
			Yes	No	1.70	15.94	150.23
			Yes	Yes	1.70	**47.01**	150.24
		5MiB	No	No	**1.70**	1.85	170.83
			No	Yes	1.70	5.33	164.79
			Yes	No	1.70	15.94	162.06
			Yes	Yes	1.70	**46.67**	153.14
		10MiB	No	No	**1.70**	1.85	160.55
			No	Yes	1.70	5.33	154.74
			Yes	No	1.70	15.94	154.51
			Yes	Yes	1.70	**46.68**	149.28

Table 4-6. 8D-8D-8D on R5F Core

Frequency	Divider	Data Size Used	DMA	Throughput (MiBps)		
				INDAC Writes	DAC Reads	Erase
166MHz	8	1KiB	No	**1.31**	3.32	0.71
			Yes	1.31	**12.22**	0.71
		10KiB	No	**1.94**	3.68	7.11
			Yes	1.94	**24.05**	7.13
		256KiB	No	**1.98**	3.63	140.42
			Yes	1.98	**26.36**	140.50
		512KiB	No	**1.98**	3.63	144.29
			Yes	1.98	**26.37**	141.02
		1MiB	No	**1.98**	3.63	144.67
			Yes	1.98	**26.37**	141.38
		5MiB	No	**1.98**	3.63	152.81
			Yes	1.98	**26.37**	144.42
		10MiB	No	**1.98**	3.63	147.95
			Yes	1.98	**26.38**	146.45

5 Observations and Conclusions

From the above experiments, following are the observations:

1. For DAC Reads, throughput is faster with DMA and PHY enabled; please refer to the above tables.
2. INDAC Reads are faster than DAC Reads with DMA and PHY disabled.
3. For Serial NOR Flash, the MCU+ SDK only enables DMA for data transfers > 1 KiB, as DMA setup overhead makes CPU copy more efficient for smaller transfers.
4. For Serial NAND Flash, the MCU+ SDK only enables DMA for data transfers > 256 Bytes, as DMA setup overhead makes CPU copy more efficient for smaller transfers.
5. The throughput is better when the input clock frequency is higher and the input clock divider value is lower.
6. The above graphs demonstrate that throughput remains nearly constant for identical configurations regardless of data size, resulting in an almost linear relationship between execution time and data size. However, for smaller data sizes, DMA overhead becomes the dominant factor, causing deviations from this linear trend; please refer to the above tables.

Please go through the following conclusions from the profiling done for different Flash parts:

1. Recommended to use:
   a. DAC Reads and INDAC writes for Serial NOR Flash.
   b. DAC Reads and DAC writes for Serial NAND Flash.
2. For faster DAC Reads, enable PHY and DMA.
3. When PHY is disabled, use highest permissible value for input clock frequency with the least value of input clock divider.
4. **Based on the numbers obtained**, TI recommends using the following protocols:
   a. 8D-8D-8D for S28HS512T (Serial NOR OSPI Flash).
   b. 4S-4D-4D for S25HL512T (Serial NOR QSPI Flash).
   c. 1S-8S-8S for W35N01JWTBAG (Serial NAND OSPI Flash).
   d. **For a custom Flash:** Use DDR primarily along with maximum number of data lines for a Custom Flash. If the Custom Flash does not support DDR, use SDR.

6 Summary

This application note provides a comprehensive Flash memory performance profiling with TI's Sitara™ MPU family, enabling engineers to optimize embedded system throughput and efficiency. The profiling data reveals critical insights for achieving maximum performance across different Flash memory types and configurations.

Protocol selection also impacts performance, with 8D-8D-8D recommended for NOR OSPI, 4S-4D-4D for NOR QSPI, and 1S-8S-8S for NAND OSPI operations. To achieve optimal flash performance, engineers should configure systems with both DMA and PHY enabled, use the highest permissible clock frequency with minimum clock division, and select the appropriate protocol based on the specific Flash type and application requirements.

7 References

1. Texas Instruments, *Serial NOR OSPI Flash Performance Numbers* , datasheet.
2. Texas Instruments, *Serial NAND OSPI Flash Performance Numbers* , datasheet.
3. Infineon Technologies, *S28HS512T datasheet* , datasheet.
4. Winbond, *1.8V 1G-Bit Serial SLC NAND Flash Memory Octal SPI With 166MHz SDR and 120Mhz DDR Buffer Read and Continuous Read* , datasheet.
5. Infineon Technologies, *S25HL512T datasheet*, datasheet.
6. Texas Instruments, *xSPI Custom Flash Debug Guide for MCU+ SDK*, application note.

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