EVM User's Guide: TMDS62LEVM

AM62L Evaluation Module

Description

The TMDS62LEVM evaluation module (EVM) is designed for low-cost and performance optimized AM62L family of application processors. The AM62L has scalable Arm® Cortex®-A53 core performance and embedded features such as: Multimedia DSI support, integrated ADC on chip, advanced lower power management modes, and extensive security options for IP protection and secure boot. The AM62L family of devices supports development with Linux® and FreeRTOS™.

The TMDS62LEVM includes an extensive set of peripherals that make it a well-suited general-purpose device for a broad range of industrial applications while offering intelligent features and optimized power architecture as well. In addition, the extensive set of peripherals included in the AM62L enables system-level connectivity, such as: USB, MMC/SD, OSPI, CAN-FD and an ADC and other interfaces to facilitate easy prototyping. Additionally, it features two on-board temperature sensors for monitoring SoC and LPDDR4 thermal conditions.

Get Started

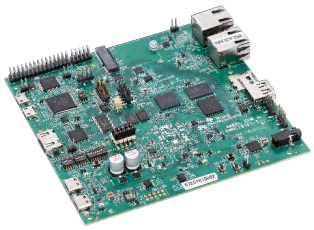
1. Order the EVM at TMDS62LEVM
2. Download the EVM Design Files.
3. Download the software from TMDS62LEVM
4. Read this EVM User's Guide.

Features

- 2x Gigabit Ethernet RJ45 connectors
- 2GB LPDDR4 memory
- 512Mb OSPI Flash memory
- 1GB QSPI Flash memory
- 32GB eMMC Flash memory
- MicroSD card slot
- 1x USB 2.0 Type-C®
- 1x USB 2.0 Type-A
- 3x MCAN headers
- 1x 3.5mm TRRS audio jack
- M.2 connector for Wi-Fi/BT module
- HDMI® connector for external display
- 2x GPIO expansion connector
- ADC header
- DSI display connector

Applications

- Building automation: smart home devices, HVAC controller, IoT devices
- Energy infrastructure: EV charging and supply equipment, smart meter
- Industrial automation: factory automation, robotics, industrial HMI
- Medical: medical devices, patient monitoring systems



TMDS62LEVM Hardware Board

This design incorporates HDMI® technology.

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1 Evaluation Module Overview

1.1 Introduction

This technical user's guide describes the hardware architecture of the AM62L EVM, a low-cost EVM built around the AM62L System-on-Chip (SoC) from Texas Instruments (TI™). The AM62L processor comprises of a Dual-Core 64-bit Arm-Cortex A53 microprocessor capable of running Embedded Linux and RTOS operating systems. The AM62L delivers scalable performance, advanced security and power efficient compute at a lower cost empowering you to accelerate development time and deploy in versatile, low-power and cost-conscious general-purpose solutions.

The AM62L EVM allows the user to experience high resolution display features through HDMI (over DPI) and MIPI DSI, as well as industrial communication solutions using serial, Ethernet, USB, and other interfaces. The AM62L EVM can communicate with other processors or systems, and act as a communication gateway. In addition, the AM62L EVM can directly operate as a standard remote I/O system or simple sensor connected to an industrial communication network. The embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ IDE from Texas Instruments (TI™).

1.2 Kit Contents

This package includes:

- "TMDS62LEVM" EVM
- EVM user's guide pamphlet
- EVM disclaimer and standard terms

1.3 Specification

Figure 1-1 shows the functional block diagram of the AM62L EVM.

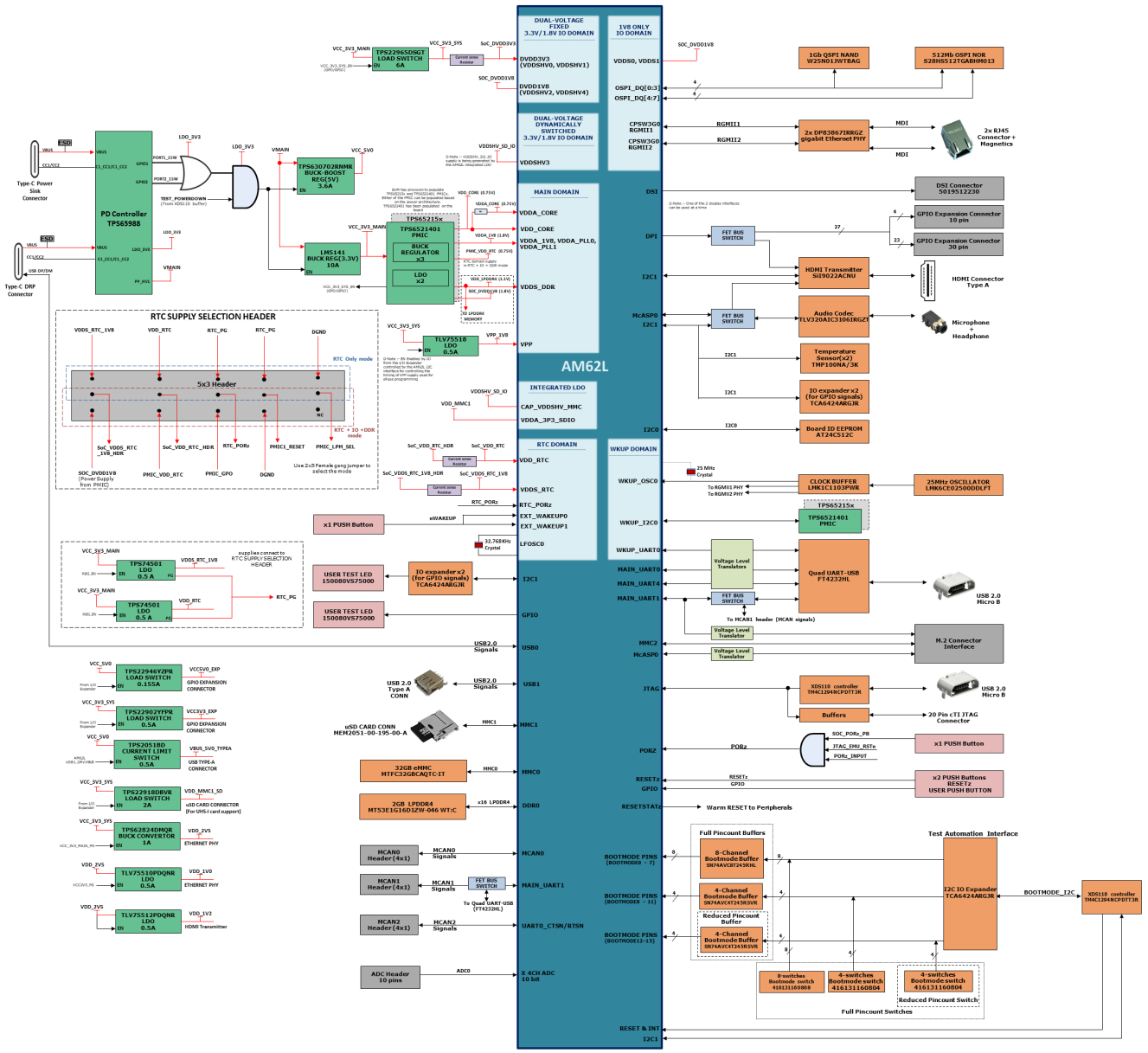

Figure 1-1. Functional Block Diagram of the AM62L EVM

1.4 Device Information

The AM62L EVM supports Linux and FreeRTOS development with a feature-rich software development kit (SDK). On-chip emulation logic allows for emulation and debugging using standard development tools such as the Code Composer Studio™ IDE from TI™ as well as an intuitive out-of-box user's guide to quickly start design evaluation.

1.5 EVM Revisions and Assembly Variants

The various AM62L EVM PCB design revisions, and assembly variants are listed in Table 1-1. The specific PCB revision is indicated in silkscreen on the PCB and the specific assembly variant is indicated with an additional sticker label.

Table 1-1. EVM PCB Design Revisions, and Assembly Variants

OPN	PCB Revision	Assembly Variant	Revision and Assembly Variant Description
TMDS62LEVM	PROC181E1	N/A (single variant produced)	First prototype, early release revision of the AM62L EVM. TPS65215x (PMIC-1) populated.
TMDS62LEVM	PROC181E1-1	N/A	Second prototype, early release revision of the AM62L EVM. Implements a number of changes and bug fixes. TPS65214x (PMIC-2) populated.
TMDS62LEVM	PROC181E1-1a	N/A	Production version with updated SoC part number (AM62L32BOGHAANB). Functionally equivalent to PROC181E1-1 with only SoC Revision change. No PCB Design modification

2 Hardware

2.1 Additional Images

Figure 2-1 and Figure 2-2 show the AM62L EVM top-side and bottom-side images and the location of various blocks on the board.

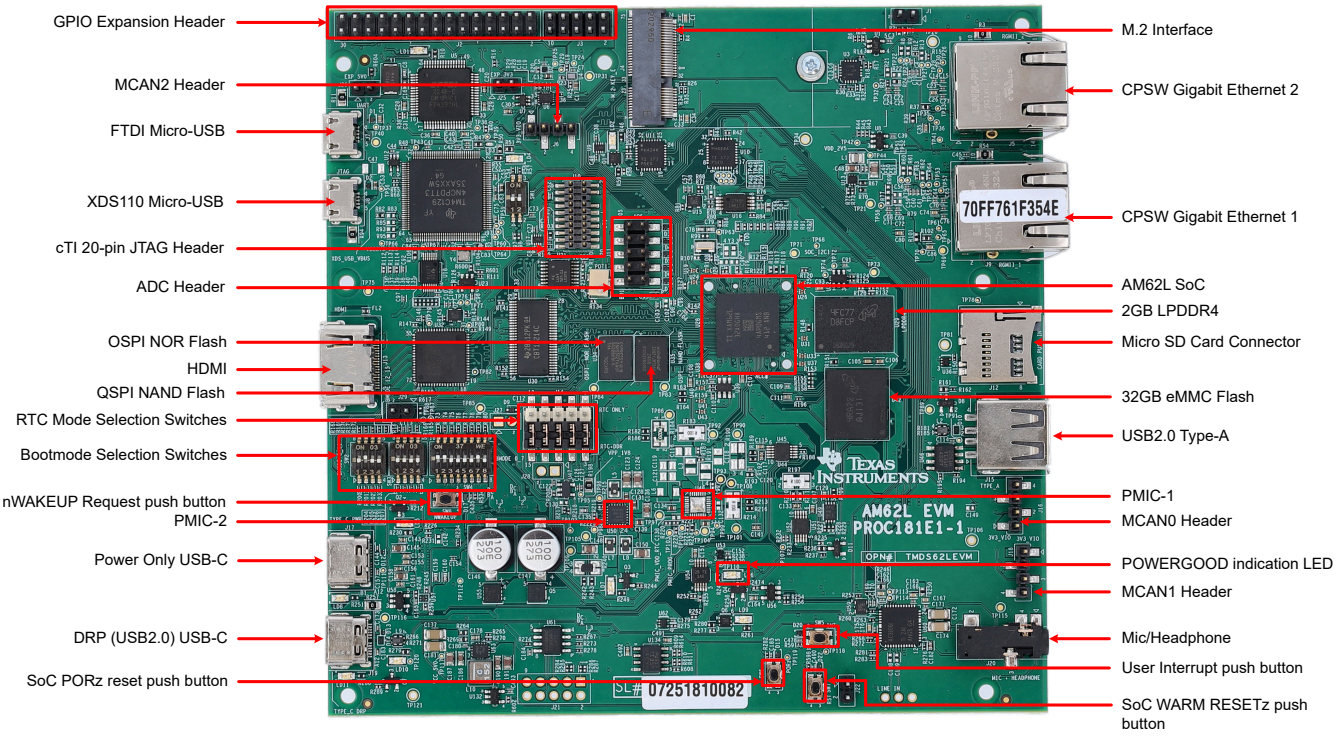

Figure 2-1. AM62L EVM Top Side

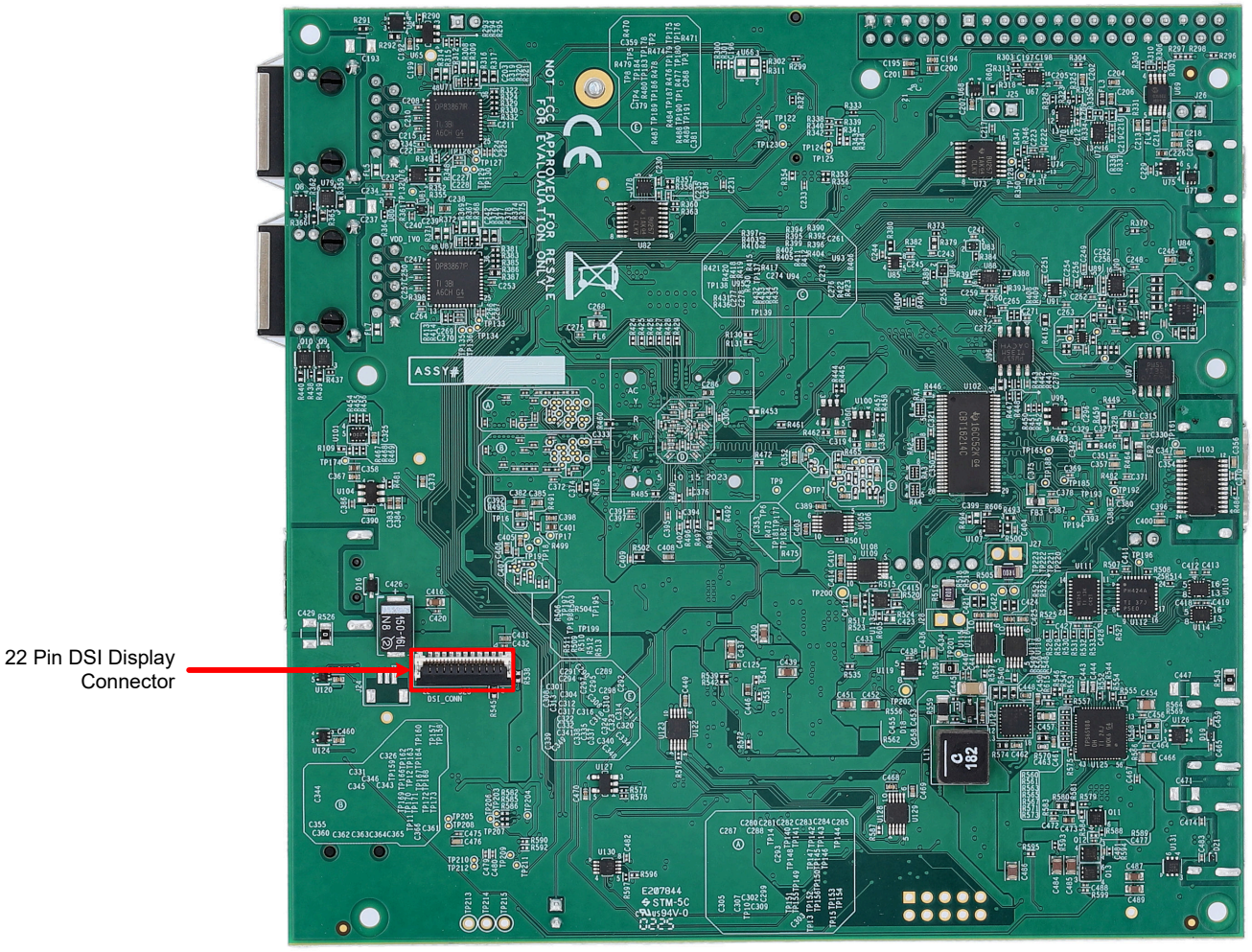

Figure 2-2. AM62L EVM Bottom Side

2.2 Key Features

The AM62L EVM is a high performance, standalone development platform that enables users to evaluate and develop industrial applications for the AM62L System-on-Chip (SoC) from Texas Instruments.

The following sections discuss the key features of the AM62L EVM:

2.2.1 Processor

- AM62L SoC, 11.9mm x 11.9mm, 373-pin BGA.

2.2.2 Power Supply

- Two USB Type-C ports (5V-12V input range)
- Optimized Power Solution with PMIC, Discrete Regulators and LDOs for the Processor and Peripherals
- RTC Supply Selection Header (5x3 Header) and Jumper (5x2) to select between RTC Only mode and RTC + xDDR mode

2.2.3 Memory

- 1x 2GB (16Gb) LPDDR4 supporting data rate up to 1600Mbps
- Micro SD® Card slot with UHS-1 support
- 1x 512Mbit Octal SPI NOR Flash memory
- 1x 1Gbit Quad SPI NAND Flash memory

- 512Kbit Inter-Integrated Circuit (I2C) board ID EEPROM
- 32GB eMMC Flash supporting HS200 mode

2.2.4 JTAG/Emulator

- XDS110 On-Board Emulator
- Supports 20-pin JTAG connection from external emulator

2.2.5 Supported Interfaces and Peripherals

- 1x USB 2.0 Type-C Interface, supports DFP and UFP modes (Data) and DRP mode (Power)
- 1x USB 2.0 Host Interface, Type-A
- 1x HDMI Interface
- Audio Line-In and MIC + Hedphone out
- M.2 Key E Interface supports both Wi-Fi and Bluetooth modules
- 2x Gigabit Ethernet ports supporting 10/100/1000Mbps data on RJ45 connector
- Quad port UART-to-USB circuit over micro-B USB connector
- User Test LEDs
- 8x INA devices for SoC power monitoring
- 2x Temperature Sensors near SoC and LPDDR4 for thermal monitoring

2.2.6 Expansion Connectors/Headers to Support Application Specific Add-On Boards

- 1x DSI Display connector
- 2x GPIO expansion connectors
- 3x MCAN headers
- 1x ADC Header

2.3 Power Requirements

The AM62L EVM can be powered through either of the two USB Type-C Connectors:

- Connector 1 (J17) - Power role – SINK, No Data role
- Connector 2 (J19) - Power role – DRP, Data role – USB 2.0 DFP or UFP

The AM62L EVM supports voltage input ranges of 5V-15V and 3A of current. A USB PD controller manufacturer part number TPS65988DHRSHR is used for PD negotiation upon cable detection to get necessary power required for the board. Connector 1 is configured to be an UFP Port and has no Data role. Connector 2 is configured as a DRP port. Connector 2 can act as DFP only when the board is being powered by Connector 1. When both the connectors are connected to external power supply, the port with highest PD power contract is selected to power the board.

The PD controller is configured to detect an external power supply source and if the source can supply greater than 15W at 5V. If the external power supply can source below or equal to 15W@5V, then the AM62L EVM enters the powered off state. The AM62L EVM is powered on when the external supply can source greater than 15W@5V.

Table 2-1. Type-C Port Power Roles

J24 (UFP)	J25 (DRP)	Board Power	Remarks
Plugged in	NC	ON – J17	J17 is UFP and only sinks power & J19 can act as DFP if a peripheral is connected
NC	Plugged in	ON – J19	J19 is UFP and can only sink power
Plugged in	Plugged in	ON – J17 or J19	Board is powered by the port with the highest PD power contract

The PD IC uses a SPI EEPROM to load the necessary configuration on power up so the PD can negotiate a power contract with a compatible power source.

The configuration file is loaded to the EEPROM using header J21. Once the EEPROM is programmed the PD obtains the configuration files via SPI communication. Upon loading the configuration files, the PD negotiates with the source to obtain the necessary power requirement.

Note

The EEPROM is preprogrammed with the configuration file for the operation of the PD controller

Power indication LEDs are provided for both the Type-C connectors for the user to identify which connector is powering the EVM Board. An external power supply (Type-C output) can be used to power the EVM but is not included as part of the EVM kit.

The external power supply requirements (Type-C) are:

Table 2-2. Recommended External Power Supplies

DigiKey Part Number	Manufacturer	Manufacturer Part Number
1939-1794-ND	GlobTek, Inc.	TR9CZ3000USBCG2R6BF2
Q1251-ND	Qualtek	QADC-65-20-08CB

Note

Minimum Voltage: 5VDC, Recommended Minimum Current: 3000mA
Maximum Voltage: 12VDC, Maximum current: 5000mA

Because the AM62L EVM implements USB PD for power, the device is able to negotiate to the highest Voltage/Current combination supported by both the Device and Power Adapter, as such, if the power supply exceeds the maximum voltage and current requirements listed above is acceptable as long as the power adapter is compliant with the USB-C PD specification.

2.4 Setup and Configuration

2.4.1 EVM DIP Switches

The AM62L EVM has one 8-position and two 4-position DIP Switches to set the desired SoC bootmode.

2.4.2 Bootmodes

Bootmode pins provide means to select the bootmode and options before the device is powered up. After every POR, the bootmode pins are the main source to populate the Boot Parameter Tables. The bootmode for the EVM is defined by three banks of switches SW2, SW3 and SW4, as shown in Figure 2-3, or by the I2C buffer connected to the Test automation (XDS110). This allows for AM62L SoC bootmode control by either the user (DIP Switch Control) or by the Test Automation (XDS110).

All the bits of switch (SW2, SW3 & SW4) have a weak pulldown resistor and a strong pullup resistor. Note that OFF setting provides a low logic level (‘0’) and an ON setting provides a high logic level (‘1’).

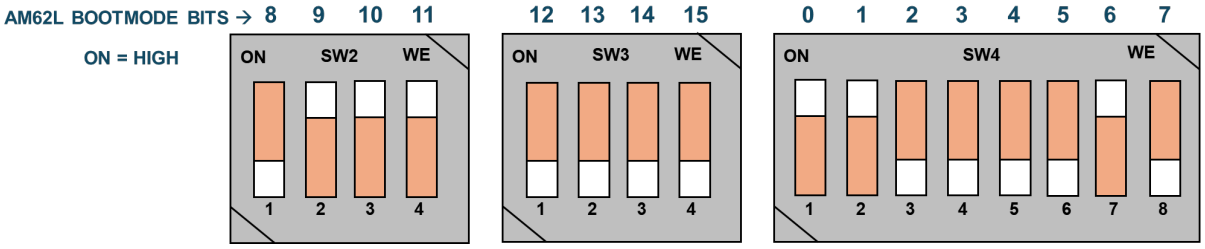

Figure 2-3. Example Bootmode switch (Full Pincount - SD Card Boot)

The bootmode pins of the SoC have associated alternate functions during normal operation. Hence isolation is provided using Buffer ICs to cater for alternate pin functionality. The output of the buffer is connected to the bootmode pins on the AM62L SoC and the output is enabled only when the bootmode is needed during a reset cycle.

The input to the buffer is connected to the DIP switch circuit and to the output of an I2C I/O Expander set by the test automation circuit. If the test automation circuit controls the bootmode, all the switches can be manually set to the OFF position. The bootmode buffer is powered by an always ON power supply to make sure that the bootmode remains present even if the SoC is power cycled.

SW4 (BOOTMODE[7:0]), SW2 (BOOTMODE[11:8]) and SW3 (BOOTMODE[15:12]) switches are used to set the SoC bootmode.

- BOOTMODE[2:0] – Denote system clock frequency (WKUP_OSC0_XI/XO) to ROM code for PLL configuration.
- BOOTMODE[6:3] – This provides primary bootmode configuration to select the requested bootmode after POR, that is, the peripheral/memory to boot from primary boot device selection details.
- BOOTMODE[9:7] – These pins provide optional configurations for primary boot and are used in conjunction with the bootmode selected.
- BOOTMODE[12:10] – Select the backup bootmode, that is, the peripheral/memory to boot from, if primary boot device failed.
- BOOTMODE[13] – This pin provides optional configurations for the backup boot devices. Switch SW3.7 when ON sets 1 and sets 0 if OFF, see the device specific TRM.
- BOOTMODE[15:14] – Selects Full or Reduced Pincount bootmode Mappings.

2.4.2.1 Bootmode Pin Mapping Options

The device supports two different BOOTMODE pin mapping options:

1. Reduced Pincount - Using only 4 of the bootstrap pins BOOTMODE[15:12]
2. Full Pincount - Using all 16 of the bootstrap pins BOOTMODE[15:0]

When the Full Pincount bootmode option is selected, all BOOTMODE[15:0] pins must be pulled up or down. The pins must not be left floating. When the Reduced Pincount option is selected, this applies only to BOOTMODE[15:12] pins.

Table 2-3. Full vs Reduced Bootmode Pin Mapping

BOOTMODE[15] SW3.4	BOOTMODE[14] SW3.3	Bootmode Mapping
OFF	OFF	Full Pincount
OFF	ON	Reduced Pincount
ON	OFF	
ON	ON	

2.4.2.2 Bootmode Pin Mapping (Reduced Pincount)

The reduced map offers the advantage of requiring less boostrap pins which can translate to fewer pullup or pulldown components required. This comes at the cost of making fewer bootmode options pin selectable.

To realize the desired reduction in pullup/pulldown components required, the input buffers for pins BOOTMODE[11:0] are disabled during POR unless BOOTMODE[15:14] are '00'. This avoids power consumption due to floating inputs on these pins if the reduced pincount option is used.

Table 2-4. BOOTMODE Pin Mapping (Reduced Pincount)

BOOTMODE[15] SW3.4	BOOTMODE[14] SW3.3	BOOTMODE[13] SW3.2	BOOTMODE[12] SW3.1	Primary	Backup	PLL Config
OFF	OFF	x	x	Selects the Full Pincount option, BOOTMODE[15:0] input buffers are enabled		
OFF	ON	OFF	OFF	Reserved		
OFF	ON	OFF	ON	Reserved		
OFF	ON	ON	OFF	No boot/Dev Boot	None	25MHz
OFF	ON	ON	ON	USB0	UART	25MHz
ON	OFF	OFF	OFF	eMMC	USB DFU	25MHz
ON	OFF	OFF	ON	QSPI	UART	25MHz

Table 2-4. BOOTMODE Pin Mapping (Reduced Pincount) (continued)

BOOTMODE[15] SW3.4	BOOTMODE[14] SW3.3	BOOTMODE[13] SW3.2	BOOTMODE[12] SW3.1	Primary	Backup	PLL Config
ON	OFF	ON	OFF	MMC/SD card	UART	25MHz
ON	OFF	ON	ON	eMMC	MMC1/SD card	25MHz
ON	ON	OFF	OFF	OSPI	UART	25MHz
ON	ON	OFF	ON	SPI	UART	25MHz
ON	ON	ON	OFF	UART	MMC1/SD card	25MHz
ON	ON	ON	ON	USB DFU	MMC1/SD card	25MHz

2.4.2.3 Bootmode Pin Mapping (Full Pincount)

This provides more flexibility and more booting peripherals to boot from.

The switch map to the bootmode functions (Full Pincount) is provided in the tables below.

Table 2-5. BOOTMODE Pin Mapping (Full Pincount)

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	Backup Bootmode Configuration	Backup Bootmode			Primary Bootmode Configuration			Primary Bootmode				PLL Configuration		

Table 2-6 gives the details on PLL reference clock selection.

Table 2-6. PLL Reference Clock Selection BOOTMODE[2:0]

BOOTMODE[2] SW4.3	BOOTMODE[1] SW4.2	BOOTMODE[0] SW4.1	PLL REF CLK (MHz)
OFF	OFF	OFF	Reserved
OFF	OFF	ON	Reserved
OFF	ON	OFF	24
OFF	ON	ON	25
ON	OFF	OFF	26
ON	OFF	ON	Reserved
ON	ON	OFF	Reserved
ON	ON	ON	Reserved

Table 2-7 gives primary boot media configuration details.

Table 2-7. Boot Device Selection BOOTMODE[6:3]

BOOTMODE[6] SW4.7	BOOTMODE[5] SW4.6	BOOTMODE[4] SW4.5	BOOTMODE[3] SW4.4	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMCSD Boot (SD Card Boot or eMMC Boot using UDA)
ON	OFF	OFF	ON	eMMC Boot
ON	OFF	ON	OFF	USB
ON	OFF	ON	ON	GPMC NAND
ON	ON	OFF	ON	Fast-xSPI
ON	ON	ON	OFF	xSPI

Table 2-7. Boot Device Selection BOOTMODE[6:3] (continued)

BOOTMODE[6] SW4.7	BOOTMODE[5] SW4.6	BOOTMODE[4] SW4.5	BOOTMODE[3] SW4.4	Primary Boot Device Selected
ON	ON	ON	ON	No boot/Dev Boot

Table 2-8 gives primary boot media configuration details.

Table 2-8. Primary Boot Media Configuration BOOTMODE[9:7]

BOOTMODE[9] SW2.2	BOOTMODE[8] SW2.1	BOOTMODE[7] SW4.8	Boot Device
Reserved	Read Mode 2	Read Mode 1	Serial NAND
Reserved	Reserved	Csel	OSPI
Reserved	Reserved	Csel	QSPI
Reserved	Mode	Csel	SPI
Reserved	Reserved	Reserved	UART
Port	Reserved	Fs/raw	MMCSD Boot (SD Card Boot or eMMC Boot using UDA)
Reserved	Reserved	Reserved	eMMC Boot
Reserved	Mode	Lane Swap	USB
Reserved	Reserved	Reserved	GPMC NAND
Reserved	Reserved	Reserved	Fast-xSPI
SFDP	Read Cmd	Mode	xSPI
Reserved	Reserved	No/Dev	No boot/Dev Boot

Table 2-9 provides backup bootmode selection details.

Table 2-9. Backup Boot Mode Selection BOOTMODE[13:10]

BOOTMODE[13] SW3.2	BOOTMODE[12] SW3.1	BOOTMODE[11] SW2.4	BOOTMODE[10] SW2.3	Backup Boot Device Selected
Reserved	OFF	OFF	OFF	None (No backup mode)
Mode	OFF	OFF	ON	USB
Reserved	OFF	ON	OFF	Reserved
Reserved	OFF	ON	ON	UART
Port	ON	OFF	ON	MMC/SD
Reserved	ON	ON	OFF	SPI

Table 2-10. Serial NAND Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW2.1]	Read Mode 2	0	Reserved (Read mode is taken from Read Mode 1)
		1	SPI/ 1-1-1 mode (Read mode is taken from Read Mode 2 and Read Mode 1 is ignored)
7 [SW4.8]	Read Mode 1	0	OSPI/ 1-1-8 Mode (valid only when Read Mode 2 is 0)
		1	OSPI/ 1-1-4 Mode (valid only when Read Mode 2 is 0)

Table 2-11. OSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
7 [SW4.8]	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 2-12. QSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
7 [SW4.8]	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 2-13. SPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW2.1]	Mode	0	SPI Mode 0
		1	SPI Mode 3
7 [SW4.8]	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 2-14. SD Card Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2] 13(1) [SW3.2]	Port	0	Reserved
		1	MMC Port 1 (4 bit width). This bit must be set to 1
7 [SW4.8]	FS/Raw	0	Filesystem mode
		1	Raw mode

(1) When MMCSD is the backup mode

Table 2-15. eMMC Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2] 13 [SW3.2]	Port	0	MMCSD Port 0 (8 bit width). This bit must be set to 0
		1	Reserved
7 [SW4.8]	FS/Raw	0	Filesystem mode
		1	Raw Mode

Table 2-16. USB Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2]	Core Voltage	0	Reserved
		1	
8 [SW2.1] 13(1) [SW3.2]	Mode	0	DFU (USB device firmware upgrade)
		1	Host (MSC boot)
7 [SW4.8]	Lane Swap	0	D+/D- lines are not swapped
		1	D+/D- lines are swapped

(1) When USB is the backup mode.

Table 2-17. xSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2]	SFDP	0	SFDP disabled
		1	SFDP enabled
8 [SW2.1]	Read cmd	0	0x0B Read Command
		1	0xEE Read Command
7 [SW4.8]	Mode	0	1S-1S-1S mode @ 50MHz
		1	8D-8D-8D mode @ 25MHz

2.4.2.4 Bootmode DIP Switch Configurations (Full Pincount)

2.4.2.4.1 Primary: SD Card, Backup: UART_0x0E43

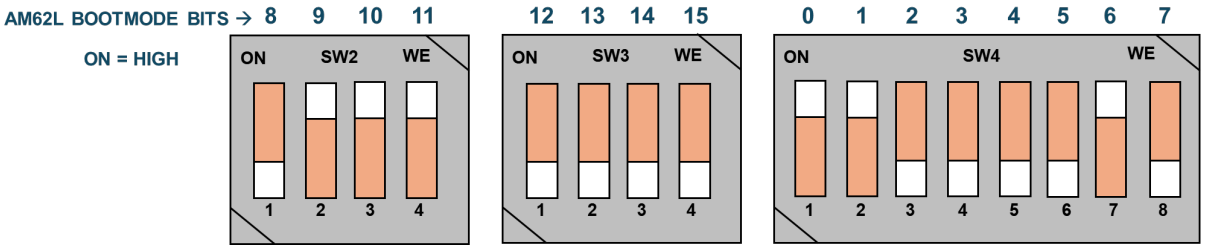

Figure 2-4. Bootmode switch Configuration for MMCSD/UART backup

2.4.2.4.2 Primary: xSPI SFPD 1, Backup: UART_0x0E73

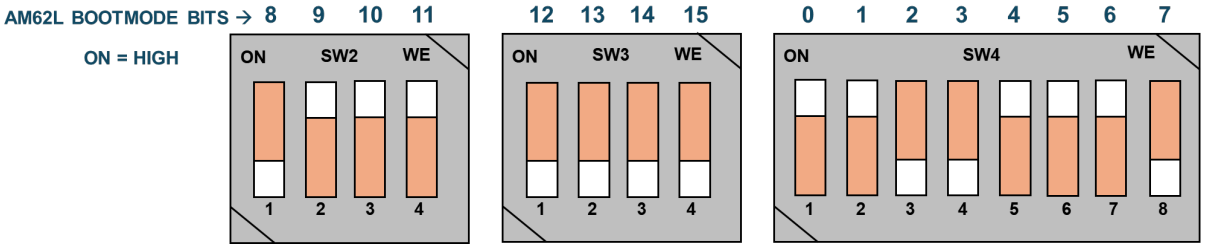

Figure 2-5. Bootmode switch Configuration for xSPI/UART backup

2.4.2.4.3 Primary: NOBOOT, Backup: None_0x00FB

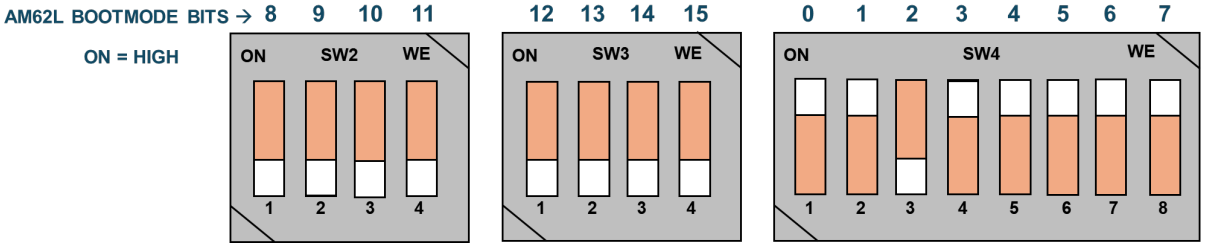

Figure 2-6. Bootmode switch Configuration for NOBOOT (DEVBOOT = 0)/No backup

2.4.2.4.4 Primary: GPMC NAND Original Timing, Backup: USB_DFU_0x04DB

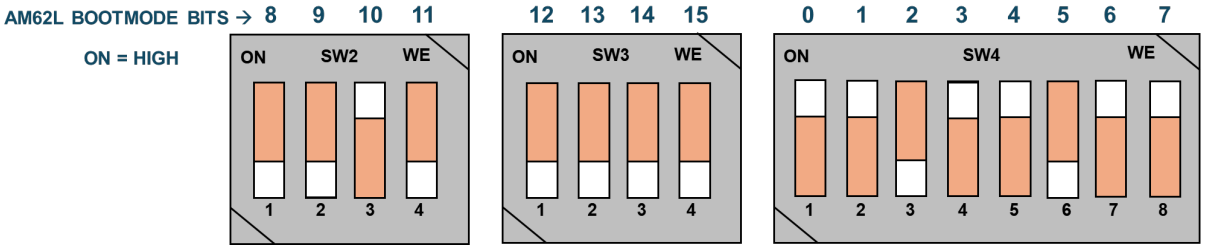

Figure 2-7. Bootmode switch Configuration for GPMC NAND/USB backup

2.4.2.4.5 Primary: GPMC NAND Original Timing, Backup: UART_0x0CDB

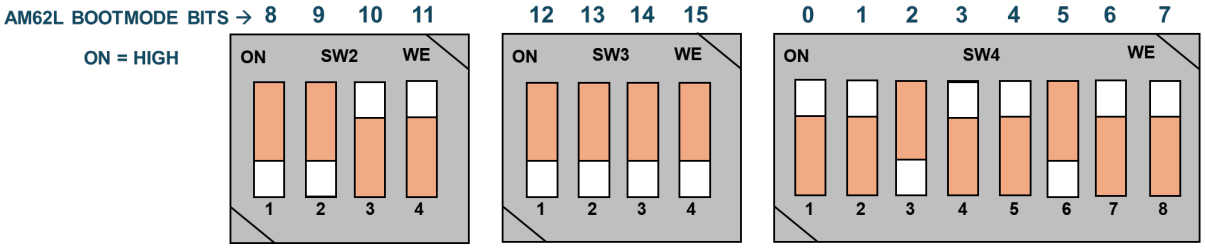

Figure 2-8. Bootmode Switch Configuration for GPMC NAND/UART Backup

2.4.2.4.6 Primary: eMMC, Backup: SD_card_0x344B

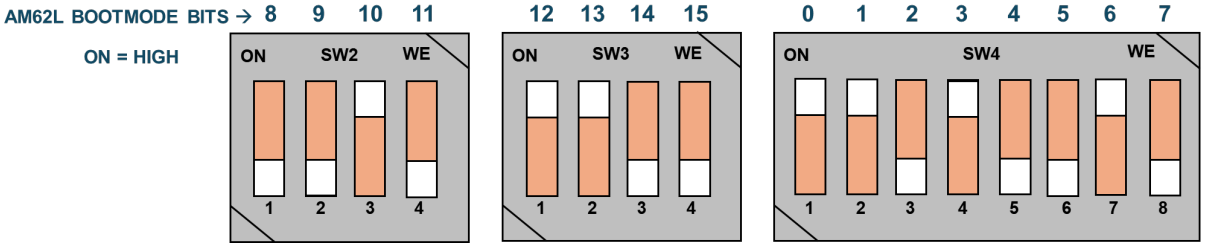

Figure 2-9. Bootmode switch Configuration for eMMC/MMCSD backup

2.4.3 User Test LEDs

The AM62L EVM board contains two LEDs for user defined functions.

Table 2-18 indicates the User Test LEDs and the associated GPIOs used to control it.

Table 2-18. User Test LEDs

Sl #	LED	GPIO used	SCH Net Names
1	LD8	GPIO0_123	SOC_GPIO0_123
2	LD2	U11.24(P27)	IO_EXP_TEST_LED

2.5 Power ON/OFF Procedures

Power to the EVM is provided through an external power supply with PD capability to either of the two USB Type-C® Ports.

Note

TI recommends the maximum length of the I/O cables not exceed 3 meters.

2.5.1 Power ON Procedure

1. Place the EVM boot switch selectors (SW4, SW3 and SW2) into selected bootmode. Example Full-Pincount bootmode for SD card is shown in Figure 2-10.
2. Connect your boot media (if applicable).
3. Attach the PD capable USB Type-C cable to the EVM Type-C (J17 or J19) Connector.
4. Connect the other end of the Type-C cable to the source, either AC Power Adapter, or Type C source device (such as a laptop computer).
5. Visually inspect that the LD6 LED is illuminated and that either the LD8 or LD11 LED is illuminated as well.
6. XDS110 JTAG and UART debug console outputs are routed to micro-USB ports J8 and J7, respectively.

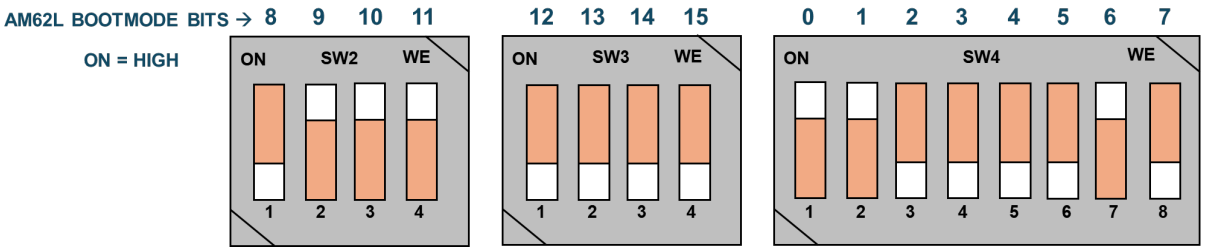

Figure 2-10. Example Full Pincount Bootmode (SD Card Boot)

2.5.2 Power OFF Procedure

1. Disconnect AC power from AC/DC converter.
2. Remove the USB Type-C cable from the EVM.

2.5.3 RTC Supply Selection Header

RTC Supply Selection Header is a 5x3 header that can be used to select either RTC Only mode or RTC + DDR mode using 5x2 Female gang jumper as shown in Figure 2-11.

Note

Refer to the AM62L Power Implementation application note (AM62L Power Supply Implementation) for more information on the connections required to support low power mode.

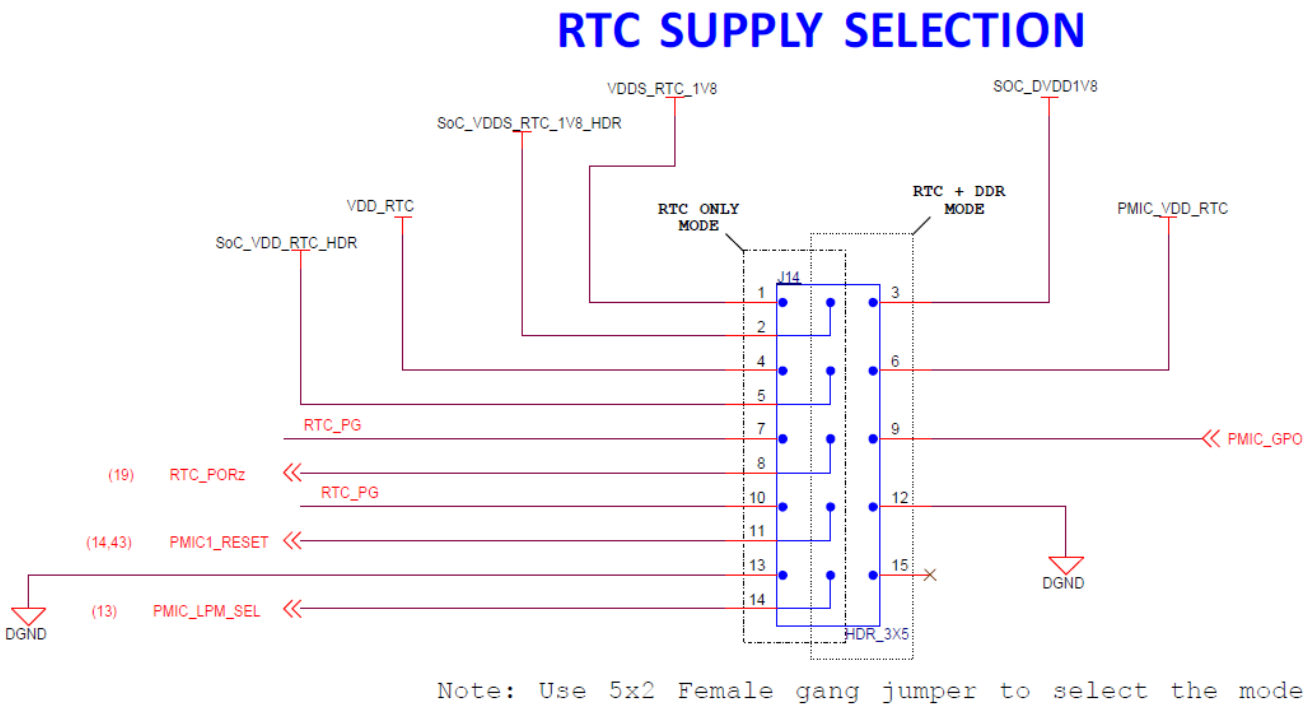

Figure 2-11. RTC Supply Selection Header

The pin-out details of the RTC Supply Selection Header are tabulated in Table 2-19.

Table 2-19. 15 pin RTC Supply Selection header (J14)

Pin No.	Net name
1	VDDS_RTC_1V8
4	VDD_RTC
7	RTC_PG
10	RTC_PG
13	DGND
2	SoC_VDDS_RTC_1V8_HDR
5	SoC_VDD_RTC_HDR
8	RTC_PORz
11	PMIC1_RESET (To PMIC 1)
14	PMIC_LPM_SEL
3	SOC_DVDD1V8
6	PMIC_VDD_RTC
9	PMIC_GPO
12	DGND
15	NC

2.5.4 RTC Only Mode

RTC Only mode is the low power mode in which only RTC domain of the device is active, and the MAIN domain is inactive.

During RTC only mode, RTC power and RTC_PORz of the SoC get supplied through the External Discrete LDOs and PMIC_LPM_EN0 signal output from the SoC used to control the PMIC_EN for powering off the PMIC.

RTC-only mode allows for maintaining time and calendar information.

2.5.5 RTC + DDR Mode

In RTC + DDR mode, both MAIN I/O domain and RTC power domain remain active. PMIC_LPM_EN0 signal output from the SoC used to enable/disable the Standby mode of the PMIC. When Standby mode is enabled, PMIC disables output from VDD_CORE and VDDA_1V8. RTC, DDR and I/O supplies from the PMIC remain active. When Standby mode is disabled, all the PMIC outputs are active.

2.5.6 Power Test Points

Test points for each power output on the board are mentioned in Table 2-20.

Table 2-20. Power Test Points

Sl #	Power Supply	Test Point	Voltage
1	VCC5V0_EXP	TP24	5
2	VCC3V3_EXP	TP25	3.3
3	VDD_1V0	TP132	1
4	VDD_1V2	TP41	1.2
5	VDDS_RTC_1V8	TP200	1.8
6	VDD_RTC	TP85	0.75
7	VPP_1V8	TP95	1.8
8	VDD_2V5	TP44	2.5
9	VDD_CORE	TP86	0.75
10	PMIC_VDD_RTC	TP97	0.75
11	VCC1V8_SYS	TP92	1.8

Table 2-20. Power Test Points (continued)

SI #	Power Supply	Test Point	Voltage
12	VDDA_1V8	TP101	1.8
13	VDD_LPDDR4	TP90	1.1
14	VCC_3V3_SYS	TP202	3.3
15	VCC_3V3_MAIN	TP102	3.3
16	VMAIN	TP112	12
17	VCC_5V0	TP117	5
18	VCC3V3_XDS	TP66	3.3
19	XDS_USB_VBUS	TP56	5
20	VCC3V3_TA	TP201	3.3
21	VBUS_5V0_TYPEA	TP91	5
22	VBUS_TYPEC1	TP111	12
23	VBUS_TYPEC2	TP120	12
24	FT4232_USB_VBUS	TP37	5
25	LDO_3V3	U61.8	3.3
26	VCC_3V3_FT4232	C20.2	3.3
27	VDD_MMC1_SD	TP174	3.3
28	VCC_5V0_HDMICONN	TP161	5

2.6 Interfaces

The following sections provide an overview of the different interfaces and circuits on the AM62L EVM. Table 2-21 shows the interface mapping for the AM62L EVM.

2.6.1 AM62L EVM Interface Mapping

Table 2-21. Interface Mapping

Interface Name	Port on SoC	Device Part Number
Memory - LPDDR4	DDR0	MT53E1G16D1ZW-046 WT:C
Memory - OSPI NOR	OSPI0	S28HS512TGABHM013
Memory - QSPI NAND	OSPI0	W25N01JWTBAG
Memory - Micro SD Socket	MMC1	MEM2051-00-195-00-A
Memory - eMMC	MMC0	MTFC32GBCAQTC-IT
Memory –Board ID EEPROM	SoC_I2C0	AT24C512C-MAHM-T
Ethernet 1 - RGMII	SoC_RGMII1	DP83867IRRGZ
Ethernet 2 - RGMII	SoC_RGMII2	DP83867IRRGZ
GPIO Port Expander 1	SoC_I2C1	TCA6424ARGJR
GPIO Expansion Connector - 2x5 HDR	UART2,VCC3V3, VCC5V0 and GPIOs	67997-410HLF
GPIO Expansion Connector - 2x15 HDR	SPI1, SPI3, UART4, I2C3 and GPIOs	PREC015DAAN-RC
USB -2.0 Type C	USB0	2012670005
USB -2.0 Type A	USB1	629104151021
DSI Interface	DSI0-TX	5019512230
3 x MCAN Interfaces	MCAN0, MCAN1 and MCAN2	TSM-104-02-L-SV
HDMI	VOUT0, McASP0and SoC_I2C1	Sil9022ACNU + TPD12S016PWR + DC04S019JA1R600
Audio Codec	McASP0 and SoC_I2C1	TLV320AIC3106IRGZT+ SJ-43514-SM
GPIO Port Expander 2	SoC_I2C1	TCA6424ARGJR
UART Terminal (UART-to-USB)	SoC_UAR SoC_UART[1:0], WKUP_UART0 and SoC_UART4	FT4232HL + 629105150521
Temperature Sensors	SoC_I2C1	TMP100NA/3K

Table 2-21. Interface Mapping (continued)

Interface Name	Port on SoC	Device Part Number
Current Monitors	SoC_I2C1	INA228AIDGSR
Connectivity - M.2 Key E	MMC2,McASP0 and SoC_UART1	2199119-4

2.6.2 DSI Interface

The DSI Display interface of the AM62L SoC is connected to a 22-pin display connector (J23) manufacturer part 5019512230 from Molex. The AM62L EVM supports 4 DSI-TX lanes for high-speed video link and low power command link with resolutions up to 1920x1080p @ 60fps. Apart from these 4 lanes, the 22-pin connector is provided with a 3.3V supply with sourcing capability till 500mA, I2C0 for any pre initializations and two GPIO's for handling interrupt and reset to the interfacing display.

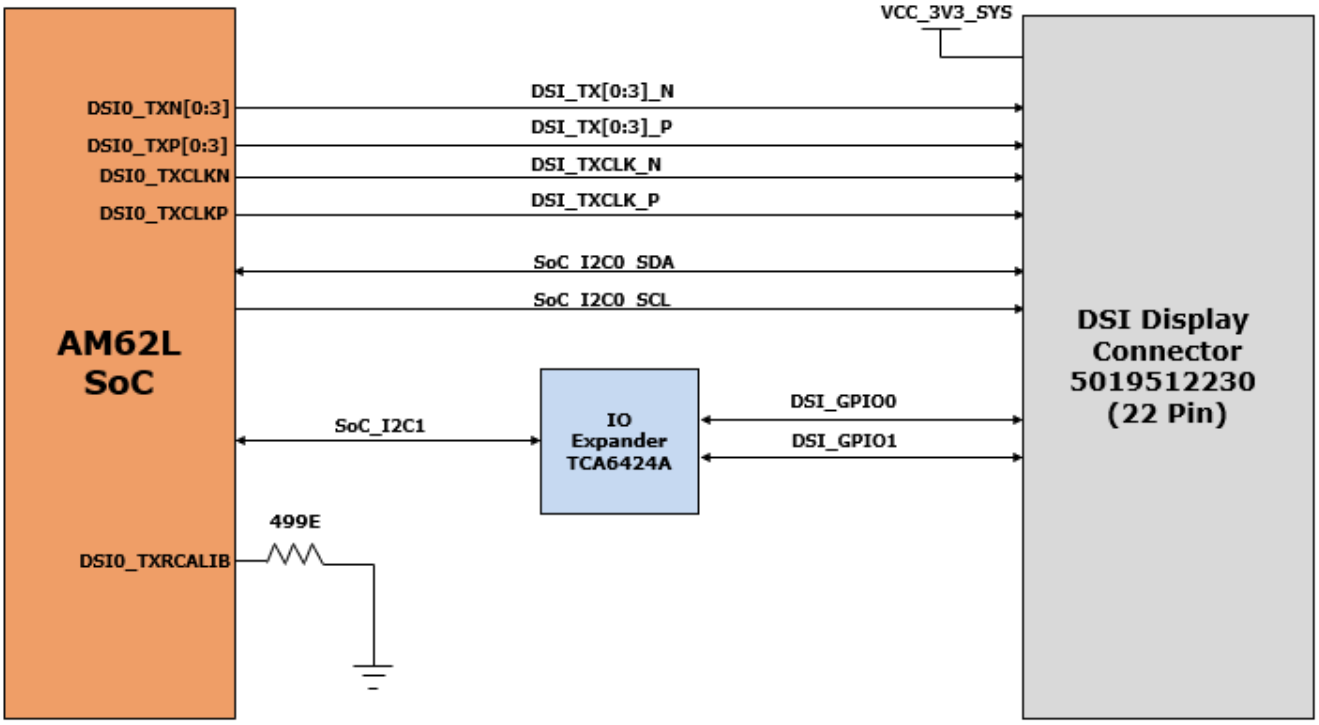

Figure 2-12. DSI Interface Block Diagram

The pin-out details of the display connector are tabulated in Table 2-22.

Table 2-22. DSI Display Connector Pinout (J23)

Pin No.	Signal
1	VCC_3V3_SYS
2	SOC_I2C0_SDA
3	SOC_I2C0_SCL
4	DGND
5	DSI_GPIO1
6	DSI_GPIO0
7	DGND
8	DSI_TX3_P
9	DSI_TX3_N
10	DGND
11	DSI_TX2_P

Table 2-22. DSI Display Connector Pinout (J23) (continued)

Pin No.	Signal
12	DSI_TX2_N
13	DGND
14	DSI_TXCLK_P
15	DSI_TXCLK_N
16	DGND
17	DSI_TX1_P
18	DSI_TX1_N
19	DGND
20	DSI_TX0_P
21	DSI_TX0_N
22	DGND

2.6.3 Audio Codec Interface

The AM62L EVM houses TI's TLV320AIC3106 Stereo Audio Codec to interface with AM62L via McASP0 group of signals.

TLV320AIC3106 is a low-power stereo audio codec with a stereo headphone amplifier, as well as multiple inputs and outputs programmable in single ended or fully differential configurations. The record path of the TLV320AIC3106 contains integrated microphone bias, digitally controlled stereo microphone preamplifier and Automatic Gain Control (AGC) with mix/Mux capability among the multiple analog inputs. The stereo audio DAC supports sampling rates from 8kHz to 96kHz.

1x Standard 3.5mm TRRS Audio Jack connector (J20) manufacturer part SJ-43514 is provided for MIC IN and Headphone output. Audio Codec's Line inputs are terminated to Test points. The codec can be configured over I2C1 with device address set to 0x1B.

The Controller Clock input, MCLK to the Audio Codec is provided through a 12.288MHz Oscillator. Audio serial data bus bit clock (BCLK) & Audio serial data bus input and output (DIN & DOUT) are connected to SOC's MCASP0 instance through a Mux/Demux. An AND output of RESETSTATz and a GPIO sourced via I/O expander is used to reset the Audio codec.

The TLV320AIC3106 is powered by an analog supply of 3.3V, a digital core supply of 1.8V, and a digital I/O supply of 3.3V.

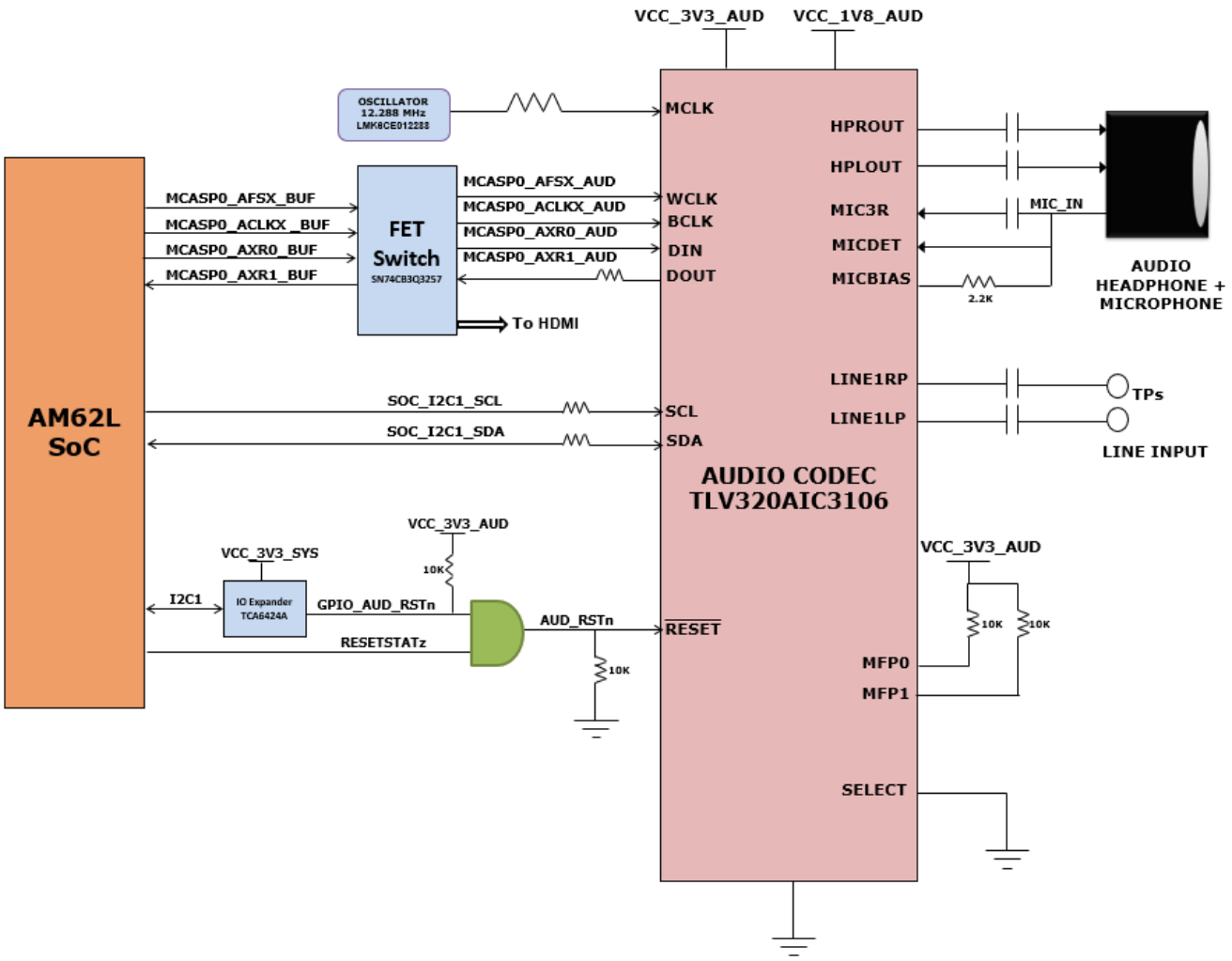

Figure 2-13. Audio Codec Interface Block Diagram

2.6.4 HDMI Display Interface

The DSS (Display Sub system) from the AM62L SoC is used on the EVM to provide HDMI Interface through a standard Type-A Connector. The EVM features a SiI9022A HDMI Transmitter from Lattice Semiconductor to convert the 24bit Parallel RGB DSS output stream as well as McASP0 signals to a HDMI-compliant digital audio and video signal.

To use SiI9022A, the SoC needs to set up the device. This is done via the I2C1 interface between the SoC and the SiI9022A. SoC_I2C1 instance connected to the HDMI Transmitter accesses the compatible mode registers, the TPI registers, and the CPI registers. Audio Data is sent from the SoC to HDMI transmitter through the McASP0 instance. HDMI_I2C Bus accesses the EDID and HDCP data on an attached sink device.

TMDS Differential data pairs along with the differential clock signals from the transmitter are connected to the HDMI connector through HDMI ESD device manufacturer part TPD12S016PWR which also acts as a load switch to limit current supplied to the HDMI connector from onboard 5V supply.

The HDMI Framer is powered using 3.3V Board I/O Supply and 1.2V for the AVCC & DVCC supply by a dedicated LDO manufacturer part TLV75512PDQNR.

The FET Switches are used to select the DSS video signals to HDMI Transmitter or GPIO Expansion header. By default, DSS video signals are connected to HDMI Transmitter and by shorting J29 1x2 header, user can change the selection to GPIO Expansion header without software dependency.

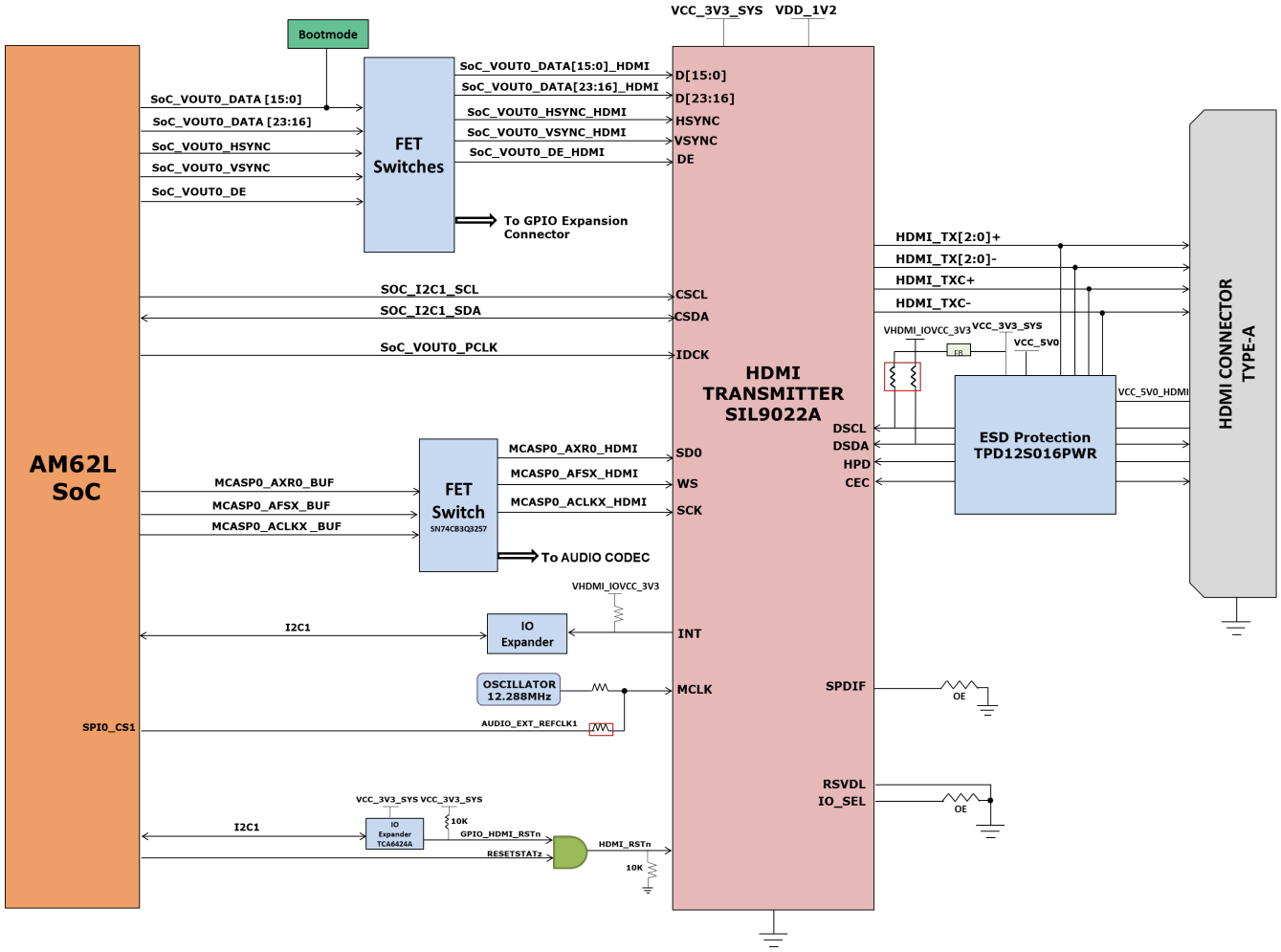

Figure 2-14. HDMI Interface Block Diagram

2.6.5 JTAG Interface

AM62L EVM includes XDS110 class on board emulation. The connection for this emulator uses a standard USB 2.0 micro-B connector and the circuit acts as a Bus powered USB device. The VBUS power from the connector is used to power the emulation circuit such that connection to the emulator is not lost when the power to the EVM is removed. Voltage translation buffers are used to isolate the XDS110 circuit from the rest of the EVM.

Optionally, JTAG Interface on the EVM is also provided through a 20-pin Standard JTAG cTI Header J10. This allows the user to connect to an external JTAG Emulator Cable. Voltage translation buffers are used to isolate the JTAG signals of cTI header from rest of the EVM. The output of the voltage translators from XDS110 Section and cTI Header Section are muxed and connected to the AM62L JTAG Interface. If a connection to the cTI 20-pin JTAG connector is sensed using an auto presence detect circuit, the mux routes the 20-pin signals from the cTI connector to the AM62L SoC in place of the on-board emulation circuit.

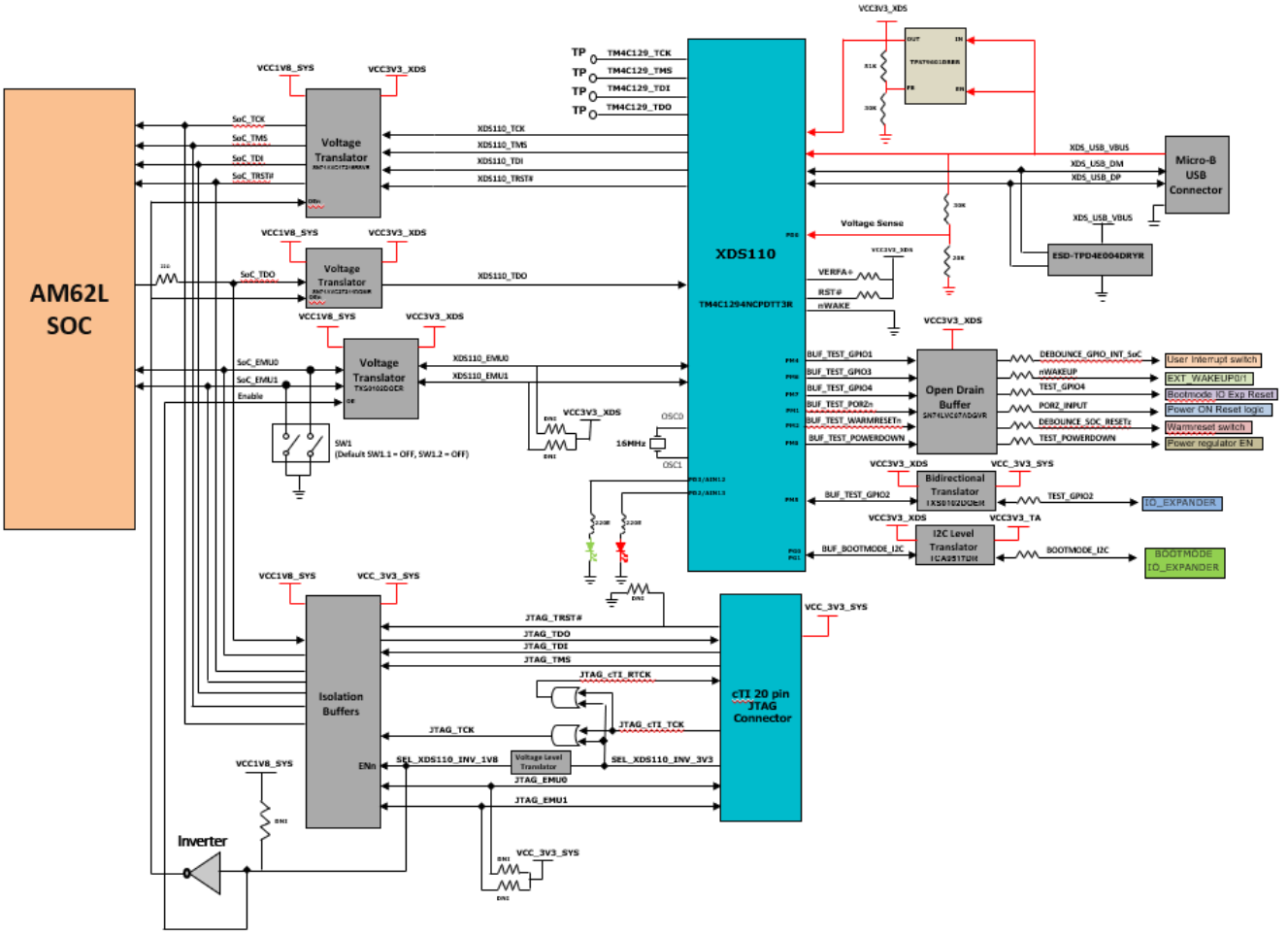

Figure 2-15. JTAG Interface Block Diagram

The pin-outs of the cTI 20-pin JTAG connector are given in Table 2-23. A ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ±15kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8kV contact discharge and ±12kV air-gap discharge.

Table 2-23. JTAG Connector (J10) Pinout

Pin No.	Signal
1	JTAG_TMS
2	JTAG_TRST#
3	JTAG_TDI
4	JTAG_TDIS
5	VCC_3V3_SYS
6	NC
7	JTAG_TDO
8	SEL_XDS110_INV_3V3
9	JTAG_cTI_RTCK
10	DGND
11	JTAG_cTI_TCK
12	DGND
13	JTAG_EMU0
14	JTAG_EMU1

Table 2-23. JTAG Connector (J10) Pinout (continued)

Pin No.	Signal
15	JTAG_EMU_RSTn
16	DGND
17	NC
18	NC
19	NC
20	DGND

2.6.6 XDS110 Test Automation

The AM62L EVM has an optional feature called TEST Automation to allow any external controller to manipulate some basic operations like Power Down, POR, Warm Reset, Bootmode control, etc. through XDS110.

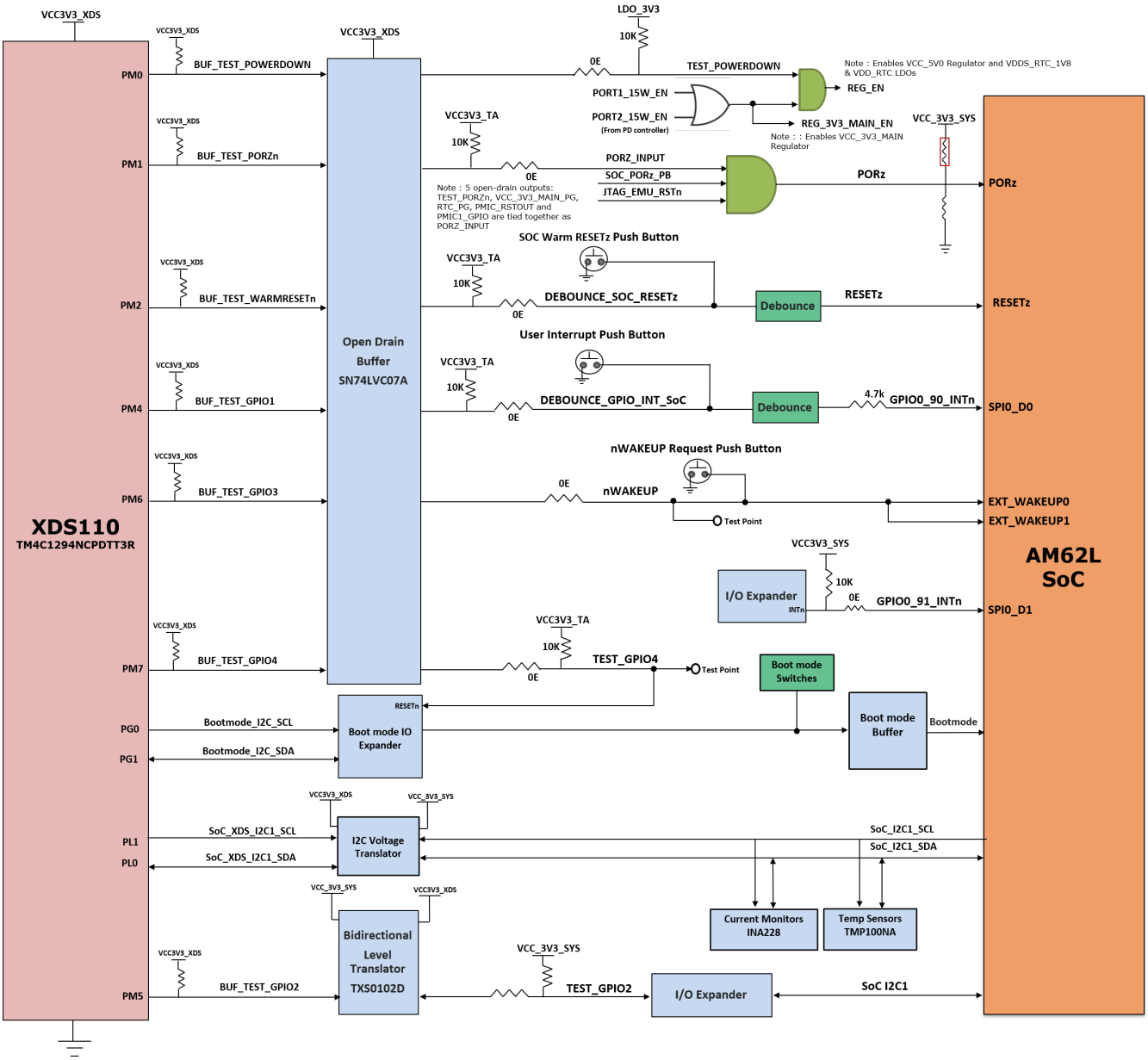

Figure 2-16. Test Automation Interface Block Diagram

The XDS110 Test automation has voltage translation circuits so that the controller is isolated from the I/O voltages used by the AM62L. Bootmode for the AM62L can be user controlled by either using DIP Switches or the XDS Test automation through the I2C I/O Expander. Bootmode Buffers are used to isolate the Bootmode controls driven through DIP Switches or I2C I/O Expander. The bootmode can also be set using one 8-bit DIP switch and two 4-bit DIP switches on the board, which connects a pullup resistor to the output of a buffer when the switch is set to the ON position and to a weaker pulldown resistor when set to OFF position. The outputs of the buffer are connected to the bootmode pins on the AM62L SoC and the output is only enabled when the bootmode is needed during a reset cycle.

When bootmode is to be set through XDS110 Test Automation, the required switch values are set at the I2C I/O expander output, which overwrites the DIP switch values to give the desired boot values to the SoC. The pins used for bootmode also have other functions which are automatically isolated by disabling the bootmode buffer during normal operation.

The power down signal from XDS110 instructs the EVM to power down all the rails except for dedicated power supplies on the board. Similarly, the PORZn signal provides a hard reset to the SoC and WARMRESETn for a warm reset to the SoC.

2.6.7 UART Interface

The four UART ports of the SoC (WKUP UART0, SoC UART0, SoC UART1 and SoC UART4) are interfaced with an FTDI Bridge FT4232HL for USB-to-UART functionality and then terminated on a micro-B USB connector (J7) on board. When the AM62L EVM is connected to a Host using USB cable, the computer can establish a Virtual COM Port which can be used with any terminal emulation application. Since the FT4232HL device is bus powered, the connection to the COM port will not be lost when the EVM power is removed.

Table 2-24. UART Port Interface

UART Port	USB-to-UART Bridge	USB Connector	COM Port
SoC_UART0	FT4232HL	J7	COM1
SoC_UART1			COM2
WKUP_UART0			COM3
SoC_UART4			COM4

The FT4232 chip is configured to operate in "Single-chip USB to four-channel UART" mode using the configuration file from an external SPI EEPROM connected to it. The EEPROM (93LC46B) supports 1Mbit/s clock rate. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from FTDI's web site. The FT_PROG is also used for programming the board serial number for users to identify the connected COM port with board serial number when one or more boards are connected to the computer.

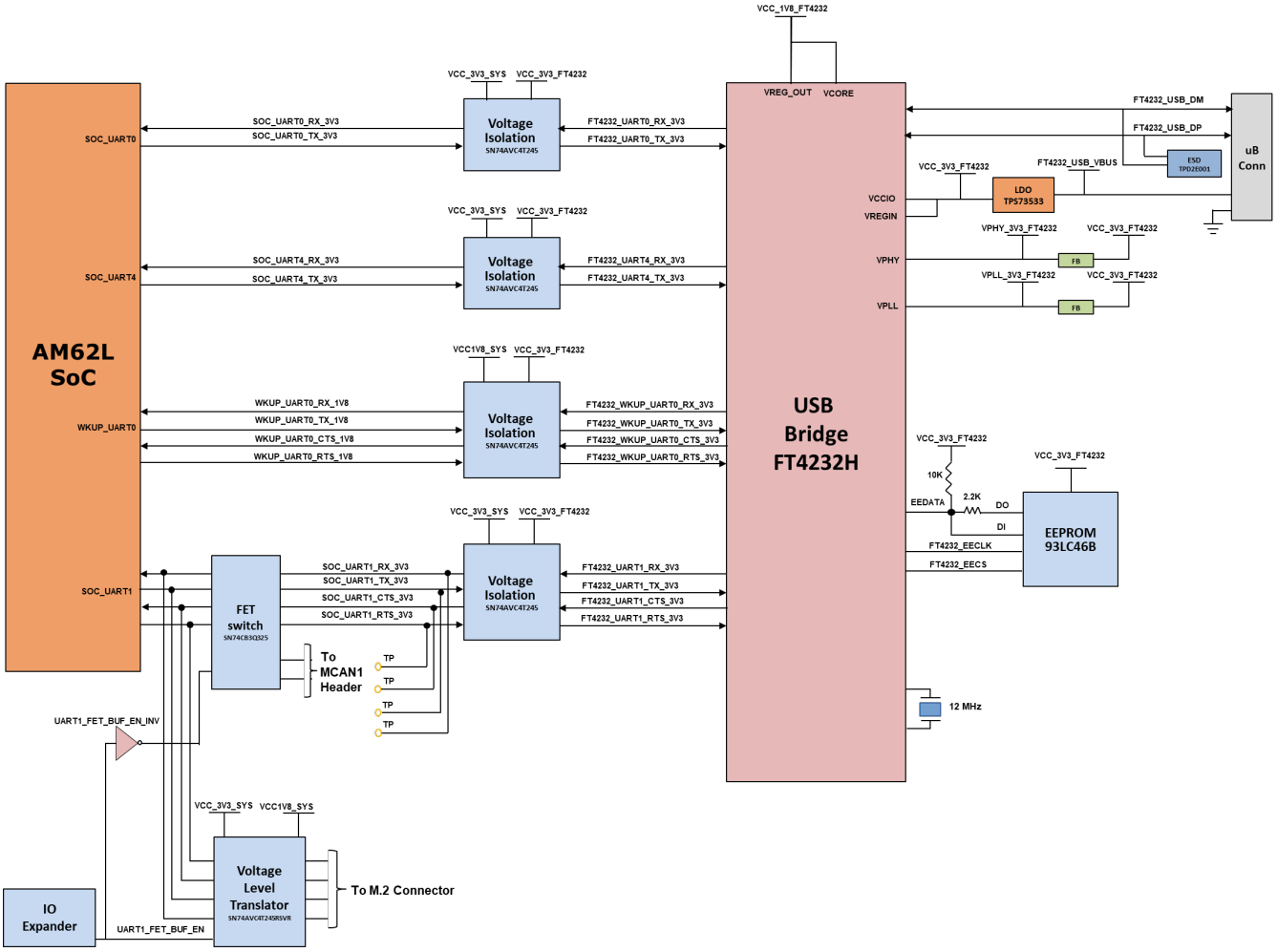

Figure 2-17. UART Interface Block Diagram

2.6.8 USB Interface

2.6.8.1 *USB 2.0 Type-A Interface*

USB 2.0 Data lines DP and DM from Type-A connector J23 are connected to the USB1 interface of the AM62L SoC to provide USB high-speed/full-speed communication. USB1_VBUS to the SoC is provided through a resistor divider network to support (5V-30V) VBUS operation. USB1_DRVVBUS from SoC controls the enable pin of a 500mA current limited Load switch manufacturer part number TPS2051BD to allow on board 5V supply to power the VBUS. This load switch has an over current indication pin connected to I2C based GPIO expander on the EVM.

A common mode choke of manufacturer part number DLW21SZ900HQ2B is provided on USB Data lines for EMI/EMC reduction along with ESD diode Protection manufacturer part number ESD122DMXR to suppress any transient voltages amd ESD diode manufacturer part number TSD05DYFR is provided to VBUS_5V0_TYPEA.

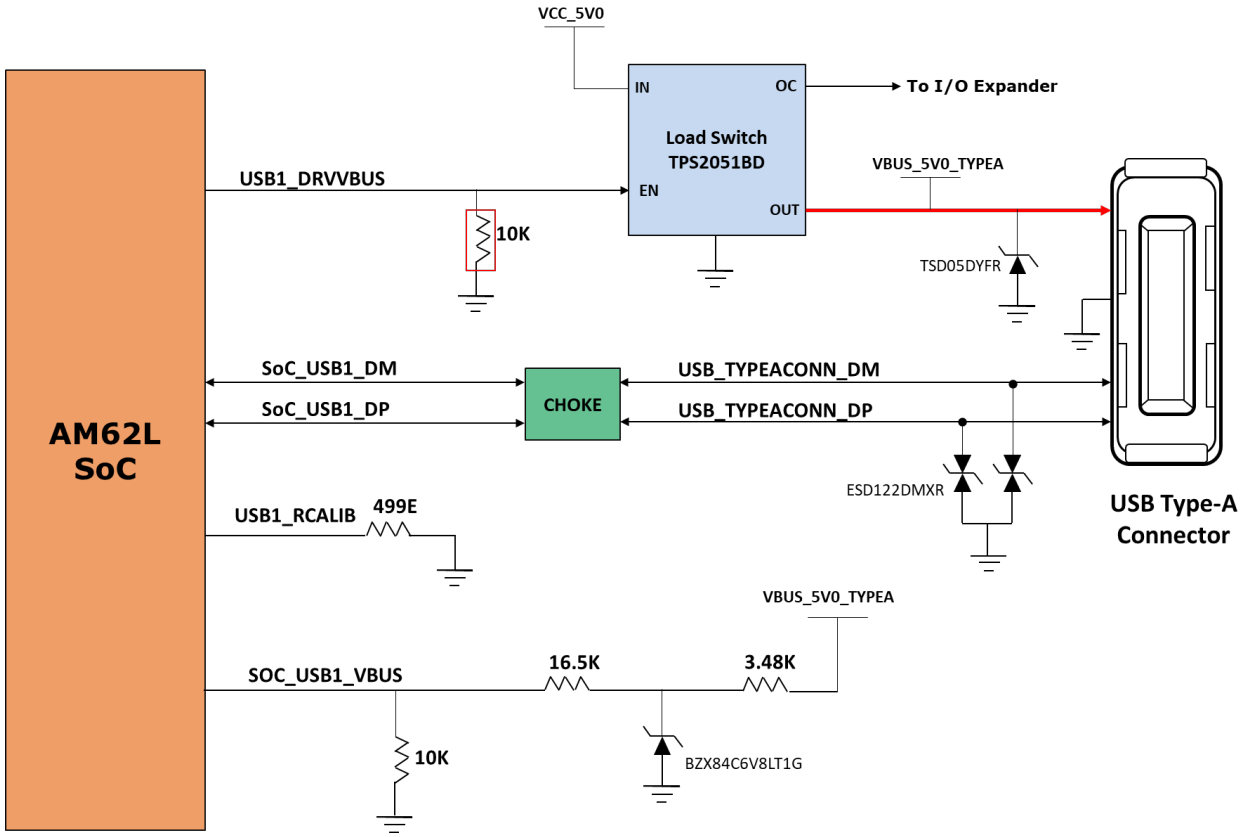

Figure 2-18. USB 2.0 Type-A Interface block diagram

2.6.8.2 USB 2.0 Type-C Interface

On the AM62L EVM, USB 2.0 Interface is offered through USB Type-C Connector J19 manufacturer part number 2012670005 which supports data rate up to 480Mbps. J19 can be used for data communication and also as a power connector sourcing supply to the EVM. J19 is configured as DRP port using PD controller TPS65988DHRSHR IC. J19 can act as either a Host or Device. The role of the port depends on the type of the device getting connected on the connector and its ability to either sink or source. When the port is acting as DFP, J19 can source up to 5V @500mA.

USB 2.0 Data lines DP and DM from J19 are provided with a choke and an ESD protection device. USB0_VBUS to the SoC is provided through a resistor divider network to support (5V-30V) VBUS operation.

A common mode choke of manufacturer part number DLW21SZ900HQ2B is provided on USB Data lines for EMI/EMC reduction. An ESD protection device of part number ESD122DMXR is included to dissipate any ESD strikes on USB 2.0 DP/DM signals. An ESD protection device of part number TPD1E01B04DPLT is included on CC signals and TVS2200DRVR IC is included on VBUS rail of Type-C Connector J19 to dissipate ESD strikes.

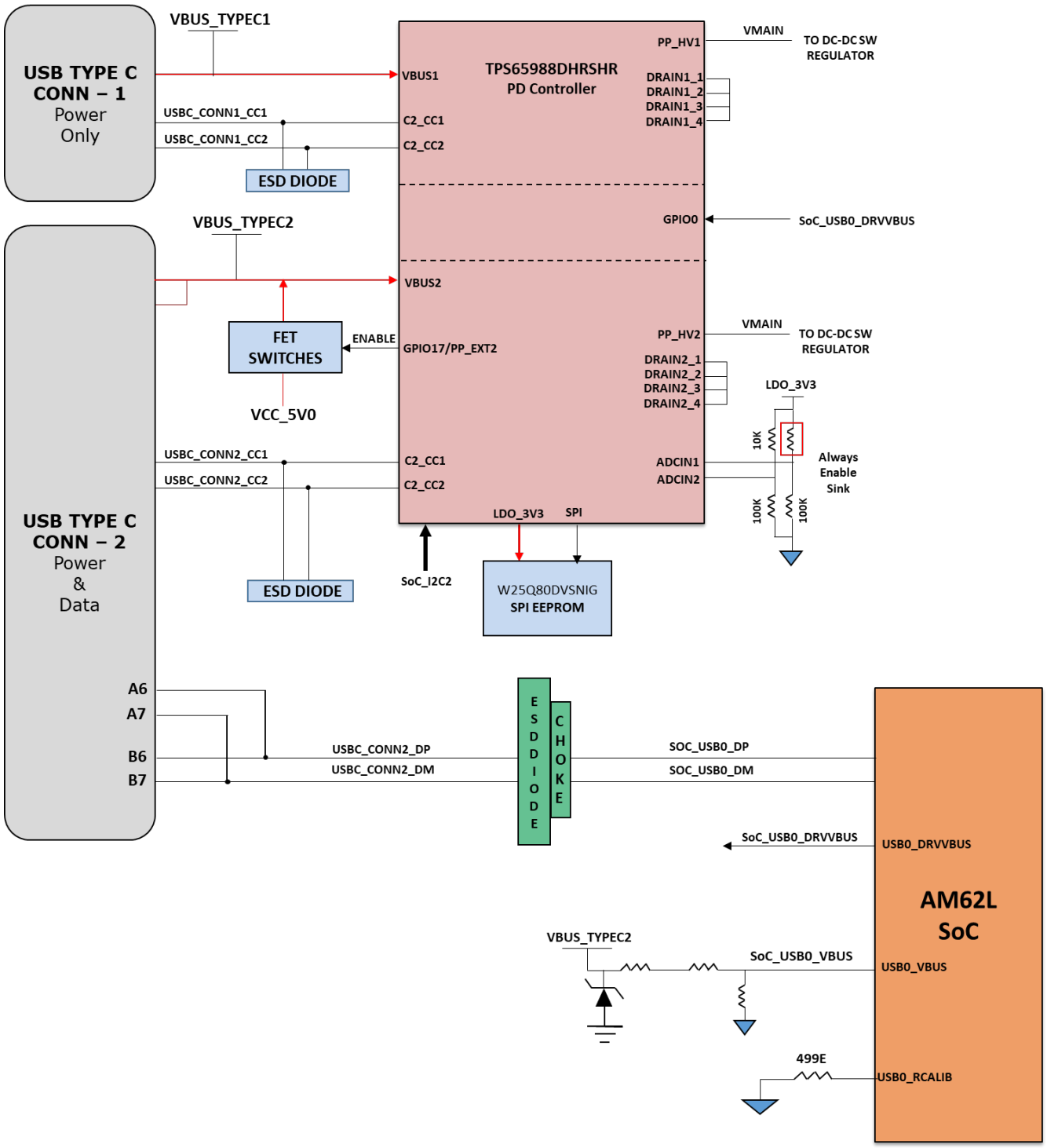

Figure 2-19. USB 2.0 Type-C Interface Block Diagram

2.6.9 MCAN Interface

The AM62L EVM includes 3 MCAN interfaces. MAIN_MCAN0, MAIN_MCAN1 and MAIN_MCAN2 shall be terminated to three 1x4 headers – J16, J6 and J18 respectively. For ESD protection, manufacturer part TPD2E001DRLR is connected to TX and RX of MCAN0, MCAN1 and MCAN2. First pins of all the three MCAN headers is connected to VCC_3V3_SYS and fourth pin is connected to GND.

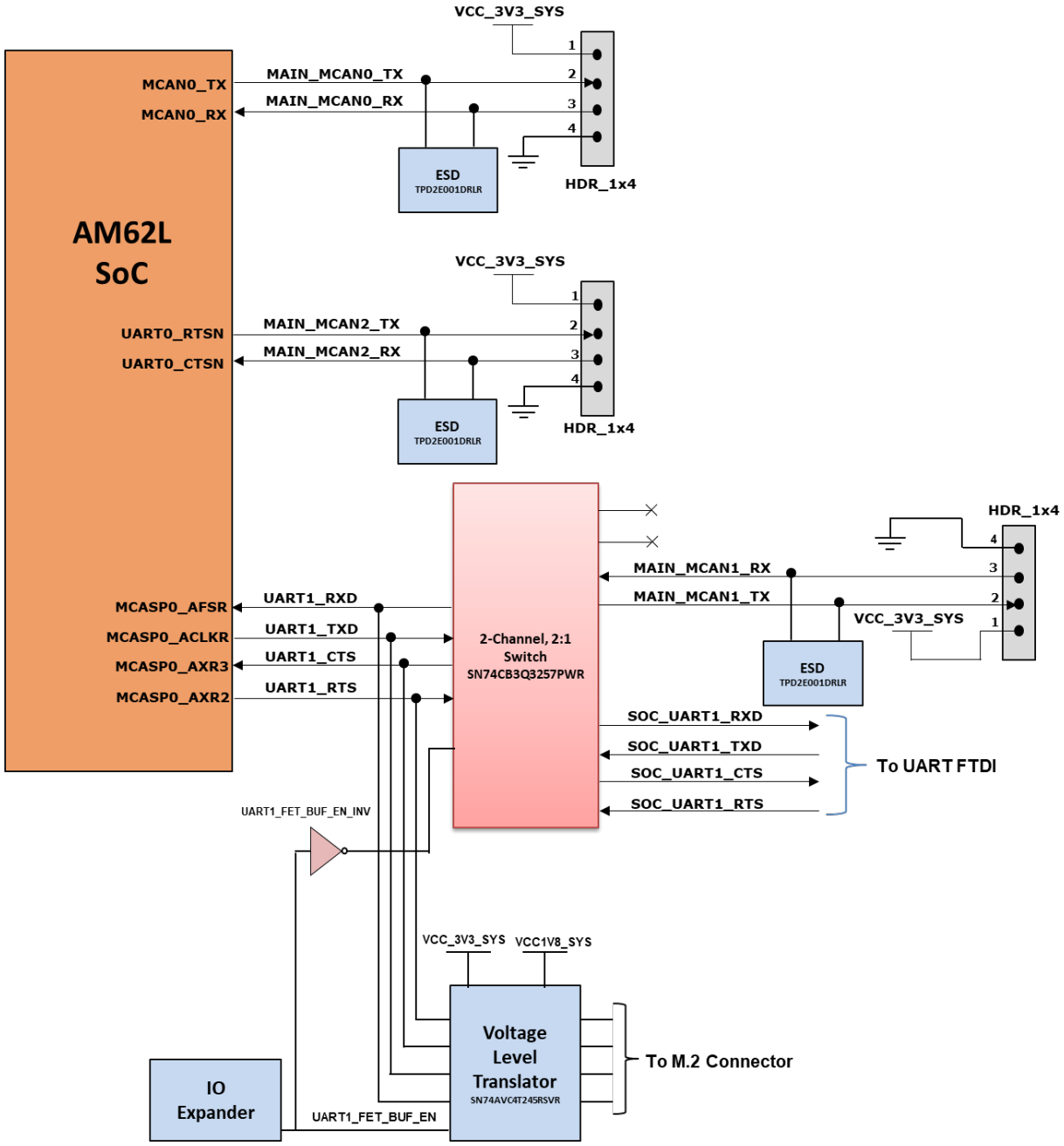

Figure 2-20. MCAN Interface Block Diagram

2.6.10 ADC Interface

AM62L EVM has four ADC inputs terminated on a 2x5 pin header (J11) with potentiometer connected to A01 pin of the header. ESD Diode, manufacturer part TPD1E10B06DPYR is provided for ADC0_AIN[0:3] signals for ESD protection.

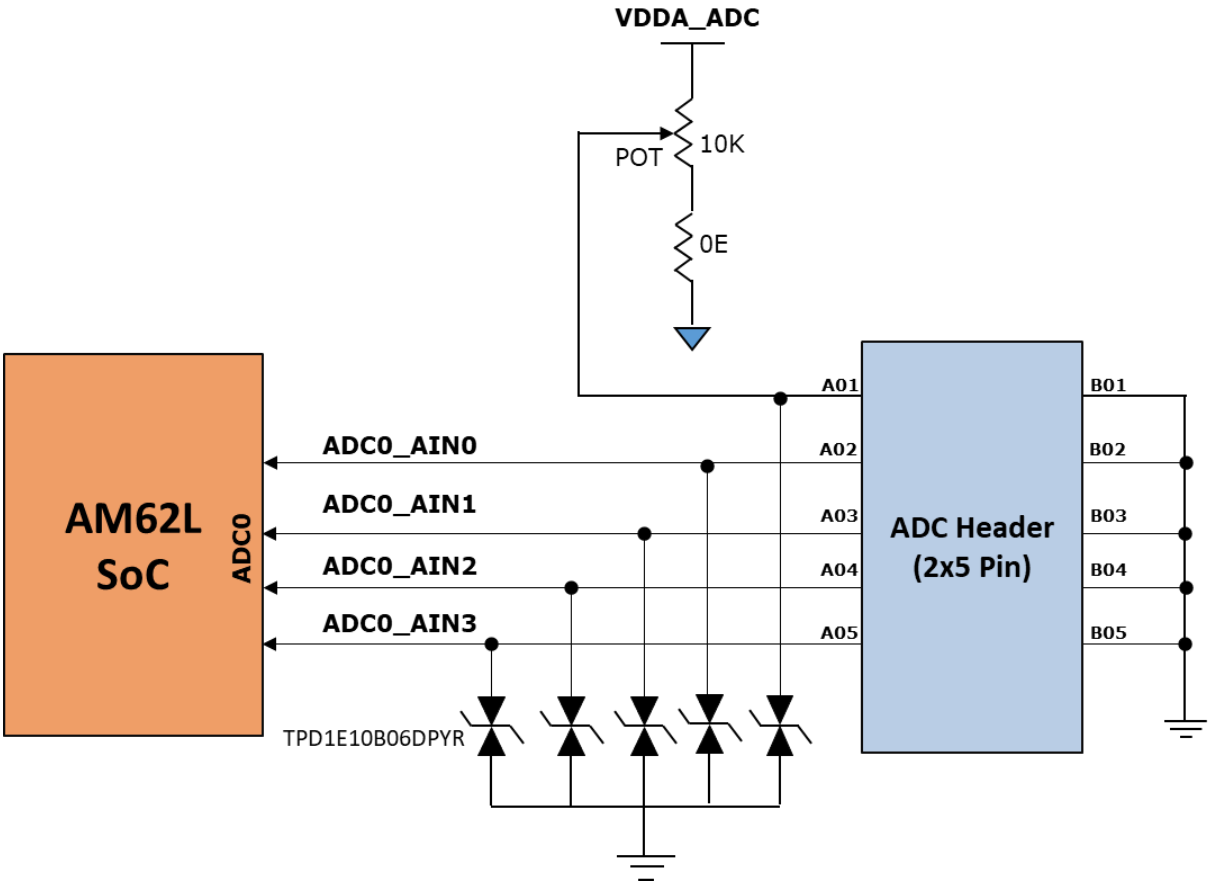

Figure 2-21. ADC Interface Block Diagram

2.6.11 Memory Interfaces

2.6.11.1 LPDDR4 Interface

The AM62L EVM houses Micron's (MT53E1G16D1ZW-046 WT:C) dual-rank, dual-die 2GB, 16-bit wide LPDDR4 memory supporting data rates up to 1600Mbps. The LPDDR4 memory is placed optimally and routed to the DDR0 group of the SoC to support point-to-point communication.

The LPDDR4 memory requires 1.8V for its core supply, thus reducing power demand. The I/Os are supplied from a 1.1V supply output from the PMIC. LPDDR4 reset (Active low) controlled by the AM62L SoC is pulled down to set the default active state. The provision for mounting a pullup resistor is also provided.

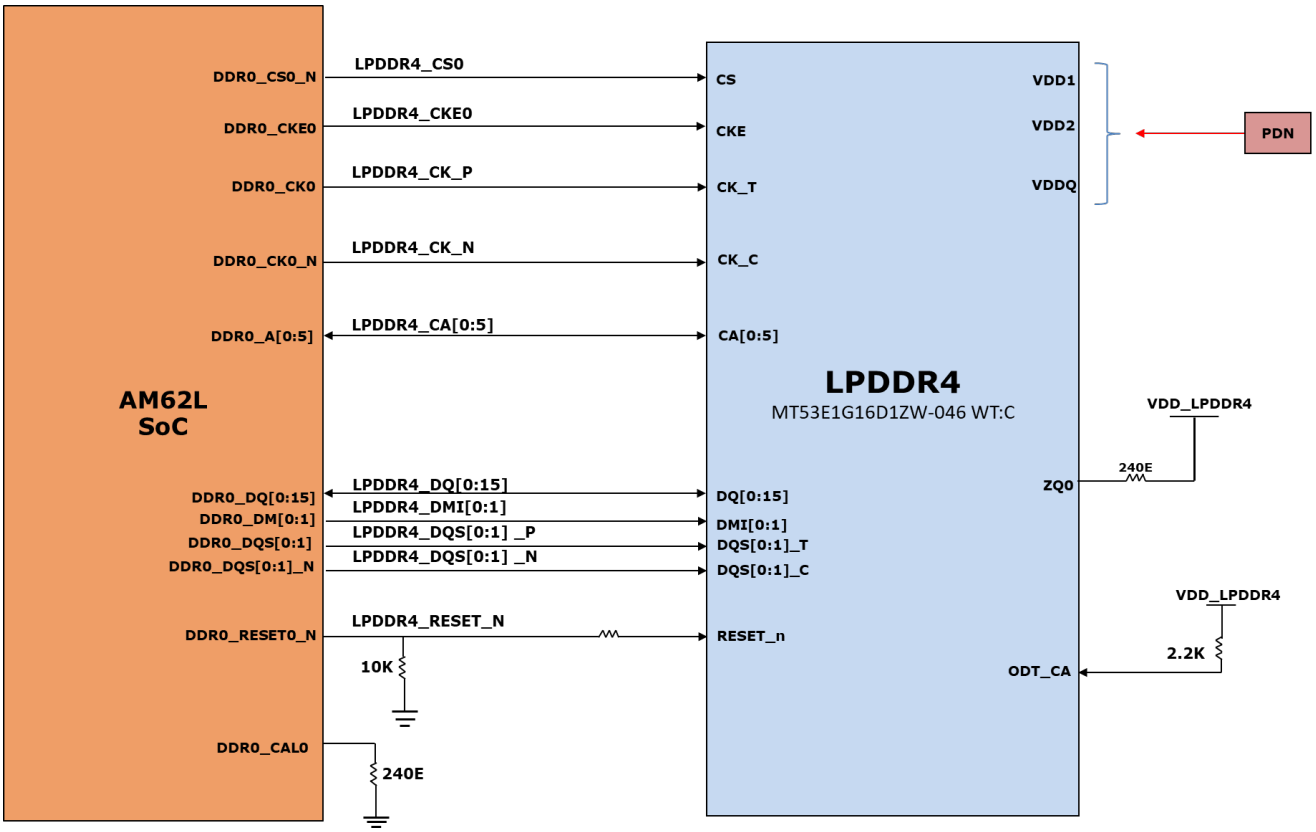

Figure 2-22. LPDDR4 Interface Block Diagram

2.6.11.2 Octal Serial Peripheral Interface (OSPI)

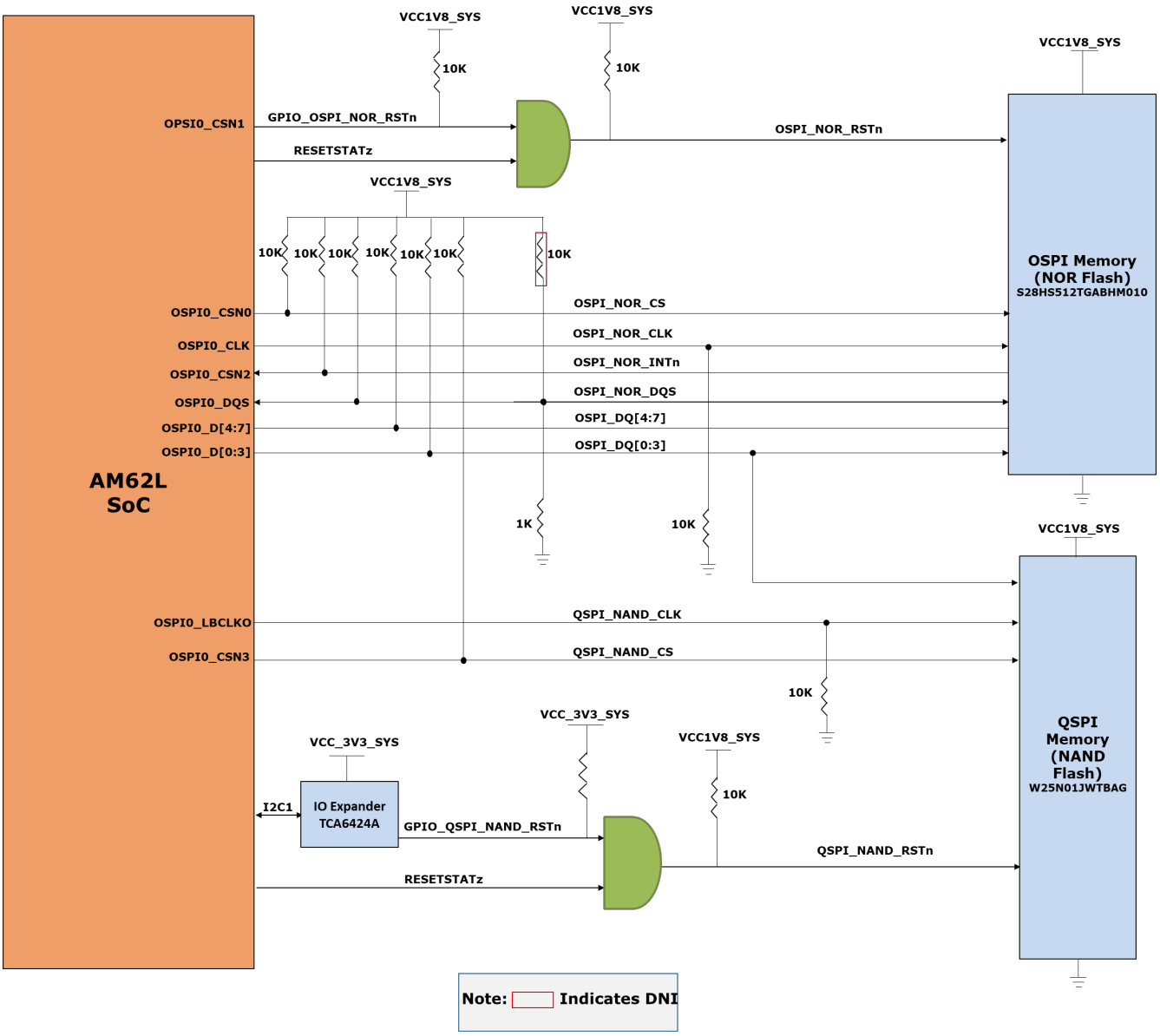

Figure 2-23. OSPI Block Diagram

2.6.11.2.1 OSPI NOR Flash

AM62L EVM board features a 512Mb OSPI NOR memory device from Cypress manufacturer part S28HS512TGABHM013 connected to the OSPI0 interface of the AM62L SoC. The OSPI memory supports single and double data rates with memory speeds up to 200MBps SDR and 400MBps DDR (200MHz clock speed). External pullup resistors are provided on DATA[7:0] to prevent bus floating. OSPI NOR Flash and QSPI NAND Flash are connected in Daisy chain method.

Reset: The reset for the OSPI NOR flash is connected to a circuit that ANDs the RESETSTATz from the AM62L with the signal GPIO_OSPI_NOR_RSTn from the SoC GPIO. A pullup resistor is provided on GPIO_OSPI_NOR_RSTn to set the default active state.

Power: Both VCC and VCCQ pins of the OSPI NOR Flash memory is supplied through an on board 1.8V system power. The OSPI I/O group is powered by the VDDS1 domain of SoC sourced from the same 1.8V system power.

2.6.11.2.2 OSPI NAND Flash

AM62L EVM board features a 1Gb QSPI NAND Flash memory device from Winbond manufacturer part W25N01JWTBAG connected to the OSPI0 interface of the AM62L SoC. The QSPI memory supports DTR (Dual Transfer Rate) up to 80MHz with 80MB/s continuous data transfer rate. QSPI NAND flash is connected to DATA[0:3].

Reset: The reset for the QSPI NAND flash is connected to a circuit that ANDs the RESETSTATz from the AM62L with the signal GPIO_QSPI_NAND_RSTn from the I/O Expander. A pullup resistor is provided on GPIO_QSPI_NAND_RSTn to set the default active state.

Power: VCC of the QSPI NAND Flash memory is supplied through an on board 1.8V system power.

2.6.11.3 MMC Interfaces

The AM62L SoC features three MMC ports (MMC0, MMC1 and MMC2). MMC0 is connected to eMMC, MMC1 is interfaced with a microSD Card connector and MMC2 is terminated to a M.2 Key E expansion connector for Wi-Fi and BT Module Interface.

2.6.11.3.1 MMC0 - eMMC Interface

The EVM board contains 32GB of eMMC flash memory from Micron manufacturer part MTFC32GBCAQTC-IT connected to the MMC0 port of the AM62L SoC.

The data bus from the flash memory is connected to 8 data bits of the MMC0 interface supporting HS200 single data rates up to 200MHz. The Micron eMMC is a communication and mass data storage device that includes a Multimedia Card (MMC) interface and a NAND Flash component. Option to mount external pullup resistors are provided on DAT[7:1] to prevent bus floating and series resistor is provided for CLK signal close to SoC pad to match the characteristic impedance.

The eMMC device requires two power supplies, 3.3V for NAND memory and 1.8V for the eMMC interface. The MMC0 interface I/Os of the SoC is powered by VDDSHV2 supplied from a fixed 1.8V supply.

The eMMC device requires active low reset from host. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it. The External Reset is provided by ANDing RESETSTATz from the SoC and a GPIO from I/O Expander. A pullup is provided on GPIO pin to set the default active state.

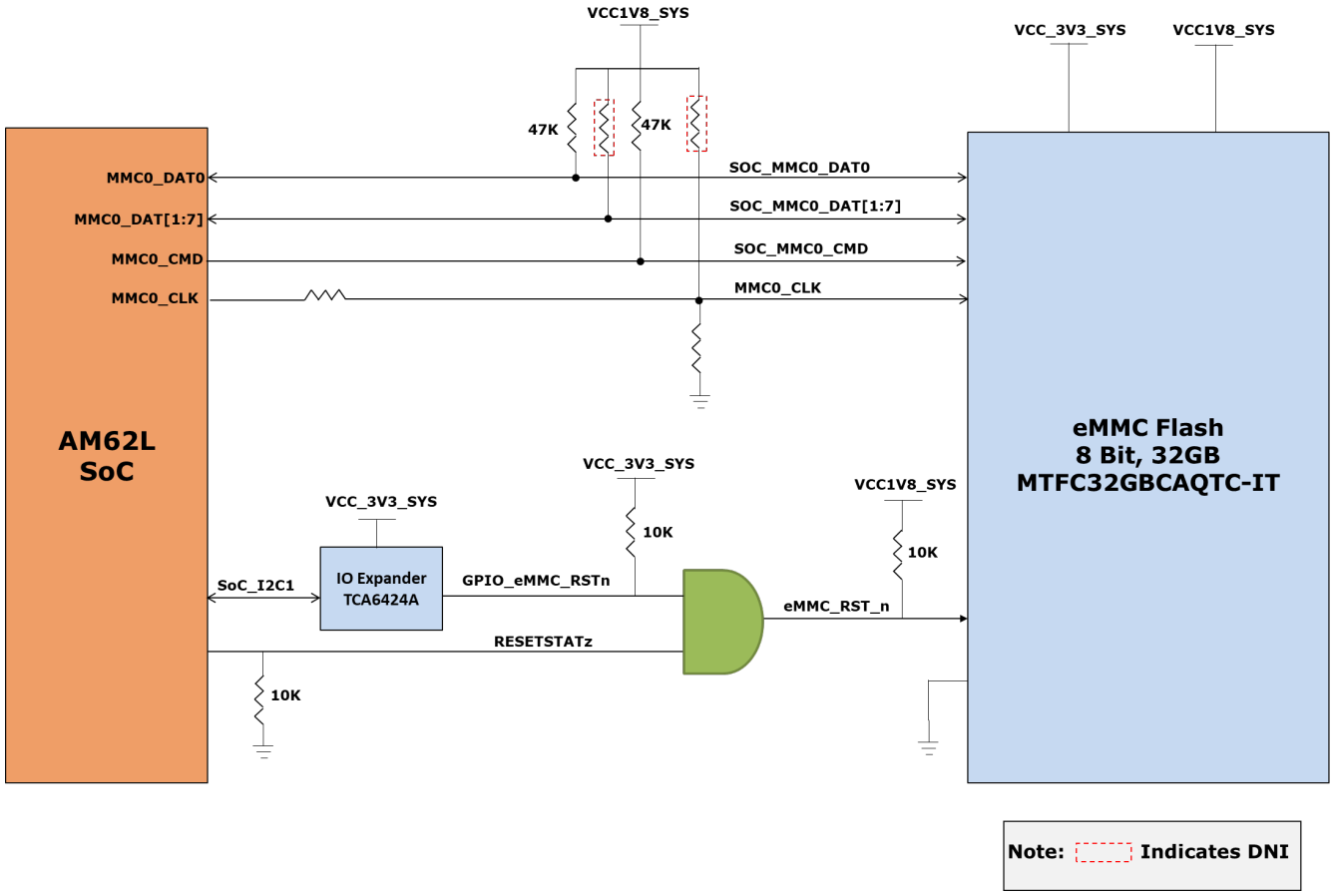

Figure 2-24. eMMC Interface Block Diagram

2.6.11.3.2 MMC1 - MicroSD Interface

The EVM board provides a microSD card Socket of manufacturer part number MEM2051-00-195-00-A connected to the MMC1 port of AM62L SoC. This supports UHS1 operation including I/O operations at both 1.8V and 3.3V. The microSD card interface is set to operate in SD mode by default. For high-speed cards, the ROM Code of the SoC attempts to find the fastest speed that the card and controller can support and then have a transition to 1.8V. The MMC1 I/O's of the SoC are powered by VDDSHV3 supplied from VDDSHV_SD_IO which is internally generated and supplied by the SoC.

The microSD card connector power is provided using a load switch of manufacturer part number TPS22918DBVR, which is controlled by ANDing the output of RESETSTATz and a GPIO from I/O Expander.

An ESD protection device of part number TPD6E001RSE is provided for data, clock, and command signals. TPD6E001RSE is a line termination device with integrated TVS diodes providing system-level IEC 61000-4-2 ESD protection, ±8kV contact discharge and ±15kV air-gap discharge.

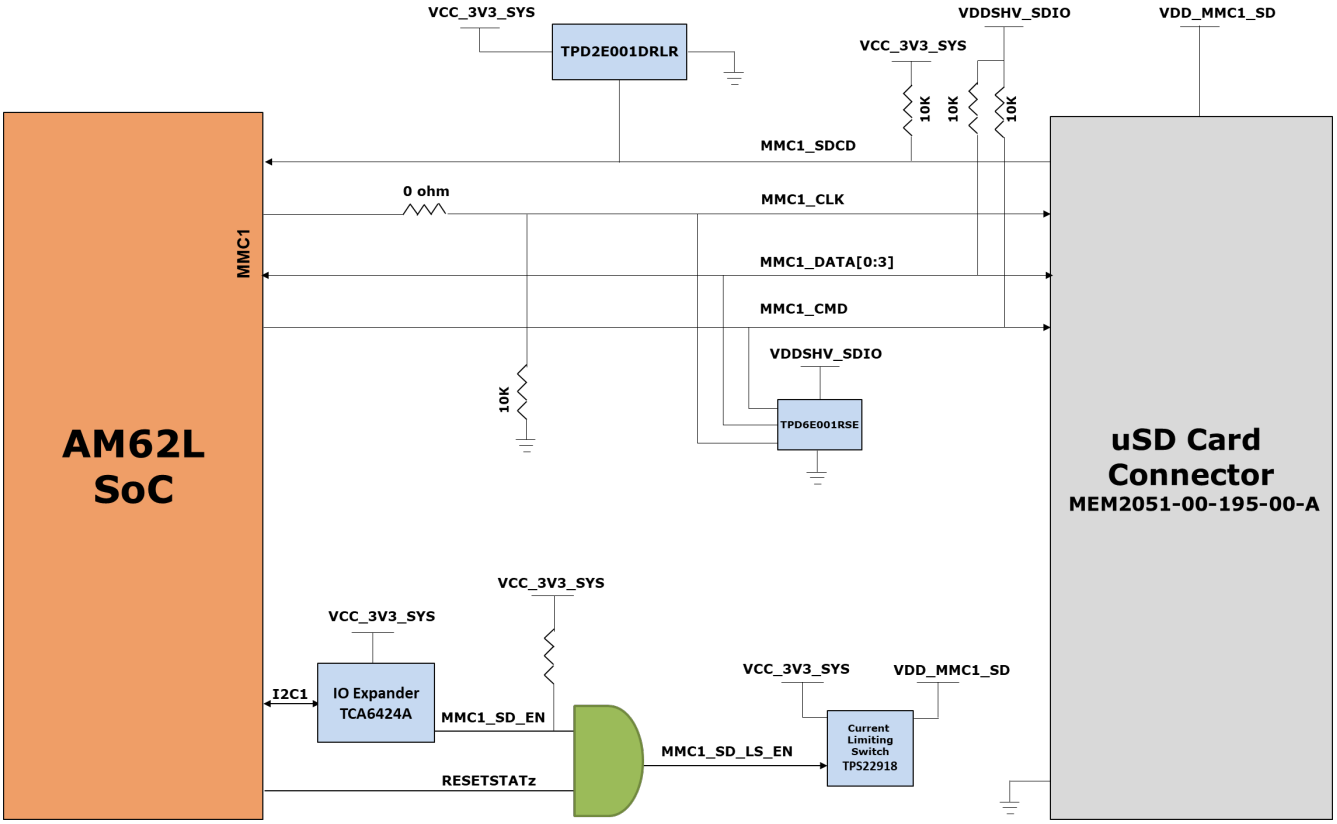

Figure 2-25. MicroSD Interface Block Diagram

2.6.11.3.3 MMC2 - M.2 Key E Interface

AM62L EVM has a M.2 Key E expansion for connecting Wi-Fi/BT modules to MMC2, UART1 and McASP0 interface through buffers. This can be used to interface with a Wi-Fi, dual-band, 2.4 and 5GHz module with antennas supporting Industrial temperature grade. The M.2 is provided with 4-bit I/O's of the MMC2 interface supporting IEEE standard 802.11a/b/g/n data. The M.2 connector can be interfaced with modules that can offer high throughput and extended range along with Wi-Fi and Bluetooth coexistence for a power-optimized design.

The M.2 Connector is provided with a 3.3V on board power supply to meet the power supply requirements of the interfacing modules. The MMC2 interface of the SoC is powered by the VDDSHV4 power domain, which is connected to 1.8V I/O supply.

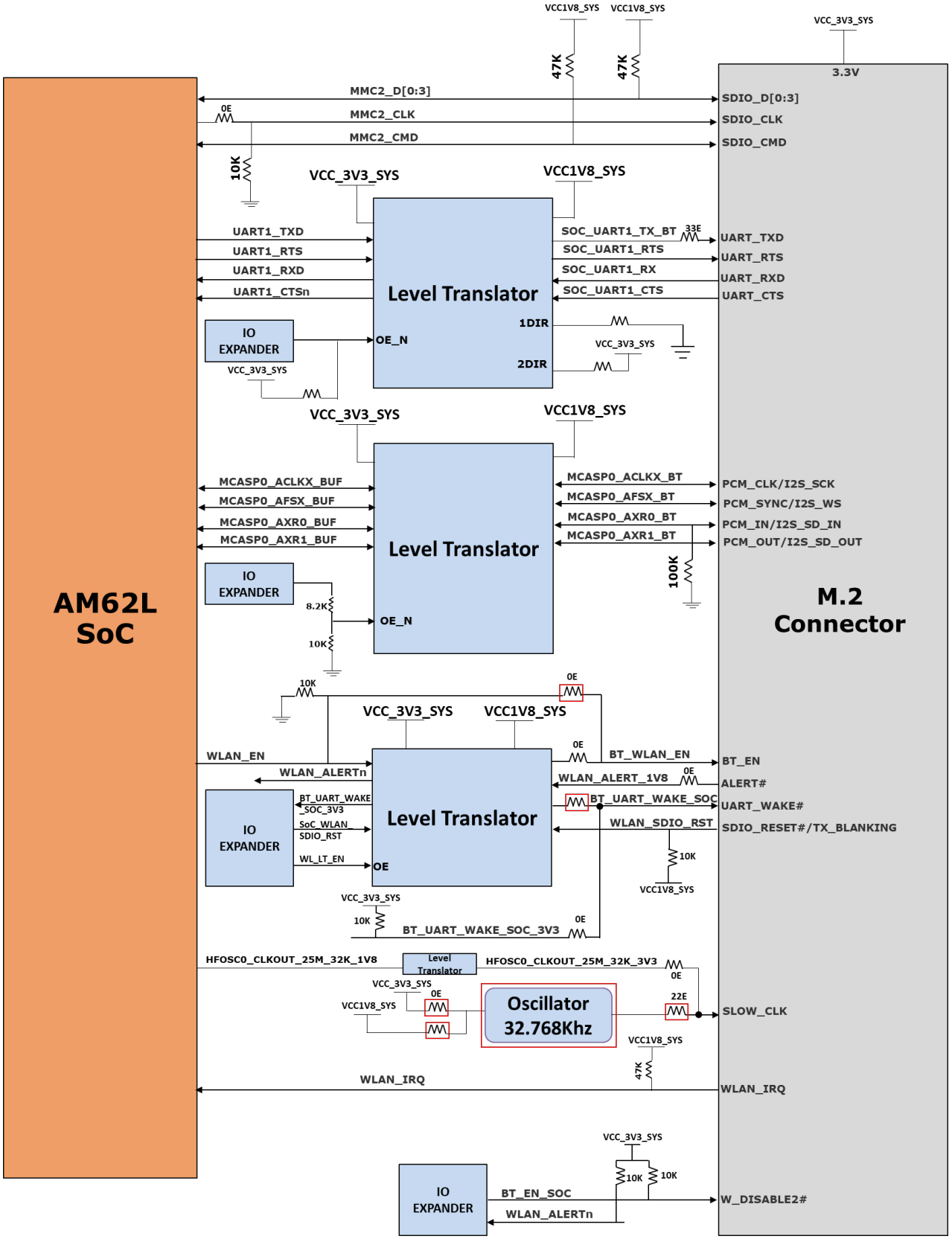

Figure 2-26. M.2 Interface Block Diagram

2.6.11.4 Board ID EEPROM

The AM62L EVM board can be identified remotely from its version and serial number data stored on the on-board EEPROM.

Board ID memory AT24C512C-MAHM-T from Microchip is interfaced to the I2C0 port of the SoC and is configured to respond to address 0x51 programmed with the header description. I2C address of the EEPROM can be modified by driving the A0 pin to high and A1, A2 pins to LOW. The first 259 bytes of memory are preprogrammed with identification information for each board. The remaining 65277 bytes are available to the user for data or code storage.

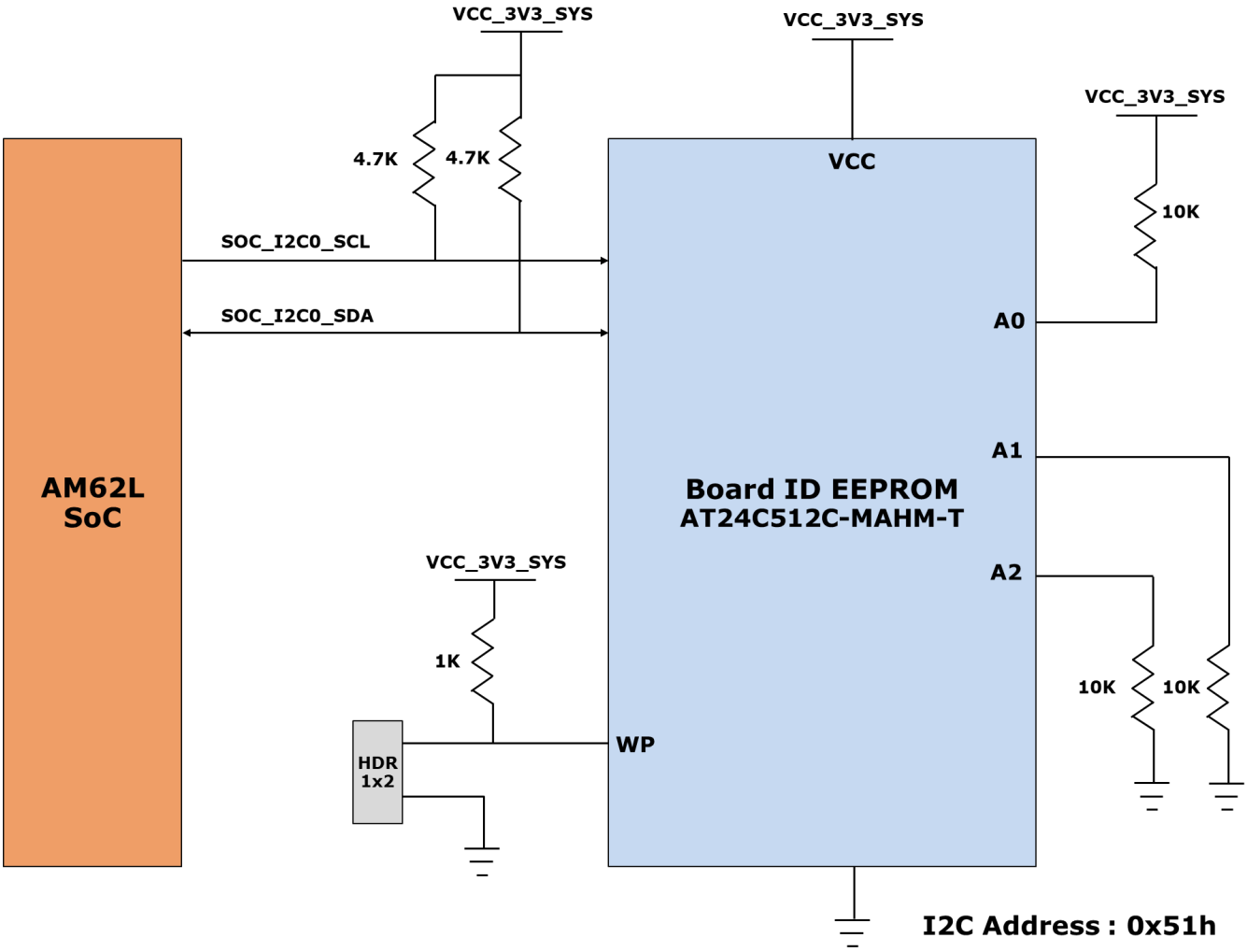

Figure 2-27. Board ID EEPROM Interface Block Diagram

2.6.12 Ethernet Interface

The AM62L EVM offers two Ethernet Ports of 1 Gigabit Speed for external Communication. Two channels of RGMII Gigabit Ethernet CPSW Ports from the AM62L SoC are connected to separate Gigabit Ethernet PHY Transceivers DP83867, which are finally terminated on two RJ45 connectors with integrated magnetics.

The 48pin version of the PHY DP83867 is configured to advertise 1-Gb operation with the Tx & Rx clock skew set to accommodate the internal delay inside the AM62L. CPSW_RGMII1 and CPSW_RGMII2 Ports share a common MDIO Bus to communicate with the external PHY Transceiver.

Two Single port RJ45 Connectors manufacturer part LPJG16314A4NL from Link-PP are used on the board for Ethernet 10/100/1000Mbps Connectivity. RJ45 Connectors have integrated magnetics and LEDs for indicating 1000BASE-T link as well as receive or transmit activity.

I/O supply to the Ethernet PHY is set to 1.8V I/O level.

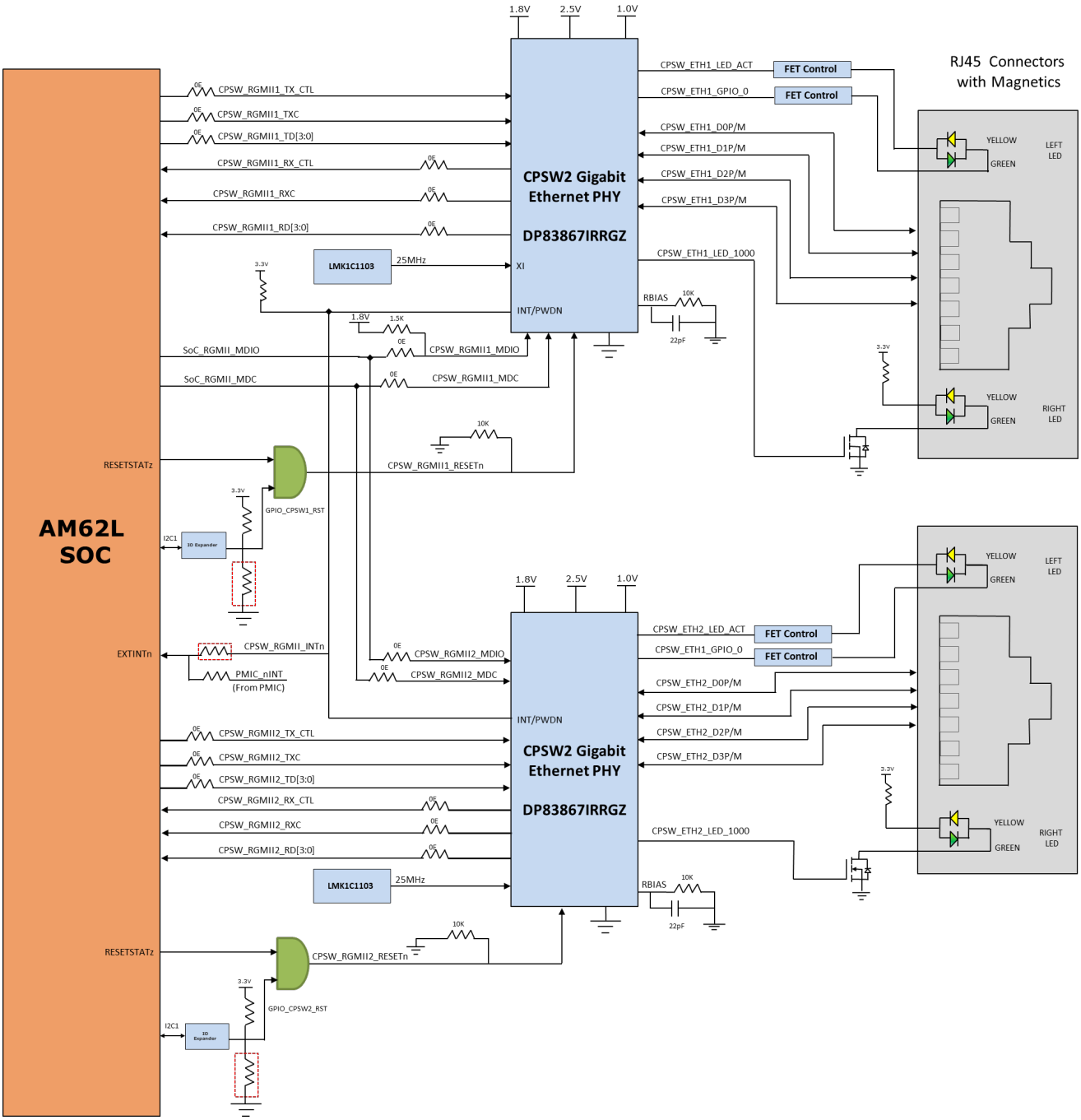

Figure 2-28. Ethernet Interface Block Diagram

2.6.12.1 CPSW Ethernet PHY Strapping

The default configuration of the DP83867 is determined using several resistor pullup and pulldown values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes. The AM62L EVM uses the 48-pin QFN package which supports the RGMII interface.

The DP83867 PHY uses four level configurations based on resistor strapping which generate four distinct voltages ranges. The resistors are connected to the RX data and control pins which are normally driven by the PHY and are inputs to the processor. The voltage range for each mode is shown below:

- Mode 1 - 0V to 0.1764V
- Mode 2 – 0.252V to 0.3438V
- Mode 3 – 0.405V to 0.5112V
- Mode 4 – 1.2492V to 1.5984V

Footprint for both pullup and pulldown is provided on all the strapping pins except LED_0. LED_0 is for Mirror Enable, which is set to Mode 1 by default, Mode 4 is not applicable and Mode 2, Mode 3 option is not desired.

Table 2-25. CPSW Ethernet PHY1 Default Configuration

PHY ADDR	00000
Auto_neg	Enabled
ANG_SEL	10/100/1000
RGMII TXCLK skew:	0ns
RGMII RXCLK skew	2ns

Table 2-26. CPSW Ethernet PHY2 Default Configuration

PHY ADDR	00001
Auto_neg	Enabled
ANG_SEL	10/100/1000
RGMII TXCLK skew:	0ns
RGMII RXCLK skew	2ns

2.6.13 GPIO Port Expander

The I/O Expanders used in the AM62L EVM are 24-Bit I2C based I/O Expander which is used for daughter cards plug-in detection and for generating resets and enable signals to various peripheral devices connected onboard. The SoC_I2C1 bus of the AM62L SoC is used to interface with the I/O Expanders. The I2C device addresses of the I/O Expanders are 0x22 and 0x23.

See Table 2-27 for the list of signals being controlled by the Expander.

Table 2-27. I/O Expander Signal Details

I/O Expander - 01			
Pin no	**Signal**	**Direction**	**Purpose**
P02	UART1_FET_SEL	OUTPUT	UART1 FET selection
P03	MMC1_SD_EN	OUTPUT	SD Card Load Switch Enable
P04	VPP_LDO_EN	OUTPUT	SoC eFuse Voltage (VPP=1.8V) Regulator Enable
P05	EXP_PS_3V3_EN	OUTPUT	EXP CONN 3.3V Power Switch Enable
P06	UART1_FET_BUF_EN	OUTPUT	SoC UART1 Mux Select
P10	DSI_GPIO0	BIDIRECTIONAL	DSI Display GPIO0
P11	DSI_GPIO1	BIDIRECTIONAL	DSI Display GPIO1
P13	BT_UART_WAKE_SOC_3V3	INPUT	BT UART WKUP Signal
P14	USB_TYPEA_OC_INDICATION	INPUT	USB Type A overcurrent indicator
P17	WLAN_ALERTn	INPUT	M.2 Module WLAN Alert Input
P20	HDMI_INTn	INPUT	HDMI Interrupt
P21	TEST_GPIO2	BIDIRECTIONAL	TEST GPIO2 from Test Automation Connector
P22	MCASP0_FET_EN	OUTPUT	MCASP0 Enable and Direction Control
P23	MCASP0_BUF_BT_EN	OUTPUT	
P24	MCASP0_FET_SEL	OUTPUT	

Table 2-27. I/O Expander Signal Details (continued)

I/O Expander - 01			
Pin no	**Signal**	**Direction**	**Purpose**
P25	DSI_EDID	INPUT	DSI to HDMI Card Device ID interrupt
P26	PD_I2C_IRQ	INPUT	Interrupt Request from PD Controller
P27	IO_EXP_TEST_LED	OUTPUT	User Test LED 2
I/O Expander - 02			
Pin no	**Signal**	**Direction**	**Device**
P00	BT_EN_SOC	OUTPUT	M.2 module Bluetooth LDO Enable
P01	VOUT0_FET_SEL0	OUTPUT	VOUT0 FET Switch Selection
P10	WL_LT_EN	OUTPUT	M.2 Interface Level Translator Enable
P11	EXP_PS_5V0_EN	OUTPUT	EXP CONN 5V Power Switch Enable
P20	GPIO_QSPI_NAND_RSTn	OUTPUT	QSPI NAND Flash Reset Control GPIO
P21	GPIO_HDMI_RSTn	OUTPUT	HDMI Transmitter Reset Control GPIO
P22	GPIO_CPSW1_RST	OUTPUT	CPSW Ethernet PHY-1 Reset Control GPIO
P23	GPIO_CPSW2_RST	OUTPUT	CPSW Ethernet PHY-2 Reset Control GPIO
P24	GPIO_BOOTMODE_BUF_ENz	OUTPUT	Bootmode Buffer Enable
P25	GPIO_AUD_RSTn	OUTPUT	Audio Codec Reset Control GPIO
P26	GPIO_eMMC_RSTn	OUTPUT	eMMC Reset control GPIO
P27	SOC_WLAN_SDIO_RST	OUTPUT	M.2 Module WLAN/SDIO Reset

2.6.14 GPIO Mapping

Table 2-28 describes the detailed GPIO mapping of AM62L Low Power SoC with AM62L EVM peripherals.

Table 2-28. Mapping of AM62D Low Power SoC with AM62L Low Power SK EVM peripherals

SL NO.	GPIO Description	GPIO Netname	Functionality	GPIO Used	Package Signal Name	Direction with Respect to Control	Default State	Active State	Voltage Domain on SoC Side	Voltage Rail Connected on SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_51	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV4	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_52	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV4	SoC_DVDD1V8
3	OSPI NOR Reset Control GPIO	GPIO_OSPI_NOR_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDS1	SoC_DVDD1V8
4	OSPI NOR Interrupt	OSPI_NOR_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDS1	SoC_DVDD1V8
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO0_105	EXTINTn	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD3V3
5	IO Expander Interrupt	GPIO0_91_INTn	INTERRUPT	GPIO0_91	SPI0_D1	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD3V3
6	User test LED control signal	SOC_GPIO0_123	ENABLE	GPIO0_123	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV1	SoC_DVDD3V3
7	User Interrupt	GPIO0_90_INTn	INTERRUPT	GPIO0_90	SPI0_D0	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD3V3
8	PMIC Interrupt	PMIC_nINT	INTERRUPT	GPIO0_105	EXTINTn	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD3V3
9	VOUT0 FET switch selection	SoC_VOUT0_FET_SEL1	SELECTION	GPIO0_87	SPI0_CS0	OUTPUT	HIGH	NA	VDDSHV1	SoC_DVDD3V3
10	VOUT0 FET switch selection	SoC_VOUT0_FET_SEL0	SELECTION	GPIO0_89	SPI0_CLK	OUTPUT	HIGH	NA	VDDSHV1	SoC_DVDD3V3
I/O EXPANDER – 01										
1	UART1 FET selection control	UART1_FET_SEL	DIRECTION CONTROL	I/O EXPANDER-P02		OUTPUT	HIGH	NA		VCC_3V3_SYS
2	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	I/O EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
3	SoC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	I/O EXPANDER-P04		OUTPUT	LOW	HIGH		VCC_3V3_SYS
4	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	I/O EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	SoC UART1 Mux Enable	UART1_FET_BUF_EN	ENABLE	I/O EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	DSI Display GPIO0	DSI_GPIO0	GPIO	I/O EXPANDER-P10		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS

Table 2-28. Mapping of AM62D Low Power SoC with AM62L Low Power SK EVM peripherals (continued)

SL NO.	GPIO Description	GPIO Netname	Functionality	GPIO Used	Package Signal Name	Direction with Respect to Control	Default State	Active State	Voltage Domain on SoC Side	Voltage Rail Connected on SKEVM
7	DSI Display GPIO1	DSI_GPIO1	GPIO	I/O EXPANDER-P11		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
8	BT UART WKUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	I/O EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
9	USB Type A overcurrent indicator	USB_TYPEA_OC_INDICATION	INTERRUPT	I/O EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
10	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	I/O EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
11	HDMI Interrupt	HDMI_INTn	INTERRUPT	I/O EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
12	TEST GPIO2	TEST_GPIO2	GPIO	I/O EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
13	MCASP0 Enable and Direction Control	MCASP0_FET_EN	ENABLE	I/O EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
14		MCASP0_BUF_BT_EN	ENABLE	I/O EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
15		MCASP0_FET_SEL	DIRECTION CONTROL	I/O EXPANDER-P24		OUTPUT	HIGH	NA		VCC_3V3_SYS
16	DSI to HDMI Card Device ID interrupt	DSI_EDID	INTERRUPT	I/O EXPANDER-P25		INPUT	HIGH	LOW		VCC_3V3_SYS
17	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	I/O EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
18	User Test LED 2	IO_EXP_TEST_LED	GPIO	I/O EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
I/O EXPANDER – 02										
1	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	I/O EXPANDER-P00		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
2	VOUT0 FET switch selection	VOUT0_FET_SEL0	SELECTION	I/O EXPANDER-P01		OUTPUT	LOW	NA		VCC_3V3_SYS
3	M.2 Interface Level Translator Enable	WL_LT_EN	ENABLE	I/O EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	I/O EXPANDER-P11		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	QSPI NAND Reset Control GPIO	GPIO_QSPI_NAND_RSTn	RESET	I/O EXPANDER-P20		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	I/O EXPANDER-P21		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	I/O EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	I/O EXPANDER-P23		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Bootmode Buffer Enable	GPIO_BOOTMODE_BUF_ENz	ENABLE	I/O EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	I/O EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	I/O EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_SYS
12	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	I/O EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS

2.7 Power

2.7.1 Power Input

Both Type-C Connectors (VBUS and CC lines) are connected to a Dual PD controller manufacturer part number TPS65988. The TPS65988 is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for two USB Type-C Connectors. Upon cable detection, the TPS65988 communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65988 enables the appropriate power path. The two internal power paths of TPS65988 are configured as sink paths for the two Type-C ports and an external FET path is provided for Type-C CONN 2 to source 5V when acting as DFP. The external FET path is controlled by GPIO17/PP_EXT2 of the PD controller along with a resistor option to also enable using USB0 DRVVBUS from the AM62L SoC.

TPS65988 PD controller can provide an output of 3A (12V max) through CC negotiation. The VBUS pins from both the Type-C connectors are connected to the VBUS pins of the PD controller. The output of the PD is VMAIN which is supplied to on board Buck-Boost and Buck regulators to generate fixed 5V and 3.3V supply for the EVM.

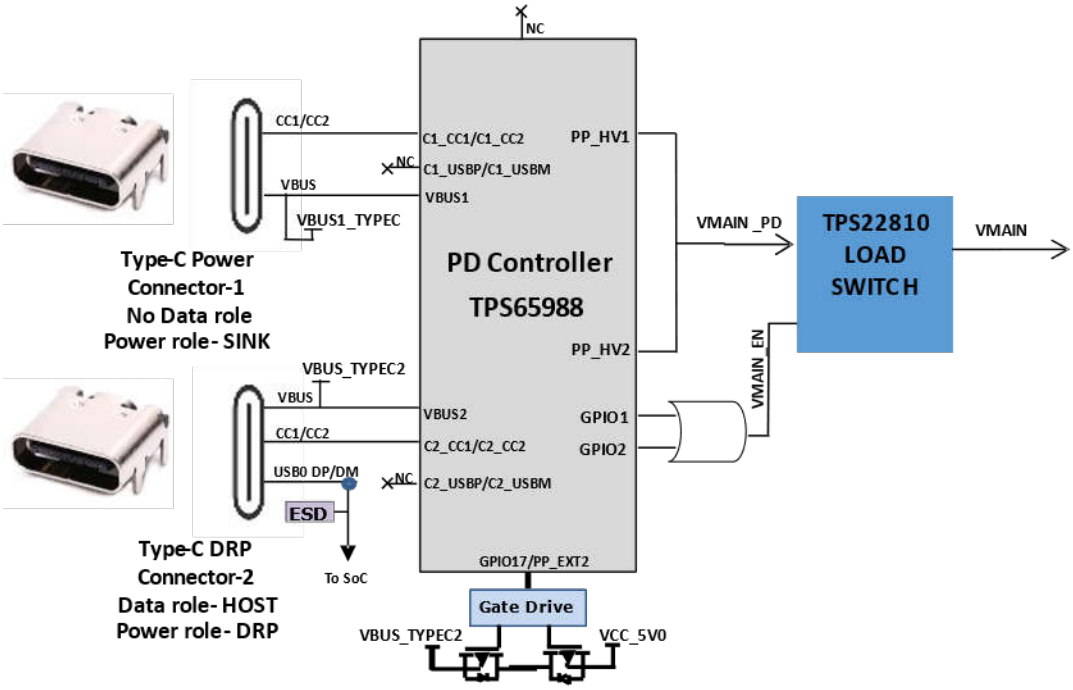

Figure 2-29. Power Input Block Diagram

2.7.2 Power Supply

The AM62L EVM utilizes an array of DC-DC converters to supply the various memories, clocks, SoC and other components on the board with the necessary voltage and the power required.

Figure 2-30 shows the various discrete regulators, PMIC and LDOs used to source power rails for each peripheral on the AM62L EVM board.

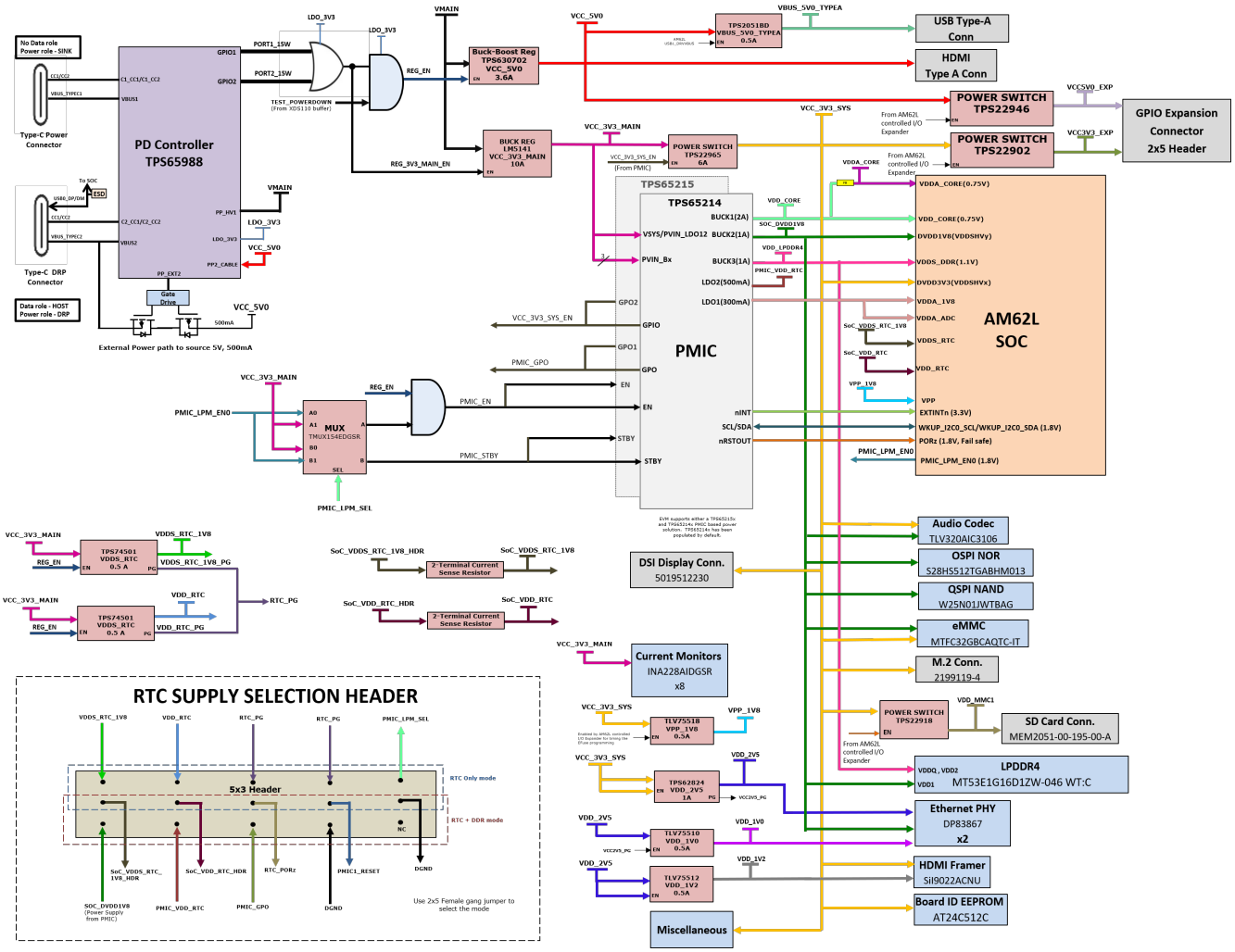

Figure 2-30. Power Architecture

The following sections describe the power distribution network topology that supplies the EVM board, supporting components and reference voltages.

Note

Refer to the AM62L Power Implementation application note (AM62L Power Supply Implementation) for more information on the connections required to support low power mode.

The AM62L EVM board includes a power solution based on discrete power supply components. The initial stage of the power supply will be VBUS voltage from either of the two USB Type-C connectors J17 and J19. USB Type-C Dual PD controller of manufacturer part number TPS65988DHRSHR is used for negotiation of the required power to the system. The net names provided to GPIO1 and GPIO2 of the PD controller are PORT1_15W_EN and PORT2_15W_EN respectively and these pins are used for negotiation if the power is ≥ 15W. This logic enables the generation of 5V and 3.3V supplies. The logic is shown in Figure 2-31.

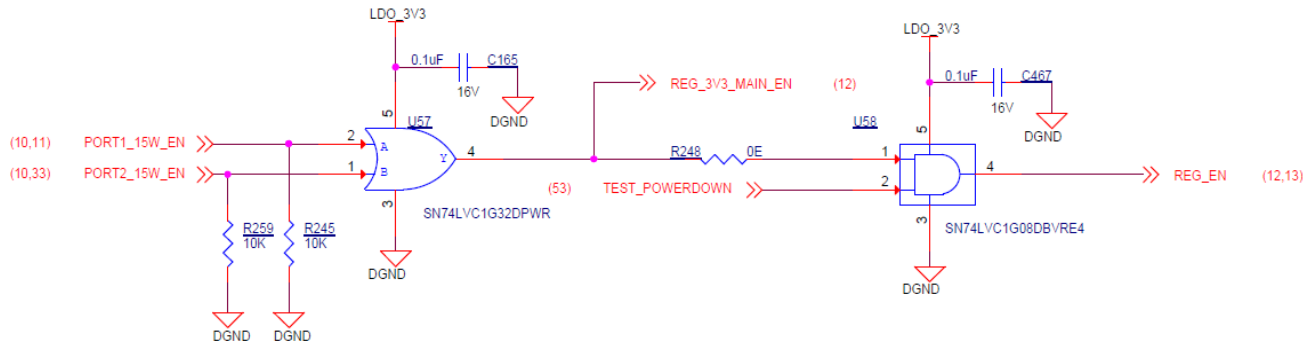

Figure 2-31. Generation of 5V and 3.3V Sipplies Enabling Logic

REG_3V3_MAIN_EN signal enables generation of 3.3V power supply and REG_EN signal enables 5V power supply generation. Buck-Boost controller TPS630702RNMR and Buck converter LM5141RGET are used for the generation of 5V and 3.3V respectively and the input to the regulators is the PD output. These 3.3V and 5V are the primary voltages for the AM62L EVM Board power resources. The 3.3V supply generated from the Buck regulator LM5141RGET is the input supply to the PMIC, various SoC regulators and LDOs. The 5V supply generated from the Buck Boost regulator TPS630702RNMR is used for powering the on-board peripherals.

Discrete regulators and LDOs used on Board are:

- TPS62824DMQR - To generate VDD_2V5 rail for Ethernet PHYs
- TLV75510PDQNR - To generate VDD_1V0 for Ethernet PHYs
- TLV75512PDQNR - To generate VDD_1V2 for HDMI Framer
- PTPS6521401VAFR (PMIC - 2) - To generate various SoC and Peripheral supplies
- TPS74501PDRVR LDO - To generate VDDS_RTC_1V8
- TPS74501PDRVR LDO - To generate VDD_RTC
- TPS79601DRBR LDO - XDS110 On board emulator
- TPS73533DRVR LDO - FT4232 UART to USB Bridge
- TLV75518PDBVR LDO - VPP e-Fuse programming of SoC

2.7.3 Power Sequencing

Figure 2-32 shows the Power Up and Power Down sequence of the AM62L SoC power supplies

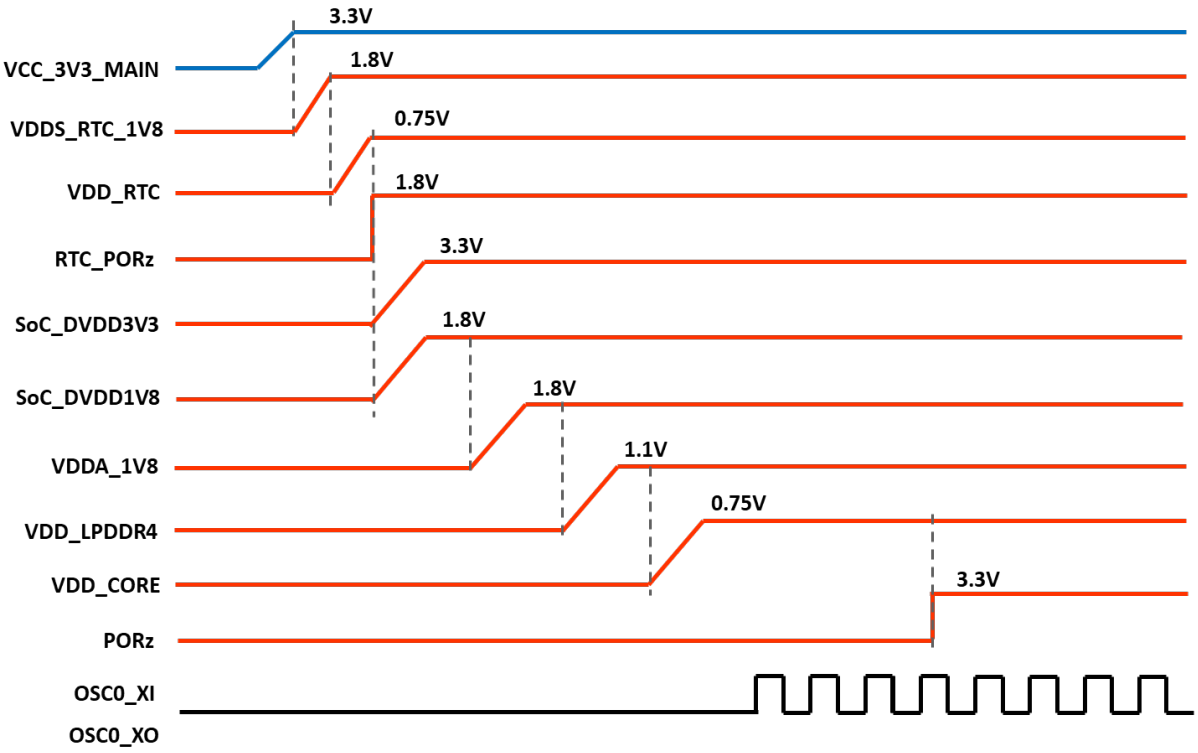

Figure 2-32. Power Sequence

2.7.4 AM62L SoC Power

The Core voltage of the AM62L SoC can be 0.75V. Current monitors are provided on all of the SoC Power rails.

The SoC has different I/O groups. Each I/O group is powered by specific power supplies as listed in Table 2-29.

Table 2-29. SoC Power Supply

Sl.No	Power Supply	SoC Supply Rails	I/O Power Group	Voltage
1	VDD_CORE	VDDA_CORE	CORE	0.75
		VDDA_DDR_PLL0		
2	VDDA_CORE	VDDA_CORE_USB	USB	0.75
		VDDA_CORE_DSI	DSI	
		VDDA_CORE_DSI_CLK		
3	SoC_VDD_RTC	VDD_RTC	RTC	0.75
4	SoC_VDDS_RTC_1V8	VDDS_RTC	RTC	1.8
5	VDDA_1V8	VDDA_1P8_DSI	DSI	1.8
		VDDA_ADC	ADC0	
		VDDS_OSC0	OSC0	
		VDDA_PLL[0:1]		
		VDDA_1P8_USB	USB	
6	VDD_LPDDR4	VDDS_DDR	DDR0	1.1
7	VPP_1V8	VPP_1V8		1.8
8	VDDSHV_SD_IO	VDDSHV3	MMC1	3.3/ 1.8

Table 2-29. SoC Power Supply (continued)

Sl.No	Power Supply	SoC Supply Rails	I/O Power Group	Voltage
9	SOC_DVDD1V8	VDDSHV2	MMC0	1.8
		VDDS_WKUP	WKUP	
		VDDSHV4	MMC2	
		VDDS0	GENERAL0	
		VDDS1	GENERAL0_1	
10	SOC_DVDD3V3	VDDSHV0	GPMC	3.3
		VDDSHV1	GENERAL1	
		VDDA_3P3_USB	USB	
11	VDD_MMC1_SD	VDDA_3P3_SDIO		3.3

2.7.5 Current Monitoring

INA228 power monitor devices are used to monitor current and voltage of various power rails of AM62L SoC. The INA228 interfaces to the AM62L SoC through I2C interface SoC_I2C1_SDA_INA and SoC_I2C1_SCL_INA (which are the level shifted versions of SoC_I2C1_SCL and SoC_I2C1_SDA respectively). TCA9517DR is a I2C level shifter that is used to level shift SoC_I2C1 from VCC_3V3_SYS to VCC_3V3_MAIN. Four terminal, high precision shunt resistors are provided to measure load current of all the supplies except for SoC_VDDS_RTC_1V8 and SoC_VDD_RTC supplies, that has been provided with two terminal wide body shunt resistors.

Note

The design supports current/voltage measurements using either INA228 or INA231. INA228 is only populated on the EVM (Implemented via stacked PCB footprint).

Table 2-30. INA I2C Device Address

Source	Supply Net	Device Address	Value of the Shunt Connected to the Supply Rail
VCC_CORE	VDD_CORE	0x40	20mΩ± 1%
VCC_3V3_SYS	SoC_DVDD3V3	0x4C	100mΩ± 0.5%
VCC1V8_SYS	SoC_DVDD1V8	0x45	100mΩ± 0.5%
VDDA1V8	VDDA_1V8	0x4D	100mΩ± 0.5%
VCC1V1_PMIC1 (from PMIC 1)	VDD_LPDDR4 (from PMIC 1)	0x47	40mΩ± 1%
VCC1V1_PMIC2 (from PMIC 2)	VDD_LPDDR4 (from PMIC 2)	0x49	40mΩ± 1%
SoC_VDD_RTC_HDR	SoC_VDD_RTC	0x44	1Ω± 0.5%
SoC_VDDS_RTC_1V8_HDR	SoC_VDDS_RTC_1V8	0x46	1Ω± 0.5%

2.8 Clocking

The Clock architecture of the AM62L EVM is shown in Figure 2-33.

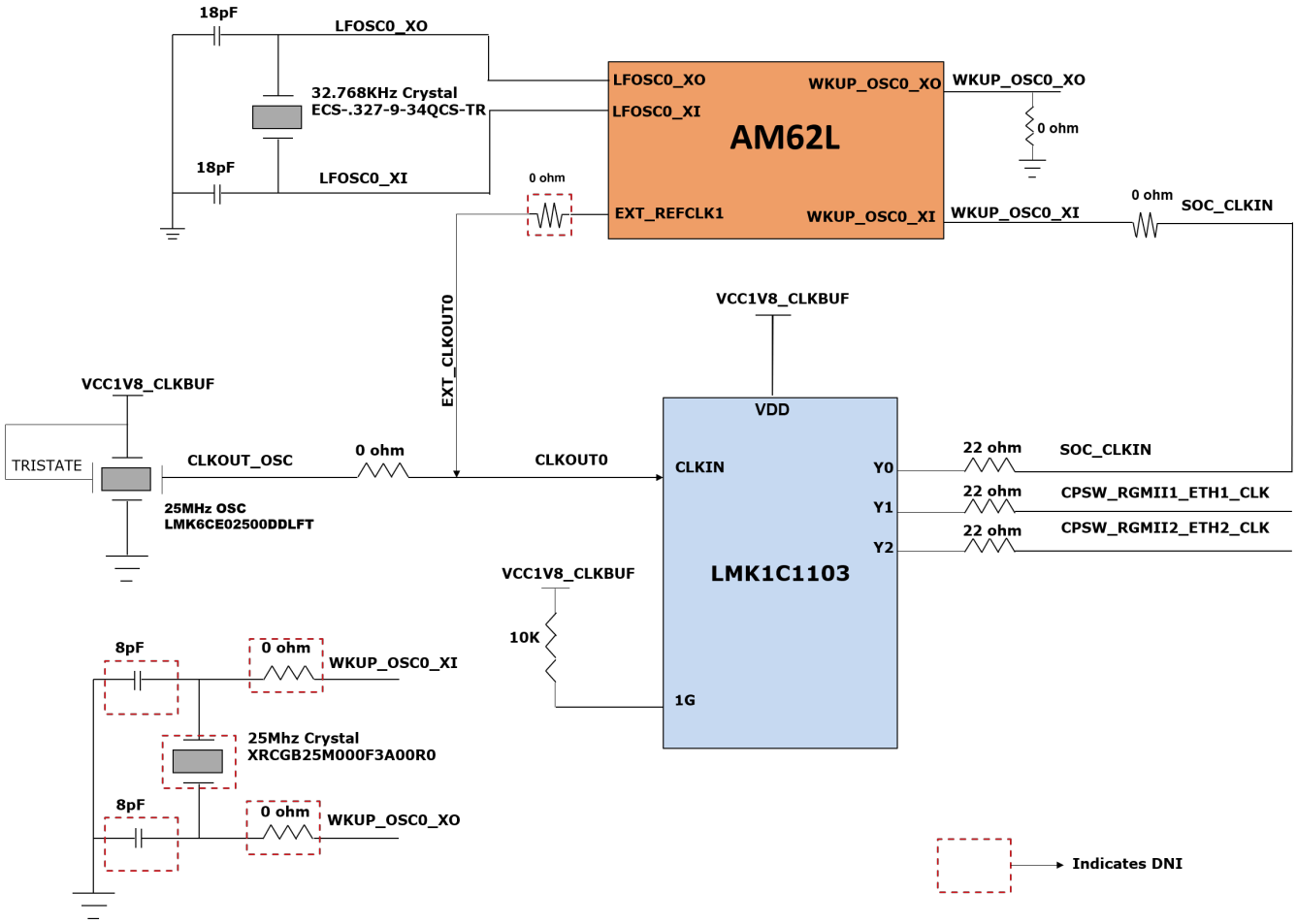

Figure 2-33. Clock Architecture

A clock buffer of part number LMK1C1103PWR is used to drive the 25MHz clock to the SoC and the two Ethernet PHYs. LMK1C1103PWR is a 1:3 LVCMOS clock buffer, which takes the 25MHz crystal/LVCMOS reference input and provides three 25MHz LVCMOS clock outputs. The source for the clock buffer shall be either the CLKOUT0 pin from the SoC or a 25MHz oscillator, the selection of which is made using a set of resistors. By default, an oscillator is used as an input to the clock buffer on the AM62L EVM. Outputs Y1 and Y2 of the clock buffer are used as reference clock inputs for the two Gigabit Ethernet PHYs.

There is one external crystal (32.768KHz) attached to the AM62L SoC to provide clock to the RTC domain.

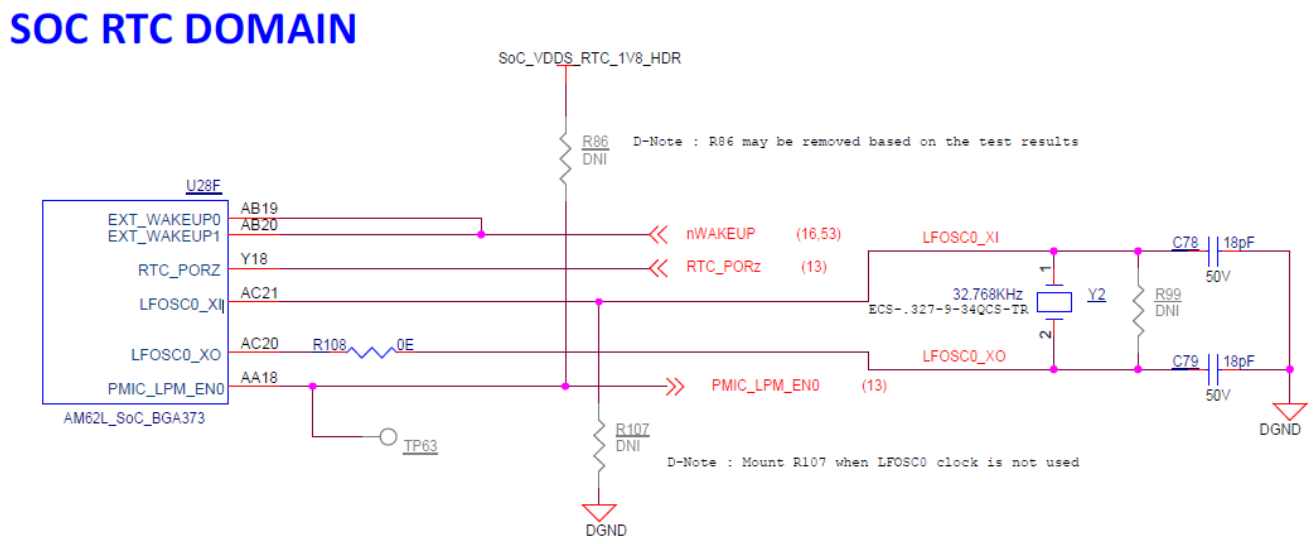

Figure 2-34. SoC RTC Domain Clock

2.8.1 Peripheral Ref Clock

Clock inputs required for peripherals such as XDS110, FT4232, M.2 Interface, HDMI Framer and Audio Codec are generated locally using separate crystals or oscillators. Crystals or Oscillators used to provide the reference clocks to the EVM peripherals are shown in Table 2-31.

Table 2-31. Clock Table

Peripheral	Manufacturer Part Number	Description	Frequency
XDS110 emulator (Y4)	XRCGB16M000FXN01R0	CRY 16.000MHz 8pF SMD	16.000MHz
FT4232 Bridge (Y1)	445I23D12M00000	CRY12.000MHz 18pF SMD	12.000MHz
M.2 Interface (U66)	ECS-327MVATX-2-CN-TR	OSC 32.768KHz CMOS SMD	32.768KHz
Audio Codec (U59)	LMK6CE012288CDLFT	OSC12.288MHz CMOS SMD	12.288MHz
HDMI Framer (U27)	LMK6CE012288CDLFT	OSC12.288MHz CMOS SMD	12.288MHz

The clock required by the HDMI Transmitter can be provided by either on-board oscillator or the SoC's AUDIO_EXT_REFCLK1, which can be selected through a resistor mux. The 32.768KHz clock to the M.2 module is provided by default from WKUP_CLKOUT0 ball of AM62L SoC.

2.9 Reset

The Reset Architecture of the AM62L EVM is shown in Figure 2-35. The SoC has the following resets:

- RESETSTATz is the MAIN domain warm reset status output
- RESETz is the MAIN domain warm reset input
- PORz is the MAIN domain power ON/ Cold Reset input
- RTC_PORz is the RTC domain power ON/ Cold Reset input

Upon Power on Reset, all peripheral devices connected to the MAIN domain get reset by RESETSTATz.

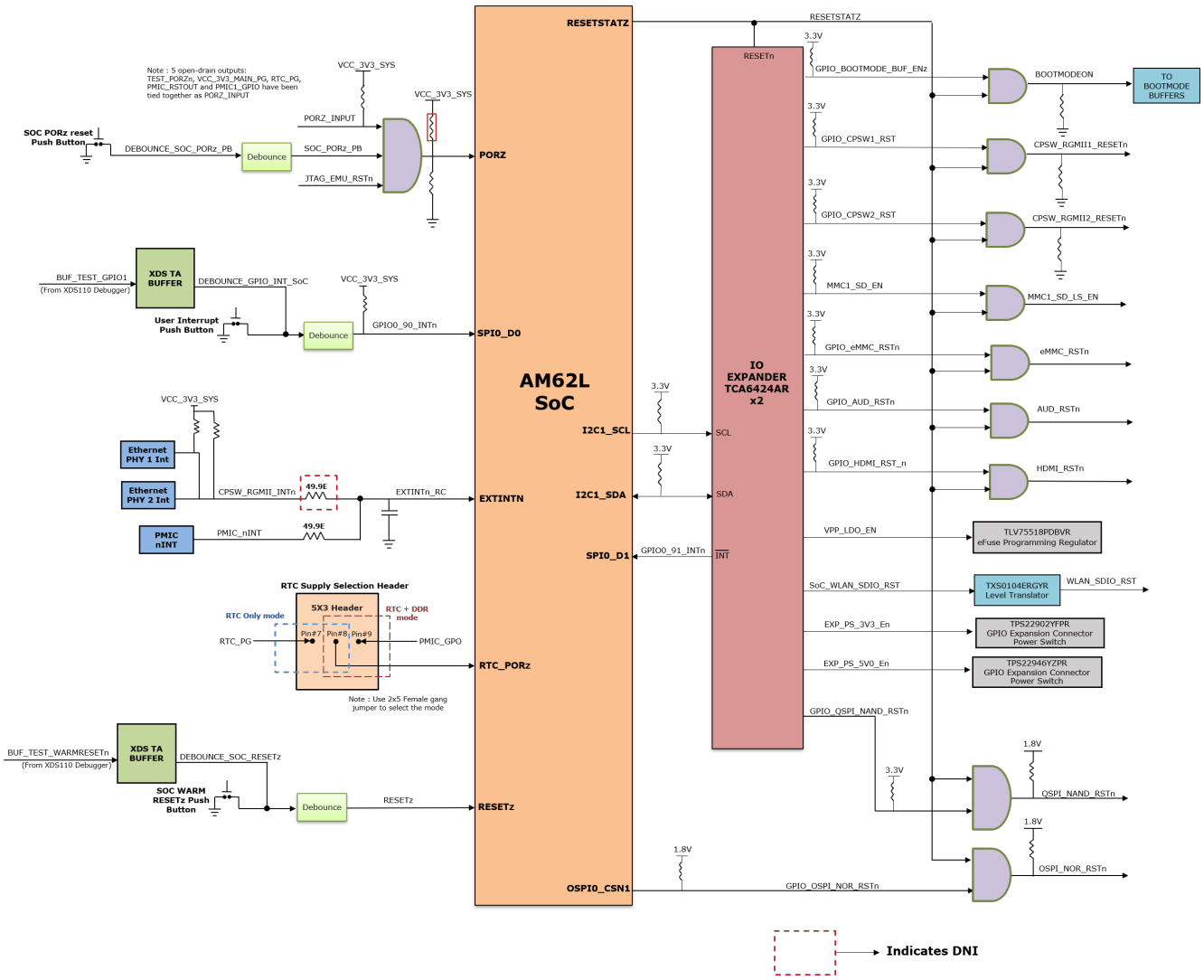

Figure 2-35. Reset Block Diagram

2.10 Expansion Headers

AM62L EVM features two GPIO expansion Headers.

2.10.1 GPIO Expansion Headers

The AM62L EVM supports GPIO expansion interface using 10-pin and 30-pin GPIO expansion connectors manufacturer part number 67997-410HLF and manufacturer part number PREC015DAAN-RC respectively.

The Following interfaces and I/Os are included on to the 10-pin and 30-pin GPIO expansion connectors:

- 2x SPI: SPI1 with 1 CS and SPI3 with 1 CS
- 1x I2C: I2C3
- 1x UART: UART4
- 13x GPI0: GPIOs from MAIN domain
- 5V and 3.3V supply (current limited to 155mA and 500mA)

Each of the power supplies 5V and 3.3V are current limited to 155mA and 500mA respectively. This is achieved by using two individual load switch TPS22902YFPR and TPS22946YZPR. Enable for the load switches are controllable by an I2C based GPIO Port expander and J26, J25 jumpers. By shorting J26, J25 jumpers can enable 5V and 3.3V supplies manually.

Signals routed from 2x5 (10 pins) GPIO Expansion connector (J3) are listed in Table 2-32.

The GPIO Expansion signals are shared with HDMI interface, By default the signals are routed to HDMI interface and the signal routing can be controlled through SoC_VOUT0_FET_SEL0, SoC_VOUT0_FET_SEL1 by software and shorting J29 jumper.

Table 2-32. 10 Pin GPIO Expansion Connector (J3)

Pin No.	SoC Ball	Net name
1	-	VCC3V3_EXP
2	-	VCC5V0_EXP
3	-	VCC3V3_EXP
4	-	VCC5V0_EXP
5	-	VCC3V3_EXP
6	-	DGND
7	F22	GPIO0_29_EXP
8	H18	GPIO0_26_EXP
9	H20	GPIO0_24_EXP
10	H19	GPIO0_23_EXP

Signals routed from 2x15 (30 pins) GPIO Expansion connector (J2) are listed in Table 2-33.

Table 2-33. 30 Pin GPIO Expansion Connector (J2)

No.	SoC Ball	Net name
1	M19	GPIO0_34_EXP
2	N19	GPIO0_32_EXP
3	-	DGND
4	N20	GPIO0_33_EXP
5	L21	GPIO0_31_EXP
6	L20	GPIO0_41_EXP
7	M21	GPIO0_40_EXP
8	-	DGND
9	N21	GPIO0_39_EXP
10	F23	GPIO0_30_EXP
11	-	DGND
12	N23	SPI3_D0_EXP
13	H21	GPIO0_25_EXP
14	P22	SPI3_CLK_EXP
15	N22	SPI3_D1_EXP
16	-	DGND
17	-	DGND
18	G22	UART4_TXD_EXP
19	P23	SPI3_CS0_EXP
20	G23	UART4_RXD_EXP
21	J22	UART4_CTSn_EXP
22	-	DGND
23	H23	UART4_RTSn_EXP
24	L22	I2C3_SCL_EXP
25	-	DGND
26	L23	I2C3_SDA_EXP
27	H22	SPI1_CLK_EXP
28	K22	SPI1_D0_EXP
29	J23	SPI1_D1_EXP

Table 2-33. 30 Pin GPIO Expansion Connector (J2) (continued)

No.	SoC Ball	Net name
30	K23	SPI1_CS0_EXP

2.11 Interrupt

The AM62L EVM supports two push buttons for providing reset input and a user generated interrupt to the AM62L SoC. These push buttons placed on the Top side of the Board and are listed in Table 2-34.

Table 2-34. EVM Push Buttons

Sl #	Push Buttons	Signal	Function
1	SW7	RESETZ	MAIN domain Warm Reset input
2	SW5	GPIO0_90_INTn	Generates interrupt on GPIO0_90 (SPI0_D0)

2.12 I2C Address Mapping

There are four AM62L I2C instances communicating with the various peripherals in the EVM board:

- SoC_I2C0 Interface: SoC I2C[0] is connected to Board ID EEPROM and DSI display connector.
- SOC I2C1 Interface: SoC I2C[1] is connected to Current Monitors (x8), Temperature Sensors (x2), Audio Codec, HDMI Transmitter & GPIO Port Expander (x2).
- SOC I2C2 Interface: SoC I2C[2] is connected to PD controller.
- WKUP I2C0 Interface: WKUP I2C[0] is connected to the PMIC.

Figure 2-36 depicts the I2C tree, and Table 2-35 provides the complete I2C address mapping details present on the AM62L EVM.

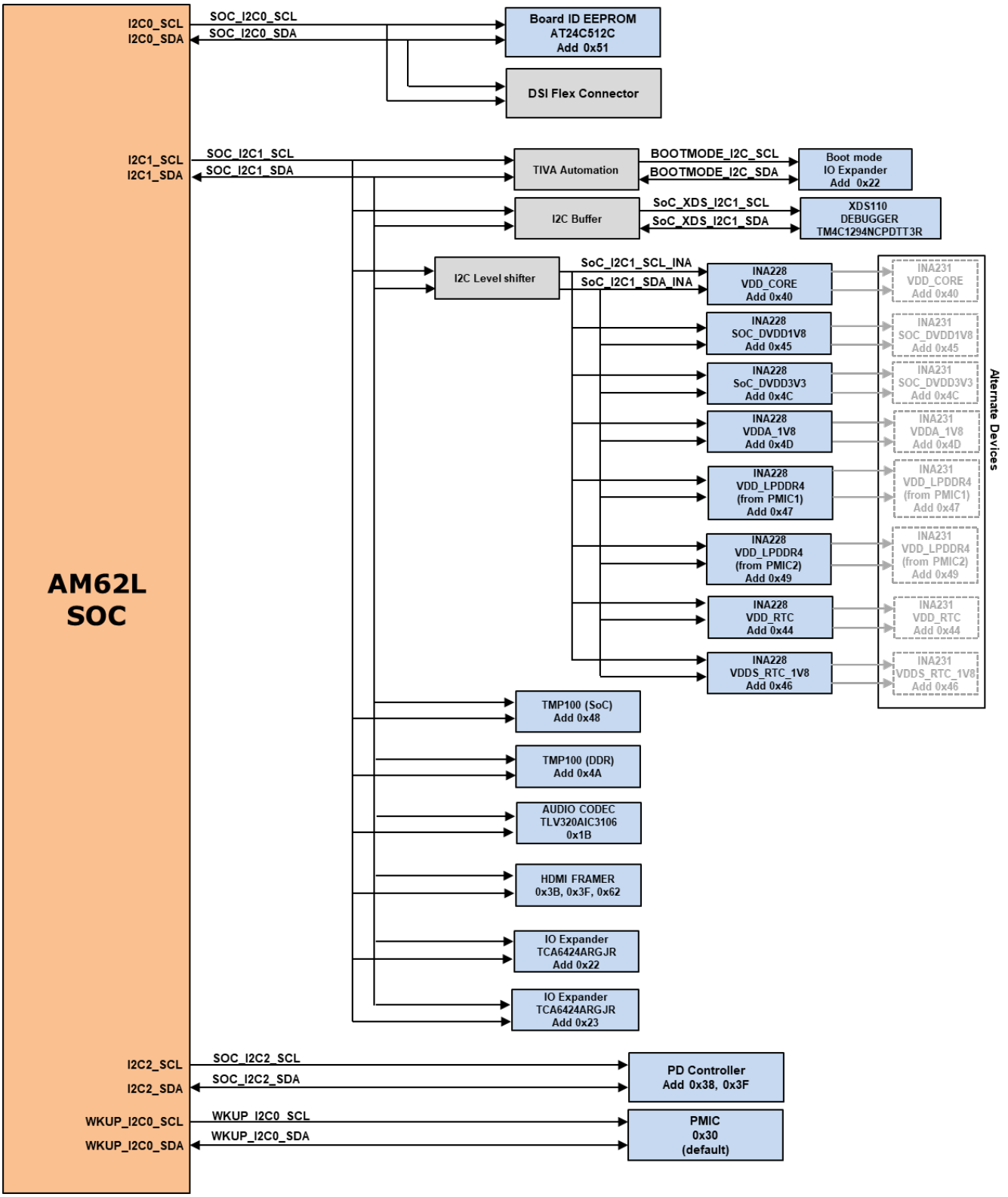

Figure 2-36. I2C Interface Tree

Table 2-35. I2C Mapping Table

I2C Port	Device/Function	Part Number	I2C Address
SoC_I2C0	Board ID EEPROM	AT24C512C-MAHM-T	0x51
	DSI Display Connector	<connector interface>	
SoC_I2C1	GPIO Port Expander	TCA6424ARGJR	0x22, 0x23
	Current Monitors	INA228AIDGSR	0x40, 0x4C, 0x45, 0x4D, 0x47, 0x49, 0x44 & 0x46
	Temperature Sensors	TMP100NA/3K	0x48, 0x4A
	Audio Codec	TLV320AIC3106IRGZT	0x1B
	HDMI Transmitter	SiI9022ACNU	0x3B, 0x3F, 0x62
SoC_I2C2	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
WKUP_I2C0	PMIC	PTPS6521401VAFR	0x30
Others			
BOOTMODE_I2C	I2C Bootmode Buffer	TCA6424ARGJR	0x22

3 Hardware Design Files

3.1 Schematics

To download schematics, see the Design Files page.

3.2 PCB Layouts

To download the PCB guidelines and example layout, see the Design Files page.

3.3 Bill of Materials (BOM)

To download the bill of materials (BOM), see the Design Files page.

4 Compliance Information

4.1 Compliance and Certifications

EMC, EMI and ESD Compliance

Components installed on the product are sensitive to Electric Static Discharge (ESD). TI recommends this product be used in an ESD controlled environment. This can include a temperature or a humidity controlled environment to limit the buildup of ESD. TI also recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

5 Additional Information

5.1 Known Hardware or Software Issues

This section describes the currently known issues on each EVM revision and applicable workarounds. Issues that have been patched have modification labels attached to the EVM assembly.

Issue Number	Issue Title	Issue Description	Variants Affected
Issue 1	External Power Path for Sourcing 5V/0.5A	An undesired leakage was observed on the VCC_5V0 rail	E1
Issue 2	Temperature Sensor - LPDDR4	Address conflict on I2C bus with U22 and U128	E1
Issue 3	Bootmode IO Expander	Bootmode IO expander power is going off while BUF_TEST_POWERDOWN assert low	E1
Issue 4	Current Monitor Access in RTC Mode	On RTC Only mode, XDS110 Test automation is not able to access current monitors	E1, E1-1

5.1.1 Issue 1 - External Power Path for Sourcing 5V/0.5A

Applicable EVM Revisions: E1

Issue Description: When the USB Type-C DRP port is connected to power, an undesired leakage occurs on the VCC_5V0 rail and causes the voltage to rise above the expected level.

Workaround: To mitigate the issue, the values of passive components can be adjusted to modify the gate-source voltage (Vgs) of the PMOS and thereby reduce leakage on the VCC_5V0 side.

5.1.2 Issue 2 - Temperature Sensor - LPDDR4

Applicable EVM Revisions: E1

Issue Description: There is an address conflict on I2C bus with U22 and U128.

Workaround: Mount the R124 resistor with 10K value.

5.1.3 Issue 3 - Bootmode IO Expander

Applicable EVM Revisions: E1

Issue Description: The Bootmode IO expander power is turned off while BUF_TEST_POWERDOWN assert low.

Workaround: Remove the VCC_3V3_MAIN enable signal from TEST_POWERDOWN logic such that VCC_3V3_MAIN remains on while BUF_TEST_POWERDOWN assert low.

5.1.4 Issue 4 - Current Monitor Access in RTC Mode

Applicable EVM Revisions: E1, E1-1

Issue Description: Due to incorrect power supply connection on current monitors, XDS110 Test automation is not able to access current monitors during RTC only mode.

Workaround: Change the power supply connection for the INA228 current monitors to VCC_3V3_MAIN.

5.2 Trademarks

6 Related Documentation

1. Texas Instruments: TMDS62LEVM Design File Package
2. Texas Instruments: *AM62L Power Supply Implementation*

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2025) to Revision B (October 2025)	Page
• Added HDMI trademark information	1
• Added PROC181E1-1a to EVM PCB Design Revisions, and Assembly Variants	6

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3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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Last updated 10/2025