User's Guide

TMDS64DC01EVM and TMDS243DC01EVM User's Guide

Table of Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The TMDS64DC01EVM (AM64x EVM IO-Link and High Speed Expansion Board) and TMDS243DC01EVM (AM243x EVM High Speed Expansion Board) are add-on modules for the AM64x and AM243x EVMs. These boards include two sections: namely an IO-Link section supporting eight (8) IO-Link ports and a general purpose signal breakout section.

The AM64x version of this board enables both the IO-Link and general purpose breakout sections, while the AM243x version of this board only supports the general purpose breakout functionality.

Table 1-1. TMDS64DC01EVM and TMDS243DC01EVM Feature Comparison

Feature	TMDS64DC01EVM	TMDS243DC01EVM
IO-Link section	Yes	No (not populated)
General purpose signal breakout section	Yes	Yes

The general purpose breakout section provides test points to all IO signals included on the High Speed Expansion (HSE) connector from AM64x and AM243x EVM.

The IO-Link section enables development of PLC and Remote I/O IO-Link master applications by providing eight M12 IO-Link connectors to help build a universal and scalable IO-Link master. IO-Link (International Electrotechnical Commission [IEC] 61131-9) is an open standards protocol that addresses the need for intelligent control of small devices such as sensors and actuators. This standard provides low-speed point-to-point serial communication between a device and a master that normally serves as a gateway to a fieldbus and PLC. The intelligent link established enables ease of communication for data exchange, configuration, and diagnostics.

An unshielded three-wire cable as long as 20 meters, normally equipped with M12 connectors, establishes an IO-Link connection. Data rates range up to 230 kbps with a nonsynchronous minimum cycle time of 400 µs, +10%. Four operating modes support bidirectional input/output (I/O), digital input, digital output and deactivation. Security mechanisms and deterministic data delivery are not specified. A profile known as the IO Device Description (IODD) contains communication properties; device parameters; identification, process and diagnostic data; and information specifically about the device and manufacturer.

The many advantages of an IO-Link system include standardized wiring, increased data availability, remote monitoring and configuration, simple replacement of devices and advanced diagnostics. IO-Link permits factory managers to receive sensor updates and plan for upcoming maintenance or replacement. Swapping out a sensing or actuation unit that needs replacement and configuring a new one from the PLC through the IO-Link master eliminates manual setup and reduces downtime. Switching production remotely from one configuration to another without visiting the factory floor facilitates easier product customization. Factories can upgrade production lines readily to IO-Link, since it is backwards-compatible with existing standard I/O installations and cabling. Altogether, these capabilities result in reduced overall costs, more efficient processes, and greater machine availability.

2 Revisions and Assembly Variants

The various TMDS64DC01EVM and TMDS243DC01EVM PCB design revisions and assembly variants are listed in the table below. Specific PCB revision is indicated in silkscreen on the PCB. Specific assembly variant is indicated with additional sticker label.

Table 2-1. TMDS64DC01EVM and TMDS243DC01EVM PCB Design Revisions and Assembly Variants

PCB Revision	Assembly Variant	Revision and Assembly Variant Description
PROC102E1	0011	First prototype, early release version of the AM64x EVM IO-Link and High Speed Expansion Board. Implements both the breakout and IO-Link sections of the board.
PROC102E1	002	First prototype, early release version of the AM243x EVM High Speed Expansion Board. Implements only the breakout section of the board.
PROC102A	0011	First production release of the AM64x EVM IO-Link and High Speed Expansion Board. Implements both the breakout and IO-Link sections of the board.
PROC102A	002	First production release of the AM243x EVM High Speed Expansion Board. Implements only the breakout section of the board.

1. The TMDS64D01EVM E1 boards do not have a sticker indicating the '001' assembly variant.

3 System Description

This IO-Link board/Breakout board has a 150-pin HSE connector and 20-pin ADC connector to mate with AM64x and AM243x evaluation board. Additionally, the AM64x version of this board has eight M12 connectors to execute IO-Link functionality.

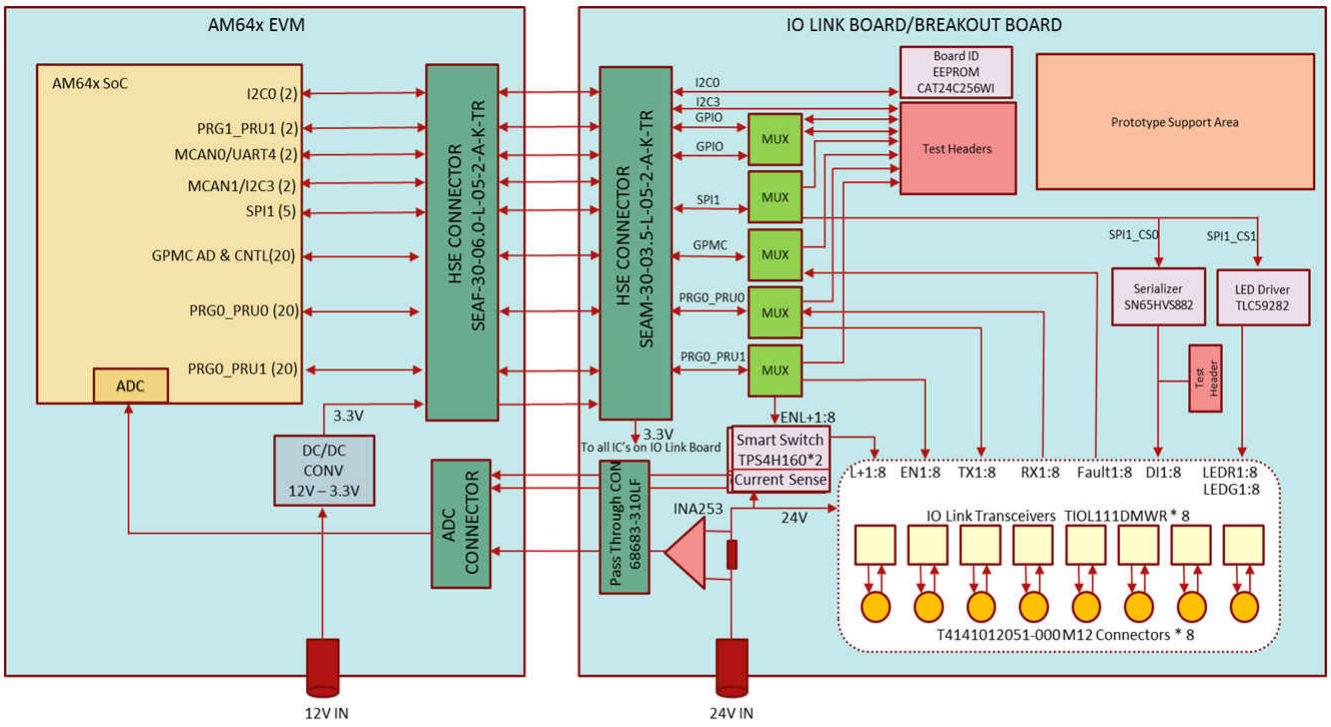

Figure 3-1. TMDS64DC01EVM System Architecture

3.1 Key Features

Table 3-1. TMDS64DC01EVM and TMDS243DC01EVM Key Features

Feature	TMDS64DC01EVM	TMDS243DC01EVM
Eight M12 IO-Link ports with fault protection	Yes	No (not populated)
Sixteen individually addressable LEDs	Yes	No (not populated)
Access to all signals on the EVM's HSE connector on standard 0.1" header pins	Yes	Yes
Signal routing of HSE connector signals between Test Headers and IO-Link section via user configurable FET switches	Yes	Yes
Large prototyping area with 0.1" pitch holes	Yes	Yes
Precision current monitoring with onboard INA253	Yes	No (not populated)

3.2 Functional Block Diagram

Figure 3-2 shows the functional block diagram of the IO-Link Breakout Board.

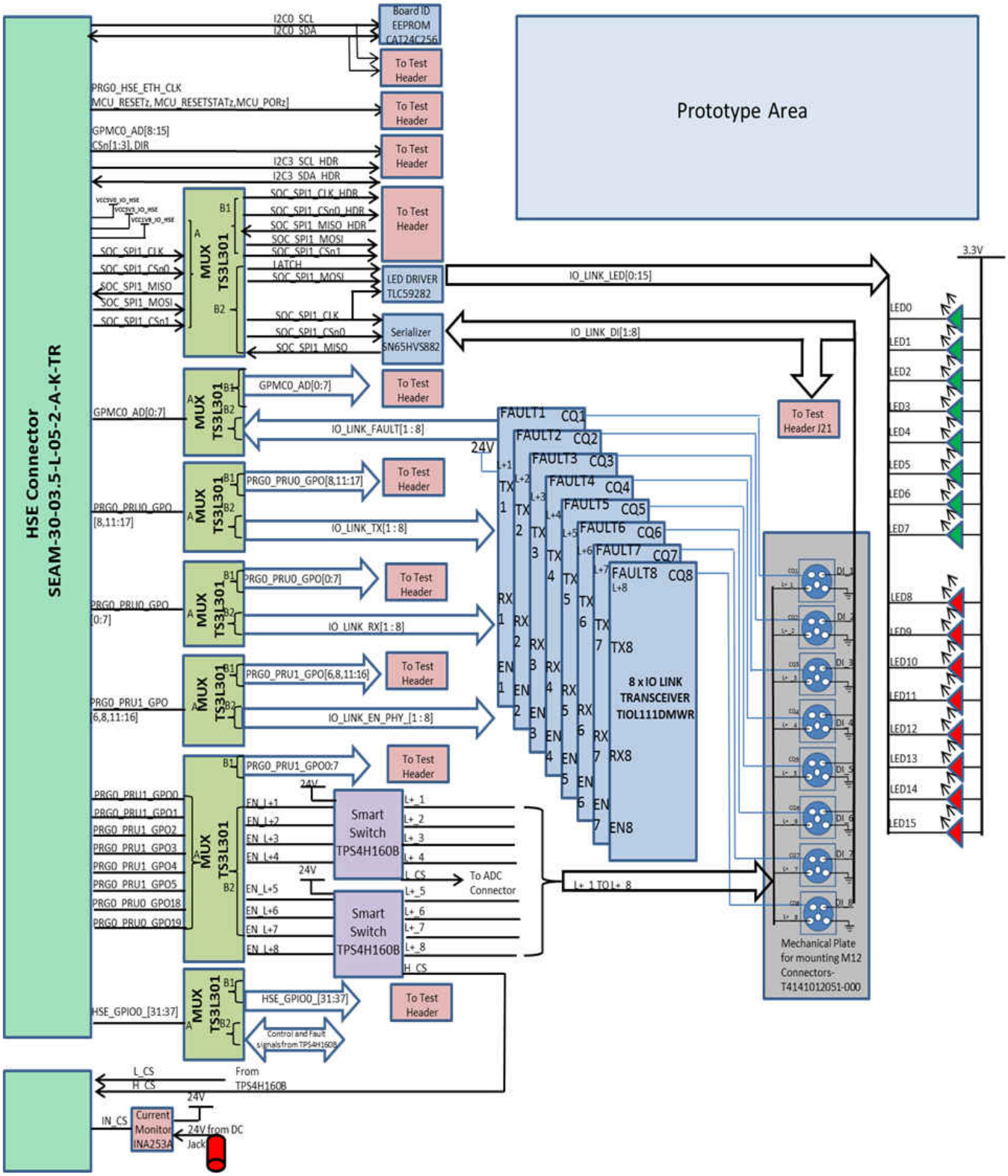

Figure 3-2. TMDS64DC01EVM Functional Block Diagram

3.3 Interfaces and Major Component Description

The following sections provide an overview of the different interfaces and circuits on the TMDS64DC01EVM and TMDS243DC01EVM.

3.3.1 Breakout Board Section

The general purpose Breakout board connects each pin of the High Speed Expansion (HSE) connector to eight, 2x10 test headers with 0.1” spacing between each pin. Additionally, the board features a circuit prototype area with standard 0.1” hole spacing.

Signals from the HSE connector are connected to the Breakout board or IO-Link section using FET switches. The FET switches are controlled using the J11 Header. Connecting the control signal of all the MUXes to ground routes all signals from the HSE connector to the Breakout board, whereas connecting the control signal to VCC3V3_IO_HSE routes all signals from the Mux to the IO-Link section.

Table 3-2. Functionality Selected by J11 Header

J11 Header Selection	Functionality	Supported Board
Short J11 pins 1 and 2	Selects IO-Link section	TMDS64DC01EVM only
Short J11 pins 2 and 3	Selects Breakout board section	TMDS64DC01EVM and TMDS243DC01EVM

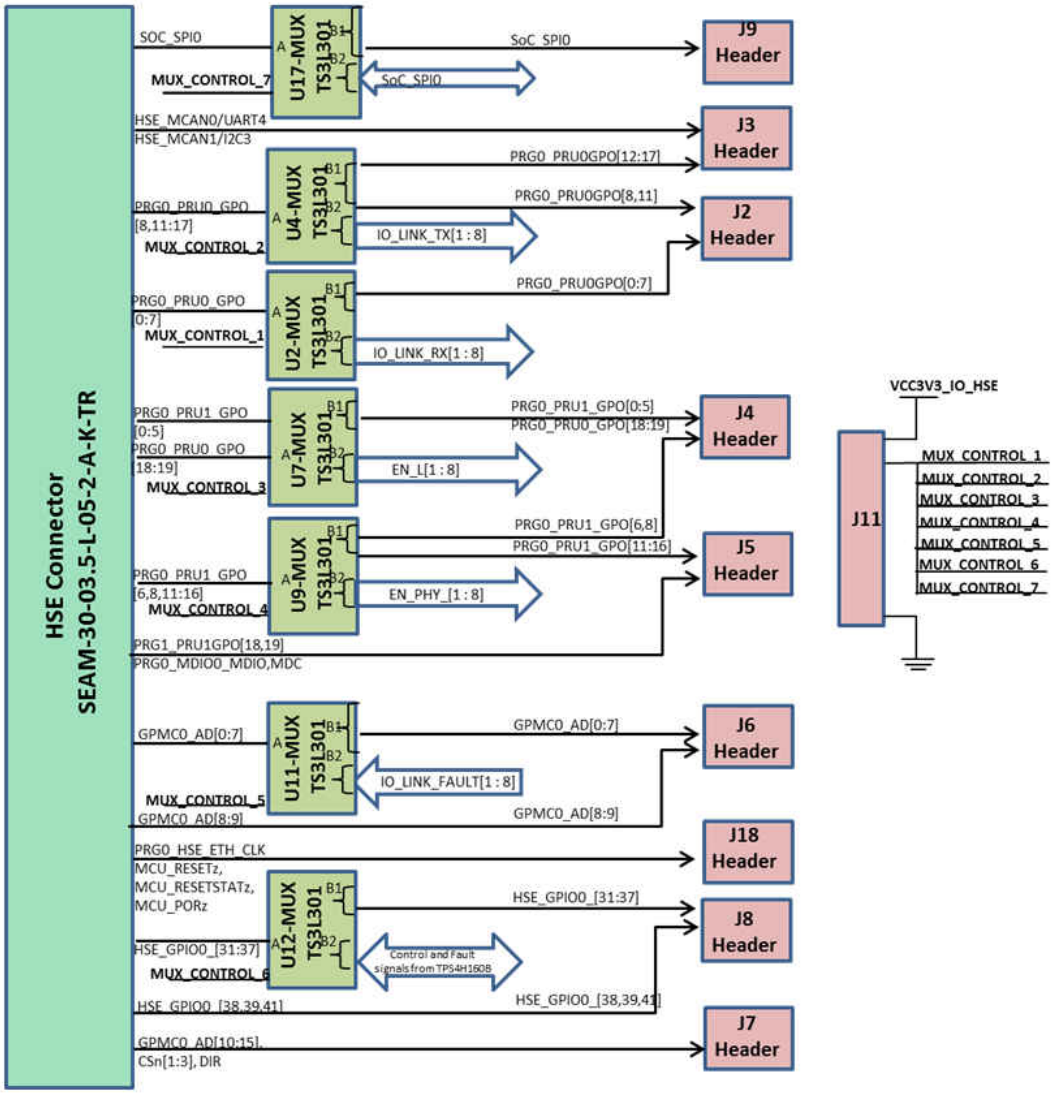

Figure 3-3. Breakout Sectional Functional Block Diagram

3.3.2 IO-Link Section Overview and Major Component Description

The IO-Link section of this board implements an IO-Link master using the TIOL111 device PHY and surrounding components needed to build a complete IO-Link master design. Therefore, on the physical side in addition to the TIOL111 device, a power supply for the ports, as well as a current sink is necessary. Also the hardware must be able to drive the wake-up pulse.

On the other side it is necessary to have a hardware as well as frame handler that support all three communication speeds. The TIOL111 device used as PHY here can handle all speeds (COM1, COM2, COM3). The eight port frame handler is implemented on the PRU of the used AM64x.

To realize an eight-port master, this design consists of eight M12 connectors and eight **TIOL111DMWR** IO-Link PHYs and associated LEDs. The IO-Link circuit is supported by two **TPS4H160BQPWPRQ1** Quad channel smart high-side switches for the L+ signals and a **SN65HVS882** serializer to support the D signals. The D signals are connected to a 10 pin header J21 for testing purpose. Both parts require a +24V which is supplied by a power jack on the board. A **TLC59282** 16bit IO expander is also included to drive the 16 LEDs. The SN65HVS882 and **TLC59282** 16bit IO expander are controlled by **SOC_SPI1** interface from GP EVM Board. SOC_SPI0. SOC_SPI1_CS0 is connected to the serializer and SOC_SPI1_CS1 is connected to the LED driver.

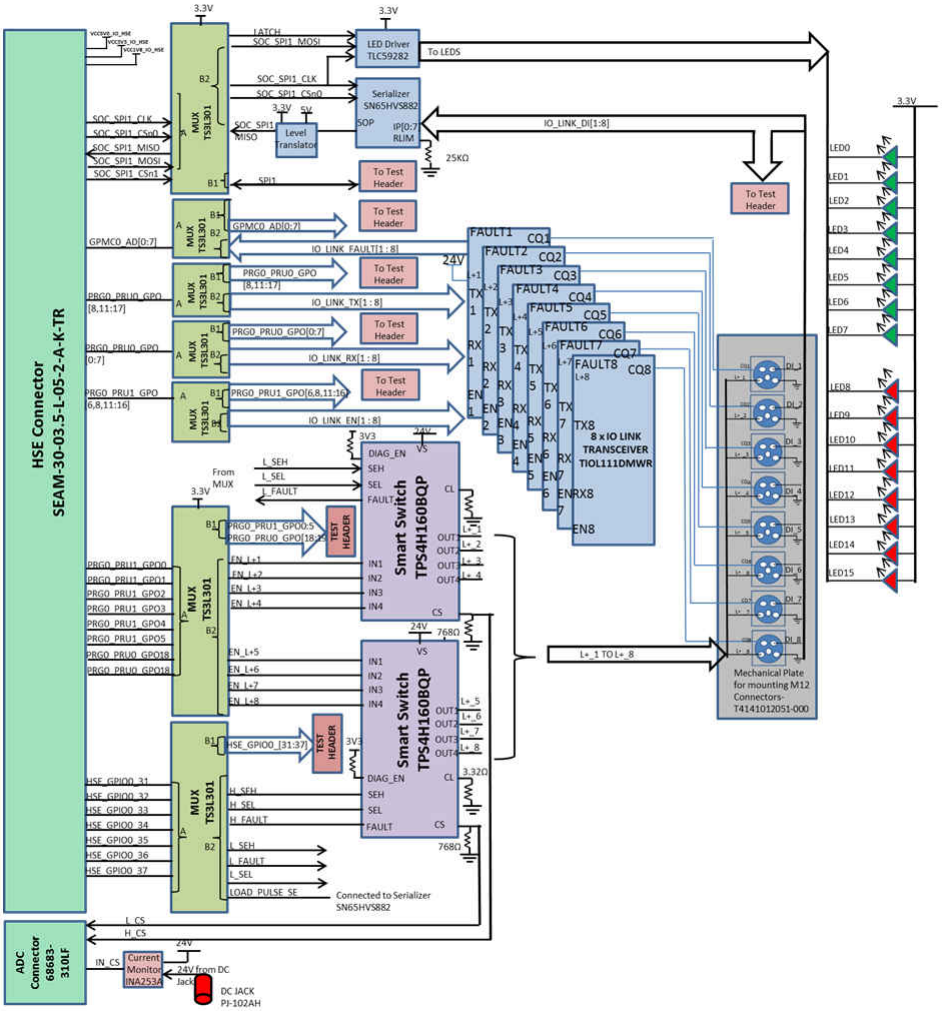

Figure 3-4. IO-Link Section Functional Block Diagram

3.3.2.1 IO Link Transceiver TIOL111DMWR

The TIOL111DMWR family of transceivers implements the IO-Link interface for industrial bidirectional, point-to point communication. There are eight IO Link PHYs used in our Board. Each PHY is connected to a M12 connector. The PRG0_PRU1 and GPMC signals are connected to the enable, RX ,TX and Fault signals of the PHYs via Muxes. The L+ pin requires 24 V, which is provided via the DC Jack.

3.3.2.2 Smart Switch TPS4H160BQPWPRQ1

The TPS4H160-Q1 device is fully protected quad channel smart high-side switch with four integrated 160-mΩ NMOS power FET. The PRG0_PRU1 and GPMC signals from HSE connector is connected to MUX which routes the signals either to Test Header or to the TPS4H160-Q1. The selection is done using on board jumpers. The OUT pins from the high side switch is connected to the L+ signals of the eight **M12 Connectors**. The OUT pins are controlled by Enable signals coming from the Mux. SEL and SEH are two pins to multiplex the shared current-sense function among the four channels. The current sense analog output is grounded via 768Ω and is connected to the AM64x EVM board via the ADC connector **68683-310LF** . A 3.33K resistor is connected to ground from the current limit pin to set the current limit threshold to 0.6A.

3.3.2.3 Serializer SN65HVS882

The SN65HVS882 is an eight channel, digital-input serializer for high-channel density digital input modules in industrial automation. In combination with galvanic isolators the device completes the interface between the high voltage signals on the field-side and the low-voltage signals on the controller side. Input signals are current-limited and then validated by internal debounce filters. Each digital input operates as a controlled current sink limiting the input current to a maximum value of I LIM. The current limit is derived from the reference current via I LIM = n × IREF, and IREF is determined by IREF = VREF/RLIM. Thus, changing the current limit requires the change of RLIM to a different value via: RLIM = n × VREF/I LIM. While the device is specified for a current limit of 3.6 mA, (via RLIM = 25 kΩ) The DI signals from the M12 connectors are connected to the input channels of the serializer. The serializer is SPI compatible Upon a low-level at the load input, LD, the information of the field inputs, IP0 to IP7 is latched into the shift register. Taking LD high again blocks the parallel inputs of the shift register from the field inputs. A low-level at the clock-enable input, CE, enables the clock signal, CLK, to serially shift the data to the serial output, SOP. Data is clocked at the rising edge of CLK. Thus, after eight consecutive clock cycles all field input data have been clocked out of the shift register and the information of the serial input, SIP, appears at the serial output, SOP.

3.3.2.4 INA253

The INA253 features a 2-mΩ, precision, current-sensing resistor and a 80-V common-mode, zero-drift topology, precision, excellent common-mode rejection ratio (CMRR), and features enhanced pulse width modulation (PWM) rejection current-sensing amplifier integrated into a single package. High precision measurements are enabled through the matching of the shunt resistor value and the current-sensing amplifier gain providing a highly-accurate, system-calibrated solution.

3.3.2.5 LED Driver TLC59282

The TLC59282 is a 16-channel, constant-current sink driver. Each channel can be individually controlled via a simple serial communications protocol that is compatible with 3.3 V or 5 V CMOS logic levels, depending on the operating VCC. Once the serial data buffer is loaded, a rising edge on LATCH transfers the data to the LEDx outputs. The BLANK pin can be used to turn off all OUTn outputs during power-on and output data latching to prevent unwanted image displays during these times. The constant-current value of all 16 channels is set by a single external resistor.

3.3.2.6 Signal Routing

The Signals routed to the Breakout Board section and IO Link section are described in Table 3-3.

Table 3-3. HSE Connector Signal Routing

HSE Connector	MUX	IO LINK Section	Breakout Board Section	Test Header
PRG0_PRU0GPO0	U2	RX_1	PRG0_PRU0GPO0_HDR	J2
PRG0_PRU0GPO1		RX_2	PRG0_PRU0GPO1_HDR	
PRG0_PRU0GPO2		RX_3	PRG0_PRU0GPO2_HDR	
PRG0_PRU0GPO3		RX_4	PRG0_PRU0GPO3_HDR	
PRG0_PRU0GPO4		RX_5	PRG0_PRU0GPO4_HDR	
PRG0_PRU0GPO5		RX_6	PRG0_PRU0GPO5_HDR	
PRG0_PRU0GPO6		RX_7	PRG0_PRU0GPO6_HDR	
PRG0_PRU0GPO7		RX_8	PRG0_PRU0GPO7_HDR	
PRG0_PRU0GPO8	U4	TX_1	PRG0_PRU0GPO8_HDR	
PRG0_PRU0GPO11		TX_2	PRG0_PRU0GPO11_HDR	
PRG0_PRU0GPO12		TX_3	PRG0_PRU0GPO12_HDR	J3
PRG0_PRU0GPO13		TX_4	PRG0_PRU0GPO13_HDR	
PRG0_PRU0GPO14		TX_5	PRG0_PRU0GPO14_HDR	
PRG0_PRU0GPO15		TX_6	PRG0_PRU0GPO15_HDR	
PRG0_PRU0GPO16		TX_7	PRG0_PRU0GPO16_HDR	
PRG0_PRU0GPO17		TX_8	PRG0_PRU0GPO17_HDR	
PRG0_PRU1GPO6	U9	EN_PHY_1	PRG0_PRU1GPO6_HDR	J4
PRG0_PRU1GPO8		EN_PHY_2	PRG0_PRU1GPO8_HDR	
PRG0_PRU1GPO11		EN_PHY_3	PRG0_PRU1GPO11_HDR	J5
PRG0_PRU1GPO12		EN_PHY_4	PRG0_PRU1GPO12_HDR	
PRG0_PRU1GPO13		EN_PHY_5	PRG0_PRU1GPO13_HDR	
PRG0_PRU1GPO14		EN_PHY_6	PRG0_PRU1GPO14_HDR	
PRG0_PRU1GPO15		EN_PHY_7	PRG0_PRU1GPO15_HDR	
PRG0_PRU1GPO16		EN_PHY_8	PRG0_PRU1GPO16_HDR	
PRG0_PRU1GPO2	U7	EN_L+5	PRG0_PRU1GPO2_HDR	J4
PRG0_PRU0GPO18		EN_L+1	PRG0_PRU0GPO18_HDR	
PRG0_PRU0GPO19		EN_L+2	PRG0_PRU0GPO19_HDR	
PRG0_PRU1GPO4		EN_L+7	PRG0_PRU1GPO4_HDR	
PRG0_PRU1GPO0		EN_L+3	PRG0_PRU1GPO0_HDR	
PRG0_PRU1GPO1		EN_L+4	PRG0_PRU1GPO1_HDR	
PRG0_PRU1GPO3		EN_L+6	PRG0_PRU1GPO3_HDR	
PRG0_PRU1GPO5		EN_L+8	PRG0_PRU1GPO5_HDR	
GPMC0_ADC0	U11	FAULT_1	GPMC0_ADC0_HDR	J6
GPMC0_ADC1		FAULT_2	GPMC0_ADC1_HDR	
GPMC0_ADC2		FAULT_3	GPMC0_ADC2_HDR	
GPMC0_ADC3		FAULT_4	GPMC0_ADC3_HDR	
GPMC0_ADC4		FAULT_5	GPMC0_ADC4_HDR	
GPMC0_ADC5		FAULT_6	GPMC0_ADC5_HDR	
GPMC0_ADC6		FAULT_7	GPMC0_ADC6_HDR	
GPMC0_ADC7		FAULT_8	GPMC0_ADC7_HDR	

Table 3-3. HSE Connector Signal Routing (continued)

HSE Connector	MUX	IO LINK Section	Breakout Board Section	Test Header
HSE_GPIO0_36	U12	L_FAULT	HSE_GPIO0_36_HDR	J8
HSE_GPIO0_35		L_SEL	HSE_GPIO0_35_HDR	
HSE_GPIO0_37		LOAD_PULSE_SE	HSE_GPIO0_37_HDR	
HSE_GPIO0_34		L_SEH	HSE_GPIO0_34_HDR	
HSE_GPIO0_31		H_SEH	HSE_GPIO0_31_HDR	
HSE_GPIO0_32		H_SEL	HSE_GPIO0_32_HDR	
HSE_GPIO0_33		H_FAULT	HSE_GPIO0_33_HDR	
HSE_GPIO0_38			HSE_GPIO0_38	
HSE_GPIO0_39			HSE_GPIO0_39	
HSE_GPIO0_41			HSE_GPIO0_41	
SOC_SPI1_MISO	U17	SOC_SPI1_MISO_SE	SOC_SPI1_MISO_HDR	J9
SOC_SPI1_MOSI		SOC_SPI1_MOSI_LED	SOC_SPI1_MOSI_HDR	
SOC_SPI1_CLK		SOC_SPI1_CLK_SE/LED	SOC_SPI1_CLK_HDR	
SOC_SPI1_CS0		SOC_SPI1_CS0_SE	SOC_SPI1_CS0_HDR	
SOC_SPI1_CS1		LATCH	SOC_SPI1_CS1_HDR	
HSE_MCAN1_RX/ I2C3_SDA			HSE_MCAN1_RX/I2C3_SDA	J3
HSE_MCAN1_TX/ I2C3_SCL			HSE_MCAN1_TX/I2C3_SCL	
HSE_MCAN0_TX/ UART4_RXD			HSE_MCAN0_TX/UART4_RXD	
HSE_MCAN0_RX/ UART4_TXD			HSE_MCAN0_RX/UART4_TXD	
GPMC0_ADC[8:9]			GPMC0_ADC[8:9]	J6
GPMC0_ADC[10:15]			GPMC0_ADC[10:15]	J7
GPMC0_CSN2			GPMC0_CSN2	
GPMC0_CSN3			GPMC0_CSN3	
GPMC0_CSN1			GPMC0_CSN1	
GPMC0_DIR			GPMC0_DIR	
PRG1_PRU1GPO18			PRG1_PRU1GPO18	J5
PRG1_PRU1GPO19			PRG1_PRU1GPO19	
PRG0_MDIO0_MDIO			PRG0_MDIO0_MDIO	
PRG0_MDIO0_MDC			PRG0_MDIO0_MDC	

3.3.3 Power Section

All necessary power required for the IO Link/Breakout Board are provided from the HSE connector and on board 24 V DC supply via DC jack. Power Good LED's are provided for 5 V, 3.3 V and 1.8 V. Figure 3-5 shows the power section of the Breakout board.

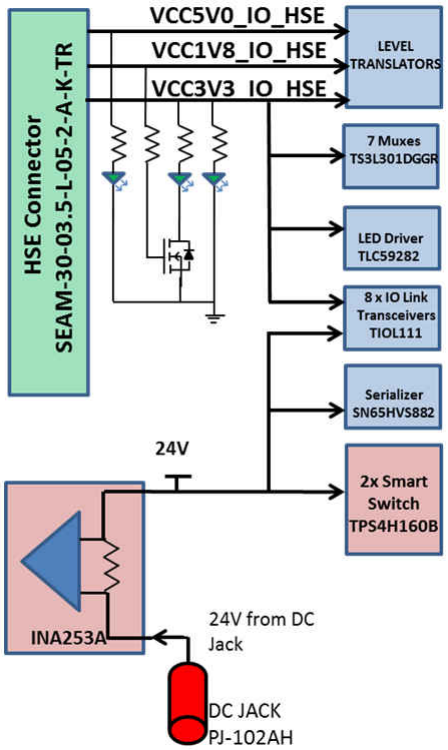

Figure 3-5. Power Input

3.3.3.1 Power Input

Nominal Output Voltage: 24V DC

Maximum Output Current: 2A

Plug Type: 2.1mm I.D. x 5.5mm O.D x 9mm Barrel Jack

Note

TI recommends using an external power supply or power accessory that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, and so forth.

3.3.4 Board Mating Connections

The pinout for the mating connectors of the IO Link/Breakout Board are listed in Table 3-4.

Note

The following HSE Connector pin names do not indicate exhaustive SoC Pin functionality. For a full list of pin and signal functions, see the device-specific GP EVM User's Guide and data sheet.

Table 3-4. 150 Pin HSE Connector (SEAM-30-03.5-L-05-2-A-K-TR)

Pin Name	Net Name	Pin Name	Net Name
A1	VCC_5V0_HSE	B1	SOC_SPI1_MISO
A2	VCC_5V0_HSE	B2	SOC_SPI1_MOSI
A3	VCC_5V0_HSE	B3	DGND
A4	PRG0_MDIO0_MDIO	B4	PRG0_PRU1GPO8

Table 3-4. 150 Pin HSE Connector (SEAM-30-03.5-L-05-2-A-K-TR) (continued)

Pin Name	Net Name	Pin Name	Net Name
A5	PRG0_MDIO0_MDC	B5	DGND
A6	DGND	B6	DGND
A7	PRG0_PRU0GPO8	B7	PRG0_PRU0GPO7
A8	PRG0_PRU0GPO2	B8	PRG0_PRU0GPO17
A9	PRG0_PRU0GPO3	B9	PRG0_PRU0GPO18
A10	DGND	B10	DGND
A11	PRG0_PRU1GPO1	B11	PRG0_PRU0GPO19
A12	PRG0_PRU1GPO0	B12	PRG0_PRU0GPO0
A13	PRG0_PRU0GPO4	B13	PRG0_PRU1GPO4
A14	PRG0_PRU0GPO12	B14	PRG0_PRU0GPO11
A15	PRG0_PRU1GPO16	B15	PRG0_PRU1GPO12
A16	DGND	B16	DGND
A17	PRG0_HSE_ETH1_CLK	B17	PRG0_HSE_ETH2_CLK
A18	DGND	B18	DGND
A19	GPMC0_AD15	B19	DGND
A20	HSE_GPIO0_36	B20	GPMC0_AD14
A21	GPMC0_AD9	B21	GPMC0_AD10
A22	GPMC0_AD8	B22	HSE_GPIO0_31
A23	DGND	B23	DGND
A24	DGND	B24	HSE_GPIO0_35
A25	DGND	B25	DGND
A26		B26	DGND
A27	VCC3V3_IO_HSE	B27	DGND
A28	VCC3V3_IO_HSE	B28	DGND
A29	VCC3V3_IO_HSE	B29	HSE_PRG0_PRU0_GPO10
A30		B30	DGND
C1	SOC_SPI1_CLK	D1	SOC_SPI1_CS0
C2	VCC1V8_HSE	D2	SOC_SPI1_CS1
C3	VCC1V8_HSE	D3	MCU_RESETZ
C4	DGND	D4	DGND
C5	PRG0_PRU0GPO13	D5	PRG0_PRU1GPO13
C6	PRG0_PRU0GPO5	D6	PRG0_PRU1GPO5
C7	DGND	D7	DGND
C8	PRG0_PRU1GPO3	D8	PRG0_PRU0GPO6
C9	PRG0_PRU0GPO14	D9	PRG0_PRU1GPO2
C10	DGND	D10	DGND
C11	PRG0_PRU1GPO15	D11	PRG0_PRU1GPO11
C12	PRG1_PRU1GPO19	D12	PRG0_PRU0GPO15
C13	DGND	D13	DGND
C14	GPMC0_AD2	D14	GPMC0_AD1
C15	GPMC0_AD5	D15	GPMC0_AD4
C16	DGND	D16	DGND
C17	DGND	D17	GPMC0_AD7
C18	DGND	D18	GPMC0_CSN2
C19	DGND	D19	GPMC0_CSN3
C20	DGND	D20	DGND
C21	GPMC0_AD12	D21	GPMC0_AD13

Table 3-4. 150 Pin HSE Connector (SEAM-30-03.5-L-05-2-A-K-TR) (continued)

Pin Name	Net Name	Pin Name	Net Name
C22	HSE_GPIO0_32	D22	HSE_GPIO0_33
C23	HSE_GPIO0_34	D23	HSE_PRG0_PRU1_GPO7
C24	HSE_GPIO0_37	D24	HSE_MCAN0_TX/UART4_RXD
C25	DGND	D25	DGND
C26	HSE_GPIO0_39	D26	HSE_GPIO0_41
C27	HSE_PRG0_PRU1_GPO19	D27	HSE_PRG0_PRU1_GPO18
C28	HSE_PRG0_PRU1_GPO17	D28	HSE_PRG0_PRU0_GPO9
C29	HSE_MCAN1_RX/I2C3_SDA	D29	HSE_MCAN1_TX/I2C3_SCL
C30	DGND	D30	DGND
E1	SOC_I2C0_SCL	E16	DGND
E2	SOC_I2C0_SDA	E17	GPMC0_AD6
E3	MCU_RESETSTATZ	E18	GPMC0_DIR
E4	HSE_DETECT	E19	GPMC0_CSN1
E5	DGND	E20	DGND
E6	DGND	E21	GPMC0_AD11
E7	DGND	E22	DGND
E8	PRG0_PRU0GPO1	E23	HSE_PRG0_PRU1_GPO9
E9	PRG0_PRU0GPO16	E24	HSE_MCAN0_RX/UART4_TXD
E10	DGND	E25	DGND
E11	PRG0_PRU1GPO6	E26	HSE_GPIO0_38
E12	PRG0_PRU1GPO14	E27	HSE_PRG0_PRU1_GPO10
E13	PRG1_PRU1GPO18	E28	DGND
E14	GPMC0_AD0	E29	DGND
E15	GPMC0_AD3	E30	MCU_PORZ

Table 3-5. 20 Pin ADC Connector 68683-310LF

Pin Name	Net Name	Pin Name	Net Name
1	NC	11	NC
2	NC	12	NC
3	NC	13	NC
4	NC	14	NC
5	NC	15	AIN_0
6	AIN_2	16	NC
7	NC	17	NC
8	NC	18	NC
9	NC	19	NC
10	AIN_4	20	NC

4 Known Issues

This section describes the currently known issues on each EVM revision and applicable workarounds.

Table 4-1. AM64x IO Link/Breakout Board Known Issues

Issue Number	Issue Title	Issue Description
1	Voltage Spike across TX Transceiver Line	Occasional voltage spikes fixed by adding a diode to Pin 1 of the transistor.

4.1 Issue 1: Voltage Spike Across the TX Line of the Transceiver

Affected PCB version: E1

Board Modification Sticker: M1

Severity: **High**

The original design of the IO Link breakout board resulted in occasional voltage spikes on the TX line of the transceiver. A fix was implemented by rotating transistors Q4, Q5, Q6, Q7, Q8, Q9, Q10 and Q11 and adding a diode in line with Pin 1 of the transistor.

This Mod was applied to all boards shipped with a 1st revision PCB.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025