Application Note

AM62Px eMMC HS400 Board Design and Simulation Guidelines

Sitara MPU HW Apps

ABSTRACT

This application report contains material applicable to the eMMC HS400 interface of AM62Px processor board designs.

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1 Overview

The AM62Px processor supports eMMC HS400. This document contains material applicable to board designs containing eMMC memories. For supported data rates, see the device-specific data manual.

1.1 Board Designs Supported

To achieve the high frequency targets of the eMMC interfaces supported by the AM62Px family of devices, an excellent PCB implementation is required. TI highly recommends that customer designs copy the SK-AM62P-LP (PROC164E2) layout exactly, and in every detail (PCB material, routing, spacing, vias, and so forth) to achieve the full specified interface frequency and data rate. If the design does not or cannot copy the TI design, then the EVM must still be used as a starting point, and simulations must be performed. The customer design needs to constrain the interface frequency and data rate based on the PCB implementation.

The goal of this document is to define a set of layout and routing and simulation rules that allow designers to successfully implement a robust eMMC HS400 design. The PCB design is required to be simulated to verify the design targets are achieved. TI limits debug and support for boards that have not been designed and simulated according to the steps defined in this document. Systems that do not follow the TI EVM implementation or do not have valid simulation results likely need to run at a reduced frequency.

This document provides an IBIS model simulation methodology as guidance for validation of the simulations results. There is still an expectation that the PCB design work (design, layout, and fabrication) is performed and reviewed by a highly knowledgeable high-speed PCB designer. Problems such as impedance discontinuities when signals cross a split in a reference plane can be detected visually by those with the proper experience.

TI only supports board designs that follow the guidelines in this document. These guidelines are based on well-known transmission line properties for copper traces routed over a solid reference plane. Declaring insufficient PCB space does not allow routing guidelines to be discounted. TI limits debug and support for designs that have not been simulated according to the steps defined in this document.

1.2 General Board Layout Guidelines

To verify good signaling performance, the following general board design guidelines must be followed:

- Always follow the TI example layouts and EVM designs as close as possible. If concepts or routing strategies are not understood, then ask questions on E2E.
- All signals need ground reference (strongly suggest on both sides).
- Avoid crossing plane splits in the signal reference planes.
- Use the widest trace that is practical between decoupling capacitors and supply pin.
- Minimize inter-symbol interference (ISI) by keeping impedance matched.
- Minimize crosstalk by isolating sensitive signals, such as strobes and clocks, and by using a proper PCB stack-up.
- Avoid return path discontinuities by adding vias or capacitors whenever signals change layers and reference planes.
- Minimize reference voltage noise through proper isolation and proper use of decoupling capacitors.
- Keep the signal routing stub lengths as short as possible.
- Add additional spacing for clock and strobe nets to minimize crosstalk.
- Maintain a common ground (also called GND) reference for all signals and for all bypass and decoupling capacitors.
- Consider the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.
- via-to-via coupling can be significant part of PCB-level crosstalk. Dimension and pitch of vias is important. For high speed interfaces, consider GND shielding vias. This via coupling is one factor for recommending data signals be routed on layers closest to processor.
- via stubs affect signal integrity. via back-drilling can improve signal integrity, and is required in some instances.

For more information, see the *High-Speed Interface Layout Guidelines* application note. This provides additional general guidance for successful routing of high-speed signals.

1.3 PCB Stack-Up

The recommended stack-up for routing designs with the AM62Px System-on-Chip (SoC) is a ten or twelve layer stack up. However, this can only be accomplished on a board with routing room with large keep-out areas. Additional layers are required if:

- The PCB layout area is restricted, which limits the area available to spread out the signals to minimize crosstalk.
- Other circuitry must exist in the same area, but on layers isolated from the eMMC routing.
- Additional planes layers are needed to enhance the power supply routing or to improve EMI shielding.

Board designs that are relatively dense can require more layers to properly allow the eMMC routing to be implemented such that all rules are met.

All eMMC signals must be routed adjacent to a solid GND reference plane. When multiple GND reference planes exist in the eMMC routing area, stitching vias must be implemented nearby wherever vias transfer signals to a different GND reference plane. This is required to maintain a low-inductance return current path.

TI recommends all eMMC signals be routed as strip-line. Some PCB stack-ups implement signal routing on two adjacent layers. This is not recommended as crosstalk occurs on any trace routed parallel to another trace on an adjacent layer, even for a very short distance. TI recommends to route eMMC signals on PCB layers closer to the SoC within the stack-up, giving the signal a shorter travel time through the via. The PCB layers farther from the SoC has longer travel times through the via, which can increase coupling between vias. Both signal and via coupling can lead to smaller timing margins.

Note a shorter via travel can mean a longer via stub (if using standard drill vias), so that is to be considered as well. Simulation can be used to determine if via stub length is an issue.

Table 1-1. PCB Stack-up Specifications

Number	Parameter(5)	MIN	TYP	MAX	UNIT
1	PCB routing plus plane layers		10 or 12		
2	Signal routing layers		6		
3	Full GND reference layers under eMMC routing region (1)	1			
4	Number of reference plane cuts allowed within eMMC routing region (2)			0	
5	Number of layers between eMMC routing layer and reference plane (3)			0	
6	PCB routing feature size		0.10		mm
7	PCB trace width, w	0.08			mm
8	Point-to-Point, single-ended impedance		50		Ω
9	Impedance control (4)	Z-10%	Z	Z+10%	Ω

(1) Ground reference layers are preferred over power reference layers. Return signal vias need to be near layer transitions.
(2) No traces must cross reference plane cuts within the eMMC routing region. High-speed signal traces crossing reference plane cuts create large return current paths, which can lead to excessive crosstalk and EMI radiation. Beware of reference plane voids caused by via anti-pads, as these also cause discontinuities in the return current path.
(3) Reference planes are to be directly adjacent to the signal layer, to minimize the size of the return current loop.
(4) Z is the nominal singled-ended impedance selected for the PCB.
(5) These specifications are to be used as a starting point for designs. TI recommends each design be extracted and simulated to make sure all requirements are met.

1.4 Bypass Capacitors

1.4.1 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the eMMC and other circuitry. Table 1-2 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Table 1-2 only covers the bypass needs of the eMMC PHY of SoC. Additional bulk bypass capacitance is needed for other circuitry. For any additional decoupling requirements for the eMMC devices, see the manufacturer's data sheet

Table 1-2. Bulk Bypass Capacitors

Number	Parameter	MIN	MAX	UNIT
1	VDDS_MMC0 bulk bypass capacitor count(1)	1 (2)		Devices

Table 1-2. Bulk Bypass Capacitors (continued)

Number	Parameter	MIN	MAX	UNIT
2	VDDS_MMC0 bulk bypass total capacitance	10 (2)		µF

(1) These devices must be placed near the devices that are bypassing, but preference needs to be given to the placement of the high-speed (HS) bypass capacitors.
(2) The capacitor recommendations in this guide reflect only the needs of this processor. For determining the appropriate decoupling capacitor arrangement for the memory device, see the eMMC device vendor's guidelines.

1.4.2 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper eMMC HS400 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors to the VDDS_MMC0 supply pin and the associated ground connections. Table 1-3 contains the specification for the HS bypass capacitors and for the power connections on the PCB. Generally speaking, TI recommends:

- Fitting as many HS bypass capacitors as possible.
- Minimizing the distance from the bypass capacitor to the pins and balls being bypassed.
- Using the smallest physical sized ceramic capacitors possible with the highest capacitance readily available.
- Connecting the bypass capacitor pads to the vias using the widest traces possible and using the largest via hole size possible.
- Minimizing via sharing. Note the limits on via sharing shown in Table 1-3.
- Using three-terminal capacitors instead of two-terminal capacitors. Three-terminal capacitors provide lower loop inductance, and one three-terminal capacitor can take the place of multiple two-terminal capacitors, further optimizing loop inductance.

For any additional eMMC device requirements, see the manufacturer's data sheet.

Table 1-3. High-Speed Bypass Capacitors

Number	Parameter	MIN	TYP	MAX	UNIT
1	Processor HS bypass capacitor count per VDDS_MMC0 rail (2)	3			Devices
2	Processor HS bypass capacitor total capacitance per VDDS_MMC0 rail	0.3			µF
3	Number of connection vias for VDDS_MMC0 power ball	3			vias
4	Trace length from processor power/ground ball to connection via (1)		0.25	0.51	mm

(1) Closer/shorter is preferable.
(2) Low-ESL and multi-terminal capacitors can reduce number of bypass capacitors required.

1.5 Velocity Compensation

For a PCB design, portions of the eMMC signal traces are microstrip (BGA break-out segments), but majority of the trace segments are stripline (internal layers). Even though there is a wide variation in the proportion of track length routed as microstrip or stripline, the length or delay matching process must include a mechanism for compensating for the velocity delta between these two types of PCB interconnects. A compensation factor of 1.1 has been specified for this purpose by JEDEC. All microstrip segment lengths are to be divided by 1.1 before summation into the length matching equation. The resulting compensated length is termed the *stripline equivalent length*. While some amount of residual velocity mismatch skew remains in the design, the process is a substantial improvement over simple length matching.

2 eMMC Board Design and Layout Guidance

2.1 eMMC Introduction

eMMC is a managed memory device specification governed by the JEDEC standard JESD84-B51, Embedded Multi-Media Card (e•MMC) Electrical Standard (5.1). This standard strives to support high throughput for large data transfers without compromising small random data accesses (code) while maintaining low power consumption required by mobile devices. Its 11-signal bus consists of Clock (CLK), Command (CMD), Data Strobe (DS), and Data (DAT[7:0]) with 3 different bus widths: 1-bit (default), 4-bit, and 8-bit. Clock frequencies range from 0-200MHz, with single- and dual-data-rate options for up-to 400MB/s max data transfer rate (HS400). In HS400 mode, the IO voltage is fixed at 1.8V.

The following sections detail the routing specification and layout guidelines for an eMMC interface with a focus on the power delivery for the AM62Px eMMC PHY.

Note

The maximum eMMC data rate supported by the AM62Px processor is defined in the AM62Px Sitara™ Processors Data Sheet. Refer to HS4005 Cycle time, MMC0_CLK in the MMC0 Switching Characteristics – HS400 Mode table.

2.2 eMMC Signal Termination

No external pulls are required for the AM62Px MMC0 eMMC signals since the PHY enables and controls the internal pulls as required for an eMMC.

Pull-ups for DAT[7:0] and CMD are internally enabled during reset and after reset. A pull-down is enabled for the DS and the clock output (CLK) is driven low after reset. There are no PADCONFIG registers associated with the MMC0 pins. The internal pulls associated with the MMC0 pins are dynamically controlled by the MMC0 host and PHY.

External pulls are not a requirement for the eMMC Data, CMD, DS or the CLK signals.

Refer to AM62P, AM62P-Q1 Processor Family Schematic Design Guidelines and Schematic Review Checklist

2.3 Signal Routing Specification

The eMMC signals are always point-to-point. TI recommends to minimize layer transitions during routing. If a layer transition is necessary, then this is better to transition to a layer using the same reference plane. If this cannot be accommodated, then make sure there are nearby ground vias to allow the return currents to transition between reference planes. The goal is to provide a low inductance path for the return current. To optimize the skew matching, TI recommends routing all nets on one layer where all nets have the exact same number of vias and the same via barrel length. The MMC0 Timing Conditions table in the AM62Px Sitara™ Processors Data Sheet defines the requirements for trace delay and trace mismatch delay.

There are no stubs allowed on the nets. All test and probe access points must be in line without any branches or stubs.

2.4 Power Supply Design

The power delivery network (PDN) of the 1.8V IO voltage to the AM62Px VDDS_MMC0 PHY IO supply pin must satisfy specific target impedance requirements at specific frequencies. The PDN for this supply on the SK-AM62P-LP (PROC164E2) has been designed and simulated to demonstrate compliance with the eMMC JEDEC specification JESD84-B51. In order to fulfill these requirements, this board requires multiple power and ground via structures connected to multiple decoupling capacitors in close proximity to the VDDS_MMC0 pin. Placement of these vias and decoupling capacitors is significant and described below. Refer also to the requirements in Table 1-3.

The SK-AM62P-LP (PROC164E2) board is 1.73mm thick with 12 layers and plated through hole (PTH) vias only (0.20mm drill).

Three separate VDDS_MMC0 vias are placed each within 0.76mm from the VDDS_MMC0 1K2 pin (distance measured from center of pin to center of via). A copper shape on the AM62Px pin side of the board surrounds and connects the 3 vias and the VDDS_MMC0 pin. These 3 power vias are surrounded by 6 GND vias that connect tightly to decoupling capacitors placed on the opposite side of the board.

Three 0.1uF 2-terminal decoupling capacitors are placed with one of their pads as close as possible to each of the 3 VDDS_MMC0 vias without implementing via-in-pad. The maximum distance from the center of any of the capacitor pads to the center of each via is less than 0.51mm. A copper shape surrounds and connects the 3 VDDS_MMC0 vias and the 3 capacitor pads that connect to VDDS_MMC0. The GND pads of each capacitor are placed as close as possible to 3 of the 6 GND vias without implementing via-in-pad. A short and wide trace connects the capacitor to each GND via (0.25mm trace width and trace length less than 0.51mm, measured center-to-center). No decoupling capacitors share the same power or GND via. The GND vias connect to multiple solid GND reference planes on inner layers. The below SK-AM62P-LP (PROC164E2) example design places capacitors at 45-degree angles, but placement restricted to 90-degree increments has also been demonstrated to perform equally as well.

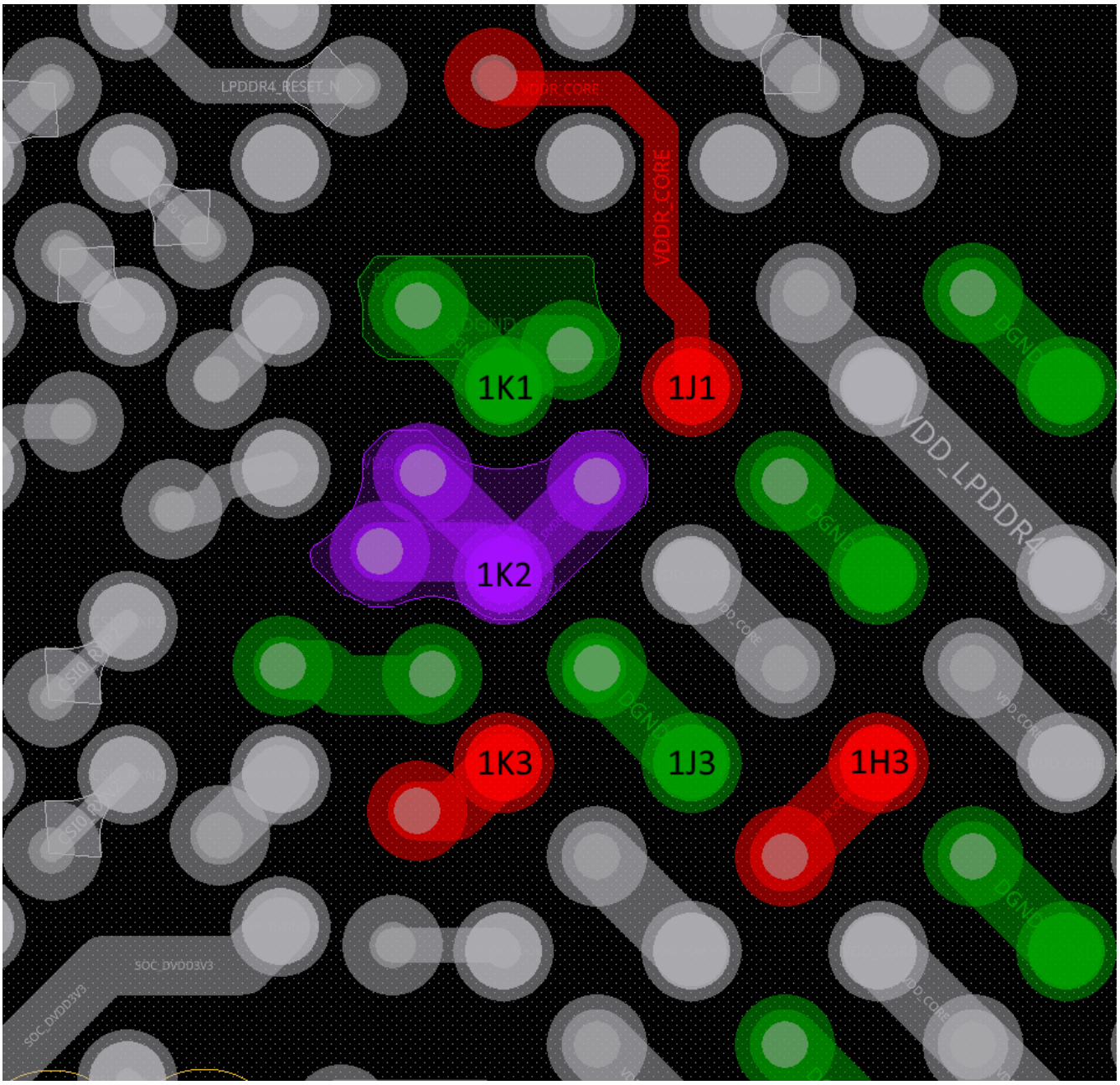

Figure 2-1. SK-AM62P-LP (PROC164E2) TOP Layer - VDDS_MMC0 (Purple), GND (Green), VDDR_CORE (Red)

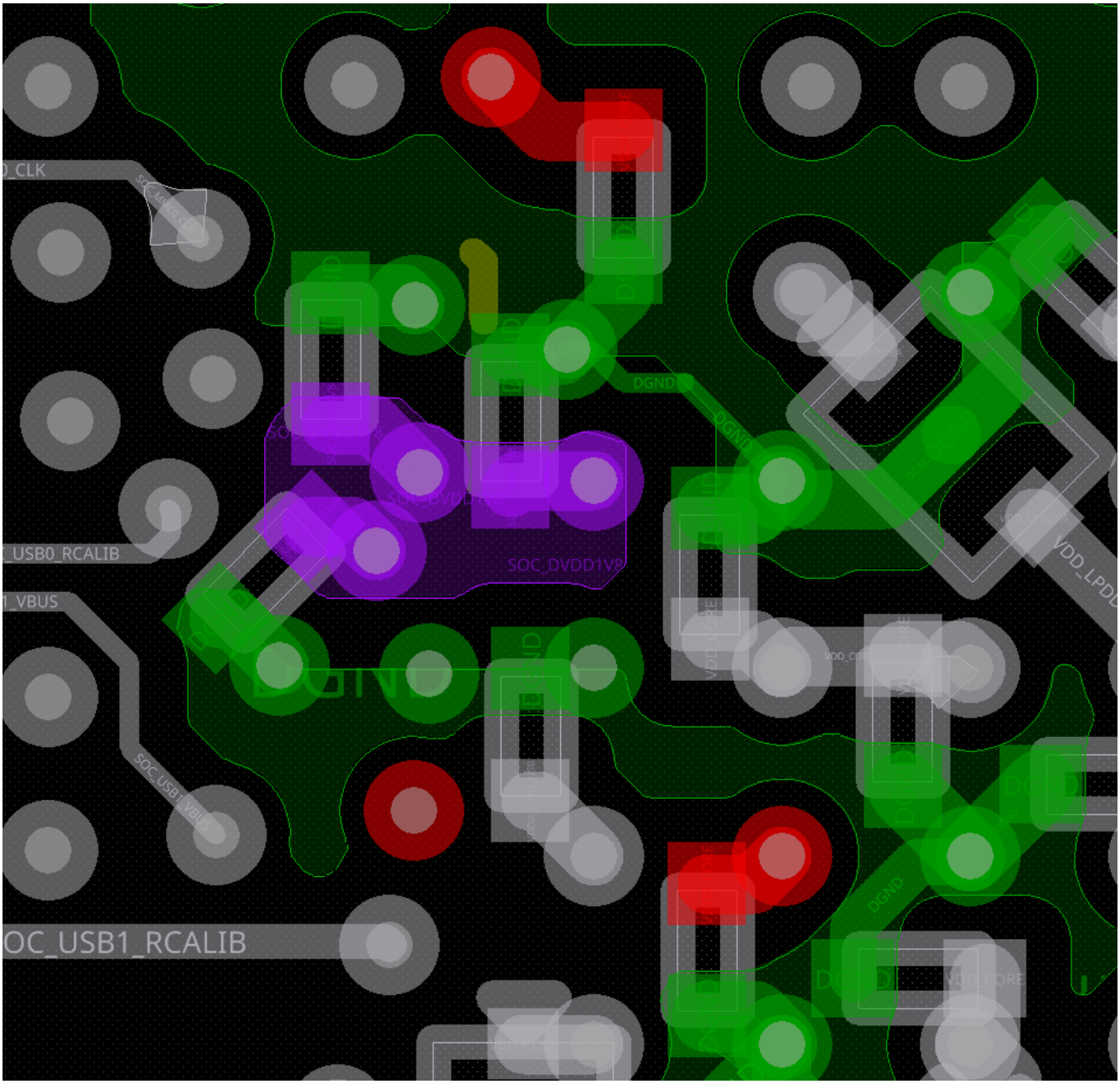

Figure 2-2. SK-AM62P-LP (PROC164E2) Bottom Layer - VDDS_MMC0 (Purple), GND (Green), and VDDR_CORE (Red)

A common 1.8V IO supply must connect to both the AM62Px VDDS_MMC0 PHY IO supply pin and the attached eMMC device IO supply. The 1.8V IO supply may also connect to other supply pins on the AM62Px, such as VDDSHV1, VDDSHV6, and VMON_1P8_SOC.

Copper pours for the AM62Px VDDS_MMC0 need to be on a PCB layer as close to the BGA pin as possible to minimize inductance. Copper pours for each individual 1.8V power rail that is shorted with VDDS_MMC0 needs to be as close to the BGA pin(s) as possible also. However, the star connection that joins VDDS_MMC0 and the different 1.8V power rails that are shorted with VDDS_MMC0 needs to be as far away from the BGA pins as possible (on a PCB layer far from the SoC BGAs). The intent of this approach is to minimize supply interference between VDDS_MMC0 and other 1.8V power rails that are shorted with VDDS_MMC0. In Section 3 of this document, the loop inductance of the decoupling capacitors for VDDS_MMC0 IO supply and the decoupling capacitors of the other 1.8V power rails that are shorted with VDDS_MMC0 are provided as a design target.

Isolation between the AM62Px VDDS_MMC0 PHY IO supply pin and neighboring supply pins must be achieved through via separation and decoupling capacitors placed in close proximity to each via.

For example, in the SK-AM62P-LP (PROC164E2) design, the minimum via-to-via spacing between any VDDS_MMC0 via and the closest VDDR_CORE via is 1.11mm. Additionally, GND vias are inserted between vias of these two supplies to further limit supply crosstalk.

The core of the AM62Px eMMC PHY is powered through the VDDR_CORE supply pins. Isolation between the 1.8V VDDS_MMC0 PHY IO supply and the 0.85V VDDR_CORE supply on the PCB is needed to prevent noise coupling from the 1.8V VDDS_MCC0 supply into 0.85V VDDR_CORE supply. Any such noise coupling into the core of the eMMC PHY leads to jitter, which reduces signal integrity margins. The via placement and decoupling capacitor placement for VDDS_MMC0 and VDDR_CORE supplies in the SK-AM62P-LP (PROC164E2) are shown in Figure 2-1 and Figure 2-2. VDDS_MMC0 is shown in purple and VDDR_CORE is shown in red.

3 eMMC Board Design Simulations

This section is intended to provide an overview of the basic system-level board extraction, simulation, and analysis methodologies for high-speed eMMC interfaces. This is an essential step to make sure the PCB design meets all the requirements to operate the targeted speeds.

3.1 Board Model Extraction

The board level extraction guidelines listed below are intended to work in any EDA extraction tool and are not tool-specific. It is important to follow the steps outlined in Section 3.2 immediately after completing touchstone model extractions. The design must be checked with these steps prior to running IBIS simulations.

1. For Power extractions, always extract power in a 3D-EM solver.
2. For signal extractions, a 2.5D extraction is sufficient
3. Use wide-band models. TI recommends to extract from DC to at least until 6x the Nyquist frequency (for example, for eMMC HS400 extract the model at least until 2.4GHz).
4. Check the board stack-up for accurate layer thickness and material properties.
   a. TI recommends to use Djordjevic-Sarkar models for the dielectric material definition.
5. Use accurate etch profiles and surface roughness for the signal traces across all layers in the stack-up.
6. If the board layout is cut prior to extraction (to reduce simulation time), then define a cut boundary that is at least 0.25 inch away from the signal and power nets.
7. Check the via pad stack definitions.
   a. Make sure that the non-functional internal layer pads on signal vias are modeled the same way the pads are fabricated.
   b. These non-functional internal layer pads on signal vias are not recommended by TI.
8. Use Spice/S-parameter models (typically available from the vendor) for modeling all passives in the system.

3.2 Board-Model Validation

The extracted board models need to be checked for the following properties:

- Passivity: This makes sure that the board model is a passive network and does not generate energy.
- Causality: This makes sure that the board model obeys the causal relationship (output follows input).

These checks can be performed in any standard EDA simulator or extraction engine.

3.3 Capacitor Loop Inductance

High frequency decoupling capacitors must have a low loop inductance to respond to instantaneous current demands. This localized response also helps to prevent supply noise from one supply pin from coupling into another pin that shares the same supply. An inductive path to the decoupling capacitors only adds to the fixed inductance of the SoC package.

High frequency decoupling capacitors must have low embedded series inductance (ESL). The SK-AM62P-LP (PROC164E2) uses ceramic 0.1uF 10V 10% 0201 capacitors with an ESL of approximately 0.146nH. The placement of each capacitor and connectivity through trace and vias must be kept short and wide to minimize total loop inductance.

The 1.8V VDDS_MMC0 eMMC PHY IO supply is typically shared among eMMC and non-eMMC supplies. Each supply pin requires decoupling capacitors placed in close proximity to the respective supply pin. The below table shows the loop inductance of each capacitor on the 1.8V rail used by the SK-AM62P-LP (PROC164E2) .

Check the loop inductance with the following steps:

1. Extract loop inductance for all high frequency decoupling capacitors on other 1.8V power rails shorted to VDDS_MMC0.
   a. Loop inductance must be extracted with a 3-D field solver. **2.5D solvers will not suffice for inductance extractions.**
   b. The inductance extraction should be from the pads of the decoupling capacitor to the SoC BGA(s).
2. Compare the extracted loop inductance to the target values published in Table 3-1.

a. The loop inductance for all decoupling capacitors on VDDS_MMC0 and other 1.8V power nets shorted to VDDS_MMC0 needs to be smaller than the target to pass loop inductance checks.

Table 3-1. Loop Inductance of Capacitors on VDDS_MMC0 and Other Shared 1.8V Power Rails

Supply Name	Description	Target
VDDS_MMC0	1.8V eMMC0 PHY IO Supply	≤ 0.72nH
VDDSHVn(1), VDDSHV_CANUART, VDDSHV_MCU	1.8V IO supplies shared with VDDS_MMC0(2)	≤ 1.37nH

(1) n = 0-6
(2) Consider only 1.8V IO supplies shared with VDDS_MMC0 supply.

3.4 AC Impedance

The below AC impedance plot of the VDDS_MMC0 eMMC PHY IO supply on the SK-AM62P-LP (PROC164E2) considers the power and GND shapes with vias and decoupling capacitors from the output of the inductor of the PMIC to the VDDS_MMC0 SoC pin. The SoC package and die are not modeled.

Through modeling of the complete system, TI has demonstrated that the AC impedance profile plotted in Figure 3-1 adequately controls the power supply noise to achieve compliance with the JESD84-B51 standard at the HS400 data rates (ie. 400MHz).

Check the AC impedance with the following steps:

1. Extract S-parameter files for the 1.8V AM62Px VDDS_MMC0 eMMC PHY IO supply of the PCB including decoupling capacitors.
   a. Power S-parameters must be extracted with a 3-D field solver. **2.5D solvers will not suffice for power extractions.**
   b. Power should be modeled from the output of the inductor of the PMIC to the AM62Px VDDS_MMC0 pin.
   c. Capacitors and any other component in the power path must be modeled accurately with S-parameter or SPICE models from the vendor.
2. Plot the AC impedance for the eMMC PHY IO supply VDDS_MMC0 and compare this to target AC Impedance profile provided in Figure 3-1 below.
   a. Check the AC impedance of VDDS_MMC0 from DC up to 400MHz. The extracted AC impedance must be equal or lower than Figure 3-1 to pass the AC impedance check.

Note

Beyond about 50MHz, the PCB power planes and decoupling capacitors have diminishing effect on impedance. As frequency rises, the SoC package inductance and on-die capacitance are more significant

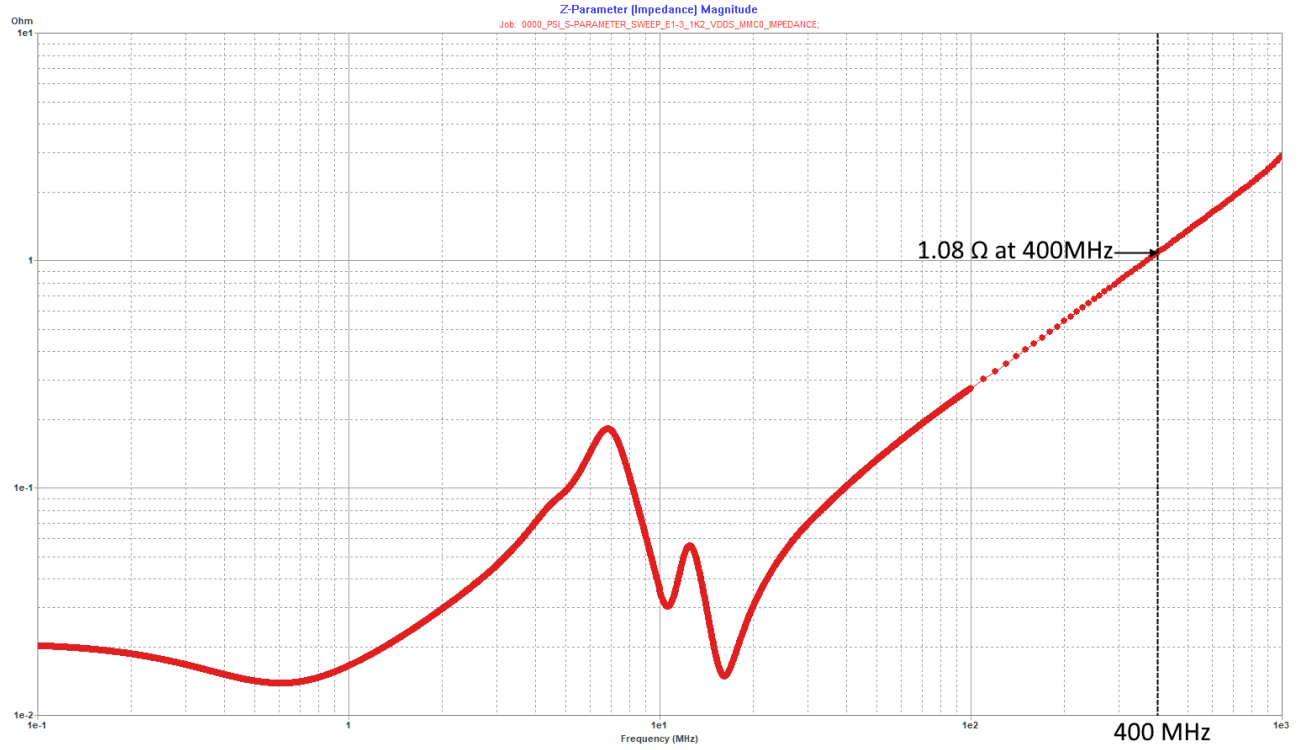

Figure 3-1. VDDS_MMC0 AC Impedance Magnitude vs Frequency (Board Only)

3.5 IBIS Model Simulations

The methodology for validating the eMMC signals is outlined in this section. Channel simulations using IBIS models and extracted PCB models are exercised with targeted data attack bit patterns (refer to Section 3.5.2) to generate signal waveforms and eye diagrams. These results are checked for conformity with setup/hold time, slew rate, DCD, and pulse width as defined in the JESD84-B51 specification. Additional checks for performed for ringback with respect to VIH/VIL voltage levels.

3.5.1 Simulation Setup

Setup the IBIS simulation with the following steps:

1. Extract S-parameter files for eMMC signals on the board.
   a. It is okay to use 2.5D extractor for board signals.
2. Obtain the SoC IBIS model at TI.com under the AM62Px product page.
3. Obtain the S-parameter model for the SoC package from your TI representative (provided separately under NDA)
   a. It is required to use the S-parameter SoC package model as the pass/fail checks documented in Section 3.5.5 are derived assuming a system with the S-parameter SoC package model.
   b. Simulations that use the SoC IBIS RLC package model instead of the S-parameter SoC package model produce optimistic results and applicable margin calculations are not available.
   c. The SoC IBIS RLC package model must not be used. Ensure the SoC IBIS model does not have a check mark next to Package Parasitics in the simulation setup.
4. Obtain the eMMC device IBIS model from the eMMC vendor.
   a. This IBIS model should include package RLC model for the eMMC device
5. Build up the simulation netlist as shown in a simulator of your choice.
   a. Set up the system-level schematic in the simulator by connecting the SoC IBIS model, board model, power supplies, and eMMC device IBIS model.
   b. A typical system-level eMMC schematic is shown in Figure 3-2.

6. Build up the process, voltage, temperature corners you are going to simulate
   a. Recommended to simulate across all processes, voltages, temperatures supported by the IBIS model
      - Typical (TT):
        – IO Voltage = 1.8V
        – Temperature = 30C
      - Minimal (SS):
        – IO Voltage = 1.8V * 0.9 = 1.62V
        – Temperature = 125C
      - Maximal (FF):
        – IO Voltage = 1.8V * 1.1 = 1.98V
        – Temperature = -40C
   b. The nominal drive strength specified by JEDEC is 50Ω. However, the customer may try other drive strengths if they are found to yield better signal integrity margins in their simulations.
7. Review Section 3.5.3 and ensure these best practices are being followed prior to running simulations.
8. Use all attack patterns provided in Section 3.5.2 as stimulus for simulations.
9. Analyze the results in a waveform analysis tool and use the pass/fail checks from Section 3.5.5 to assess the quality of results

Do not setup a power-aware simulation. Power supply noise is controlled through Loop Inductance and AC Impedance checks as outlined in previous sections of this document.

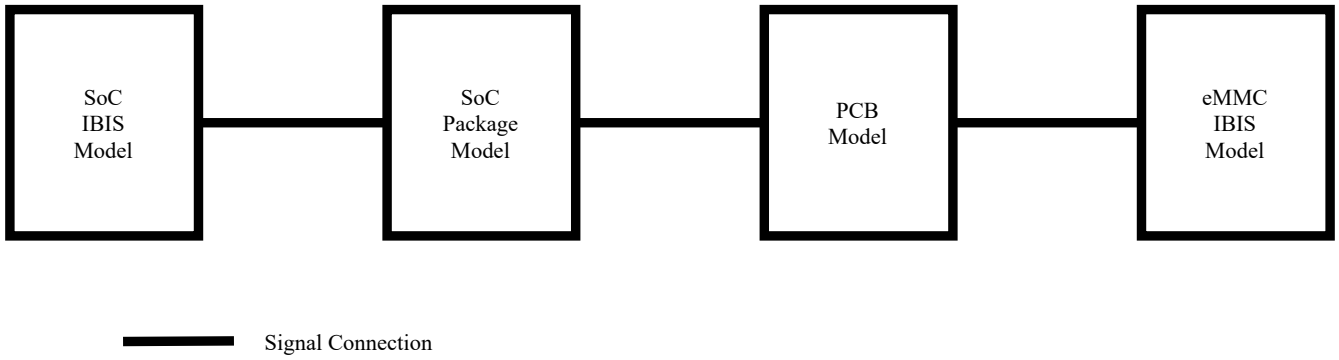

Figure 3-2. Typical System-Level eMMC Schematic

3.5.2 Simulation Bit Patterns

Targeted data attack bit patterns can be downloaded here.

These patterns are designed to exercise the system to real, but worst-case conditions. Each data line uses a separate pattern. All data lines are to be simulated simultaneously. Each bit pattern consists of 6964 bits that concatenate 6 groups of attack patterns described below:

1. 2096 bits - Attack VIH/VIL and attacks at 200MHz and 400MHz
2. 296 bits - Supplemental attack at 200MHz
3. 2124 bits - Worst case ISI/SSO attack pattern - combination of PRBS and ISISSO38 that attacks all 8 bits
4. 296 bits - Supplemental attack at 400MHz
5. 1000 bits - ISI/SSO attack 3-UI 8-bit
6. 1152 bits - PRBS patterns rotated across all 8 bits

3.5.3 Simulation Best Practices

Guidance provided is not specific for any EDA tool. The following list of best practices can be implemented in the simulator of choice by working with the appropriate EDA vendor

- While simulating with S-parameters, it is highly recommended to include options which allow smoothing of the S-parameters to help simulator convergence and result in accurate waveforms
- Timestep and accuracy settings in the simulator need to be set appropriately to enable simulator convergence and result in accurate waveforms
- Extract board signal and board power models up to 5GHz
- Extracted S-parameters need to be checked for causality and passivity. Non-causal or non-passive S-parameters can result in inaccurate results
- It is recommended to perform a short 10 - 15 bit simulation to validate the simulation setup and connectivity, before running the full set of simulations with attack patterns
- It is recommended to check the impedance of the signal traces in the extracted model to ensure that the variations in impedance are within acceptable limits

3.5.4 Simulation Strategy and Examples

An explanation of the simulation strategy and purpose is provided along with details of calculations used to asses whether each parameter in the JESD84-B51 specification is satisfied with positive margin.

Simulate with IBIS models of the SOC and eMMC devices using accurate models for SOC package, board, and eMMC package interconnects. Combine measurements from IBIS simulations with output timing parameters from the TI data sheet to demonstrate timing margin against the JESD84-B51 specification.

TI has performed both power-aware SPICE simulation and the IBIS simulation approach described in this application note with identical systems (SOC model, eMMC model, package models, and board). Measurements from IBIS simulations must include an adjustment from IBIS / SPICE correlation to align the results of the IBIS simulation approach with the power-aware SPICE simulation. This is how the impact of power supply noise is being accounted for in the IBIS simulations. The main intent is to account for any optimism in IBIS simulations with regards to power-aware SPICE simulations. Do not setup a power-aware IBIS simulation since power supply noise is controlled to within an acceptable level through Loop Inductance and AC Impedance checks. Refer to sections Section 3.3 and Section 3.4.

Signal crosstalk on the board and package is accounted for by including all signal traces in the respective S-parameter models extracted for the IBIS simulations.

The SOC IBIS model supports Typical (TT), Minimal (SS), and Maximal (FF) process corners:

- Typical (TT):
  - IO Voltage = 1.8V
  - Core Voltage = 0.85V
- Minimal (SS):
  - IO Voltage = 1.8V * 0.9 = 1.62V
  - Core Voltage = 0.85V * 0.9 = 0.765V
- Maximal (FF):

  - IO Voltage = 1.8V * 1.1 = 1.98V
  - Core Voltage = 0.85V * 1.1 = 0.935V

Setup/Hold Time

Setup and Hold Time for DAT and CMD must satisfy Input setup time and Input hold time parameters in the JESD84-B51 specification. The simulation strategy described below is used to calculate overall margin in the system based on IBIS model simulations. For these calculations Output setup time and Output hold time parameters in the TI data sheet are used.

The Output setup time parameter and Output hold time parameter are defined in the data sheet MMC0 Switching Characteristics – HS400 Mode table. These parameters include the maximum propagation delay mismatch value defined in the MMC0 Timing Conditions table in the TI data sheet. It is important to note that for setup/hold time calculations, the subtraction of the slowest signal slew between VCC/2 and VIL/VIH is required because the TI data sheet timing references for these parameters are from VCC/2 of the DAT or CMD signal transition to VCC/2 of the CLK signal transition while JESD84-B51 defines the setup timing references from VIL or VIH of the DAT or CMD signal transition to VCC/2 of the CLK signal transition.

- E: Overall margin
  - E = (A – B – C) – D
  - E needs to be greater than zero to have margin
  - Perform the overall margin calculations for Data setup, Data hold, CMD setup, and CMD hold using measurements from FF and SS simulations (and the respective FF / SS adjustment from IBIS / SPICE correlation). Consider the result E that gives the least margin when evaluating overall margin. Table 3-2 provides an example of the FF corner, which is the worst case for SK-AM62P-LP (PROC164E2) .
- A: AM62P AC timing specification from the data sheet
  - Output setup time HS4008 (CMD), HS4009 (DAT)
  - Output hold time HS40010 (CMD), HS40011 (DAT)
- B: Worst case rise/fall time from VCC/2 to VIH/VIL for CMD or DAT signal at eMMC device – measured from the IBIS simulation result. Refer to Figure 3-5 and Figure 3-6.
- C: Adjustment from IBIS / SPICE correlation
  - IBIS models are more optimistic with respect to SPICE for setup/hold time calculations
  - • 80ps for FF corner
    • 35ps for SS corner
  - This adjustment needs to be subtracted from overall margin calculation for respective FF or SS corner being simulated
- D: Input set-up time / Input hold time for CMD / DAT as defined in JESD84-B51 specification.

Table 3-2. Example Setup/Hold (FF) Overall Margin Calculation for SK-AM62P-LP (PROC164E2)

Metric	A: AC Timing Specification	B: VCC/2 to VIH/VIL Value (from IBIS simulations)	C: Required additional margin from correlation between SPICE and IBIS	D: JESD84-B51 specification	E: Overall margin
Data (SETUP)	0.70ns (HS4009)	0.150ns	0.080	0.4ns	0.070ns
Data (HOLD)	0.76ns (HS40011)	0.150ns	0.080	0.4ns	0.130ns
CMD (SETUP)	2.86ns (HS4008)	0.124ns	0.080	1.4ns	1.256ns
CMD (HOLD)	1.16ns (HS40010)	0.124ns	0.080	0.8ns	0.156ns

VIH/VIL (Ring-back)

Signals may exhibit ring-back due to reflections, supply noise, crosstalk, and other factors. The simulated CLK signal must be monotonic for both rising and falling transitions in the voltage region between (VIL - 60mV) and (VIH + 60mV). See Figure 3-7. Setup/hold time margins for DAT and CMD may be reduced if ring-back occurs around the VIH/VIL levels. Excessive ring-back can even cause an IO buffer to switch logic states and result in functional fails. Therefore it is important to ensure that any ring-back is simulated and assessed.

IBIS models are more optimistic with respect to SPICE for VIH/VIL ring-back. 60mV is the required adjustment from IBIS / SPICE correlation due to optimism in IBIS simulations with regards to SPICE. This is required to account for the impact of supply noise on ring-back that is included in the SPICE simulations.

The simulation method for IBIS simulations described in Table 3-5 and is used to quantify the impact of ring-back on signal quality and how to adjust setup/hold time margins in the system if ring-back occurs around VIH/VIL levels.

Due to the complex nature of ring-back, it is not possible to determine up-front which process corners will result in worst case ring-back. Therefore, simulations need to be run at least at SS and FF process corners. Voltage thresholds from the JESD84-B51 specification for the respective TT, SS, and FF process corners being simulated in IBIS simulations are below:

- Typical (TT):
  - VIH = 1.8V * 0.65 = 1.170V
  - VIL = 1.8V * 0.35 = 0.630V
- Minimal (SS):
  - VIH = 1.62V * 0.65 = 1.053V
  - VIL = 1.62V * 0.35 = 0.567V
- Maximal (FF):
  - VIH = 1.98V * 0.65 = 1.287V
  - VIL = 1.98V * 0.35 = 0.693V

The 60mV adjustment will need to be applied to the above voltage thresholds to account for optimism in IBIS simulations. Refer to VIH/VIL (Ring-back) in Table 3-5 and see Figure 3-9 and Figure 3-10.

Slew Rates

Slew Rates of all signals measured from VIL to VIH and from VIH to VIL at the eMMC device must be greater than or equal to the Min Slew rate requirement of 1.125V/ns per the Slew Rate parameter in JESD84-B51. Supply noise, crosstalk, and reflections present in the system will impact signal slew rates. IBIS models are more optimistic with respect to SPICE for slew rates due to the additional impact of supply noise being modeled in SPICE.

Due to optimism in IBIS simulations with regards to SPICE a slew rate of 1.45V/ns (JESD84-B51 specification of 1.125V/ns with 30% adjustment from IBIS / SPICE correlation) is required as a sign off for IBIS simulations. See Figure 3-11 and Figure 3-12 for CLK. See Figure 3-13 and Figure 3-14 for DAT/CMD without ring-back. See Figure 3-15 and Figure 3-16 for DAT/CMD with ring-back in the VIH/VIL region where slew rate must be satisfied after 60mV adjustment is applied to VIH/VIL.

DCD

Total DCD must be less than 300ps according to JESD84-B51 specification. The simulation strategy described below is used to calculate overall margin in the system based on IBIS model simulations.

- G: Overall margin
  - G = A - B - C - D - E - F
  - G needs to be greater than zero to have margin
- A: JESD84-B51 specification (Maximum duty cycle distortion tCKDCD: 300ps)
- B: DCD measurement from IBIS simulations
  - Refer to tCKDCD timing definition in JESD84-B51 Figure 88 — HS400 Device Data input timing
  - Plot CLK signal with the trigger in center, one positive and one negative pulse width to left of trigger, and one positive and one negative pulse width to the right of trigger. Refer to Figure 3-17.
  - Measure minimum and maximum CLK pulse widths for both left and right sides of trigger (4 measurements). Consider both positive and negative pulses on each side.
  - Measure between VCC/2 (Vt) crossings with VCC/2 scaled with the IO voltage of the process corner being simulated:
    - Typical (TT): VCC/2 = 1.8V / 2 = 0.90V
    - Minimal (SS): VCC/2 = 1.62V / 2 = 0.81V

    - Maximal (FF): VCC/2 = 1.98V / 2 = 0.99V
  - Start with one end of each measurement at the trigger to avoid double counting CLK jitter
  - Record minimum and maximum pulse widths left and right of the trigger (4 measurements)
  - Subtract the pulse width of the ideal clock from each min/max measurement (2.5ns for 200MHz CLK for HS400)
  - Take the absolute value of each difference
  - DCD is the largest (worst) of the 4 numbers
  - DCD measurement example:
    1. Min Pulse Width (Left): absval(2.387ns - 2.5ns) = 0.113ns
    2. Max Pulse Width (Left): absval(2.618ns - 2.5ns) = 0.118ns (WORST)
    3. Min Pulse Width (Right): absval(2.392ns - 2.5ns) = 0.108ns
    4. Max Pulse Width (Right): absval(2.613ns - 2.5ns) = 0.113ns
    5. DCD = max(0.113ns, 0.118ns, 0.108ns, 0.113ns) = **0.118ns**
- C: Adjustment from IBIS / SPICE correlation for DCD
  - IBIS models are more optimistic with respect to SPICE for DCD calculations
  - 39ps is the adjustment due to optimism in IBIS simulations with regards to SPICE
  - This adjustment needs to be subtracted from overall margin calculation
- D: Adjustment from beta process (SF/FS) corners
  - IBIS model simulations of Typical (TT), Minimal (SS), and Maximal (FF) silicon process variations do not simulate beta process (SF/FS) corners
  - 8ps is the adjustment for beta process (SF/FS) corners
  - This adjustment needs to be subtracted from overall margin calculation
- E: Impact of CLK tree and PHY level shifter
  - IBIS model simulations do not account for DCD contributions of the clock tree and level shifter between the eMMC controller and PHY inside the AM62Px SoC
  - 42ps is the contribution of the clock tree and level shifter between the eMMC controller and PHY
  - This value needs to be subtracted from overall margin calculation
- F: Impact of PLL jitter
  - IBIS model simulations do not account for DCD contributions of the PLL jitter inside the AM62Px SoC
  - 61ps is the contribution of the PLL jitter
  - This value needs to be subtracted from overall margin calculation

Table 3-3. Example DCD Overall Margin Calculation for SK-AM62P-LP (PROC164E2)

A: JESD84-B51 specification	B: DCD measurement from IBIS simulations	C: Adjustment from IBIS / SPICE correlation	D: Adjustment from beta process (SF/FS) corners	E: Impact of CLK tree and PHY level shifter	F: Impact of PLL jitter	G: Overall margin
0.3ns	0.118ns	0.039ns	0.008ns	0.042ns	0.061ns	0.032ns

Pulse Width

Total pulse width must be more than 2.2ns according to JESD84-B51 specification. The simulation strategy described below is used to calculate overall margin in the system based on IBIS model simulations.

- G: Overall margin
  - G = B - A - C - D - E - F
  - G needs to be greater than zero to have margin
- A: JESD84-B51 specification (Minimum pulse width tCKMPW: 2.2ns)
- B: Minimum Pulse Width measurement from IBIS simulations
  - Refer to tCKMPW timing definition in JESD84-B51 Figure 88 — HS400 Device Data input timing.
  - Plot CLK signal with the trigger in center, one positive and one negative pulse width to left of trigger, and one positive and one negative pulse width to the right of trigger. Refer to Figure 3-17.
  - Measure minimum CLK pulse widths for both left and right sides of trigger (2 measurements). Consider both positive and negative pulses on each side.

  - Measure between VCC/2 (Vt) crossings with VCC/2 scaled with the IO voltage of the process corner being simulated:
    - Typical (TT): VCC/2 = 1.8V / 2 = 0.90V
    - Minimal (SS): VCC/2 = 1.62V / 2 = 0.81V
    - Maximal (FF): VCC/2 = 1.98V / 2 = 0.99V
  - Base one end of each measurement at the trigger to avoid double counting CLK jitter
  - Minimum Pulse Width is the smallest (worst) of the two measurements
  - Minimum Pulse Width measurement example:
    1. Min Pulse Width (Left): 2.387ns
    2. Min Pulse Width (Right): 2.392ns
    3. Min Pulse Width = min(2.387ns, 2.392ns) = **2.387ns**
- C: Adjustment from IBIS / SPICE correlation for Pulse Width
  - IBIS models are more optimistic with respect to SPICE for Pulse Width calculations
  - 39ps is the adjustment due to optimism in IBIS simulations with regards to SPICE
  - This adjustment needs to be subtracted from overall margin calculation
- D: Adjustment from beta process (SF/FS) corners
  - IBIS model simulations of Typical (TT), Minimal (SS), and Maximal (FF) silicon process variations do not simulate beta process (SF/FS) corners
  - 8ps is the adjustment for beta process (SF/FS) corners
  - This adjustment needs to be subtracted from overall margin calculation
- E: Impact of CLK tree and PHY level shifter
  - IBIS model simulations do not account for DCD contributions of the clock tree and level shifter between the eMMC controller and PHY inside the AM62Px SoC
  - 42ps is the contribution of the clock tree and level shifter between the eMMC controller and PHY
  - This value needs to be subtracted from overall margin calculation
- F: Impact of PLL jitter
  - IBIS model simulations do not account for DCD contributions of the PLL jitter inside the AM62Px SoC
  - 61ps is the contribution of the PLL jitter
  - This value needs to be subtracted from overall margin calculation

Table 3-4. Example Pulse Width Overall Margin Calculation for SK-AM62P-LP (PROC164E2)

B: Minimum Pulse Width measurement from IBIS simulations	A: JESD84-B51 specification	C: Adjustment from IBIS / SPICE correlation	D: Adjustment from beta process (SF/FS) corners	E: Impact of CLK tree and PHY level shifter	F: Impact of PLL jitter	G: Overall margin
2.387ns	2.2ns	0.039ns	0.008ns	0.042ns	0.061ns	0.037ns

3.5.5 Pass/Fail Checks

Table 3-5 below describes the setup/hold time, slew rate, DCD, and pulse width checks for conformity to the JESD84-B51 specifications. An additional ring-back check ensures signals satisfy the VIH/VIL voltage level requirements. Each check is detailed separately for CLK, DATA, and CMD, as applicable. For the JEDEC checks, refer to JESD84-B51 Table 212 - HS200 Device Input Timing (JESD84-B51 Section 10.8.2) and Table 215 - HS400 Device Input Timing (JESD84-B51 Section 10.10.1).

Table 3-5. Pass/Fail Checks

Parameter	CLK	DATA	CMD
Setup/Hold Time	• NA	• Run simulations with IBIS models in non-power-aware mode and profile results • Apply 1/4 clock cycle delay to the DAT[7:0] signals relative to the CLK signal (see Figure 3-3). • Use appropriate Output setup time or Output hold time from the data sheet Switching Characteristics timing table. For example, the Output setup time (HS4009) when checking setup margin and use the Output hold time (HS40011) when checking hold time margin. • **Setup time:** Overall Margin E = (A – B – C) – D, Subtract the following three values from the data sheet min output setup time parameter (A) to determine if there is enough margin for the setup requirement of the attached device: – B: Slowest simulated DAT signal slew measured from VCC/2 to VIH on rising transitions (see Figure 3-5) or VCC/2 to VIL on falling transitions (see Figure 3-6) at the BGA of the attached eMMC device.(4) – C: Adjustment from IBIS / SPICE correlation: (3) • 80ps for FF corner • 35ps for SS corner – D: 400ps setup time required by the attached eMMC device (per the JESD84-B51 standard(1)) • After subtracting these three values from the data sheet min output setup time value, the Overall Margin (E) needs to be positive to pass • **Hold time:** Overall Margin E = (A – B – C) – D, Subtract the following three values from the data sheet min output hold time parameter (A) to determine if there is enough margin for the hold requirement of the attached device:	• Run simulations with IBIS models in non-power-aware mode and profile results • Apply 1/4 clock cycle + 400ps delay to the CMD signal relative to each rising CLK transition (see Figure 3-4). • Use appropriate Output setup time or Output hold time from the data sheet Switching Characteristics timing table. For example, the Output setup time (HS4008) when checking setup margin and use the Output hold time (HS40010) when checking hold time margin. • **Setup time:** Overall Margin E = (A – B – C) – D, Subtract the following three values from the data sheet min output setup time parameter to determine if there is enough margin for the setup requirement of the attached device: – B: Slowest simulated CMD signal slew measured from VCC/2 to VIH on rising transitions (see Figure 3-5) or VCC/2 to VIL on falling transitions (see Figure 3-6) at the BGA of the attached eMMC device.(4) – C: Adjustment from IBIS / SPICE correlation:(3) • 80ps for FF corner • 35ps for SS corner – D: 1400ps setup time required by the attached eMMC device (per the JESD84-B51 standard(2)) • After subtracting these three values from the data sheet min output setup time value, the Overall Margin (E) needs to be positive to pass • **Hold time:** Overall Margin E = (A – B – C) – D, Subtract the following three values from the data sheet min output hold time parameter to determine if there is enough margin for the hold requirement of the attached device:

Table 3-5. Pass/Fail Checks (continued)

Parameter	CLK	DATA	CMD
		– B: Slowest simulated DAT signal slew measured from VIL to VCC/2 on rising transitions (see Figure 3-5) or VIH to VCC/2 on falling transitions (see Figure 3-6) at the BGA of the attached eMMC device.(4) – C: Adjustment from IBIS / SPICE correlation: (3) • 80ps for FF corner • 35ps for SS corner – D: 400ps hold time required by the attached eMMC device (per the JESD84-B51 standard(1)) • After subtracting these three values from the data sheet min output hold time value, the Overall Margin (E) needs to be positive to pass	– B: Slowest simulated CMD signal slew measured from VIL to VCC/2 on rising transitions (see Figure 3-5) or VIH to VCC/2 on falling transitions (see Figure 3-6) at the the BGA of attached eMMC device.(4) – C: Adjustment from IBIS / SPICE correlation:(3) • 80ps for FF corner • 35ps for SS corner – D: 800ps hold time required by the attached eMMC device (per the JESD84-B51 standard(2)) • After subtracting these three values from the data sheet min output hold time value, the Overall Margin (E) needs to be positive to pass
VIH/VIL (Ring-back)	• Run simulations with IBIS models in non-power aware mode and profile results • Ensure the simulated CLK signal remains monotonic for both rising and falling transitions in the voltage region between (VIL - 60mV)(3) and (VIH + 60mV)(3). • Also ensure the simulated CLK signal rising transition rises above (VIH + 60mV)(3) and remains above (VIH + 60mV)(3) until the next falling transition, where the falling transition falls below (VIL - 60mV)(3) and remains below (VIL - 60mV)(3) until the next rising transition. • The CLK signal may be non-monotonic outside the voltage region between (VIL - 60mV)(3) and (VIH + 60mV)(3). See example in Figure 3-7). • The CLK signal **must not** be non-monotonic between (VIL - 60mV)(3) and (VIH + 60mV)(3). See example in Figure 3-8).	• Run simulations with IBIS models in non-power aware mode and profile results • Ensure the simulated DAT signal rising transitions rises above VIH and falling transitions fall below VIL with enough timing margin to pass the setup test described above in Setup/Hold Time Pass/ Fail Checks. • If the simulated DAT signal has ring-back, the slowest simulated DAT signal slew component used in above setup time calculation needs to be measured from the last crossing above (VIH + 60mV)(3) for rising edge transitions or below (VIL - 60mV)(3) for falling edge transitions. • See an example of this slew measurement on a rising DAT signal with ring-back in Figure 3-9 and on a falling DAT signal with ring-back in Figure 3-10	• Run simulations with IBIS models in non-power aware mode and profile results • Ensure the simulated CMD signal rising transitions rises above VIH and falling transitions fall below VIL with enough timing margin to pass the setup test described above in Setup/Hold Time Pass/ Fail Checks. • If the simulated CMD signal has ring-back, the slowest simulated CMD signal slew component used in above setup time calculation needs to be measured from the last crossing above (VIH + 60mV)(3) for rising edge transitions or below (VIL - 60mV)(3) for falling edge transitions. • See an example of this slew measurement on a rising CMD signal with ring-back in Figure 3-9 and on a falling CMD signal with ring-back in Figure 3-10

Table 3-5. Pass/Fail Checks (continued)

Parameter	CLK	DATA	CMD
Slew Rates	• Run simulations with IBIS models in non-power aware mode and profile results • Ensure the simulated CLK signal Slew Rates measured from VIL to VIH on rising transitions and measured from VIH to VIL on falling transitions at the attached eMMC device is greater to or equal to the Min Slew rate requirement of **1.45V/ns** (1.125V/ns per the Slew Rate in JESD84-B51 with 30% additional margin required for IBIS simulations[3]) • Refer to Input CLK Slew Rate in JESD84-B51 Table 215 — HS400 Device input timing. • Examples of passing and failing slew rates are shown for rising CLK signals in Figure 3-11 and falling CLK signals in Figure 3-12	• Run simulations with IBIS models in non-power aware mode and profile results • Ensure the simulated DAT signal Slew Rates measured from VIL to VIH on rising transitions and measured from VIH to VIL on falling transitions at the attached eMMC device is greater to or equal to the Min Slew rate requirement of **1.45V/ns** (1.125V/ns per the Slew Rate in JESD84-B51 with 30% additional margin required for IBIS simulations[3]) • If the simulated DAT signal has ring-back, then ensure the simulated DAT signal Slew Rates measured from VIL to (VIH + 60mV)[3] on rising transitions and measured from VIH to (VIL - 60mV)[3] on falling transitions at the attached eMMC device is greater to or equal to the Min Slew rate requirement of **1.45V/ns** (1.125V/ns per the Slew Rate in JESD84-B51 with 30% additional margin required for IBIS simulations[3]) • Refer to Input DAT Slew Rate in JESD84-B51 Table 215 — HS400 Device input timing. • Examples of passing and failing slew rates are shown for rising DAT signals in Figure 3-13 and falling DAT signals in Figure 3-14 • Examples of passing and failing slew rates are shown for rising DAT signals with ring-back in Figure 3-15 and falling DAT signals with ring-back in Figure 3-16	• NA

Table 3-5. Pass/Fail Checks (continued)

Parameter	CLK	DATA	CMD
DCD	• Run simulations with IBIS models in non-power aware mode and profile results • Overall Margin G = A - B - C - D - E - F, Subtract the following values from the worst simulated CLK signal duty cycle distortion measurement (B) to determine if there is enough margin: – A: JESD84-B51 specification (tCKDCD max 300ps) – B: DCD measurement from IBIS simulations – refer to tCKDCD timing definition in JESD84-B51 Figure 88 — HS400 Device Data input timing. Refer also to Section 3.5.4 – C: Adjustment from IBIS / SPICE correlation for DCD (39ps)(3) – D: Adjustment from beta process (SF/FS) corners (8ps) – E: Impact of CLK tree and PHY level shifter (42ps) – F: Impact of PLL jitter (61ps) – After subtracting these values from the measured DCD, the Overall Margin (G) needs to be positive to pass • Refer to tCKDCD timing in JESD84-B51 Table 215 — HS400 Device input timing and Figure 88 — HS400 Device Data input timing. • Refer also to Figure 3-17	• NA	• NA

Table 3-5. Pass/Fail Checks (continued)

Parameter	CLK	DATA	CMD
Pulse Width	• Run simulations with IBIS models in non-power aware mode and profile results • Overall Margin G = B - A - C - D - E - F, Subtract the following values from the worst simulated CLK pulse width measurement (B) to determine if there is enough margin: – B: Pulse Width from IBIS simulations – refer to tCKMPW timing definition in JESD84-B51 Figure 88 — HS400 Device Data input timing. Refer also to Section 3.5.4 – A: JESD84-B51 specification (Min tCKMPW: 2.2ns) – C: Adjustment from IBIS / SPICE correlation for Pulse Width (39ps)(3) – D: Adjustment from beta process (SF/FS) corners (8ps) – E: Impact of CLK tree and PHY level shifter (42ps) – F: Impact of PLL jitter (61ps) – After subtracting these values from the measured pulse width, the Overall Margin (G) needs to be positive to pass • Refer to tCKMPW timing in JESD84-B51 Table 215 — HS400 Device input timing and Figure 88 — HS400 Device Data input timing. • Refer also to Figure 3-17	• NA	• NA

(1) JEDEC HS400 Specification refers to Table 215 - HS400 Device Input Timing (eMMC JESD84-B51 Section 10.10.1).
(2) JEDEC HS200 Specification refers to Table 212 - HS200 Device Input Timing (eMMC JESD84-B51 Section 10.8.2).
(3) Results from IBIS simulations require adjustment from IBIS / SPICE correlation (IBIS simulation results are optimistic when compared to SPICE simulation results).
(4) For setup/hold time calculations, the subtraction of the slowest signal slew between VCC/2 and VIL/VIH is required because the TI data sheet timing references for these parameters are from VCC/2 of the DAT or CMD signal transition to VCC/2 of the CLK signal transition while JESD84-B51 defines the setup timing references from VIL or VIH of the DAT or CMD signal transition to VCC/2 of the CLK signal transition.

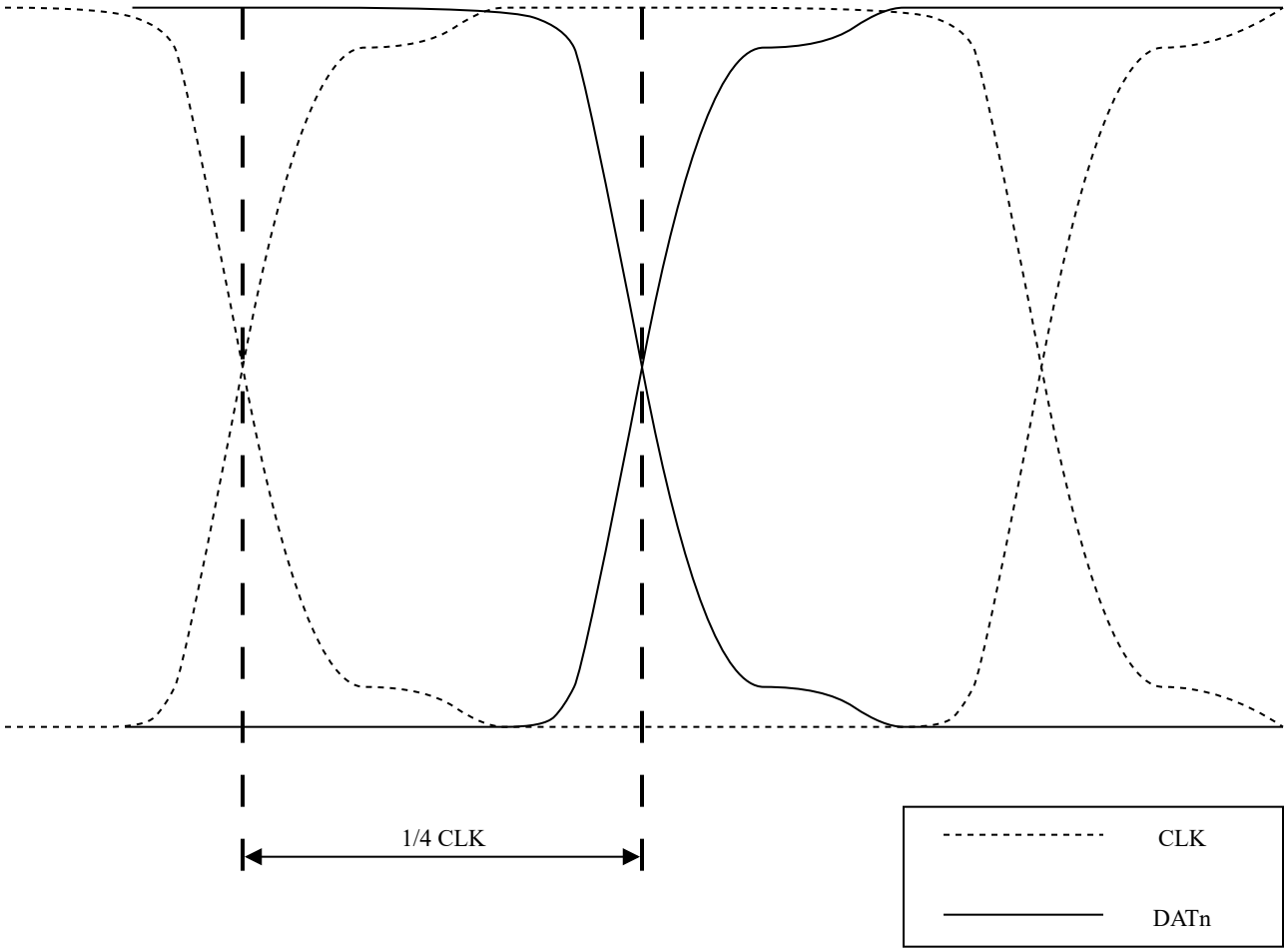

Figure 3-3. Setup/Hold Time: CLK to DATA Offset 1/4 CLK Cycle Delay

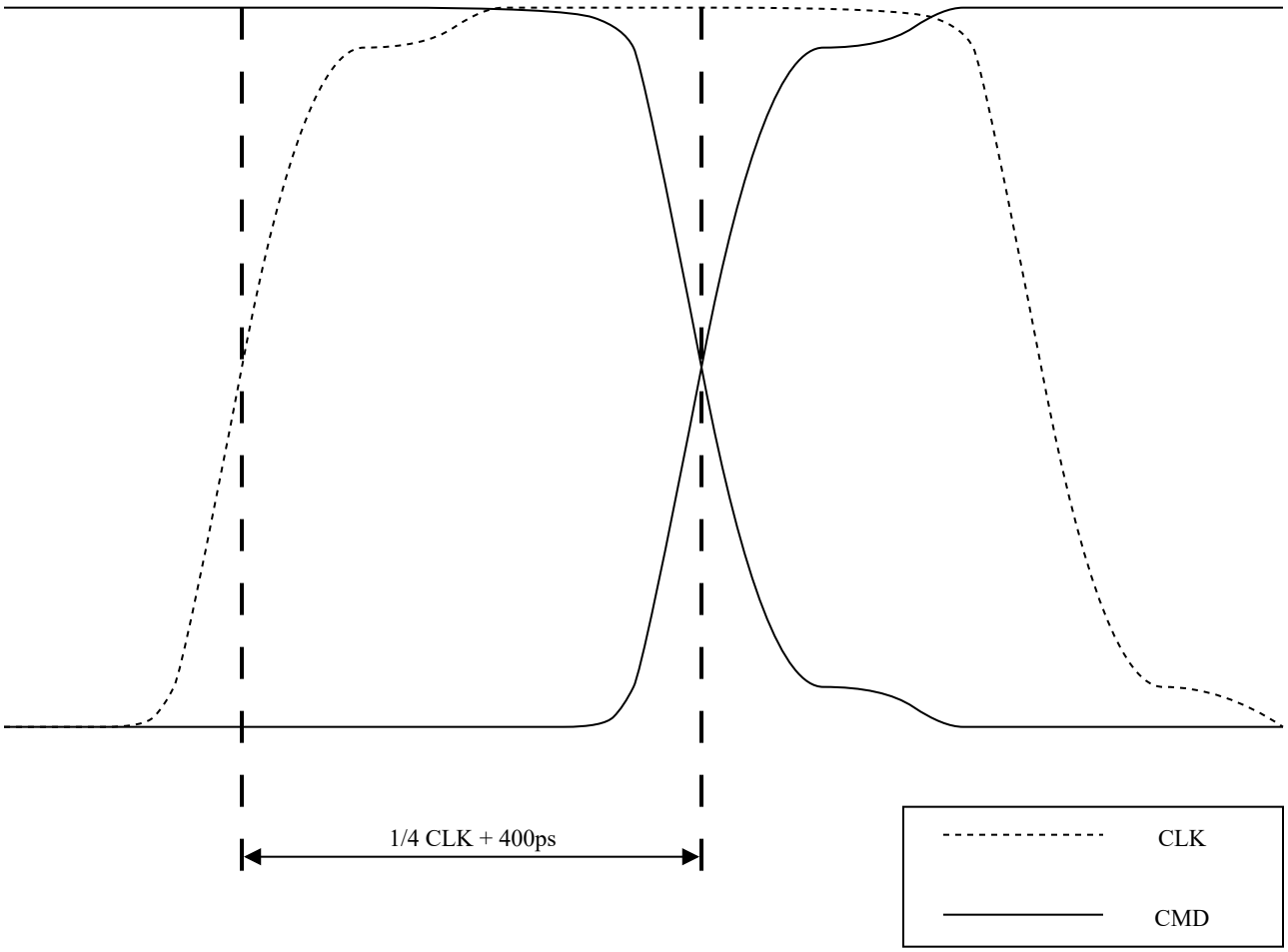

Figure 3-4. Setup/Hold Time: CLK to CMD Offset 1/4 CLK Cycle + 400ps Delay

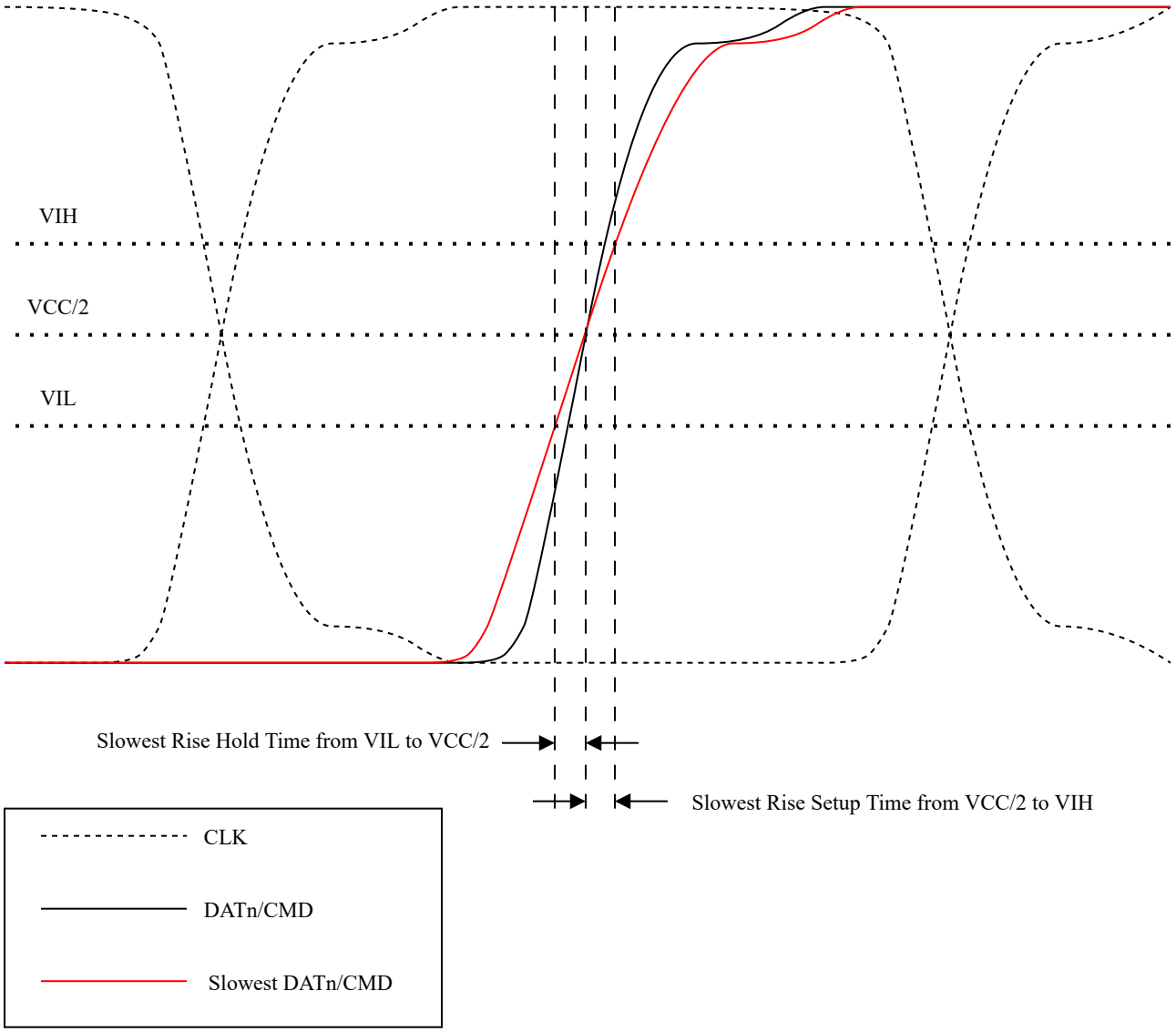

Figure 3-5. Setup/Hold Time: Slowest DATn/CMD Rising Edge Slew VCC/2 to VIH (Setup) and VIL to VCC/2 (Hold)

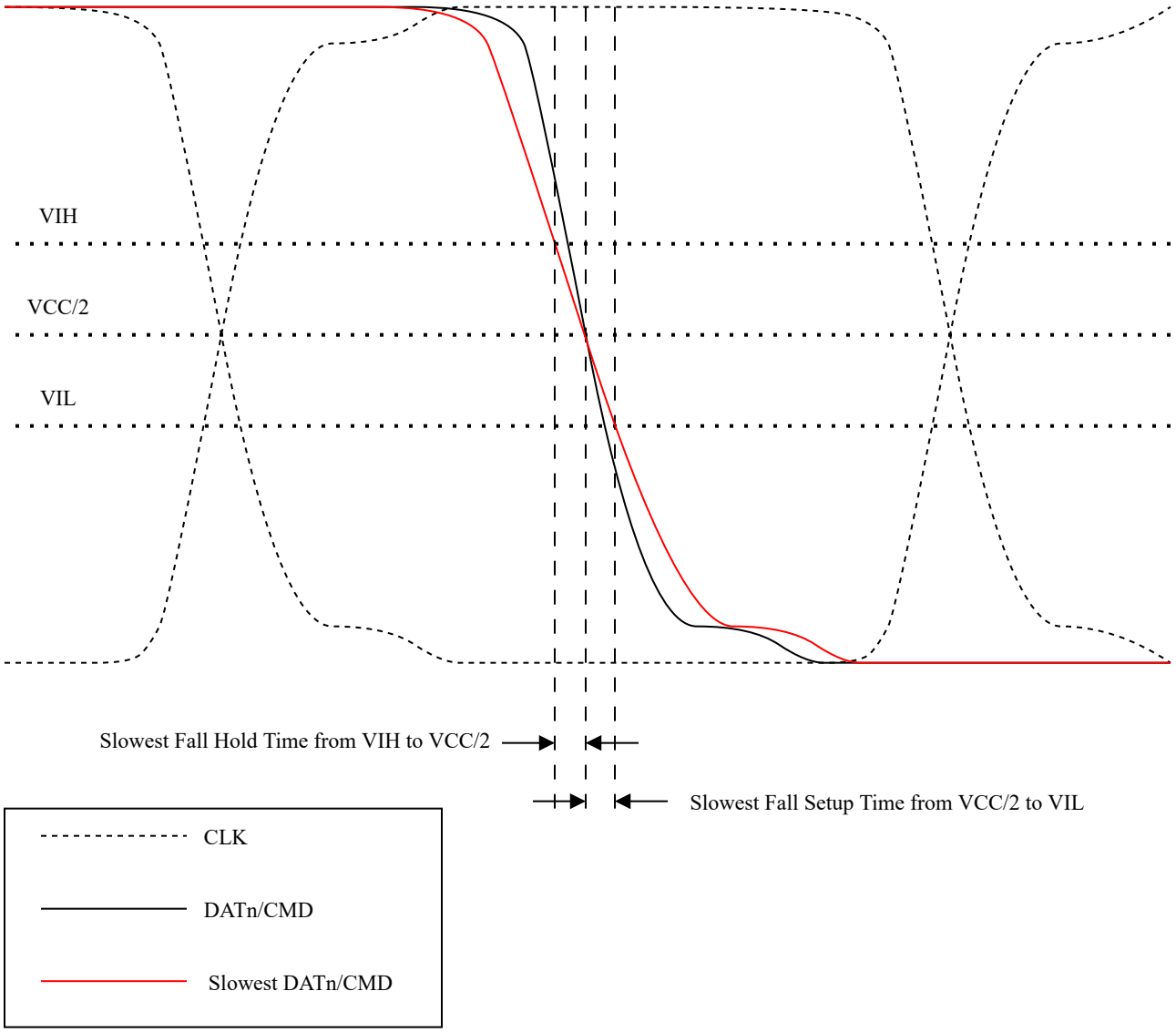

Figure 3-6. Setup/Hold Time: Slowest DATn/CMD Falling Edge Slew VCC/2 to VIL (Setup) and VIH to VCC/2 (Hold)

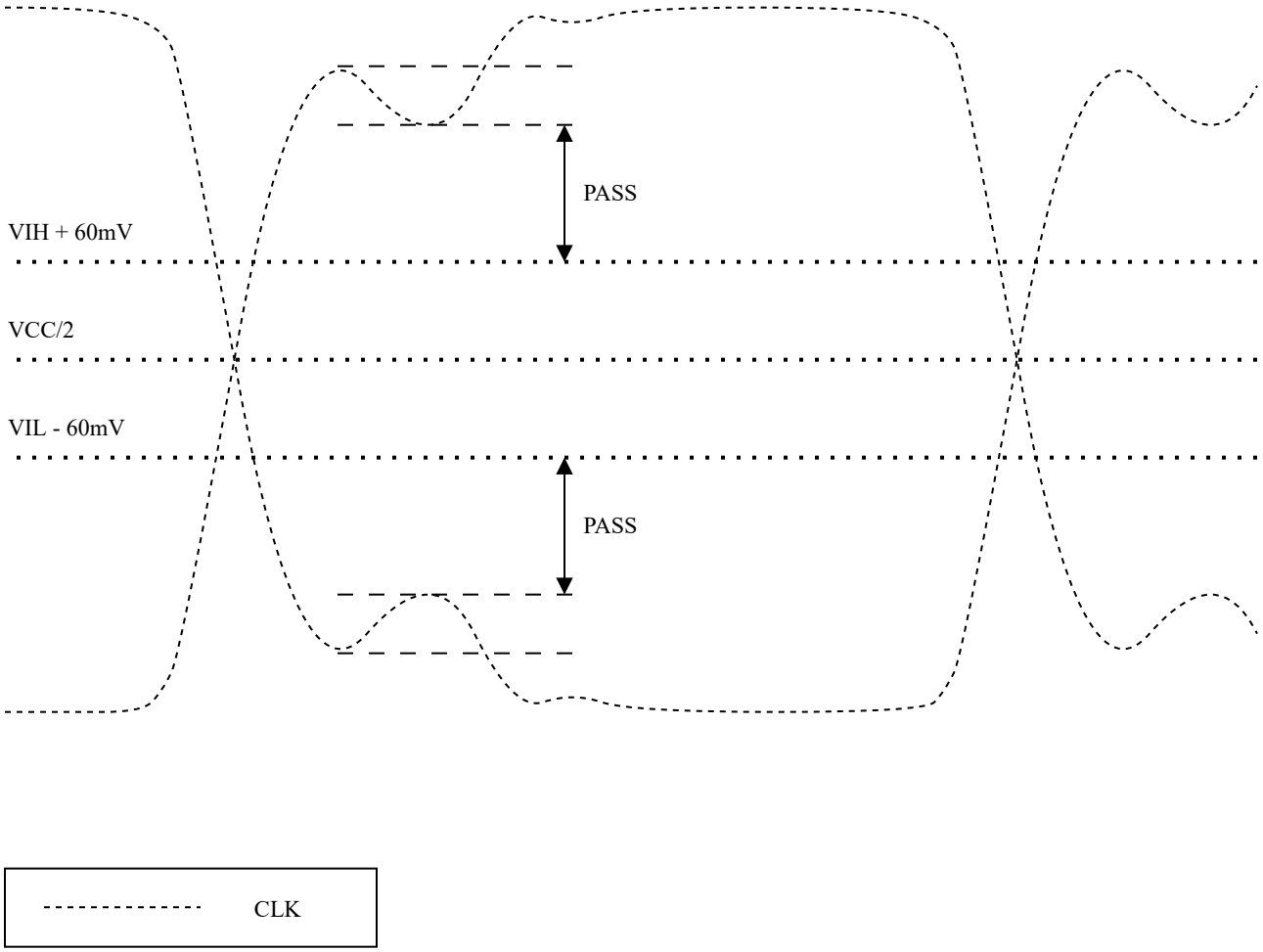

Figure 3-7. VIH/VIL: Non-monotonic CLK Good Example (Monotonic in VIL - 60mV to VIH + 60mV Range)

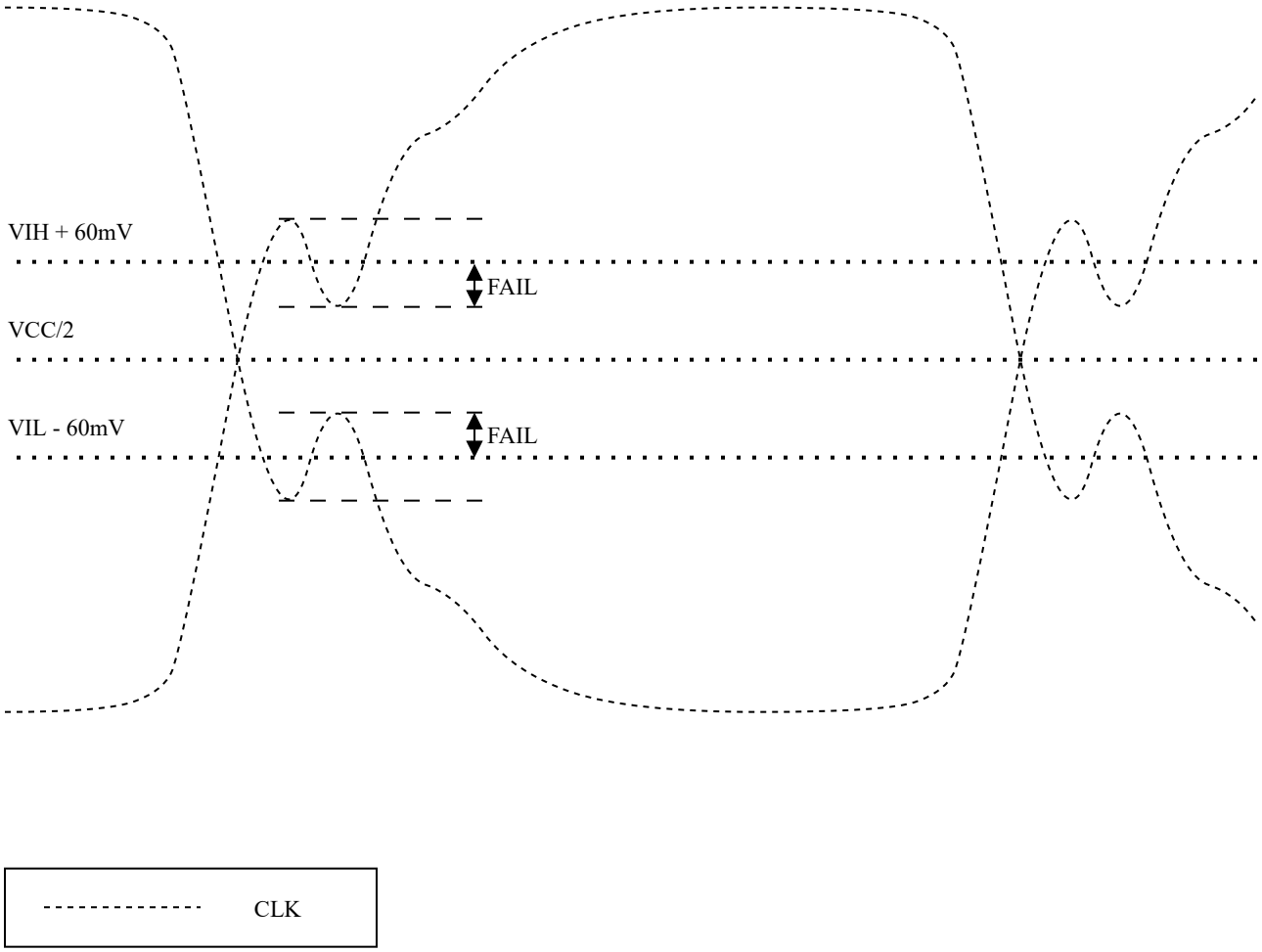

Figure 3-8. VIH/VIL: Non-monotonic CLK Bad Example (Non-monotonic in VIL - 60mV to VIH + 60mV Range)

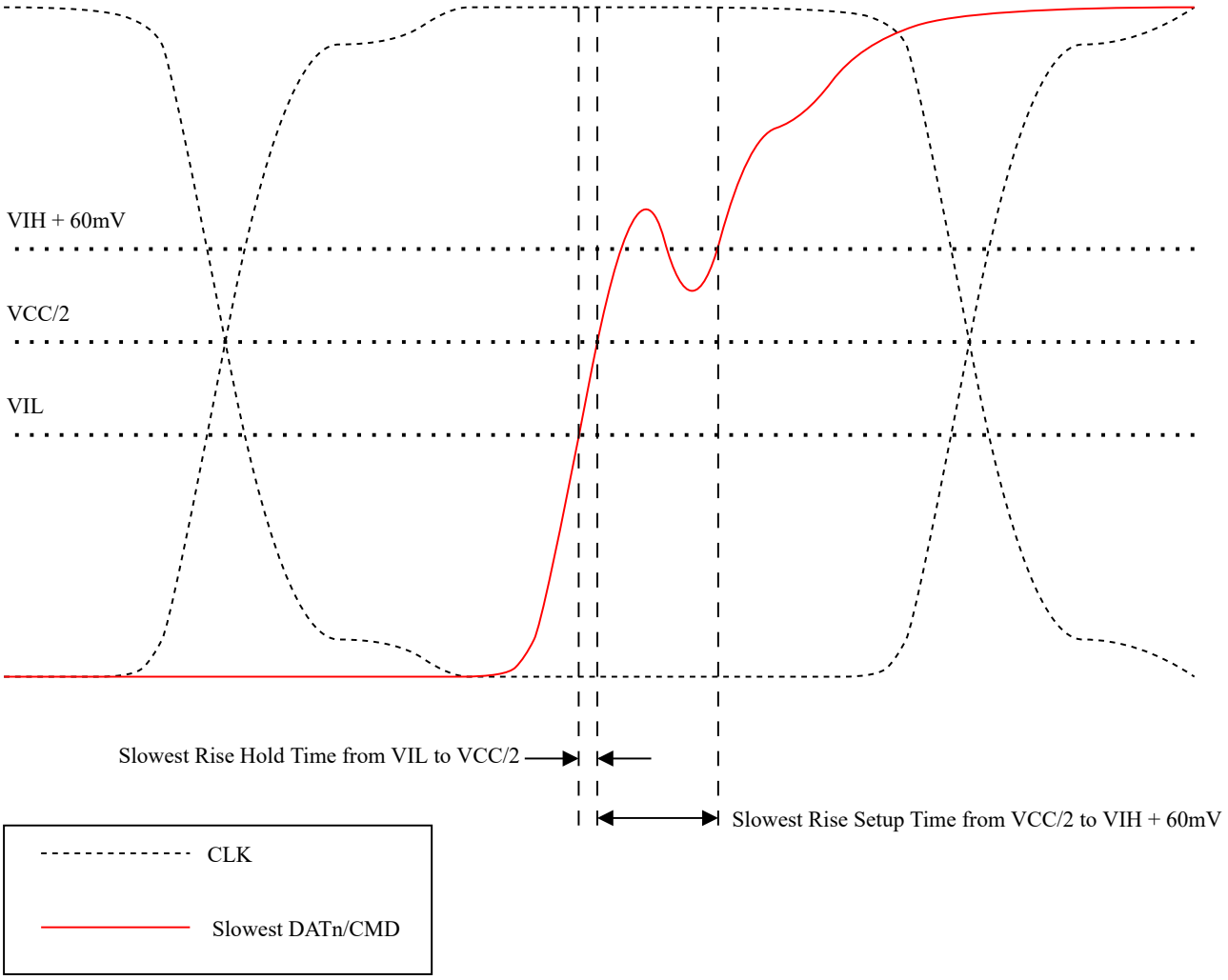

Figure 3-9. VIH/VIL: Slowest DATn/CMD Rising Edge Slew with Ring-Back (Measure to Last VIH + 60mV Crossing Before Next Capture CLK Edge)

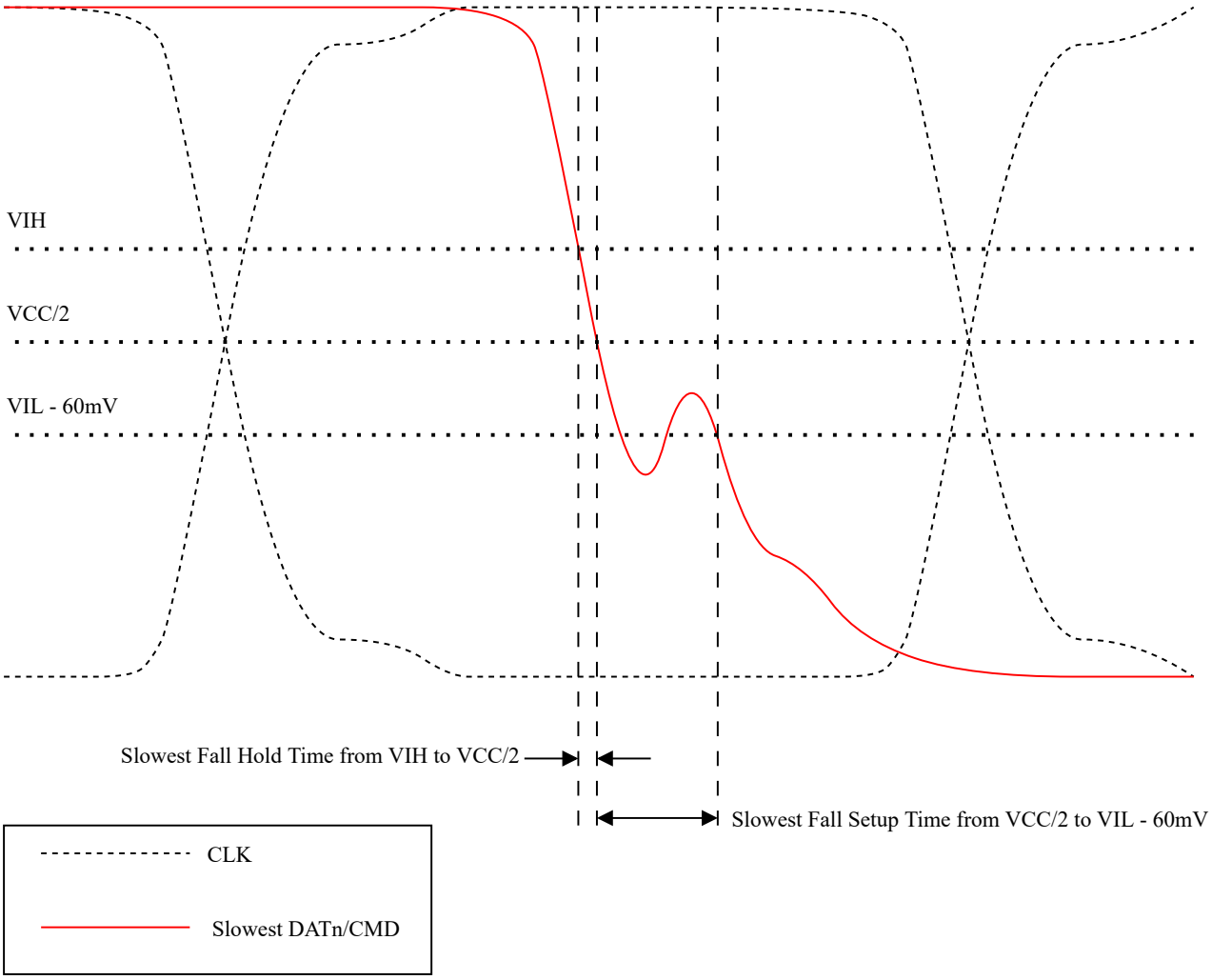

Figure 3-10. VIH/VIL: Slowest DATn/CMD Falling Edge Slew with Ring-Back (Measure to Last VIL - 60mV Crossing Before Next Capture CLK Edge)

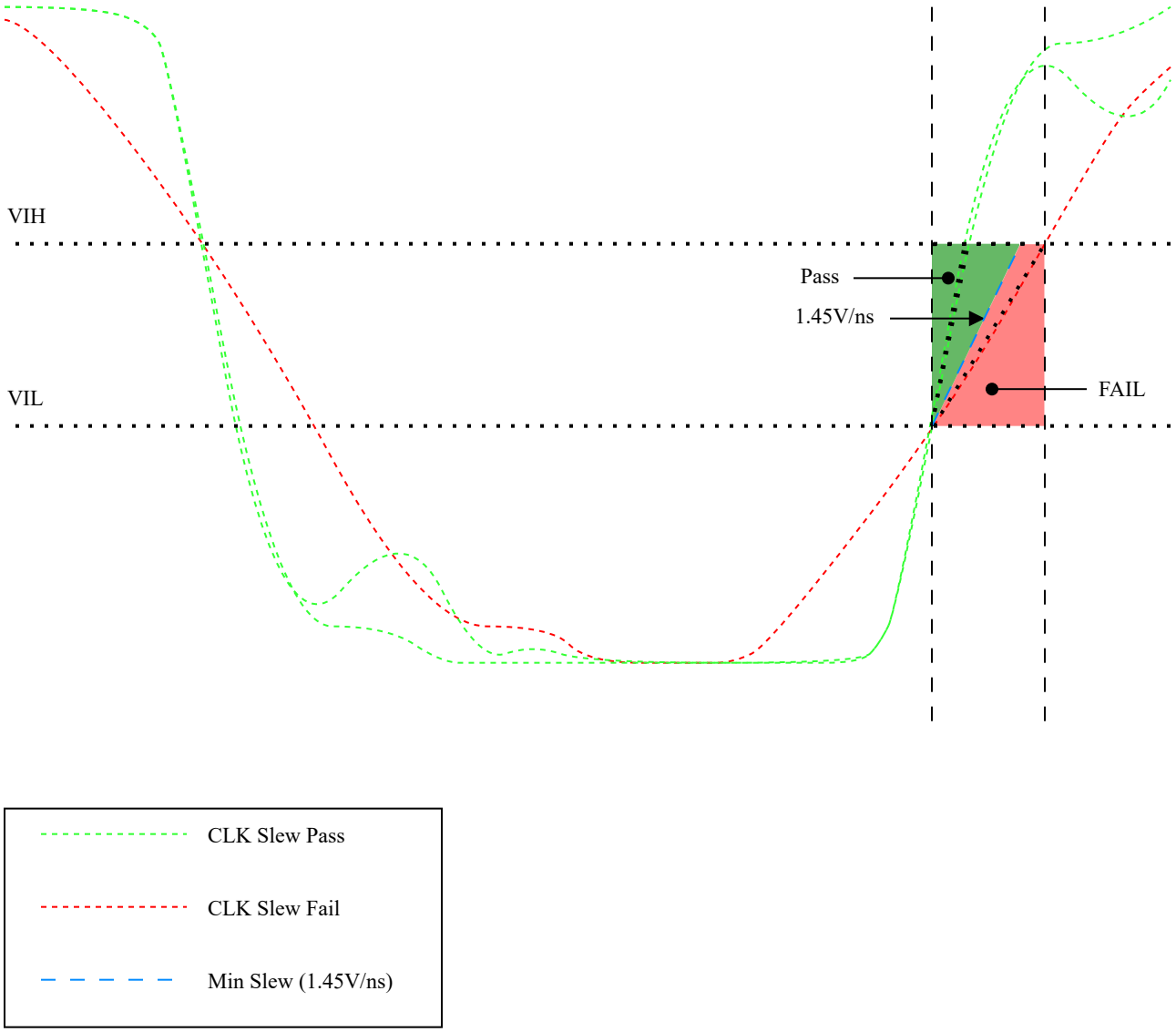

Figure 3-11. Slew Rates: CLK Rising Edge - Slew Rate Between VIL and VIH Must Be Faster than 1.45V/ns

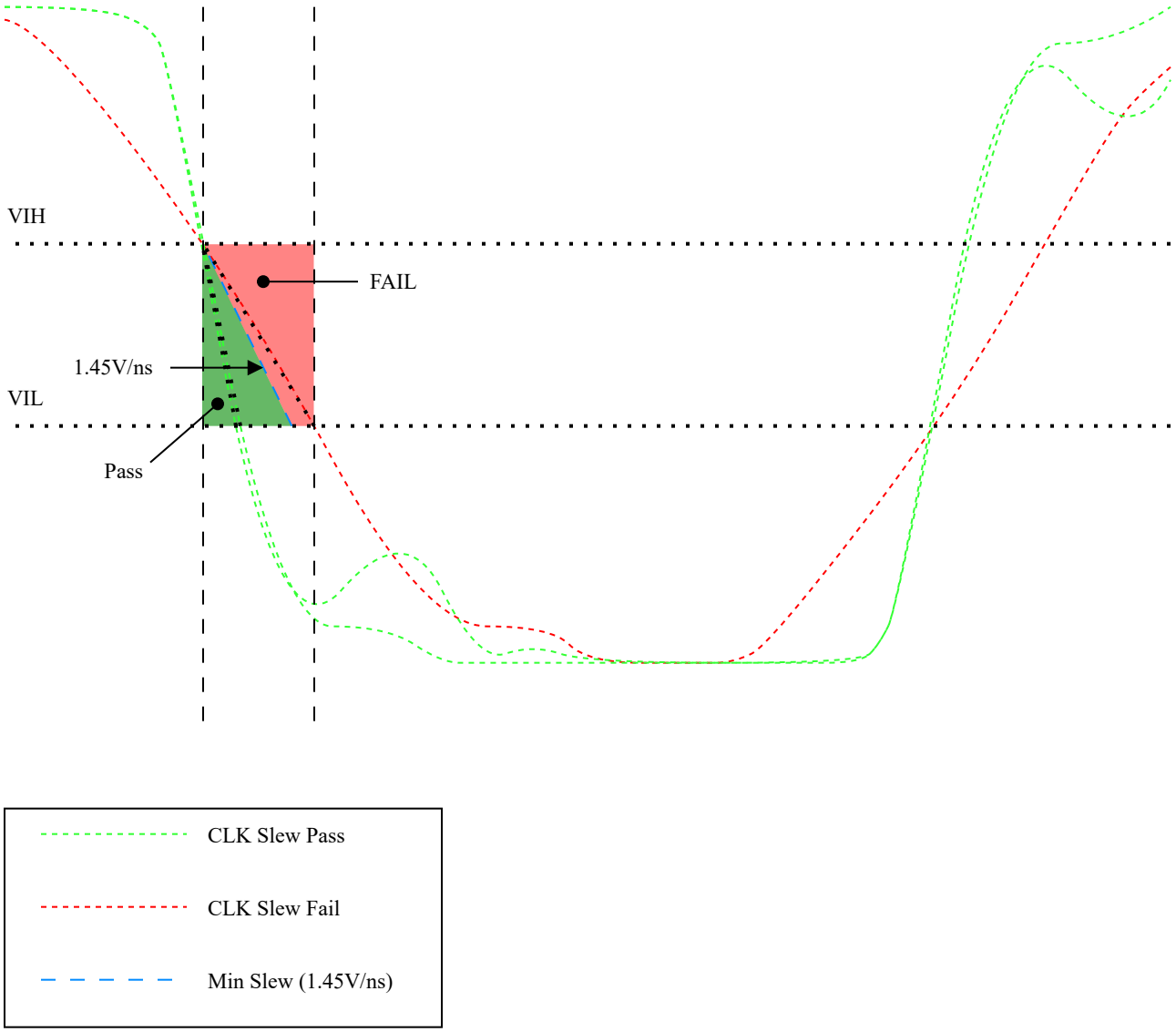

Figure 3-12. Slew Rates: CLK Falling Edge - Slew Rate Between VIH and VIL Must Be Faster than 1.45V/ns

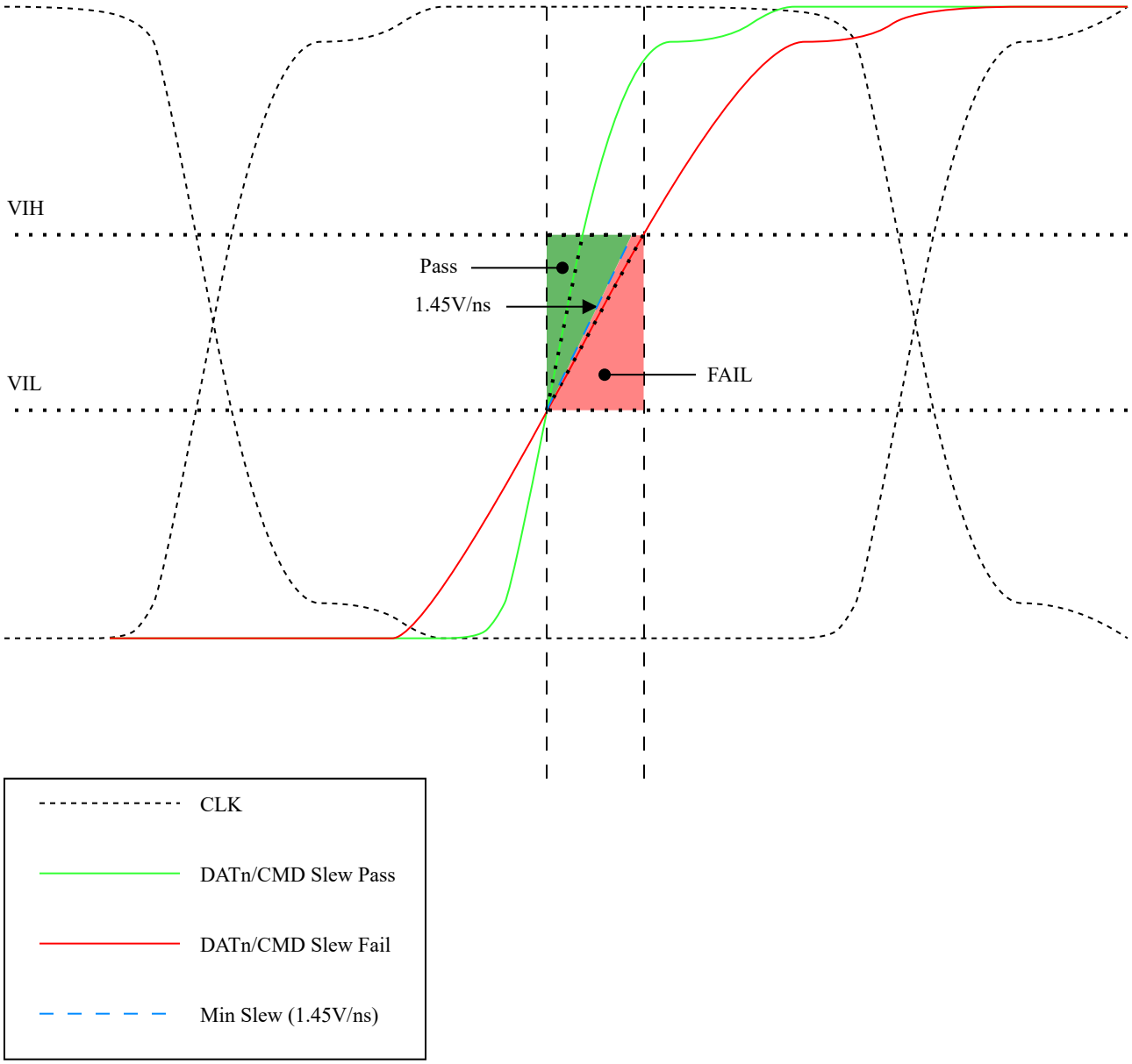

Figure 3-13. Slew Rates: DATn/CMD Rising Edge - Slew Rate Between VIL and VIH Must Be Faster than 1.45V/ns

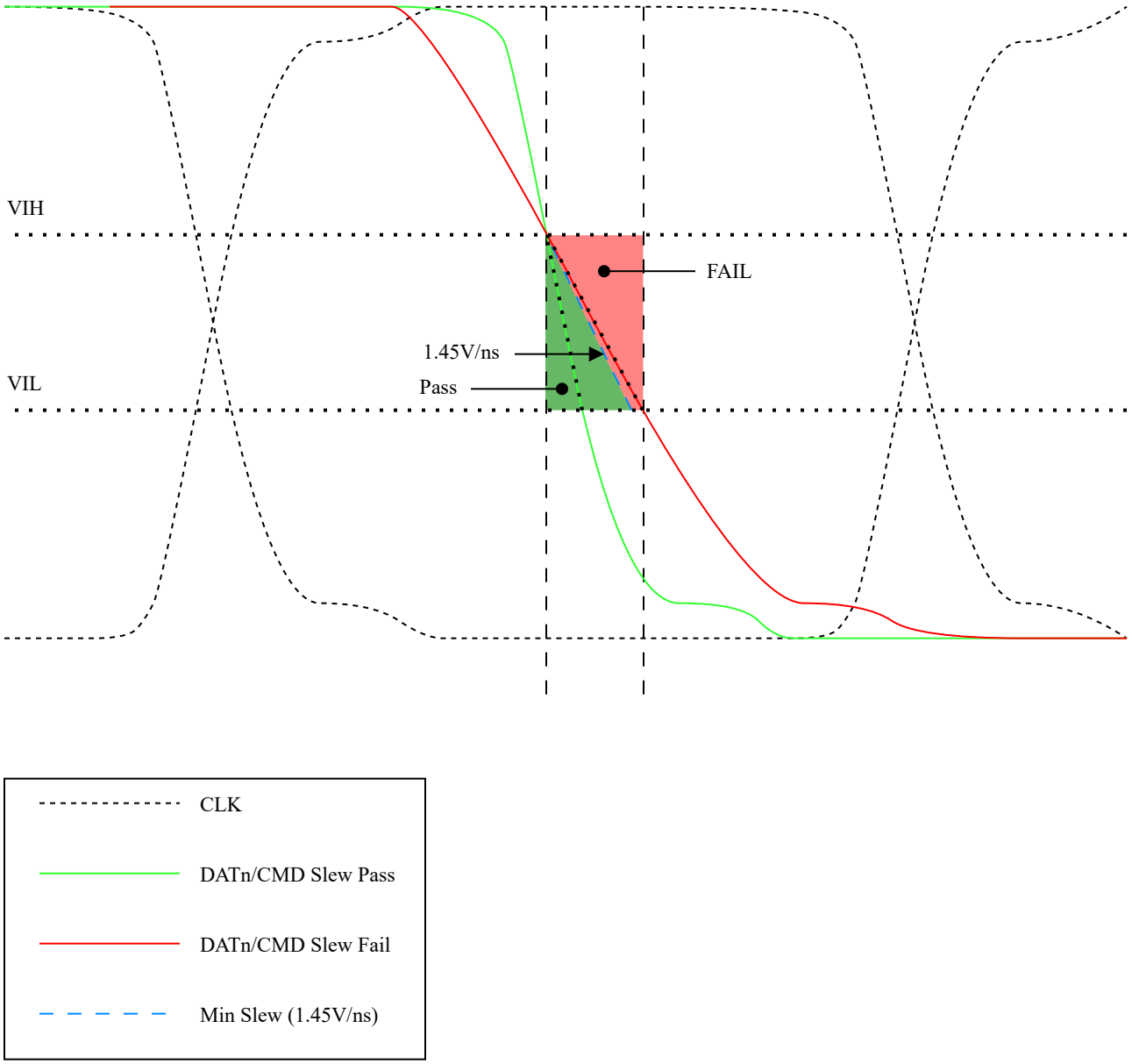

Figure 3-14. Slew Rates: DATn/CMD Falling Edge - Slew Rate Between VIH and VIL Must Be Faster than 1.45V/ns

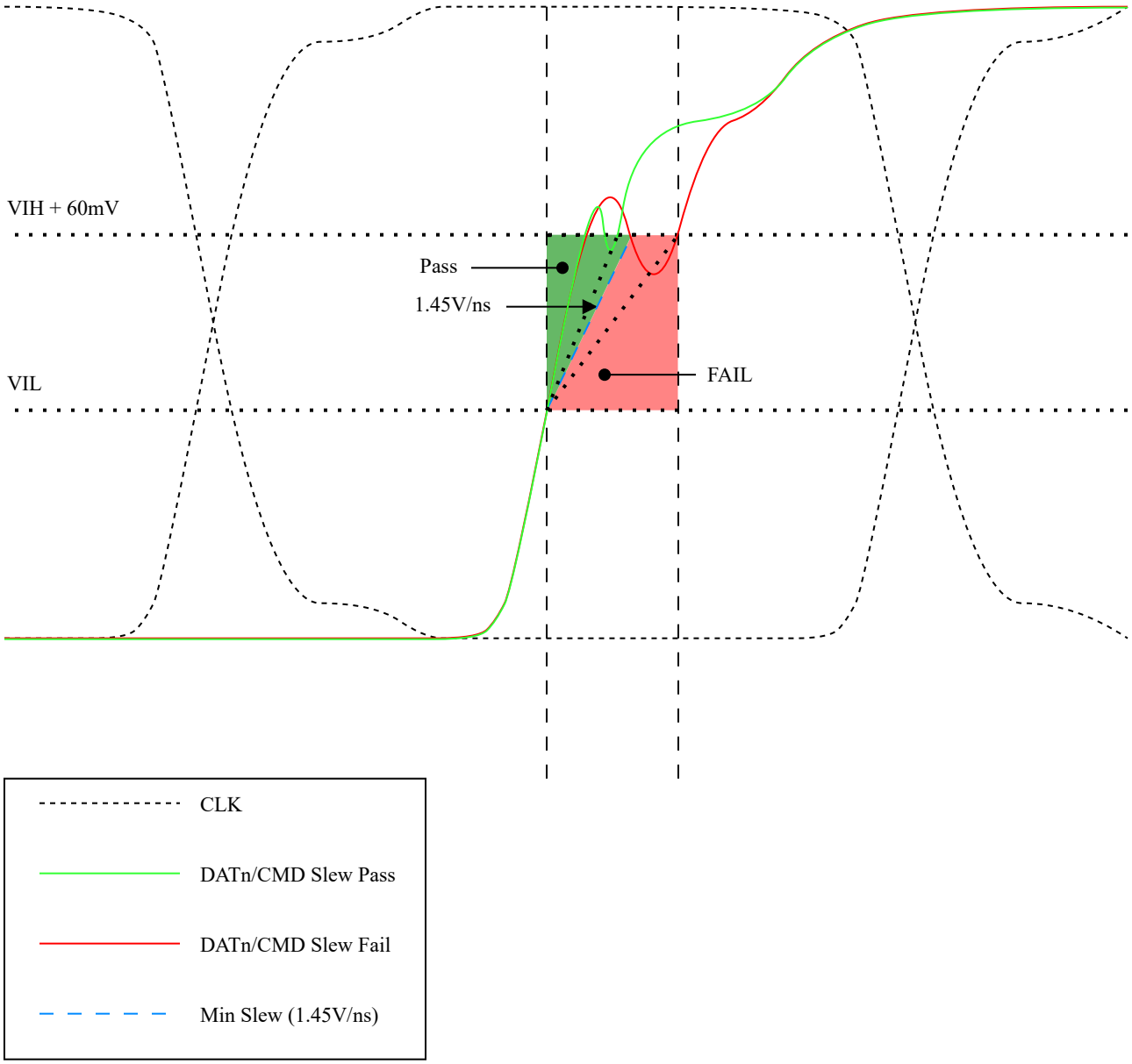

Figure 3-15. Slew Rates: DATn/CMD Rising Edge with Ring-Back - Slew Rate Between VIL and VIH + 60mV Must Be Faster than 1.45V/ns

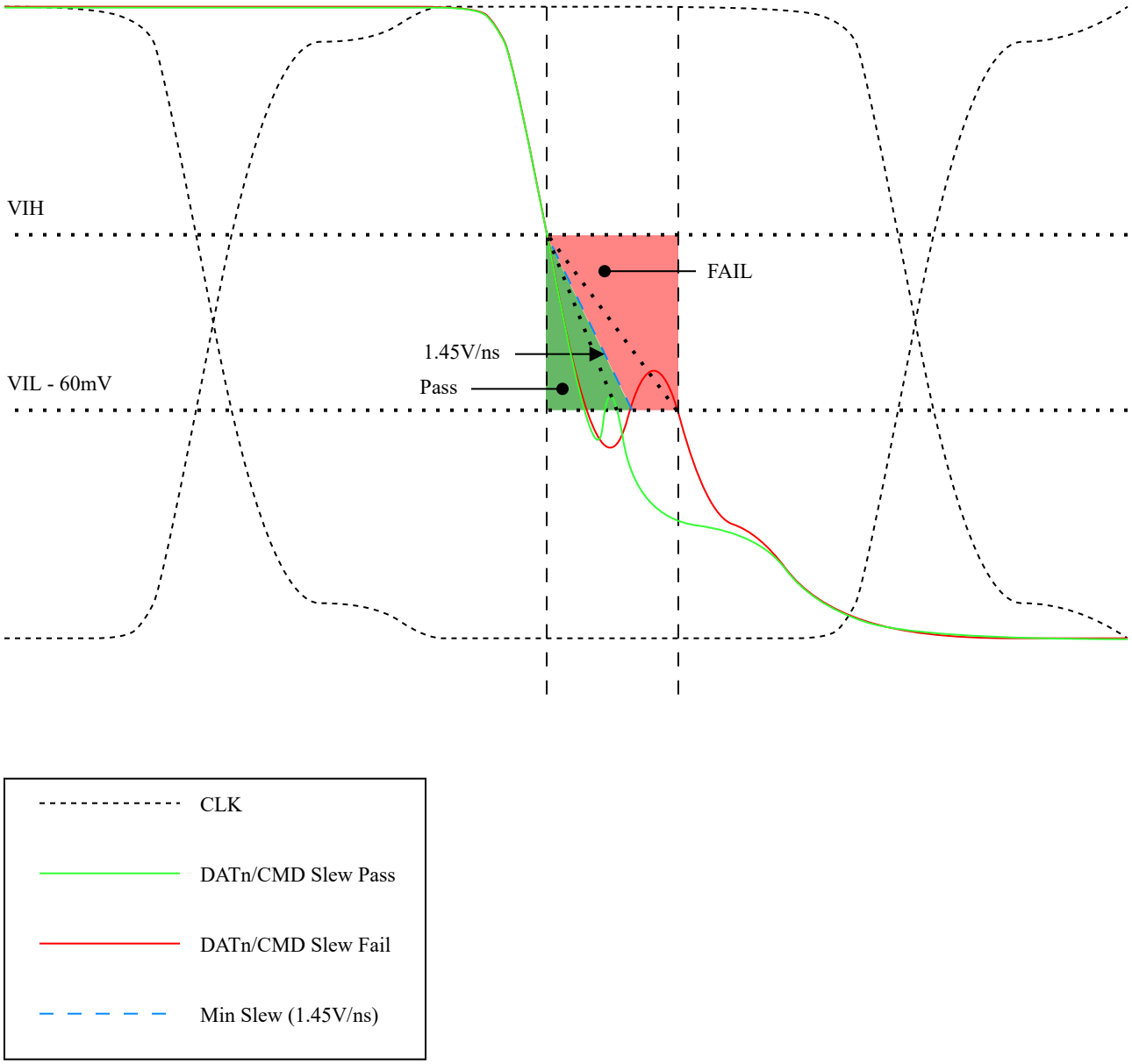

Figure 3-16. Slew Rates: DATn/CMD Falling Slew with Ring-Back - Slew Rate Between VIH and VIL - 60mV Must Be Faster than 1.45V/ns

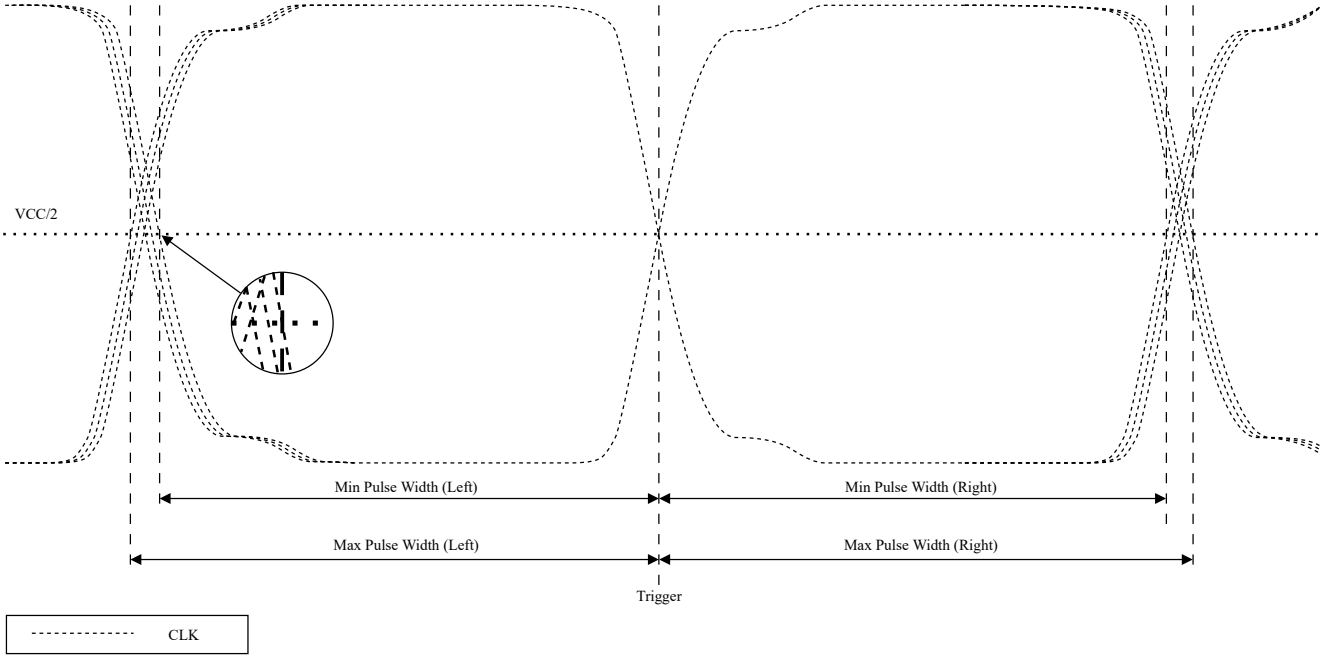

Figure 3-17. Measuring Pulse Width for DCD and Pulse Width Measurements

Note

VCC/2 scales with the IO voltage for TT, SS, FF corner being simulated.

4 Design Example

This section documents the stack-up, power routing, and signal routing implemented in the SK-AM62P-LP (PROC164E2) . This design has been simulated by TI and shown to have positive margin against the pass/fail checks documented in Section 3.5.5. This design can be used as a baseline reference for AM62Px eMMC designs.

4.1 Stack-Up

These guidelines recommend a 10- or 12-layer PCB stack-up for full device entitlement. Below is a 12-layer example stack-up used by SK-AM62P-LP (PROC164E2) :

Table 4-1. Example 12-layer PCB Stack-up

Layer No	Stack-up	Routing Plan Highest Priorities and Layer
	Solder mask	
1	TOP - PWR/SIG	PMIC, SoC, and eMMC devices and BGA breakouts, GND
2	GND	REF
3	PWR/SIG	eMMC signals, LPDDR4 data signals, VDDA_1V8, GND, LVCMOS escape
4	GND	REF
5	SIG/GND	GND, LPDDR data signals, LVCMOS escape
6	GND	REF
7	PWR	VCC1V8_SYS (eMMC supply from PMIC L4 inductor to vias beneath eMMC device), VDD_CORE, VDD_LPDDR4, DVDD_3V3
8	PWR/GND	DVDD_1V8 (VDDS_MMC0 supply from SoC region to vias beneath VDDS_MMC0 pin), VDD1_LPDDR4_1V8, GND, VDDA_x
9	PWR/GND	DVDD_1V8 (VDDS_MMC0 supply from PMIC L4 inductor to SoC region), GND, VDDR_CORE, VDDA_1V8, DVDD_3V3,
10	SIG/GND	GND, LPDDR CA signals, LVCMOS escape
11	GND	REF
12	BOTTOM - SIG/PWR	eMMC CLK series termination resistor (close to SoC), eMMC DS series termination (close to eMMC), decoupling capacitors, LVCMOS escape, GND
	Solder mask	

4.2 Power Routing

The below 2D layout in Figure 4-1 and the 3D layout view in Figure 4-2 shows the VDDS_MMC0 power routing implemented on the SK-AM62P-LP (PROC164E2) .

The 1.8V power rail for the AM62Px eMMC PHY supply VDDS_MMC0 and eMMC IO supply both originate from a common inductor from the PMIC switching regulator. In order to measure power of the SoC supplies independently of the eMMC, the VCC1V8_SYS supply crosses a shunt resistor and becomes SoC_DVDD1V8 before reaching the VDDS_MMC0 supply and other SoC supply pins.

The 2D layout indicates which layer is used for each shape and the 3D layout view clearly shows the vias used to transition layers. Solid GND planes exist on layers 2, 4, 6, and 11.

This layout was demonstrated through simulations to satisfy the power supply noise requirements to meet eMMC JEDEC specifications with margin. Further improvements such as solid GND on layer adjacent to VDDS_MMC0 supply, fewer layer transitions for the supply and/or additional vias between layer transitions should only help AC impedance performance and improve signal integrity margin. Board designers are encouraged to make the best PCB that is feasible.

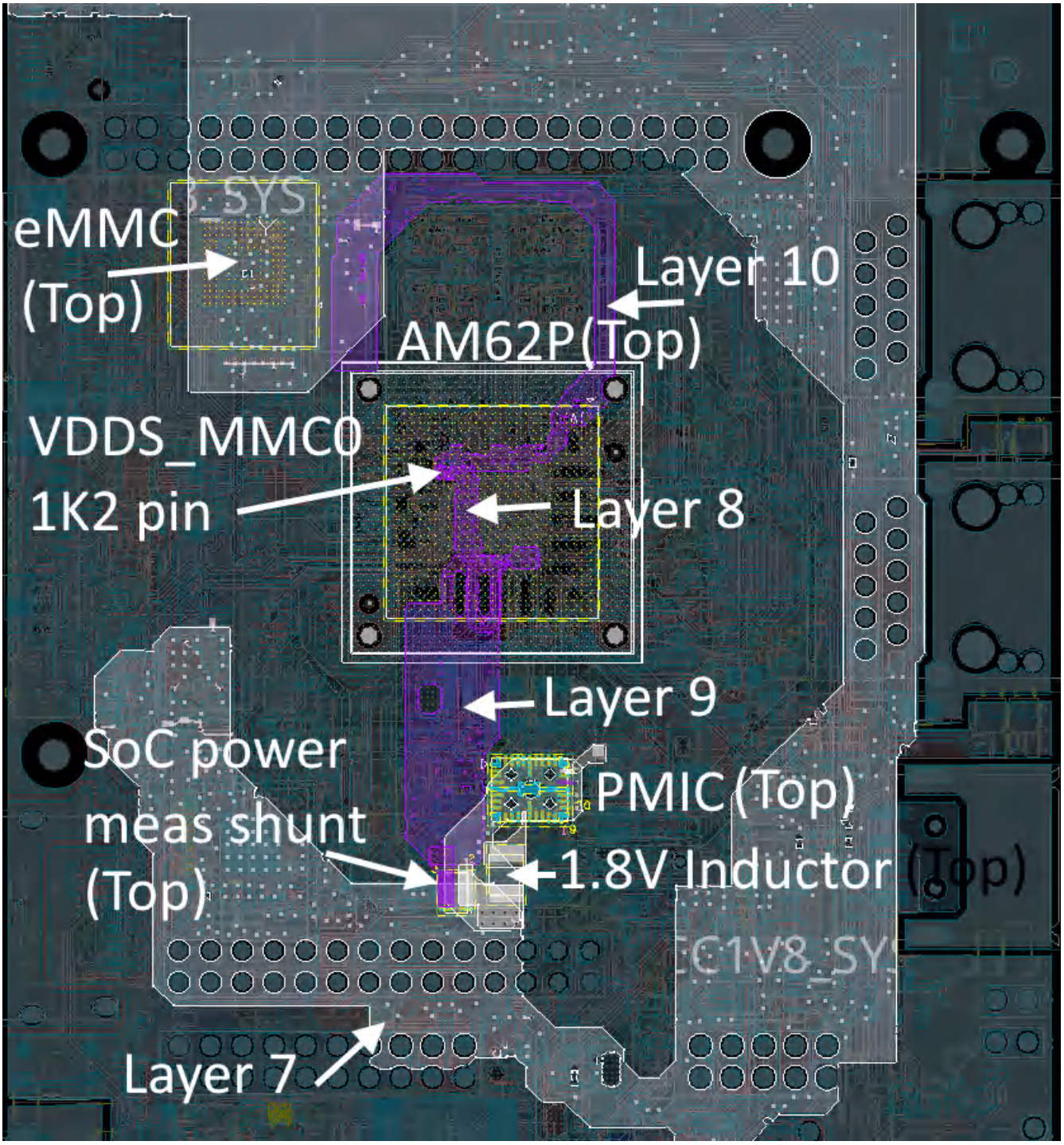

Figure 4-1. SK-AM62P-LP (PROC164E2) eMMC Power Routing 2D Layout - VCC1V8_SYS (White) and SoC_DVDD1V8 (Purple)

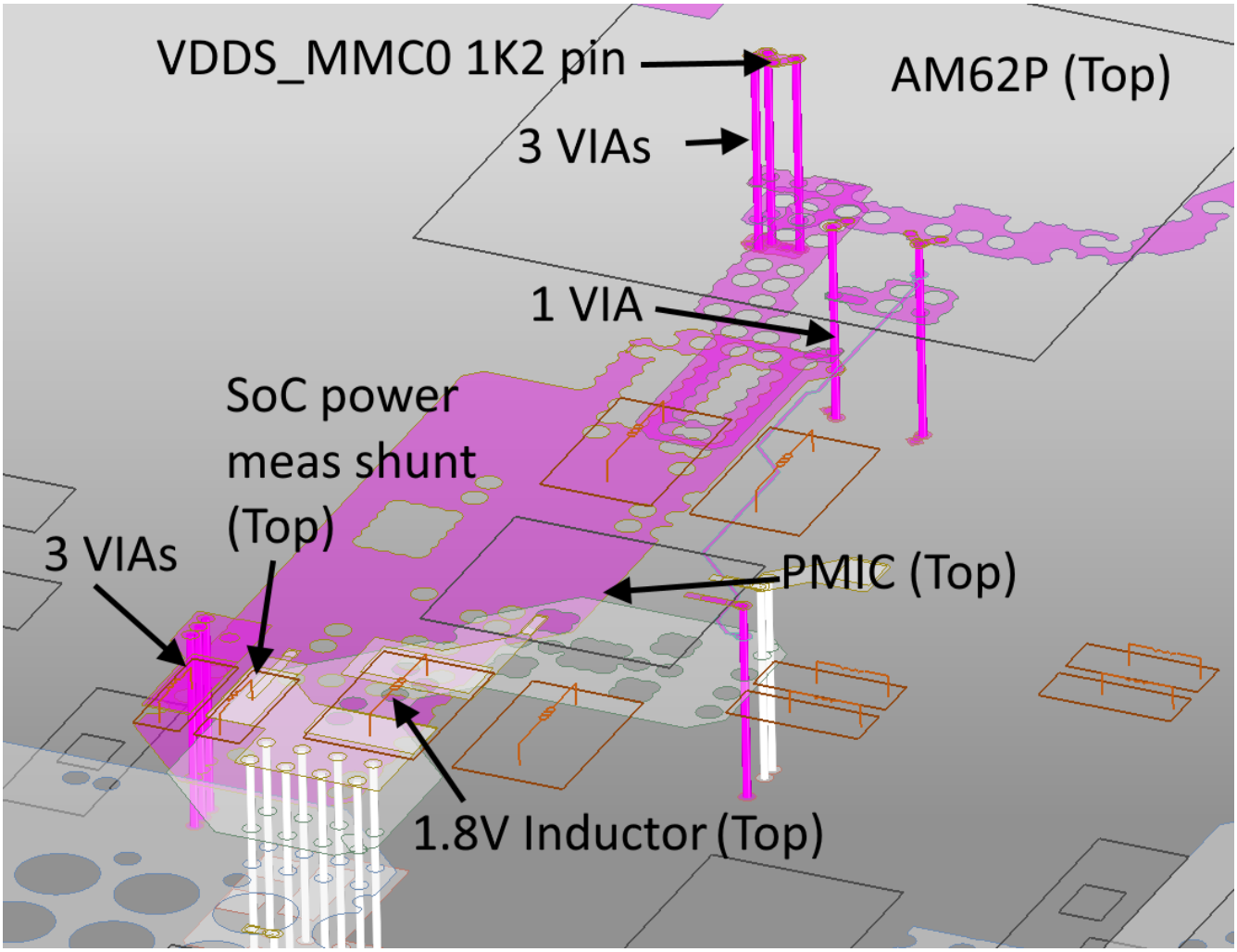

Figure 4-2. SK-AM62P-LP (PROC164E2) eMMC Power Routing 3D Layout - VCC1V8_SYS (White) and SoC_DVDD1V8 (Purple)

4.3 Signal Routing

The example signal routing in Figure 4-3 and Figure 4-4 below shows the eMMC signal routing used on the SK-AM62P-LP (PROC164E2) 12-layer PCB design.

The eMMC signals CMD and DAT[7:0] are routed entirely as stripline on layer 3 with target impedance of 50Ω.

CLK is routed with target impedance of 50Ω from the SoC pin to a series termination resistor on the bottom layer beneath to the SoC before transitioning to Layer 3 with target impedance of 50Ω.

DS is routed with target impedance of 50Ω from the eMMC pin to a series termination resistor on the bottom layer beneath the eMMC device before transitioning to Layer 3 with target impedance of 50Ω.

GND stitching vias facilitate a continuous GND return path for the CLK and DS signals on both sides of the vias to the series termination resistor on the bottom layer.

This layout was demonstrated through simulations to satisfy with margin the Pass/Fail checks mentioned above to show compliance with the JEDEC specifications.

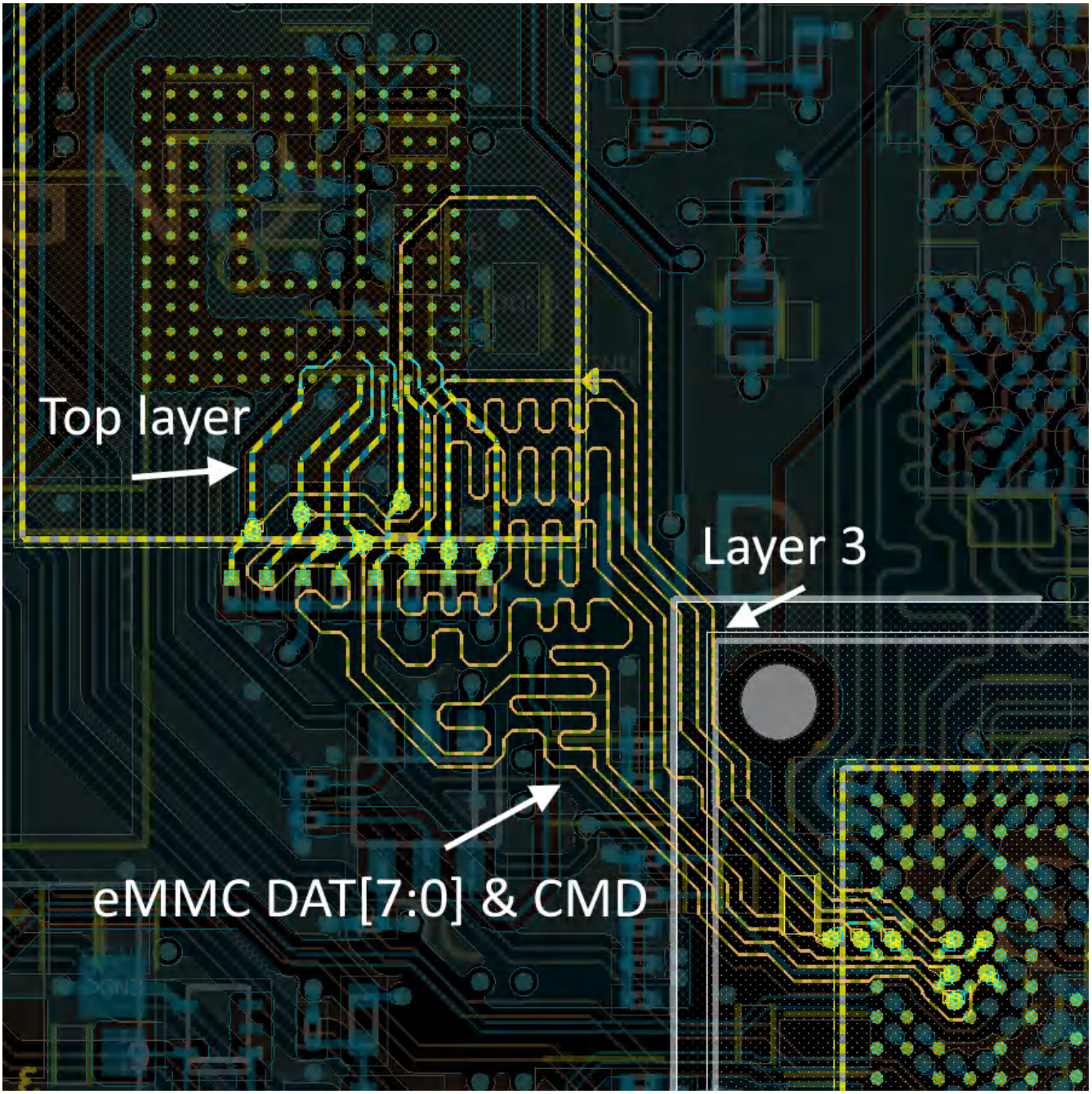

Figure 4-3. SK-AM62P-LP (PROC164E2) eMMC Signal Routing - CMD and DAT[7:0]

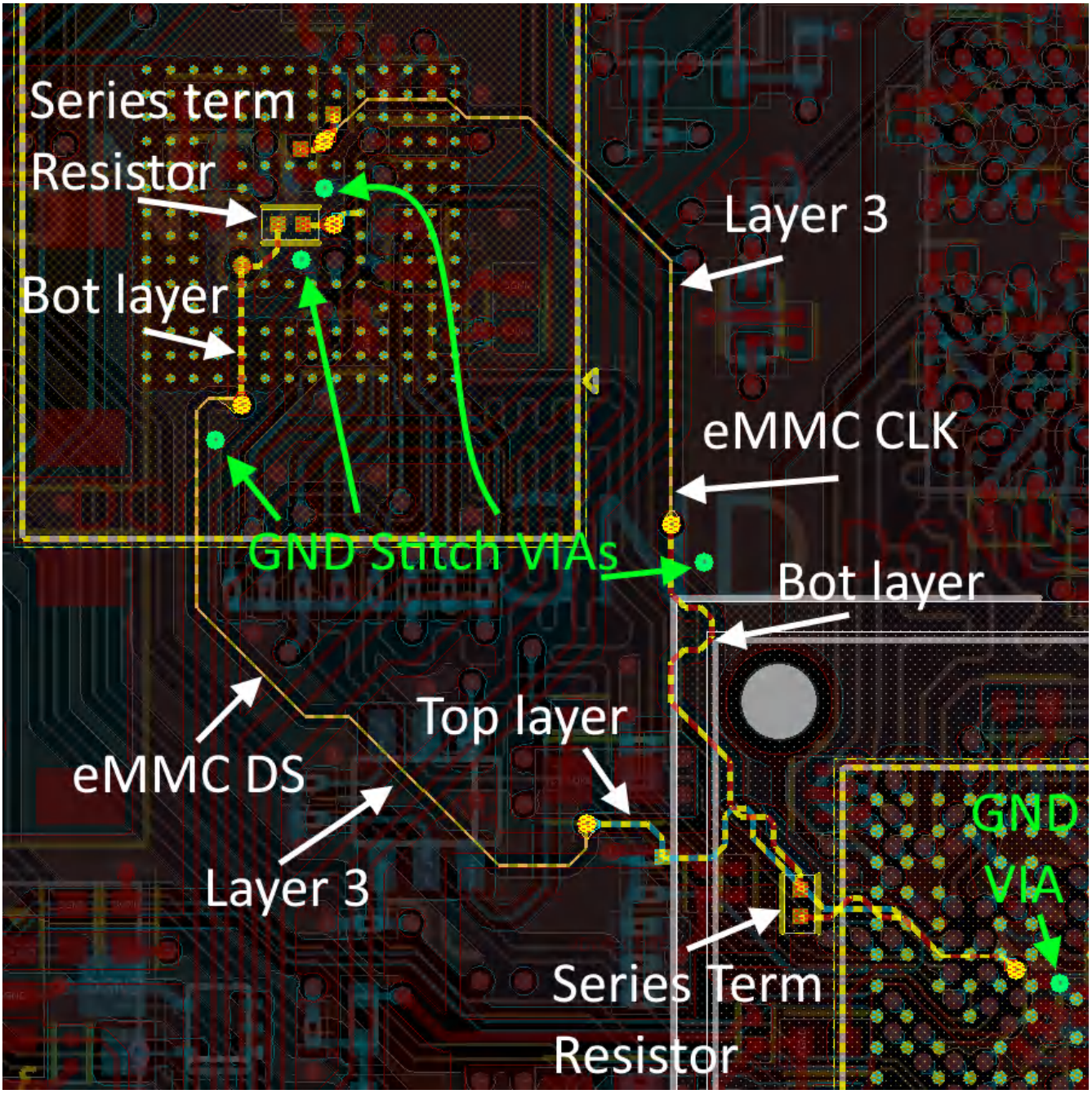

Figure 4-4. SK-AM62P-LP (PROC164E2) eMMC Signal Routing - CLK and DS

Table 4-2. Example eMMC Trace Impedance Summary

Layer	Signals	Single Ended Impedance (Ω)
L3	eMMC CLK(1), CMD, DAT[7:0], DS(1)	49.87
L12	eMMC CLK(1), DS(1)	50.13

(1) CLK and DS transition to L12 (bottom layer) to series termination resistors then transition back to L3 for remainder of the route

5 Summary

This application report describes how to plan, route, and simulate a PCB for successful eMMC HS400 operation with AM62Px processor designs. Topics include board layout guidelines, power supply noise checks, IBIS simulations with pass/fail criteria, and examples from an actual board design.

6 References

- Texas Instruments, SK-AM62P-LP (PROC164E2)
- Texas Instruments, eMMC Data Attack Bit Patterns
- Texas Instruments, AM62Px Sitara™ Processors Product Page
- Texas Instruments, AM62Px Sitara™ Processors Data Sheet
- Texas Instruments, EVM User's Guide: SK-AM62P-LP
- Texas Instruments, AM62x, AM62Ax, AM62D-Q1 and AM62Px Processor Families Schematic, Design Guidelines and Review Checklist

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Last updated 10/2025