Application Brief

Space-Grade, 100-krad, 125-kHz Photodiode Transimpedance Amplifier (TIA) Circuit

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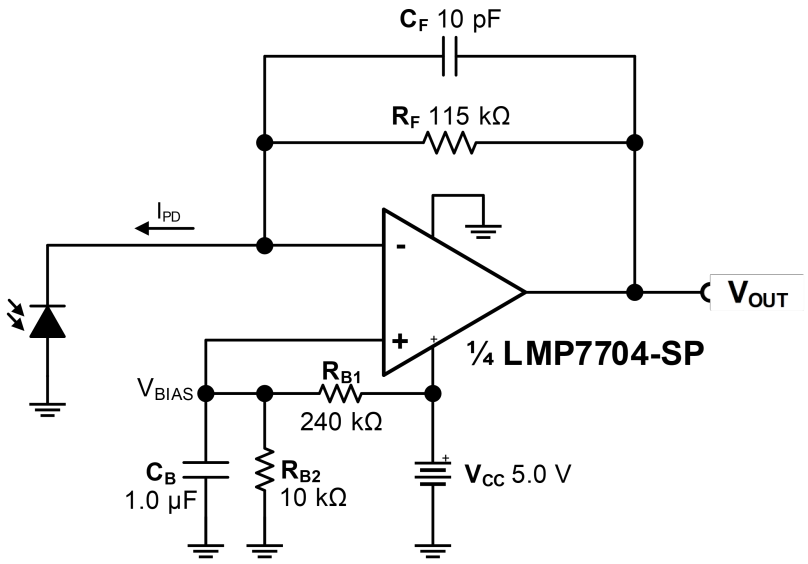
Design Goals

Parameter	Design Goal
Analog Bandwidth (BW)	125 kHz
Photodiode Input Current Range	0 - 20 µA
Transimpedance Gain	115 kV/A
Output Range	0.2–2.5 V
Supply Current (per Channel)	< 2.0 mA
Op Amp Supply	5.0 V (Single Supply)
Total Ionizing Dose (TID)	100 krad(Si)
Single-Event Latch-up (SEL) Immunity	LET = 85 MeV·cm^2/mg

Design Description

Transimpedance amplifiers (TIA) are commonly used to amplify the output of current-based sensors like photodiodes. Applications in spacecraft can range from scientific instruments like precision UV spectrometers, to precision optical encoders for motor driver feedback. TIA circuits can be deceptively simple; the proper design of a single-supply photodiode amplifier requires the consideration of many factors including stability and input and output voltage range limitations. Furthermore, the effects of DC error sources such as input bias current and input offset voltage are often ignored and can degrade the accuracy of the circuit.

This application brief examines the proper design process for a rad hard photodiode transimpedance amplifier (TIA) using the QMLV, radiation-hardness-assured (RHA) LMP7704-SP precision op amp as the TIA. The system is assumed to only offer a single 5.0-V supply and the TIA maximum output voltage is determined by the ADC maximum input voltage which is assumed to be 2.5 V.



Design Notes

- Only microcircuit components are expected to have radiation hardness and space qualifications.
- 1% resistors are assumed to be used in this application brief. If greater precision is required, higher tolerance resistors may be used.
- The compensation capacitor, C_F, should be a NP0, C0G type ceramic capacitor to avoid affecting the frequency response or output distortion of the amplifier.
- Capacitor C_B can be a high-k dielectric type with a suitable voltage rating. The decoupling capacitors used on the PCB were also high-k ceramic capacitors.
- For proper operation, the power supplies must be decoupled. For supply decoupling, TI recommends placing 10-nF to 1.0-µF capacitors as close as possible to the operational-amplifier power supply pins.
- Depending on the mission and system de-rating requirements it might be required to consider specifications like NASA's EEE-INST-002 or the ESCC's ECSS-Q-ST-30-11C Rev.1. For example, EEE-INST-002 recommends an 80% de-rating of the supply voltage, meaning that for a 5.0-V supply requirement, the absolute maximum supply voltage of the op amp chosen should be at least 6.3 V.

Design Steps

Photodiode Sensor Parameters

This circuit considers Hamamatsu's S1336-5BK Si photodiode, which is targeted for UV to NIR precision photometry applications. Some of the key specifications are:

- Diode Capacitance (C_{PD}) = 65 pF
- Shunt Resistance (R_{PD}) = 1 GΩ
- Maximum Reverse Current ($I_{PD(max)}$) = 20 µA

Transimpedance Gain Calculation

First, to determine the maximum transimpedance gain, consider two factors: the maximum reverse current, $I_{PD(max)}$, and the desired output voltage range, $V_{OUT(max)}$ and $V_{OUT(min)}$. The minimum voltage range is determined to be 0.2 V so that the amplifier does not saturate to V– or GND in this case. The value of the feedback resistor (R_F), which sets the transimpedance amplifier (TIA) gain can be calculated by dividing the maximum output by the maximum reverse current:

$$R_F = \frac{V_{OUT(max)} - V_{OUT(min)}}{I_{PD(max)}} = \frac{2.5\,V - 0.2\,V}{20\,\mu A} = 115\,k\Omega$$

Feedback Capacitor Calculation

The feedback capacitor, in combination with the feedback resistor, forms a pole (f_P) in the frequency response of the amplifier:

$$f_P = \frac{1}{2\pi \times R_F \times C_F}$$

Above this pole frequency, the amplification of the circuit declines. The maximum feedback capacitor value can be determined from the feedback resistor value and the desired bandwidth:

$$C_F \leq \frac{1}{2\pi \times R_F \times f_P} = \frac{1}{2\pi \times 115\,k\Omega \times 125\,kHz} = 11.07\,pF \rightarrow 10\,pF$$

Keeping the feedback capacitor at or below the calculated value, ensures that thecircuit meets the stated bandwidth requirements. In this case, 10 pF is chosen as the closest standard capacitor below the value calculated for C_F.

Bias Network Calculations

The photodiode acts as a reverse biased diode at DC, so the gain from the non-inverting terminal of the op amp is 1. Therefore, when the photodiode current is 0 A, V_{OUT} = V_{Bias}. Consider the case where V_{Bias} is 0 V and an amplifier has a maximum output voltage swing (V_{OUT}) of 200 mV. If the photodiode current is 0 A, the amplifier with a noise gain of 1 attempts to produce a 0-V output, resulting in the amplifier saturating and its bandwidth compromised due to the saturation recovery time. It is best to account for the V_{OUT} requirement of the amplifier by adding a bias voltage that defaults the TIA output above the maximum V_{OUT} from the negative rail. The bias at the non-inverting input is given by the equation:

$$V_{Bias} = \frac{V_{CC} \times R_{B2}}{R_{B1} + R_{B2}}$$

For many rail-to-rail input/output (RRIO) op amps, the typical output swing limitations range from 30 to 60 mV depending on operating conditions, and in some instances can be as high as 200 mV. A bias voltage (V_{Bias}) of 200 mV is used to account for the worst-case scenario.

Selecting a value for R_{B2} of 10 kΩ, calculate R_{B1} to be:

$$R_{B1} = \frac{R_{B2} \times (V_{CC} - V_{Bias})}{V_{Bias}} = \frac{10\,k\Omega \times (5.0\,V - 0.2\,V)}{0.2\,V} = 240\,k\Omega$$

Capacitor C_B is placed in parallel with resistor R_{B2} to reduce the noise contribution of the resistor divider and prevent power supply noise from affecting the amplifier output. Selecting a value of 1 µF for C_B produces a corner frequency (f_c) of:

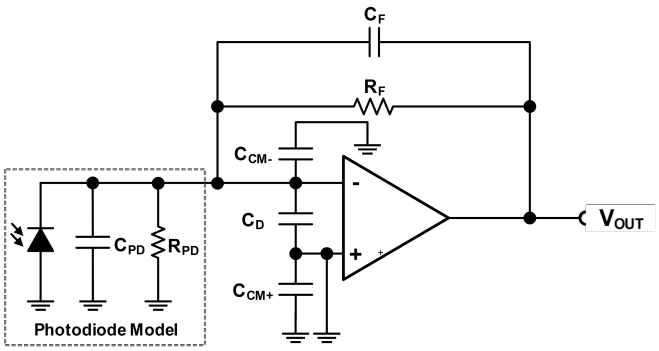
$$f_c = \frac{1}{2\pi \times (R_{B1} || R_{B2}) \times C_B} = \frac{1}{2\pi \times (10\,k\Omega || 240\,k\Omega) \times 1\,\mu F} = 16.6\,Hz$$

The calculated corner frequency should be low enough to prevent power supply noise from passing to the output.

Amplifier Gain Bandwidth Calculation

Having calculated the maximum feedback capacitor value allowable to meet the bandwidth design requirement, it is necessary to calculate the necessary op amp gain bandwidth for the circuit to be stable.

The following figure shows a version of the circuit which has been redrawn to include the photodiode junction capacitance (C_{PD}) and the differential (C_D) and common-mode (C_{CM-}, C_{CM+}) input capacitances of the amplifier. The bias voltage applied to the non-inverting input is considered an AC ground.



From this illustration it is apparent that C_{PD}, C_D, and C_{CM-} are in parallel and the capacitance at the inverting input is described by the following equation:

$$C_{IN} = C_{PD} + C_D + C_{CM-}$$

To calculate the unity gain bandwidth (UGBW) requirement for this design, C_{IN} must first be determined. C_D and C_{CM-} are not known at this time since a specific op amp has not been selected, but 10 pF can be used

as a reasonable guess for the sum of these values. The exact value can be substituted later to confirm the appropriateness of an op amp.

$$C_{IN} = 65\,pF + 10\,pF$$

Now, the values for C_F, R_F, and C_{IN} can be inserted into the following equation to find the target op amp gain bandwidth (GBW):

$$GBW > \frac{C_{IN} + C_F}{2\pi \times R_F \times (C_F)^2} = \frac{75\,pF + 10\,pF}{2\pi \times 115\,k\Omega \times (10\,pF)^2} = 1.176\,MHz$$

Op Amp Selection

The basic requirements for the op amp used in this application are outlined in the following table:

Specification	Design Goal
Total Ionizing Dose (TID) (krad(Si))	100
SEL Immunity (MeV·cm²/mg)	85
V_{CC} Range (V)	2.7–5.5
V_{CC} Abs Max (V)	> 6.3
Input Bias Current (pA)	< 1000
Typ. Iq per Channel (mA)	< 2.0
Input Voltage Range (Typ)	(V–) + 200 mV
Output Voltage Range (Typ)	(V–) + 200 mV, (V+) – 200 mV
GBW	> 1.176 MHz

The requirements for supply voltage and current were given in the *design requirements*. The input and output voltage range requirements are selected to ensure linear operation over the desired signal amplitudes. Finally, the gain bandwidth requirement was calculated in the *Amplifier Gain Bandwidth Calculation* section.

In addition to these basic requirements, the op amp should contribute negligible errors from voltage offset, input bias current, and voltage or current noise. Op amps with JFET or CMOS inputs are the most commonly-selected type because these op amps typically have much lower bias current than those with BJT input devices. This results in reduced DC error voltages and lower noise due to reduced input current noise. A complete noise analysis of this amplifier is beyond the scope of this document, see *reference* 6 for more information on noise in photodiode amplifiers. Zero-drift amplifiers or amplifiers with chopper inputs such as LMP2012QML-SP should be avoided due to the nature of the chopper input stage, the input bias current is not constant. The input MOSFET chopping stage creates dynamic transient currents on the inputs due to charge injection, which differ from the actual static bias current and could cause transients at the circuit output if the switching frequency is below the cutoff frequency.

The LMP7704-SP was selected for this design because of its excellent combination of low bias current (as an op amp with CMOS inputs), offset voltage, power consumption, radiation performance and wider supply range, which could allow for re-use in other applications in the system, as well as use without a bias voltage in systems that have bipolar voltage rails available. Relevant LMP7704-SP specifications are given in the following table:

Specification	Target	LMP7704-SP
TID (krad(Si))	100	100
SEL Immunity (MeV·cm^2/mg)	85	85
V_{CC} Range (V)	2.7–5.5	2.7–12
V_{CC} Abs Max (V)	> 6.3	13.2
V_{OS} (Max. at 25°C) (µV)	–	200
Input Bias Current (pA)	< 1000	0.2
Typ. Iq per Channel (mA)	< 2.00	0.73
Input Voltage Range (Typ)	(V_{EE}) + 200mV	(V_{EE}) – 200 mV
Output Voltage Range (Typ)	(V_{EE}) + 200mV, (V_{CC}) – 200mV	(V_{EE}) + 50mV, (V_{CC}) – 60mV
GBW (MHz)	> 1.176	2.500
Slew Rate (V/µs)	–	1

The LMP7704-SP meets or exceeds all required specifications for the design. However, the parallel combination of the differential and common-mode input capacitances (C_D + $C_{CM–}$) is 25 pF, which is higher than the estimated value used to calculate the required gain bandwidth product, so the gain bandwidth requirement previously calculated should be re-calculated to verify that the GBW of the LMP7704-SP is sufficient.

$$GBW > \frac{C_{PD} + C_{IN\_LMP7704-SP} + C_F}{2\pi \times R_F \times (C_F)^2} = \frac{65\,pF + 25\,pF + 10\,pF}{2\pi \times 115\,k\Omega \times (10\,pF)^2} = 1.384\,MHz$$

LMP7704-SP has 2.5 MHz of gain bandwidth (GBW), which provides more than enough adequate margin to achieve a stable design. It should also be noted that the slew rate (SR) of the op amp might be a limitation to the full power bandwidth of the circuit, the full power bandwidth is the highest frequency sinusoid that can be reproduced at the full output swing of the amplifier. The full power bandwidth (f_{FP}) can be calculated using the equation:

$$f_{FP} = \frac{SR}{2\pi \times A}$$

"SR" is the slew rate of the op amp in Volts per Second, and "A" is the amplitude of the sinusoid. The full output swing of this amplifier is from 0.2 V to 2.5 V, or a swing of 2.3 V. Therefore the amplitude of the sinusoid is 2.3 V / 2 = 1.15 V. The resulting full power bandwidth is:

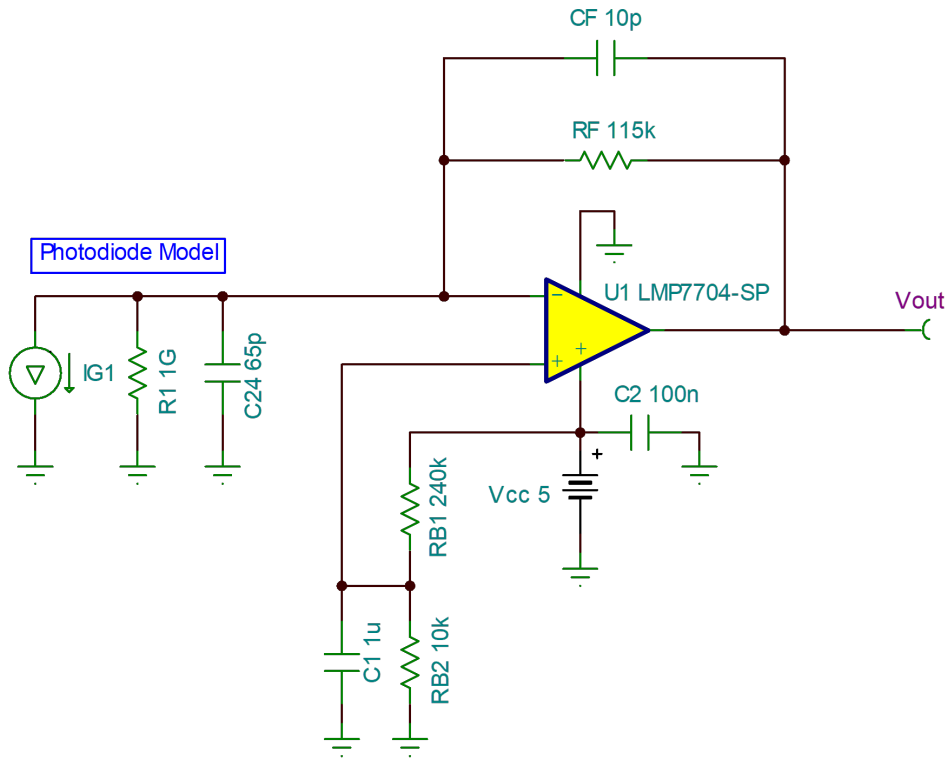
$$f_{FP} = \frac{SR}{2\pi \times A} = \frac{1 \times 10^6}{2\pi \times 1.15\,V} = 138.396\,kHz$$

The resulting full power bandwidth is above the TIA bandwidth, so SR limitations should not be a significant contributing factor to distortion for full-scale signals.

Design Simulations

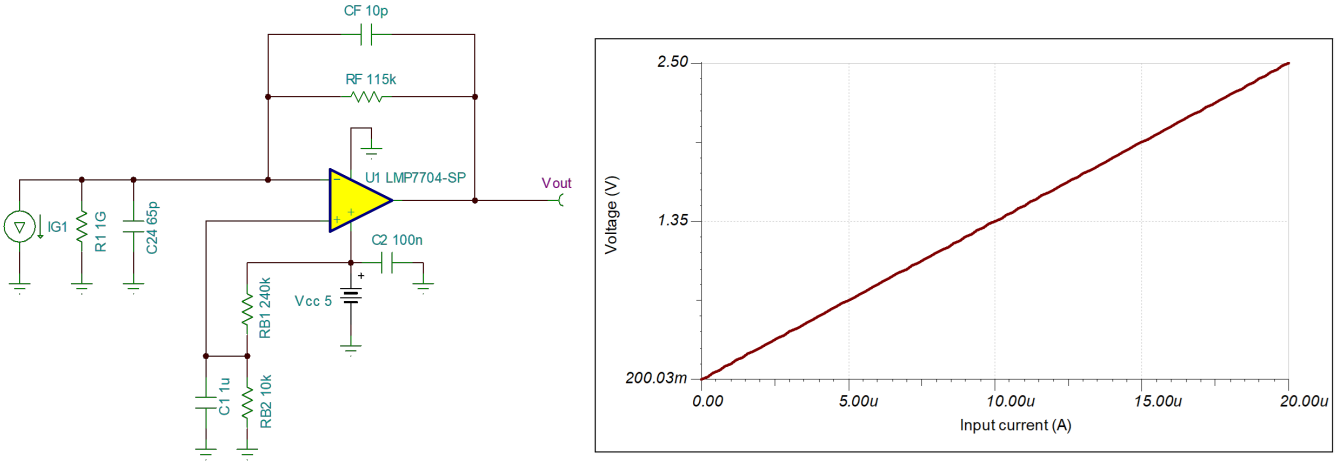
Simulation

The following figure shows the TINA-TI™ simulation schematic of the photodiode amplifier. The current source IG1 and the capacitor C24 serve to form a simple model that represents the reverse current, I_{PD}, of the photodiode and junction capacitance C_{PD}, respectively.



DC Transfer Function

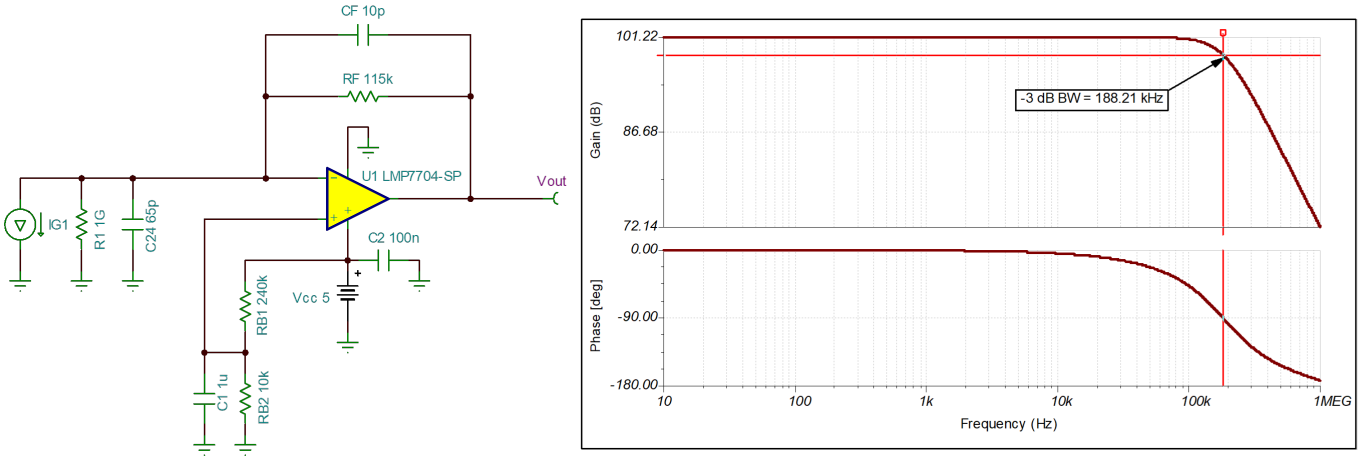
A DC transfer characteristic analysis is used to verify the gain and output voltages of the circuit. The output current of IG1 is swept from 0 to 20 µA and the output voltage is plotted.



For zero input current, the simulated output voltage is 200.032 mV, and at 20-µA input current, the simulated output voltage is 2.500 V and the gain is 115 kV/A.

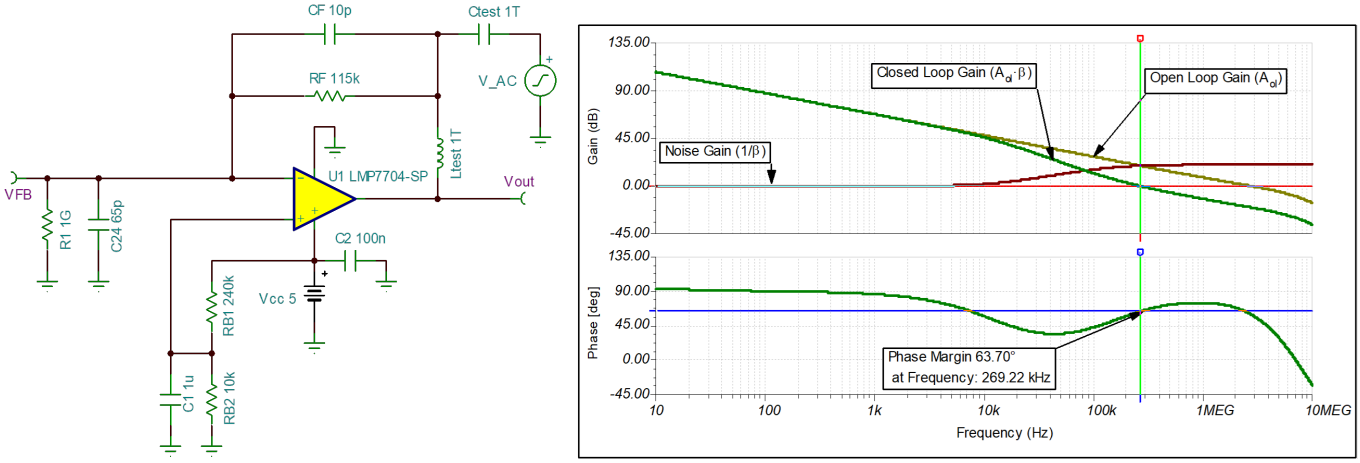
AC Transfer Function

The AC transfer function was measured using an AC transfer characteristic analysis in TINA-TI™. The simulated –3-dB point was 188.21 kHz.



Stability Analysis

For simulation of the loop stability, the feedback path of the amplifier is broken at the output using a large inductor (Ltest). This inductor allows the circuit to converge to the proper DC bias point but acts as an open circuit in an AC transfer characteristic simulation. Voltage source V_AC is AC coupled into the feedback loop by capacitor (Ctest) and the loop gain is measured by voltage probe Vout.



The loop gain plot shows the loop closure point (loop gain is 0 dB) at 269.22 kHz with 63.70 degrees of phase margin.

Design References

1. Texas Instruments, *1 MHz, Single-Supply, Photodiode Amplifier Reference Design*
2. Texas Instruments, *Noise Analysis of FET Transimpedance Amplifiers*
3. Texas Instruments, *What op amp bandwidth do I need? (Transimpedance Amplifiers)*
4. Texas Instruments, *Zero Drift Amplifiers: Features and Benefits*
5. Texas Instruments E2E™ Design Support Forums, *LMP2012QML-SP: (or commercial LMP2012) - What is the Max/Min Input bias Current?*
6. A. Kay, *Operational Amplifier Noise: Techniques and Tips for Analyzing and Reducing Noise*. Elsevier, 2012.
7. Hamamatsu, *S1336 Si Photodiode Series Datasheet*
8. Sahu, K., and Leidecker, H. (April 2008). *EEE-INST-002: Instructions for EEE Parts Selection, Screening, Qualification, and Derating*. Retrieved from https://nepp.nasa.gov/docuploads/FFB52B88-36AE-4378-A05B2C084B5EE2CC/EEE-INST-002_add1.pdf
9. European Cooperation for Space Standardization. (October 2011). *ECSS-Q-ST-30-11C Rev.1 – Derating – EEE components*. Retrieved from https://ecss.nl/standard/ecss-q-st-30-11c-rev-1-derating-eeecomponents-4-october-2011

Design Featured Op Amp

LMP7704-SP	
Supply voltage range	2.7 V to 12 V
Supply current per channel (typical)	0.73 mA
Input common-mode voltage range	V_{EE} – 200mV to V_{CC} + 200mV
Output voltage range	V_{EE} + 50mV to V_{CC} – 60mV
Input offset voltage (typ)	±37 µV
Input bias current (typ)	±0.2 pA
Unity-gain bandwidth (typ)	2.5 MHz
Slew rate	1.0 V/µs
#Channels	4
Total Ionizing Dose (TID)	100 krad(Si)
Single-Event Latch-up (SEL) Immunity	LET = 85 MeV·cm^2/mg
www.ti.com/product/LMP7704-SP	

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