EVM User's Guide: LMKDB1120EVM

LMKDB1120 Evaluation Module

Description

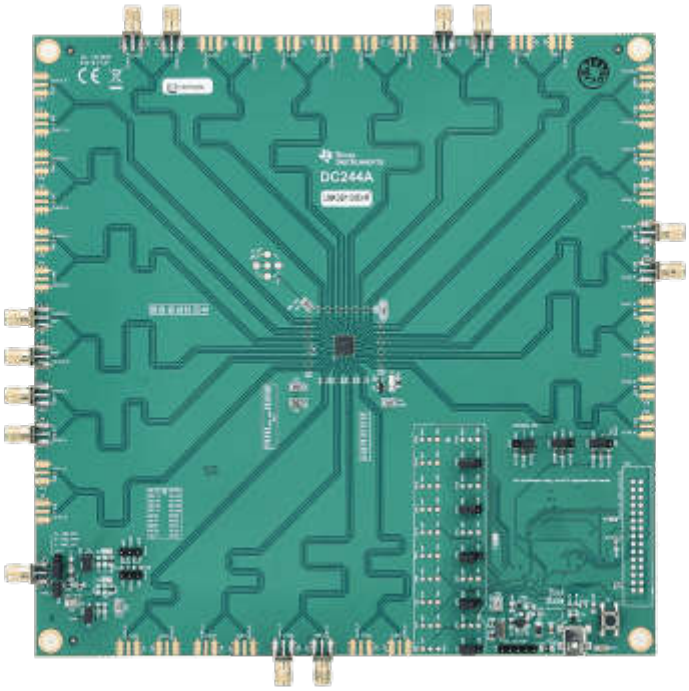
The LMKDB1120 Evaluation Module (EVM) is designed to provide a quick setup to evaluate the LMKDB1120 LP-HCSL buffer that supports PCIe Gen 1 to Gen 6 and is DB2000QL compliant. The printed circuit board (PCB) contains several jumpers and a USB connection to enable the LMKDB1120 with desired user programming and setup. The evaluation module provides flexibility for compliance testing, system prototyping, and performance evaluation of LMKDB1120 device.

Features

- PCIe Gen 1 to Gen 6 and DB2000QL compliant buffer
- External and USB power supply options
- Programmablity through TICS Pro Software GUI graphical user interface (GUI)
- Onboard input and output expander for output enable or disable through pin controls

Applications

- High performance computing
- Server motherboard
- NIC/SmartNIC
- Hardware accelerator



LMKDB1120 EVM Default Settings

1 Evaluation Module Overview

1.1 Introduction

The EVM can be configured through an on-board USB microcontroller (MCU) interface using a PC with TI's TICS Pro Software GUI. TICSPro can also be used to import and export register data for flexible programming of device. Input and outputs of LMKDB1120 can be interfaced with external system for evaluating compatibility and performance through a coaxial cable. On-board LDOs give users an option to use the USB as power supply to minimize the number of test equipment needed. Side Band Interface (SBI) header pins can be used to daisy chain or control the outputs of LMKDB1120 for fast switching.

1.2 Kit Contents

LMKDB1120EVM box contains:

- One LMKDB1120EVM board (DC244A).
- 3-ft. mini-USB cable (MPN 3021003-03).

1.3 Specification

Some key specifications for LMKDB1120 device and EVM are noted in Table 1-1.

Table 1-1. LMKDB1120 Key Parameters

Parameter	Value
Ambient temperature	-40ºC to 105ºC
Power supply	1.8V ± 10%, 3.3V ± 10%
Operating frequency	1MHz to 400MHz. (automatic output disable (AOD) disabled)
	25MHz to 400MHz. (automatic output disable (AOD) enabled)
Output format	LP-HCSL

1.4 Device Information

The LMKDB1120 is a high performance LP-HCSL buffer that supports PCIe Gen 1 to Gen 6 and is DB2000QL compliant. LMKDB1120 has extremely low additive jitter, fail safe inputs, flexible power-up sequence, individual output enable pins (OE#), loss of input signal detection (LOS), and 3-wire or 4-wire SBI and SMBus interface. The EVM has integrated LDOs for excellent power supply noise suppression with operating supply voltage of 3.3V.

2 EVM Quick Start

The default jumper configuration for the EVM to power the device from an onboard 3.3V LDO with USB supply option is shown in Table 2-1. Configure the EVM for initial bring up as specified in Table 2-1. The EVM can also be configured to external power supply by changing the position of jumper JP17 as described in Table 2-1.

Table 2-1. Default Jumper Configuration

Category	Reference Designator	Default Position	Description
Power	J5	1-2	Connect USB or external supply to VDDA of device.
	J6	1-2	Connect USB or external supply to output bank and digital supply of the chip (VDD).
	J7	1-2	Connect USB or external supply to IO pins on board (VDD_IO).
	JP17	2-3	Choose between USB power supply and external. Current configuration is for USB option. To change to external supply, change jumper position to 1-2.
Output Enable Control Pins	JP1, JP5, JP9, JP13, JP18	2-3	Pull down to GND to enable output (OE#0, OE#4, OE#8, OE#12, OE#16) with pin control option.
	JP2, JP3, JP4, JP6, JP7, JP8, JP10, JP11, JP11, J12, JP14, JP15, JP16, JP19, JP20, JP21	-	Not populated on the EVM. If additional outputs are needed, then these jumpers need to be soldered onto the EVM, as well as the respective output edge SMA connectors.
SMBus Address Control Pins	JP25, JP26	-	Refer to Table 3-6 or selecting SMBus address.
Digital Pins	JP23, JP24	1-2	TCA Reset and CLKPWRGD_PD# pulled high.
	JP22	1-3	SBEN pin = GND
	J49	-	SN74LVC125 buffer enable control pin. Default pull down to GND.

2.1 Hardware Setup

LMKDB1120 EVM Default Settings shows default jumper configuration for the EVM. Make sure to adjust the jumpers as shown for initial boot-up using USB power supply option.

To begin using the LMKDB1120EVM, follow the steps below.

1. Verify the EVM default jumper as described in Table 2-1 and LMKDB1120 EVM Default Settings.
2. Connect the USB cable to USB port at J51.
3. Connect 100MHz reference clock to CLKIN_P/N. Refer to Figure 3-1 for different input reference configurations.

A labeled image of the LMKDB1120EVM is shown in Figure 2-1.

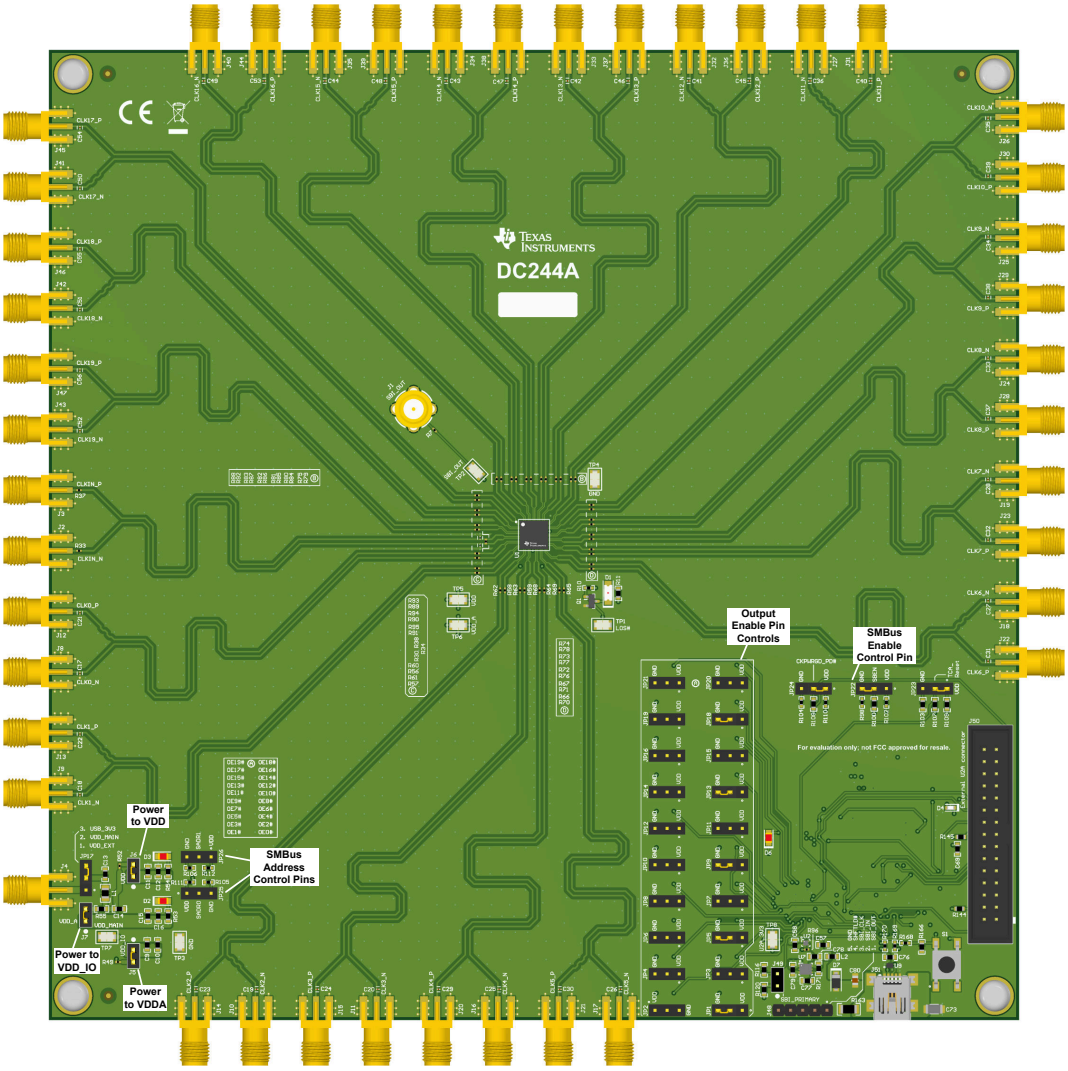


Figure 2-1. LMKDB1120EVM Labeled

2.2 Software Setup

2.2.1 TICS Pro GUI Setup

1. If not already installed, then install TICS Pro software from TI website: TICS Pro Software GUI.
2. Start TICS Pro software.
3. Make sure the steps under Section 2.1 have been completed before performing this step. Select the LMKDB1108 profile from *Select Device* → *Clock Distribution with Divider* → *LMKDB1108*.
4. Confirm communication with the board as follows:
   a. Click *USB Communication* from the menu bar.
   b. Click *Interface* to launch the *Communication Setup* pop-up window.
   c. Confirm following field the *Communication Setup* pop-up window:
      i. Make sure *USB2ANY* is selected as the interface.
      ii. In case of multiple USB2ANY, select desired interface. If a USB2ANY is currently in use in another TICS Pro, then the user must release that interface by changing the interface setting to *Demo Mode*.
      iii. Click *Identify* to blink LED shown in Figure 2-2. After clicking the *Identify* button, the LED flashes quickly at about 0.5 second on, 0.5 second off for about 5 seconds. This confirms the connection to the board. However, be aware that USB2ANY devices connected to the PC, but not attached to a TICS Pro instance, can blink at a slow rate of 1 second on, 1 second off continuously.
   d. Confirm all the fields match the ones shown in Figure 2-3.

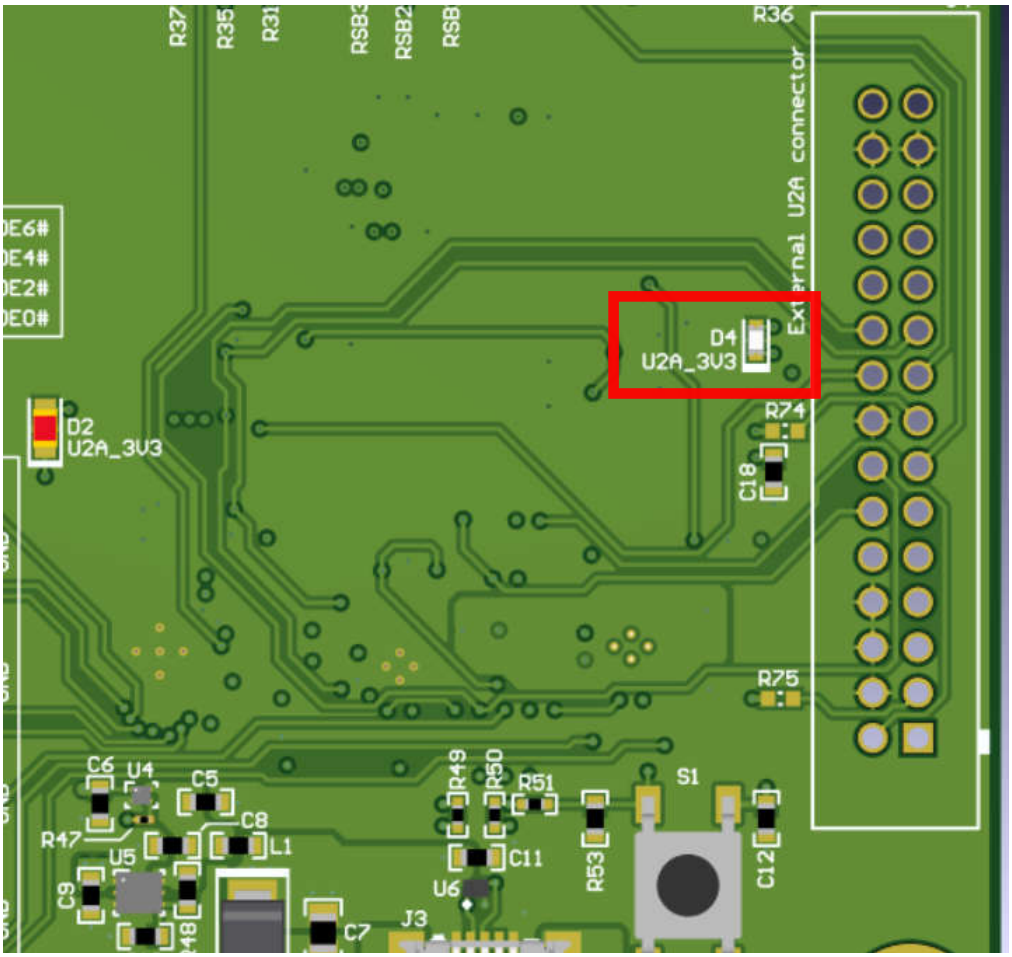


Figure 2-2. USB LED

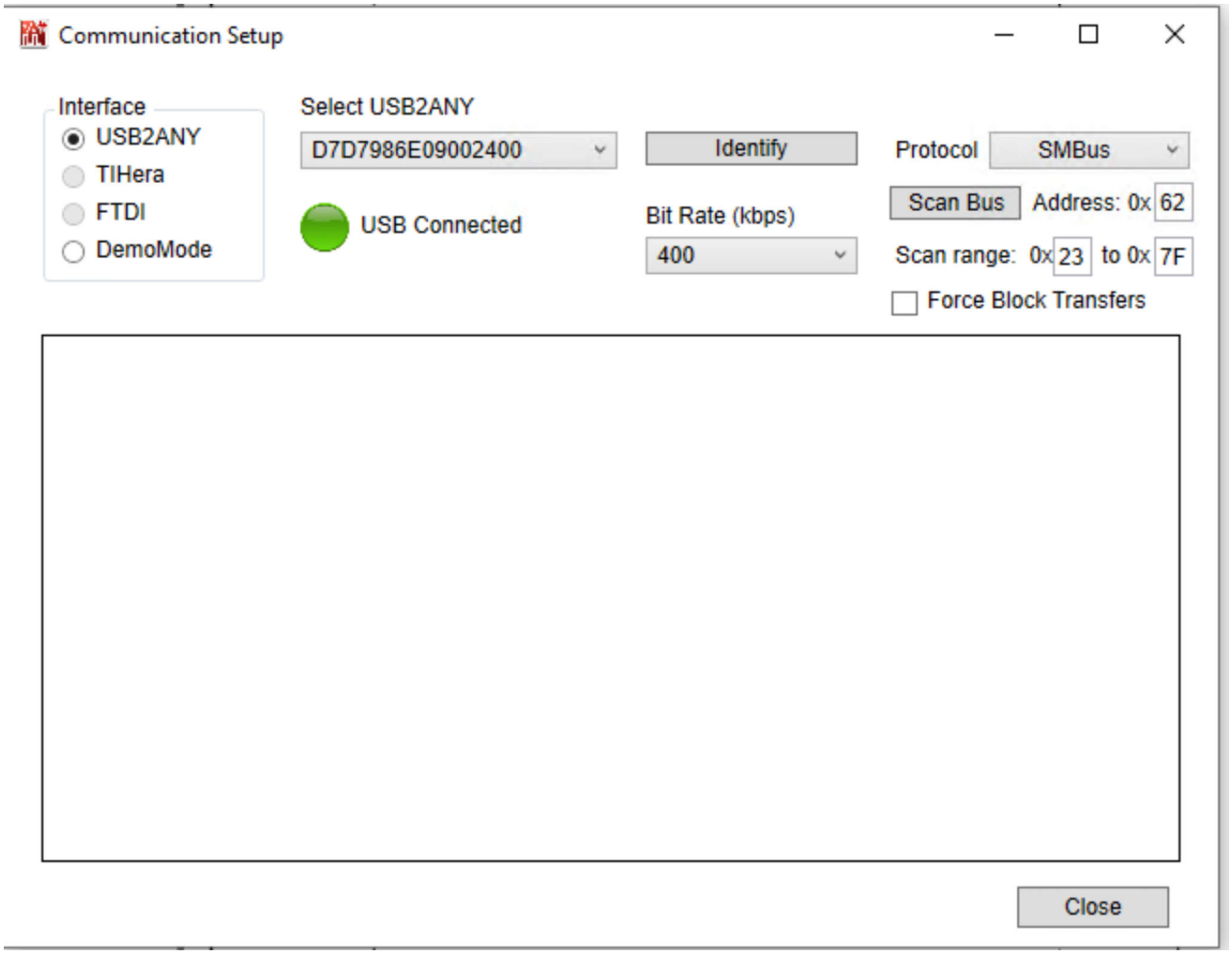


Figure 2-3. Communication Setup

2.2.2 Power Up Sequence

By default, the LMKDB1120 and the GUI are started with the default configuration. When using the on-board USB supply option, the following steps can be followed to avoid any improper power up sequence issues when plugging the USB calculate to the EVM.

1. After all the steps above, toggle the *USB 3V3 Supply* pin *Low* → *High* for power reset. This step is not necessary but recommended if there are any issues with the readback or improper start up on EVM.
2. Click on *Scan Bus* in the *Communication Setup* window to find and update device address.
3. Click on *Read All Regs* to update the register readback from the device.

2.3 EVM Measurements

Measurements can now be made on the clock outputs using an oscilloscope or a phase noise analyzer.

3 Hardware

3.1 Device Operation Modes

The LMKDB1120 can be configured to start up in one of two modes during power-on/reset (POR). SBEN enable pin determines the mode of operation during power supply ramp up. Below are both of the modes for the device:

1. **SMBus Mode Only** (EVM default): When SBEN pin is set to low during power up, SBI interface is disabled and output enable (OE) control is only accessible through the SMBus and OE control pins.
2. **SBI Mode and SMBus Mode**: When SBEN pin is set to high during power up, SBI interface is enabled and the outputs can be controlled through SBI interface, as well as SMBus and OE control pins. OE pin control is not possible for pins L8, L10, and E11 since these pins are being used for SBI communications.

3.2 EVM Configuration

The LMKDB1120EVM can be configured for multiple modes using on board MCU and can be powered via USB or external power supply. The following sections describes power, logic, clock input, and output interfaces on the EVM and how to configure the EVM accordingly.

Some of the key components and the reference designator are noted in Table 3-1.

Table 3-1. Key Components Reference Designator and Descriptions

Item No.	Reference Designators	Description
1	U1A	LMKDB1120
2A	J4	External VDD option through a SMA Port.
2B	JP17	Jumper header to select between external or onboard 3.3V USB supply option.
3	J2, J3	SMA ports for clock input (CLKIN_P, CLKIN_N).
4	J8 to J47	SMA ports for clock outputs (CLKXX_P, CLKXX_N).
5	JP25, JP26	SADR0_tri and SADR1_tri jumper header option to select different address as defined in Table 3-6.
6	JP22	SBEN pin header jumper to enable or disable SBI interface during power-up.
7	JP23	TCA_RESET pin header jumper for Input / Output (IO) Expander. TCA_RESET pin header jumper needs to be connected to pull-up for proper operation. Default configuration is set to pull-up.
8	JP24	CLKPWRGD_PD# pin header jumper to enable or disable the LMKDB1120.
11A	J48	SBI Connector header jumper for daisy chain option.
11B	J49	SBI_PRIMARY header jumper option to disable the U3A, U3B, U3C, U3D buffer part on the EVM.
12	U2	USB power option LDO.
13	U3A, U3B, U3C, U3D	Hi-Z buffer part used on SBI lines for daisy chain configuration.
14	U4	MUX part to choose between MCU and IO expander option on OE#5, OE#6, and OE#10 pins.
15	U5	IO Expander used for all OE# pin controls.
16	U8	MSP430F5529IPN MCU.

3.2.1 Power Supply

The LMKDB1120 has VDDA and VDD supply pins that operate from 1.8V ± 10% and 3.3V ± 10%. The EVM has two different method of supplying power to the device as listed in Table 3-2.

For 3.3V supply option, the EVM has an on-board LDO which is selected by default to reduce the need for external power supply and operate the EVM using a USB cable with a PC.

To use 1.8V ± 10% supply on the EVM, J4 can be used to force external supply voltage.

Table 3-2. EVM Power Modes

EVM Power Mode	Designator	Position	Supply Voltage	Description
External	J4	External Supply	1.8V ± 10%, 3.3V ± 10%	External supply option is selected.
	JP17	1-2		
USB (default)	J4	Not Connected	3.3V ± 10%	USB 3.3V supply option is selected.
	JP17	2-3		

3.2.2 Logic Input and Outputs

The logic input and output pins on LMKDB1120 provides different options to select device functional modes, output enable and disable control, loss of signal (LOS) detection, and different device address selection. The following section describes the function of different input and output logic pins. Voltage levels for input pins can be set through TICSPro GUI or using on-board jumper as specified in Table 3-1.

Table 3-3. Device Start-Up Modes

SBEN_EN Input Level	Start-up Mode
Low (default)	SBI inactive
High	SBI active

Table 3-4. Output Enable Pin Control

OE0# to OE19# INPUT LEVEL	OUTPUT STATUS
Low (default)	Active
High	Inactive

Table 3-5. Loss of Signal Detection (LOS)

LOSb OUTPUT LEVEL (Status pin)	LOS STATUS
Low	Detected
High	Not detected

Table 3-6. SMBus Address Decode

Address Selection		Binary Value								Hex Value	
SADR1_tri	SADR0_tri	7	6	5	4	3	2	1	Rd/Wrt	Without Rd/Wrt	With Rd/Wrt
0	0	1	1	0	1	1	0	0	0	6C	D8
	M	1	1	0	1	1	0	1	0	6D	DA
	1	1	1	0	1	1	1	1	0	6F	DE
M	0	1	1	0	0	0	0	1	0	61	C2
	M	1	1	0	0	0	1	0	0	62	C4
	1	1	1	0	0	0	1	1	0	63	C6
1	0	1	1	0	0	1	0	1	0	65	CA
	M	1	1	0	0	1	1	0	0	66	CC
	1	1	1	0	0	1	1	1	0	67	CE

Note

SMBus address for the device is Bits[7:1]. Often Rd/Wrt bit is included in the hex value depending on the different vendors. *With **Rd/Wrt*** column shows hex value when Rd/Wrt value is considered 0, while *Without **Rd/Wrt*** is the SMBus address.

3.2.3 Clock Input

LMKDB1120 can support different input interfaces depending on the input swing and common mode voltage. There are four input interfaces type that can be configured on LMKDB1120 using external components and internal termination schemes as shown in Figure 3-1. If using signal generator, then make sure to populate *R34* with a *100Ω* resistor or use internal or external 50Ω termination to ground.

1. DC Coupled HCSL/LP HCSL Input.
2. DC Coupled LVDS Input.
3. External AC Coupled Input.
4. Internal 50Ω to ground terminations.

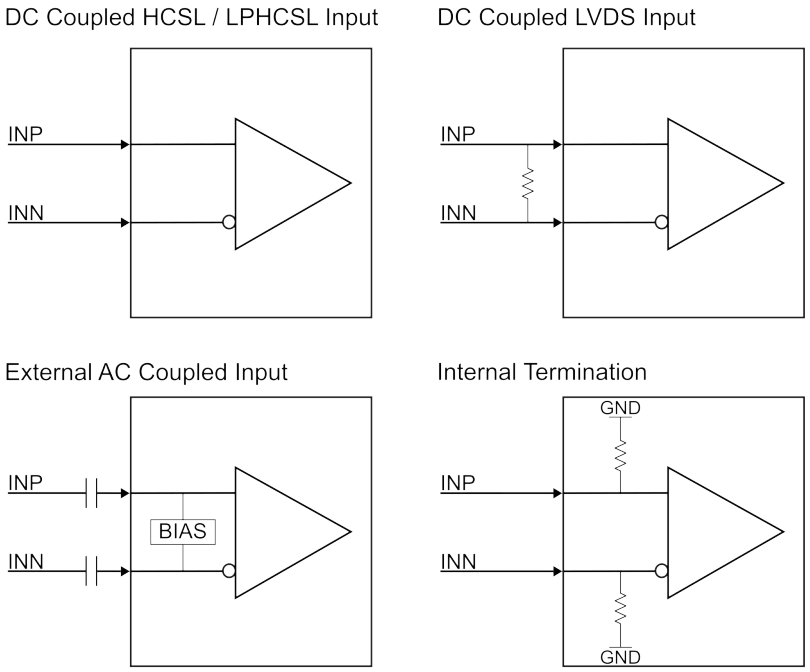


Figure 3-1. Input Interfaces

How to setup all different interfaces supported by LMKDB1120 is outlined in Table 3-7.

Table 3-7. Input Interfaces

Input Interface	Configuration
DC coupled HCSL or LP-HCSL	This is default EVM and device configuration. *R33* and *R37* values are ***0Ω*** and *Input Interface Type* on *Input* page is selected to *DC Coupled*.
DC coupled LVDS input	Populate *R34* with a ***100Ω*** resistor and set *Input Interface Type* on *Input* page to *DC Coupled*.
External AC coupled input	Replace *R33* and *R37* with ***0.1uF*** capacitor and set *Input Interface Type* on *Input* page to *AC Coupled*.
Internal termination	To enable internal 50Ω to ground terminations, set the *Input Termination* on *Input* page to *Enabled*.

3.2.4 Clock Outputs

LMKDB1120 have 20 differential clock outputs (CLK[19:0]_P/N).

All the outputs are DC coupled with a capacitive load of 2pF. CLK0_P/N, CLK4_P/N, CLK8_P/N, CLK12_P/N, and CLK16_P/N have SMA ports populated on the EVM for measurements. To evaluate all other outputs, SMA ports need to be soldered to connect outputs to a measurement instrument.

WARNING

DC-coupled clocks must not be directly connect to RF equipment, which cannot accept DC voltages greater than 0V, such as spectrum analyzers and phase noise analyzers.

3.2.5 Status Outputs, LEDs, and Test Points

LMKDB1120EVM have status output signal from LMKDB1120, LEDs and test points to monitor signal voltage and supply voltage on the board. All the status signals and test points on the board are summarized in Table 3-8.

Table 3-8. Status Output, LEDs and Test Points

Function or Test Signal	Status Pin / LED Designator	Description
LOSb	TP1	Test point to monitor LOSb status.
	D1	LED status light for LOSb detection.
SBI OUT	J1	SMA Port for SBI OUT pin.
	TP2	Additional test point for SBI OUT pin.
	J48	Jumper header for SBI OUT, SBI_IN, SBI_DATA, and SHFT_LD# pins to connect all signals needed for daisy chain in one place.
VDDA	D2	LED status light for VDDA supply pin.
	TP6	Test point for VDDA supply pins.
VDD	D3	LED status light for VDD supply pins.
	TP5	Test point for VDD supply pins.
VDD_MAIN	TP7	Test point to measure the VDD supply selected from USB option or external option through JP17.
GND	TP3, TP4	Test points for GND reference on the board.
USB LED	D6	USB LED status light to verify USB2ANY communication to board.
U2A_3V3	D4	USB2ANY LDO supply status LED.
	TP8	Test point for USB2ANY LDO supply pin.

4 Software

4.1 TICS Pro LMKDB1120 Software

LMKDB1120 TICS Pro GUI provides full functionality to interact with the device through SMBus, SBI, and OE pin option to interact with the device. TI recommends to use GUI interface while evaluating LMKDB1120EVM to fully utilize all the functionalities of the EVM. The GUI interface consists of *User Controls* and *Raw Register* page to write directly into each register bit or field values. The GUI interface also has *Input*, *Device Info*, and *Output* pages, which can be used to evaluate functions available on the device. The following sections describe the details of each page.

4.1.1 Input

Input page provides access to configure different input modes and read back live status for loss of signal (LOSb) as shown in Figure 4-1.

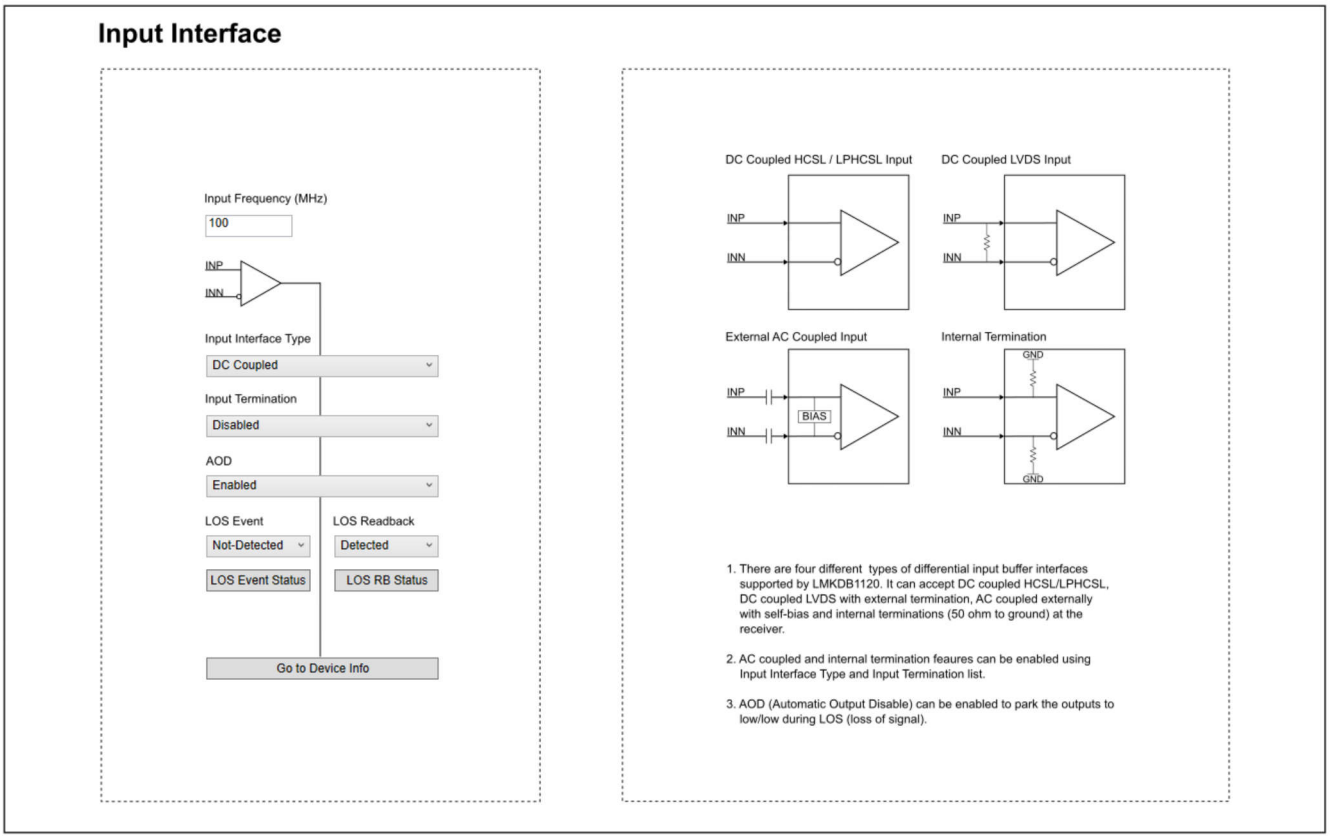


Figure 4-1. Input Interface

4.1.1.1 Input Interface Type

Input interface type can be configured as AC Coupled or DC coupled. AC coupled option provides internal bias to the clock inputs connected.

4.1.1.2 Input Termination

Internal 50Ω to ground terminations can be enabled or disabled using the *Input Termination* drop-down menu.

4.1.1.3 Automatic Output Disable (AOD)

Automatic output disable (AOD) can be enabled or disabled using this control. AOD is enabled by default on LMKDB1120. AOD disables the outputs when low when there is a loss of signal (LOS) detected on the input. When AOD is disabled, outputs follow the input clock in DC state.

4.1.1.4 LOS Event

LOS Event Status gives information when there is loss of signal (LOS) event. Make sure to clear the LOS event by writing 1 or selecting *Detected* from the *LOS Event* drop-down menu.

4.1.1.5 LOS Readback

LOS Readback provides live status of loss of signal detection.

4.1.2 Device Info and EVM Setup

The *Device Info* page contains three different sections and LMKDB1120EVM information.

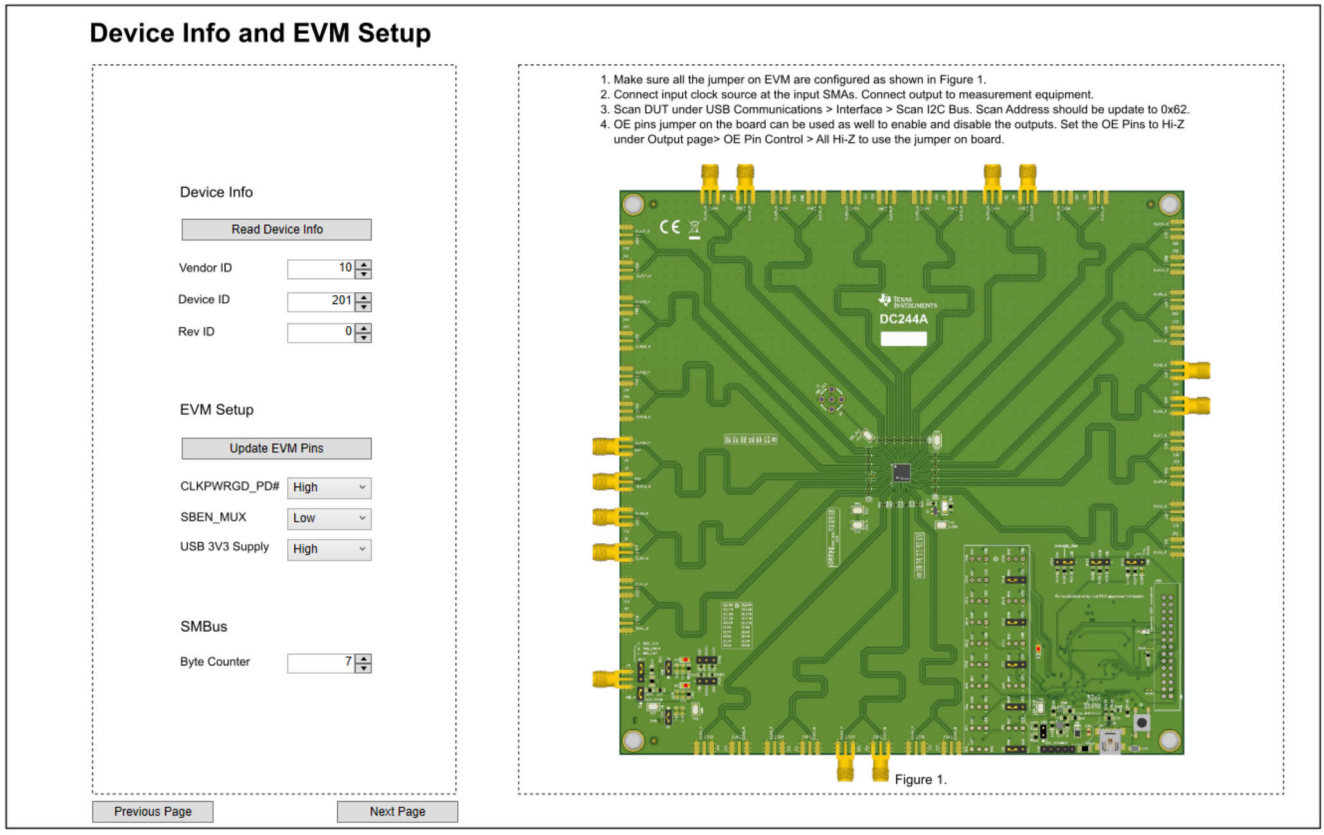


Figure 4-2. Device Info

4.1.2.1 Device Info

This section contains following information related to device which can be read back using *Read Device Info* button.

1. Vendor ID
2. Device ID
3. Rev ID

4.1.2.2 EVM Setup

EVM setup has key pins to configure device. The tables below outlines usage of each pin option.

Table 4-1. CLKPWRGD_PD#

Pin Level	Function
Low	LMKDB1120 power down mode.
High	LMKDB1120 normal operation mode (default).
Hi-Z	When Hi-Z is selected, on-board header jumper JP24 can be used to force external voltages on the pin.

Table 4-2. SBEN_MUX

Pin Level	Function
Low	SBEN MUX (U4) configured to OE option for pin OE5#, OE6# and OE10# through IO expander (default).
High	SBEN MUX (U4) switches to USB2ANY MCU for SBI_IN, SBI_DATA, and SHFT_LD#. SBI becomes available after power reset in this setting on the device. Output page have *Enable SBI Control* button to configure all the setting automatically.
Hi-Z	When Hi-Z is selected, on-board header jumper can be used to force external voltages on the pin.

4.1.2.3 SMBus

Byte counter value determines the number of register readback during block read operation.

4.1.3 Output

The output page in TICS Pro has controls for clock outputs through SMBus, OE pins, and SBI.

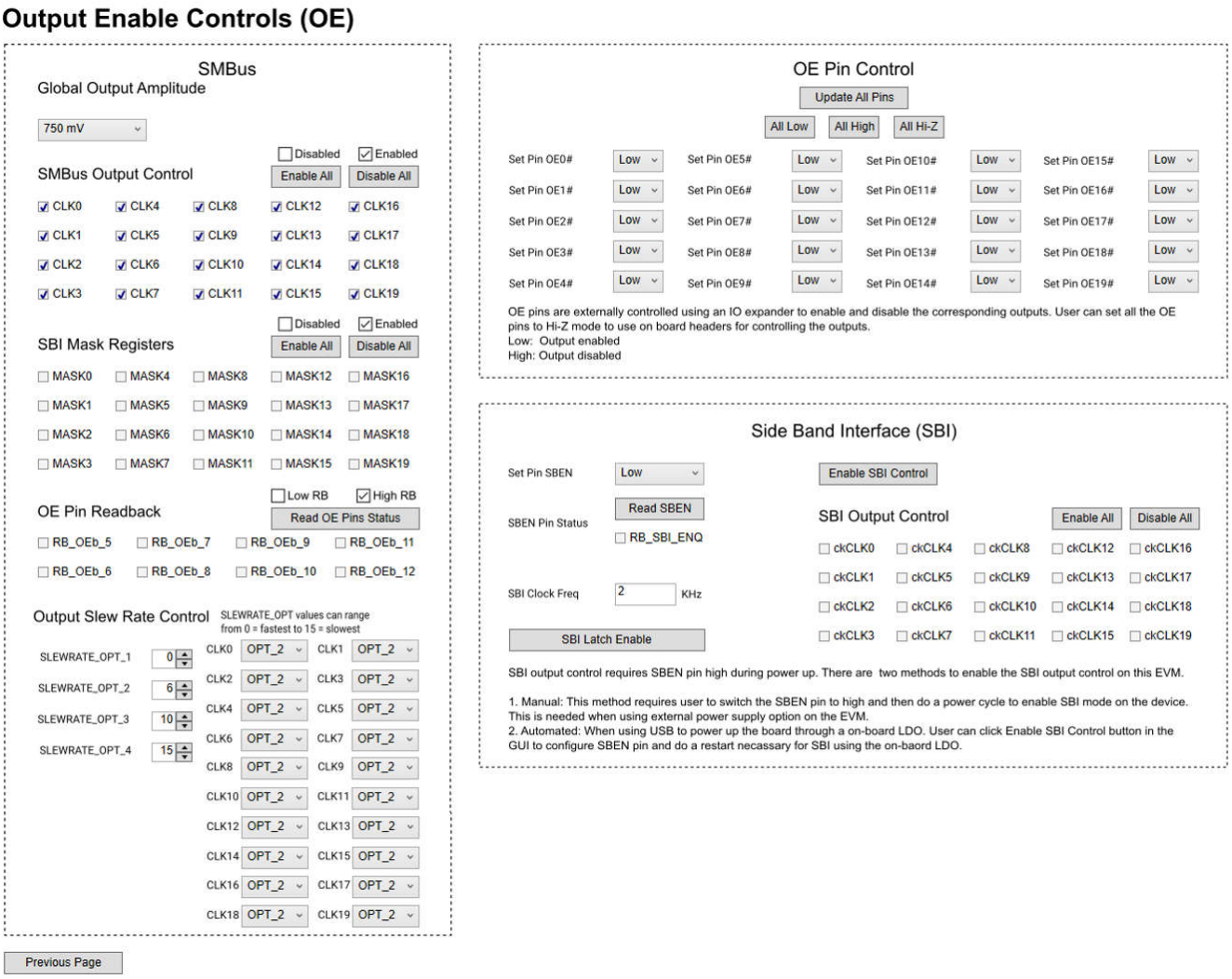


Figure 4-3. Output

4.1.3.1 SMBus

SMBus can be used to control the following parameters on the outputs:

1. Global Output Amplitude: To program output VOD (single-ended swing) from 600mV to 975mV with a step size of 25mV.
2. SMBus Output Control: To enable or disable CLK0 to CLK19 through register bits.
3. Output Slew Rate Control: To program slew rate values for a specifc output.
4. SBI Mask Register: To enable or disable SBI mask bits. When a mask bit is enabled, an output is controlled through SMBus and SBI control doesn't have any affect on the output. This is used when critical outputs needs to stay on.
5. OE# Pin Readback: To read status of OE# pins.

4.1.3.1.1 Programmable Output Slew Rate Control

The LMKDB1120 has 16 different slew rates options that can be assigned to the outputs. 0x0 is the fastest slew rate setting and 0xF is the slowest slew rate setting. To set the slew rate of each output, follow these steps:

1. There are four different registers, SLEWRATE_OPT#, that can store up to four different slew rates. Select your desired slew rates by assigning a value from 0x0 (fastest) to 0xF (slowest) to each SLEWRATE_OPT# register. The default values set to each SLEWRATE_OPT# register can be found in Table 4-3.
   a. For example, if you wanted the fastest, second fastest, and the slowest slew rate, assign 0x0, 0x1, and 0xF to registers SLEWRATE_OPT#. SLEWRATE_OPT1 = 0x0 (fastest), SLEWRATE_OPT2 = 0x1 (second fastest), and SLEWRATE_OPT3 = 0xF (slowest). SLEWRATE_OPT4 does not have to be assigned, but if you want more than one register set to a slew rate, then SLEWRATE_OPT4 can be assigned to any of the three previous settings. For this example, SLEWRATE_OPT4 = 0xF (slowest) as shown in Figure 4-4.

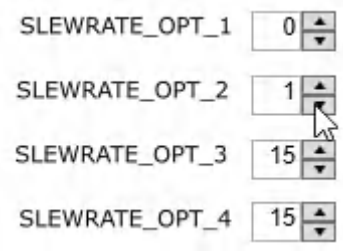


Figure 4-4. SLEWRATE_OPT# Assignment Example in TICS Pro

Table 4-3. Default SLEWRATE_OPT_# Values

Register Field Name	Default Value	Default Slew Rate
SLEWRATE_OPT_1	0x0	Fastest
SLEWRATE_OPT_2	0x6	Fast
SLEWRATE_OPT_3	0xA	Slow
SLEWRATE_OPT_4	0xF	Slowest

2. Set a slew rate for each output by using the drop-down menus under the *Output Slew Rate Control* Section. The default SLEWRATE_OPT# register assignment for all outputs is SLEWRATE_OPT2, which has a default slew rate of 0x6.
   a. Following the example from step 1a, if you wanted CLK0, CLK1, CLK2, and CLK3 to have the fastest slew rate, CLK4 and CLK7 to have the slowest slew rate, and CLK 5 and CLK6 to have the second fastest slew rate, set the drop-down menus of CLK0, CLK1, CLK2, and CLK3 to OPT_1, CLK4 and CLK7 to OPT_3 or OPT_4, and CLK5 and CLK6 to OPT_2 as shown in Figure 4-5. Repeat this step to set the slew rate of the other 12 outputs.

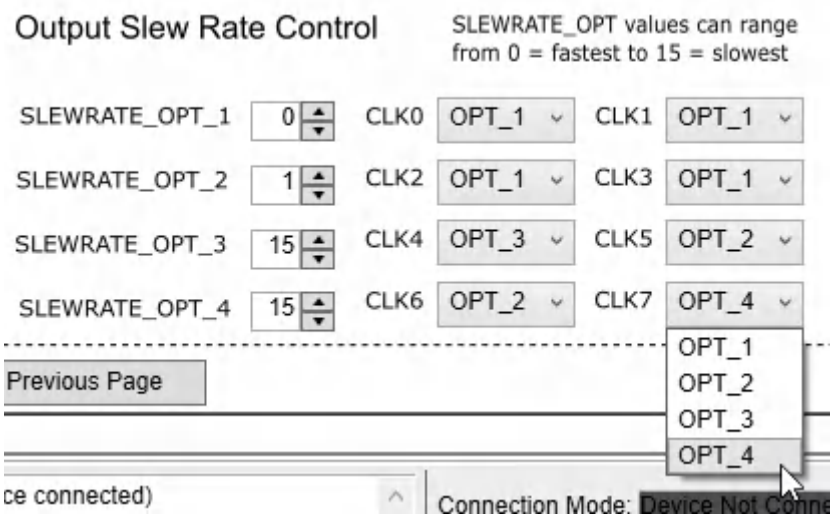


Figure 4-5. Setting Output Slew Rate Example in TICS Pro

4.1.3.2 OE Pin Control

LMKDB1120EVM has on-board IO expander to provide output enable and disable controls for OE# pins. Low and high voltage levels can be set on all the pins using GUI without needing on-board headers. If on-board headers are used, then set all the OE# pins to Hi-Z using the *All Hi-Z* button under the OE Pin Control on output page.

4.1.3.3 Side Band Interface (SBI)

Side band interface can be evaluated using controls available on the output page. There are two methods that can be used to enable SBI on the LMKDB1120.

1. Automated: When using on-board USB power supply option on the EVM, clicking once on the *Enable SBI Control* button configures the LMKDB1120 into SBI mode.
2. Manual: This method requires to set the *Set Pin SBEN* to *High* followed with a power cycle on the board. This is needed when using external supply option or when not using the *Enable SBI Control* button. SBI is enabled on LMKDB1120 after the restart.

After using any of the method above, press *Read SBEN* to verify status of SBI mode on the device. Use check boxes for CLK0 to CLK19 to enable (checked) or disable (unchecked) the desired outputs. Once selected, click on *SBI Latch Enable* to load data into shift register.

5 Implementation Results

5.1 Typical Phase Noise Characteristic

The typical phase noise performance for 156.25MHz reference clock input using a SMA100B is shown in Figure 5-1.

LMKDB1120EVM was configured in cascaded mode to get these measurements:

1. SMA100B → LMKDB1120EVM input. Then, LMKDB1120EVM to secondary LMKDB1120 EVM. This was done to get good slew rate at the input. Other methods like a clipping circuit can be used to get a desired slew rate and square wave form from the SMA100B.
2. Outputs phase noise is measured through a Balun to convert the differential waveform from the LMKDB1120 into a single-ended waveform for a phase noise analyzer.

   As shown below in Figure 5-1, reference input jitter is 36.7 fs. The measured jitter on the output of LMKDB1120 is 43.7 fs is shown in Figure 5-2. Calculated typical additive jitter is about 24 fs for the LMKDB1120.

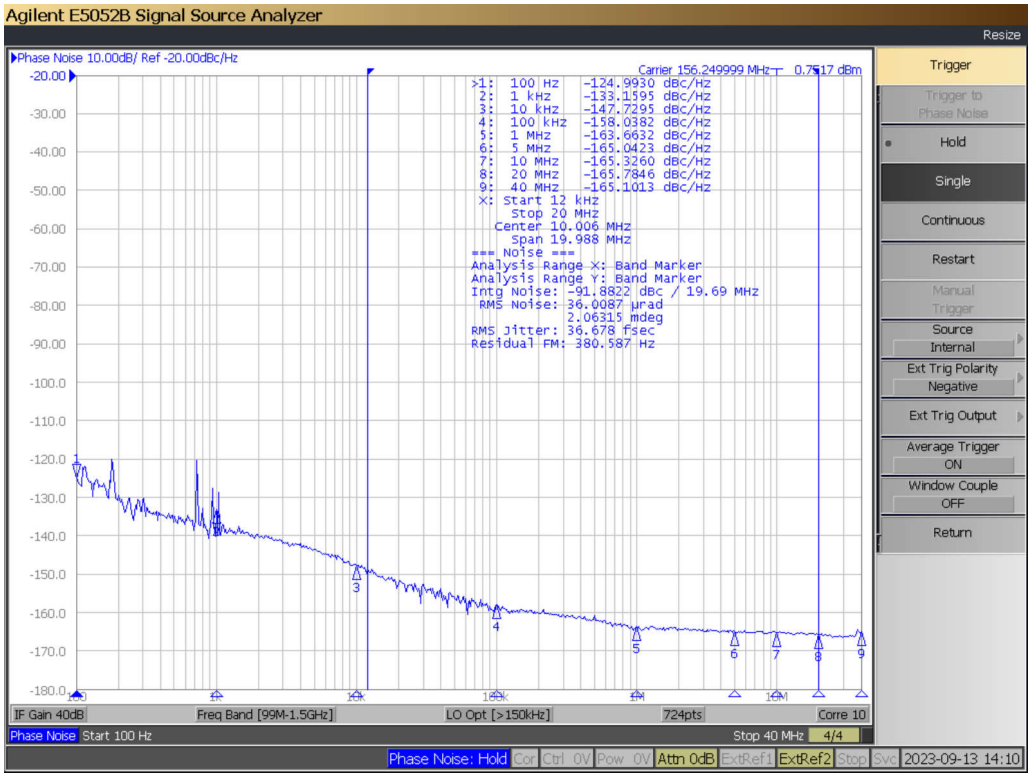


Figure 5-1. Reference Clock Input Phase Noise

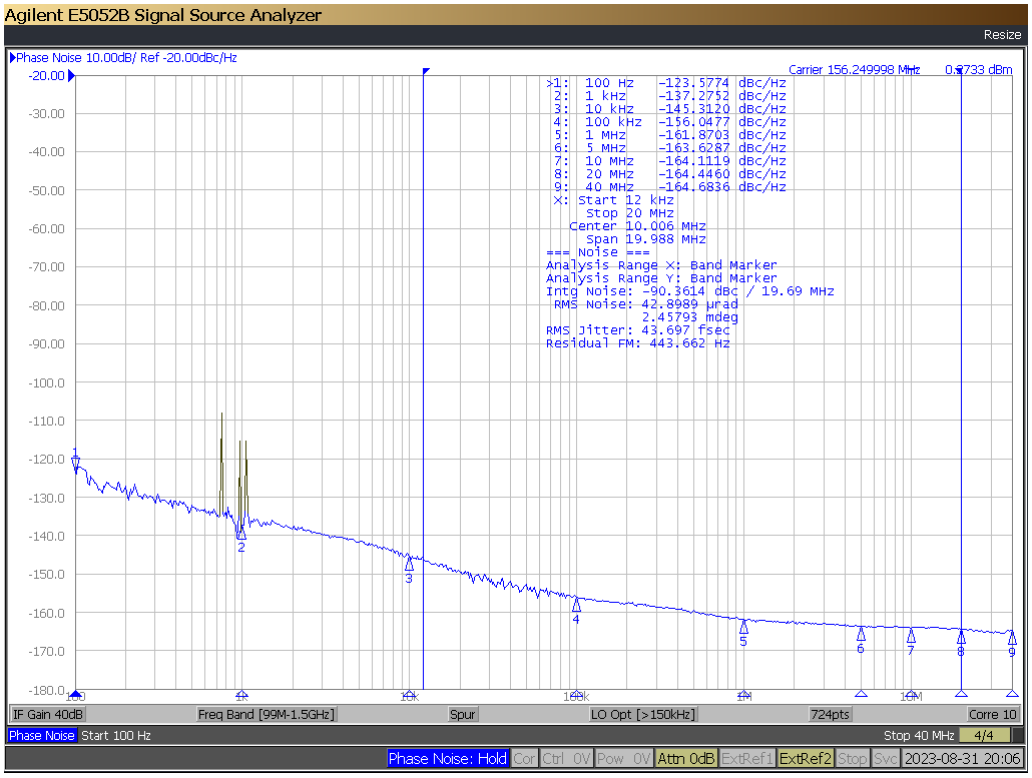


Figure 5-2. LMKDB1120 Output Clock Phase Noise

6 Hardware Design Files

6.1 Schematics

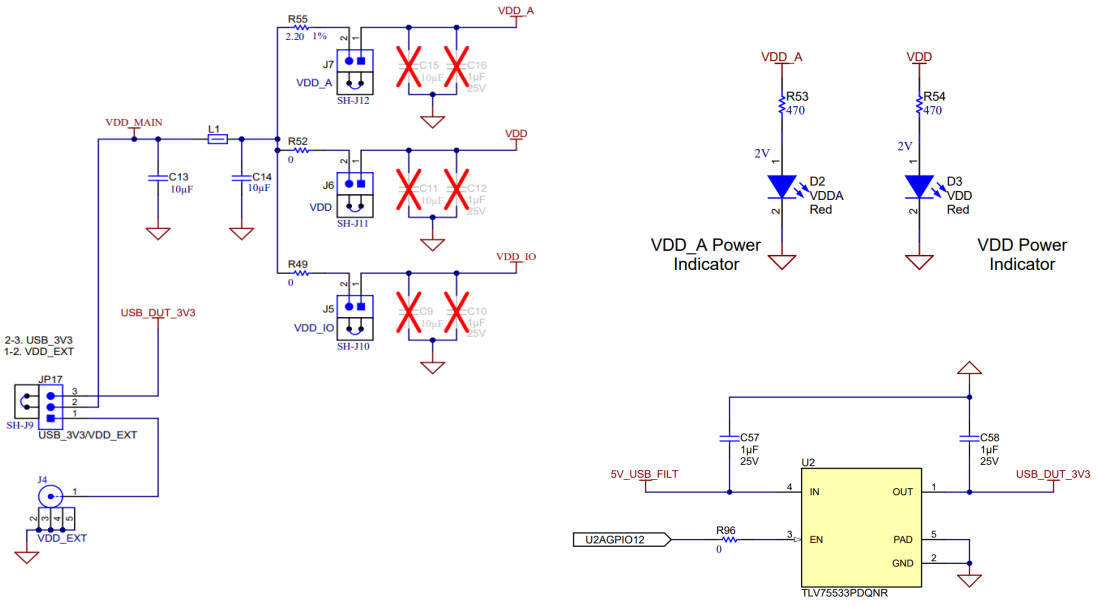


Figure 6-1. Power Supply (External and USB option)

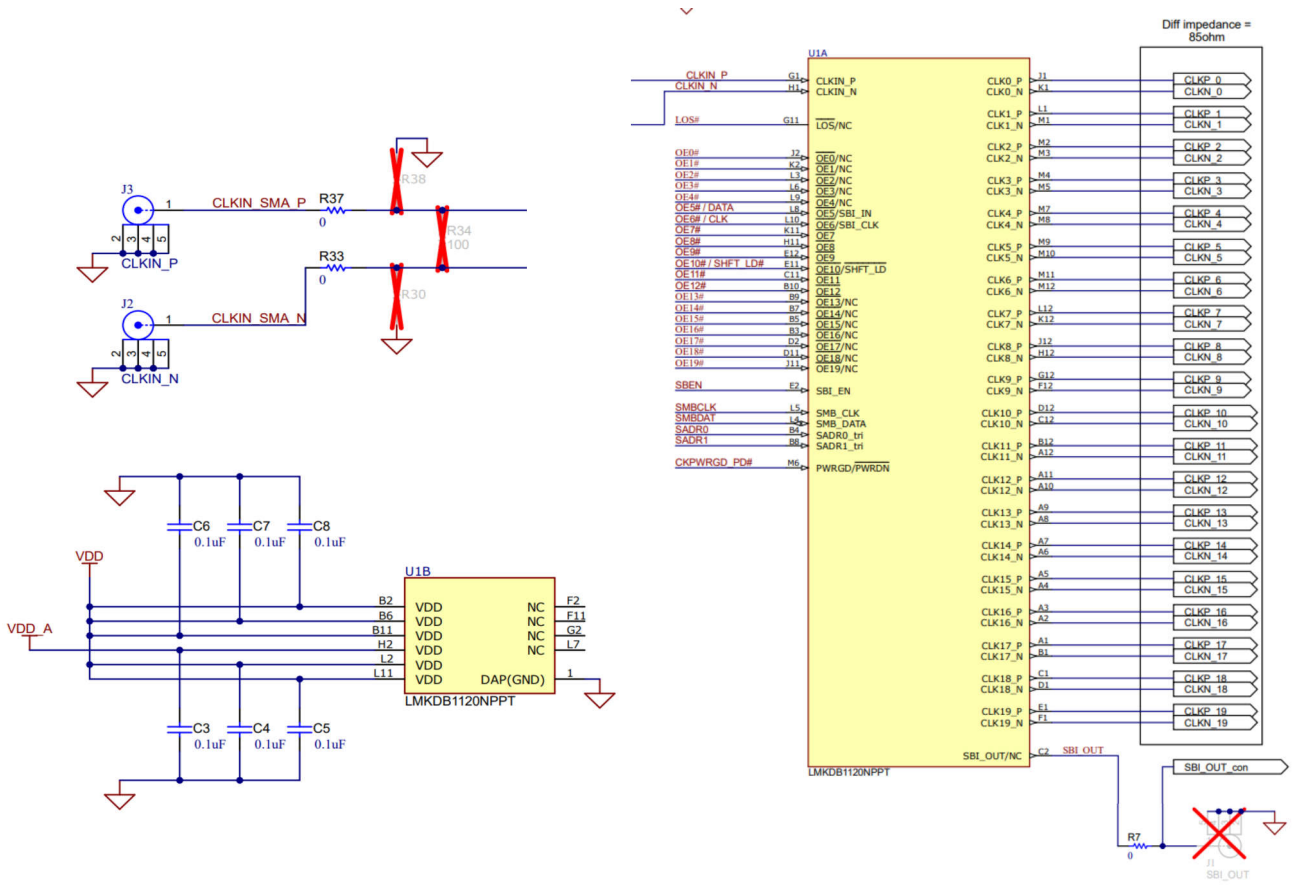


Figure 6-2. LMKDB1120 Device and CLKIN_P/N Reference

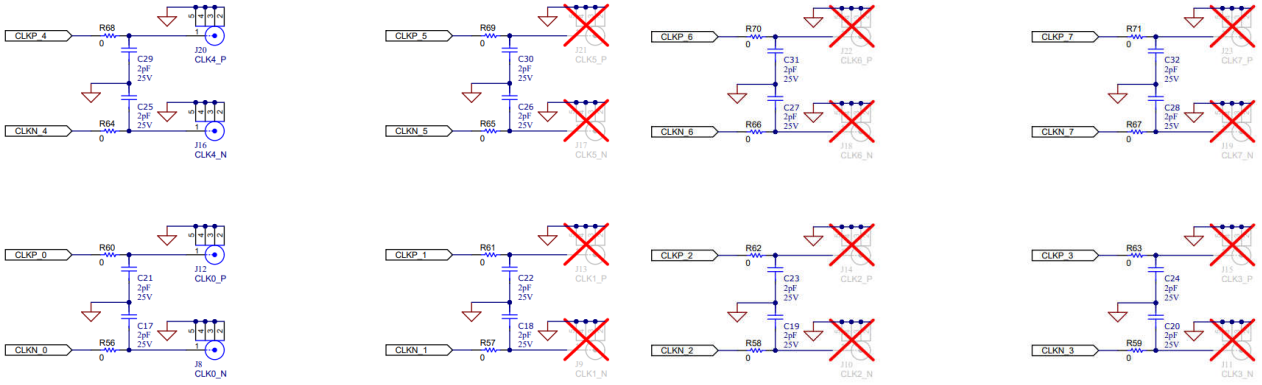


Figure 6-3. Clock Outputs CLK0 to CLK7

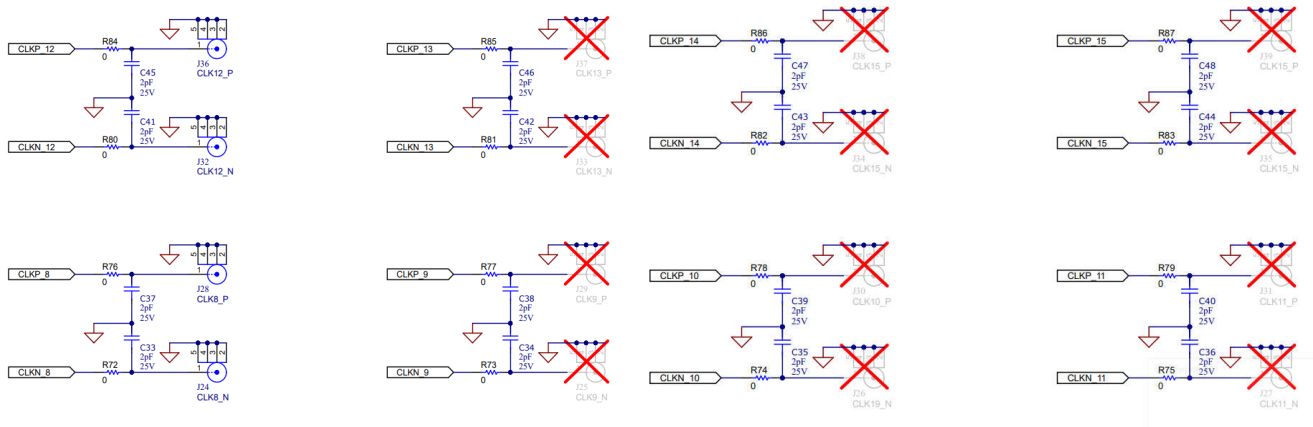


Figure 6-4. Clock Outputs CLK8 to CLK15

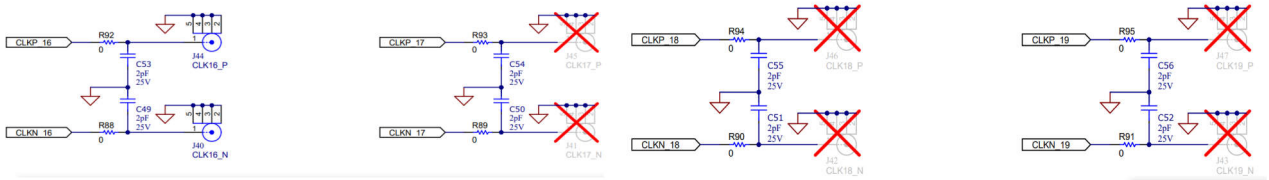


Figure 6-5. Clock Outputs CLK16 to CLK19

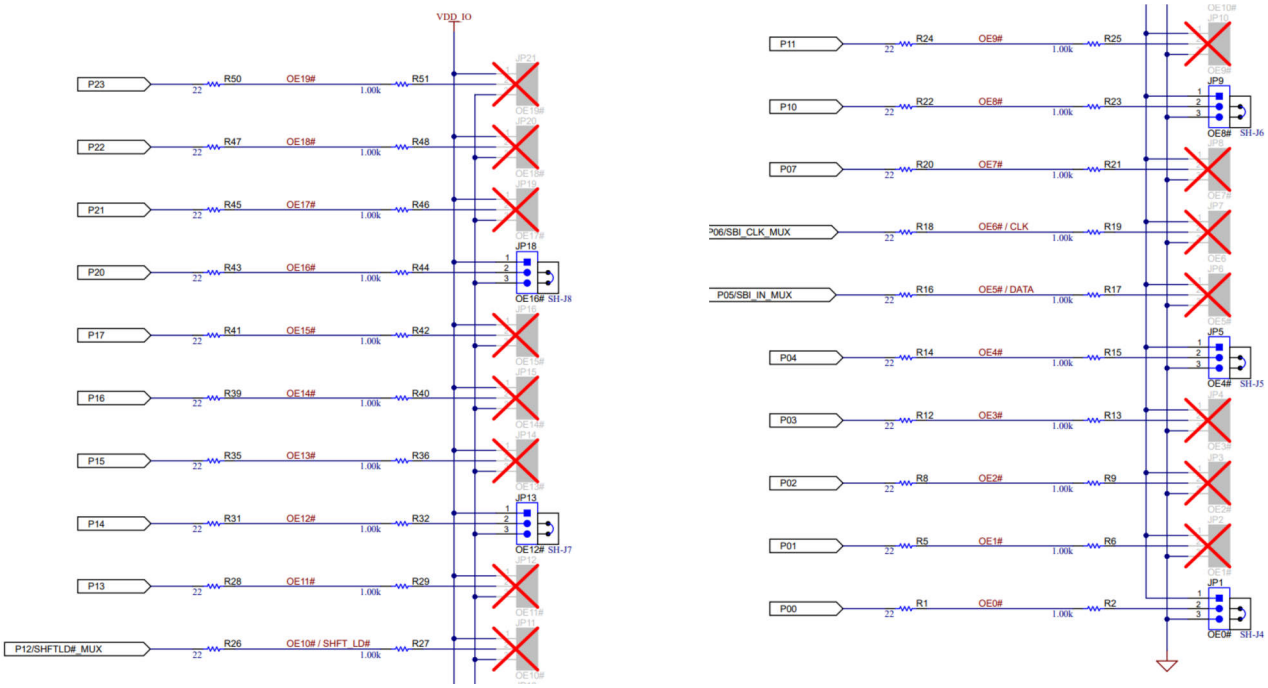


Figure 6-6. Output Enable Pins (OE#)

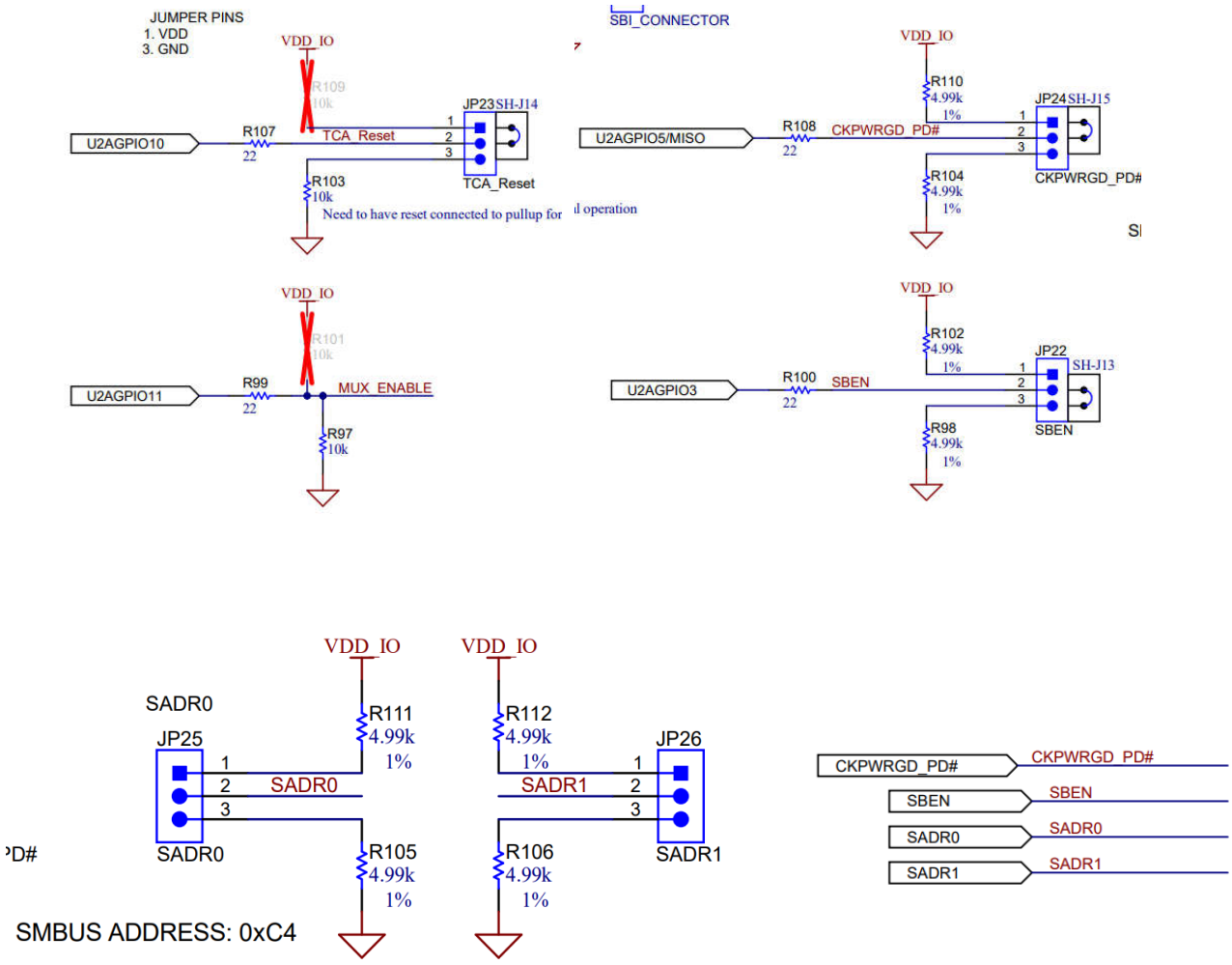


Figure 6-7. Logic I/O Jumpers

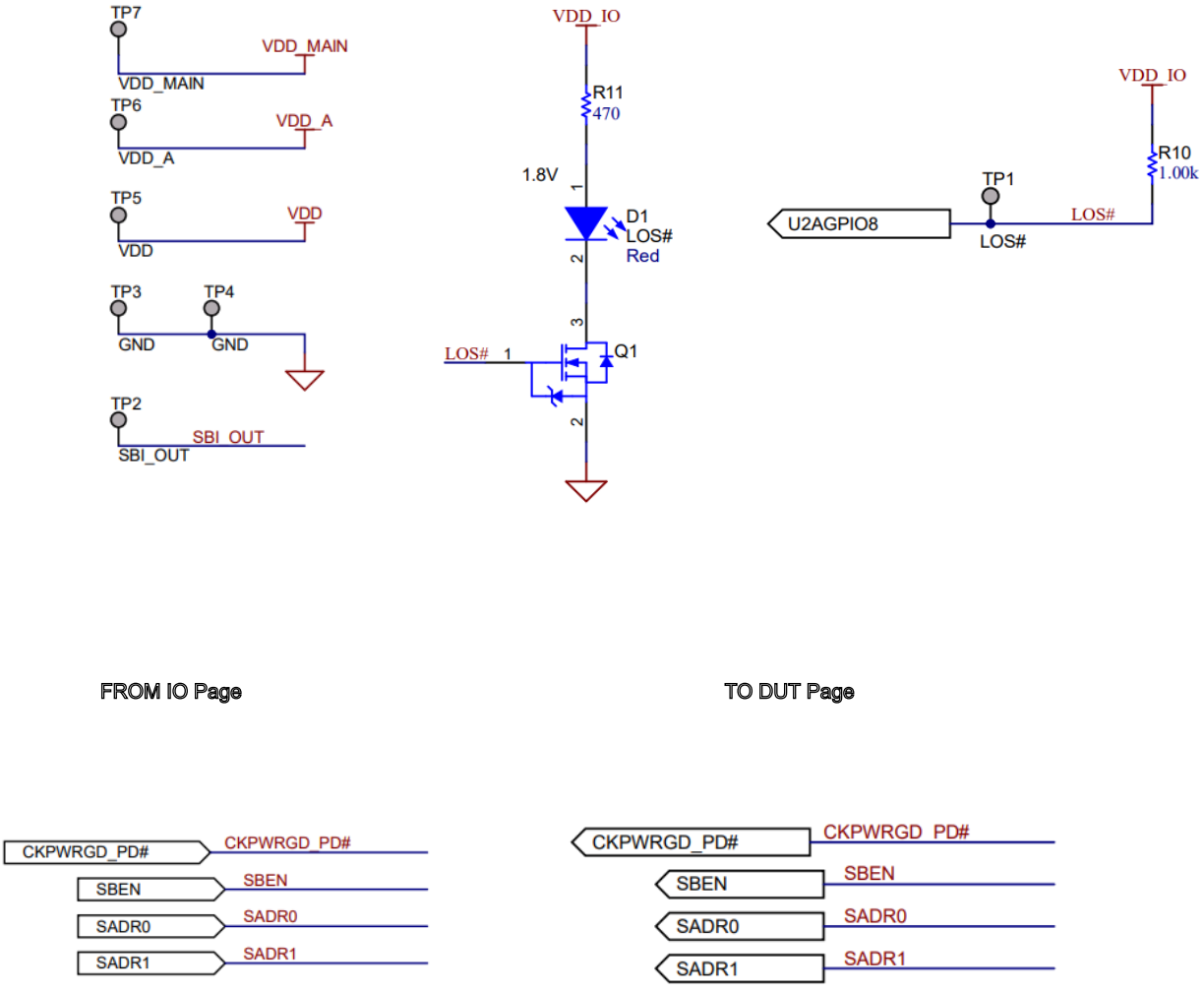


Figure 6-8. Status LEDs and Test Points

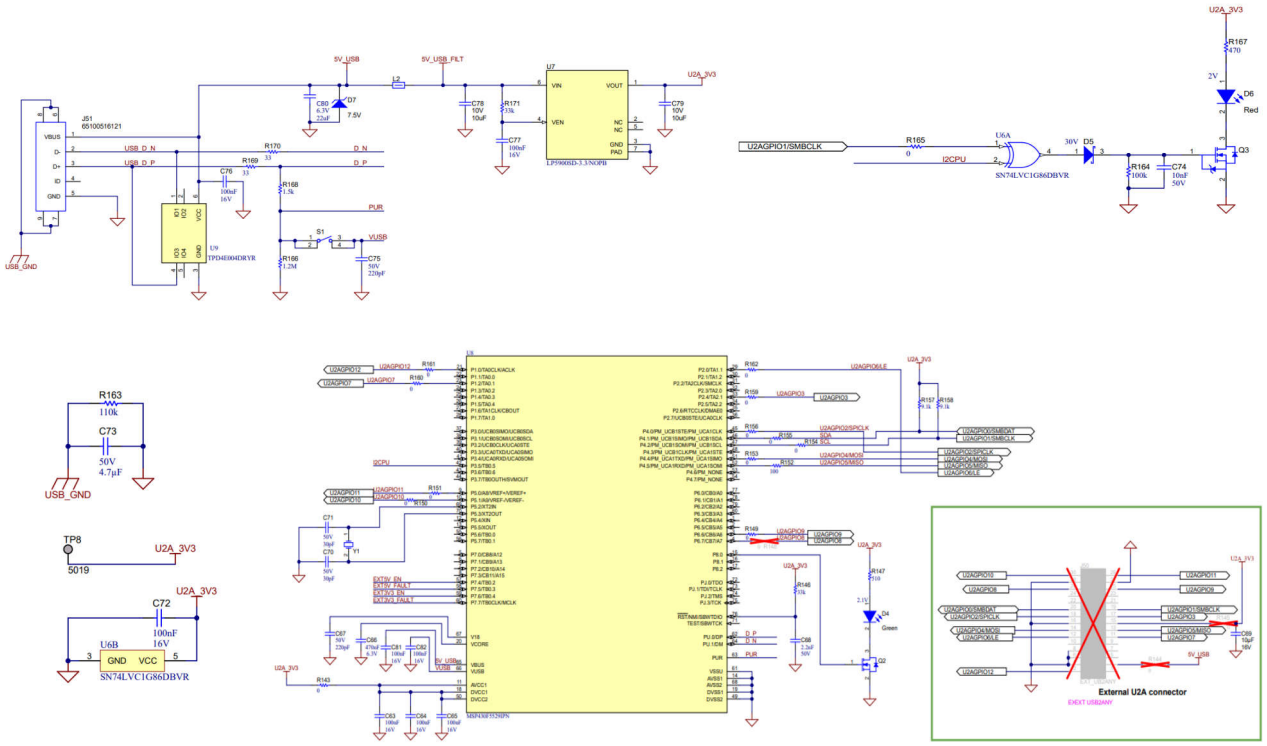


Figure 6-9. USB Schematic

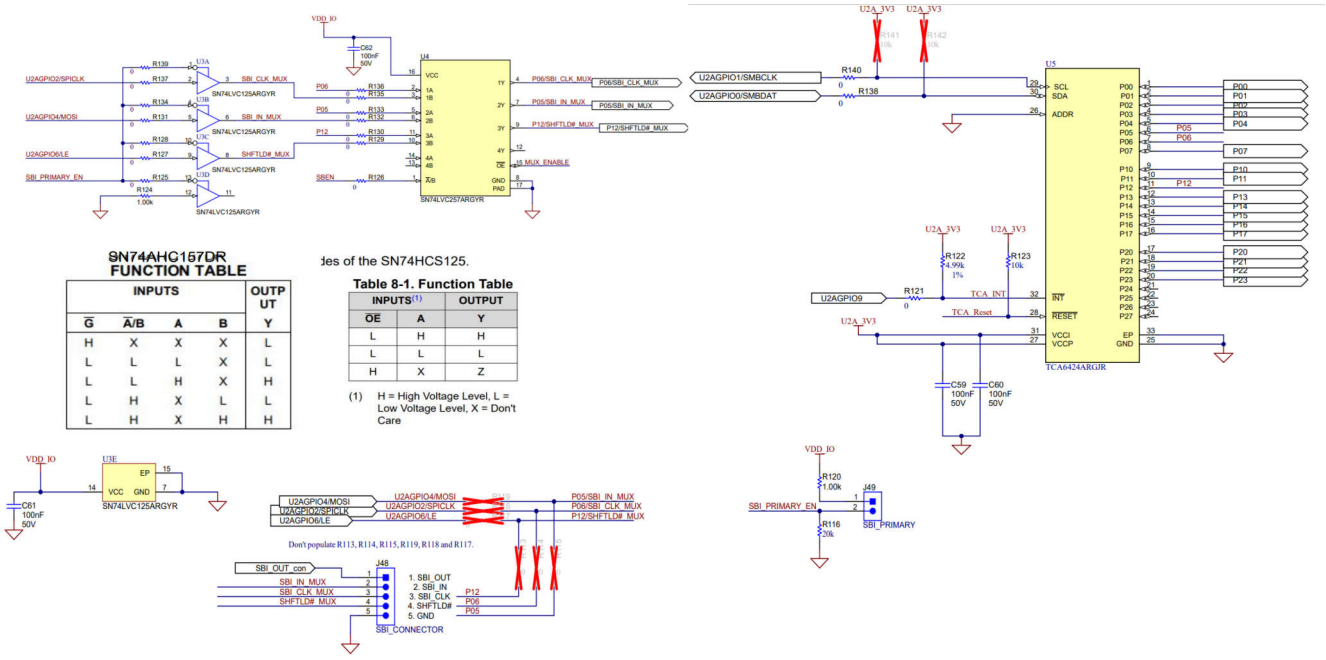


Figure 6-10. I/O Expander, MUX and Buffer used for SBI and OE pin Control

6.2 PCB Layouts

Layer Stackup :

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.80mil	3.5	
1	Top Layer	Copper	2.10mil		
	Dielectric 1	FR-4 High Tg	6.00mil	4.2	
2	GND 1	Copper	1.40mil		
	Dielectric 2	FR-4 High Tg	10.00mil	4.2	
3	Signal 1	Copper	1.40mil		
	Dielectric 3	FR-4 High Tg	18.60mil	4.2	
4	PWR	Copper	1.40mil		
	Dielectric 4	FR-4 High Tg	10.00mil	4.2	
5	GND 2	Copper	1.40mil		
	Dielectric 5	FR-4 High Tg	6.00mil	4.2	
6	Bottom Layer	Copper	2.10mil		
	Bottom Solder	Solder Resist	0.80mil	3.5	
	Bottom Overlay				

Figure 6-11. Layer Stackup

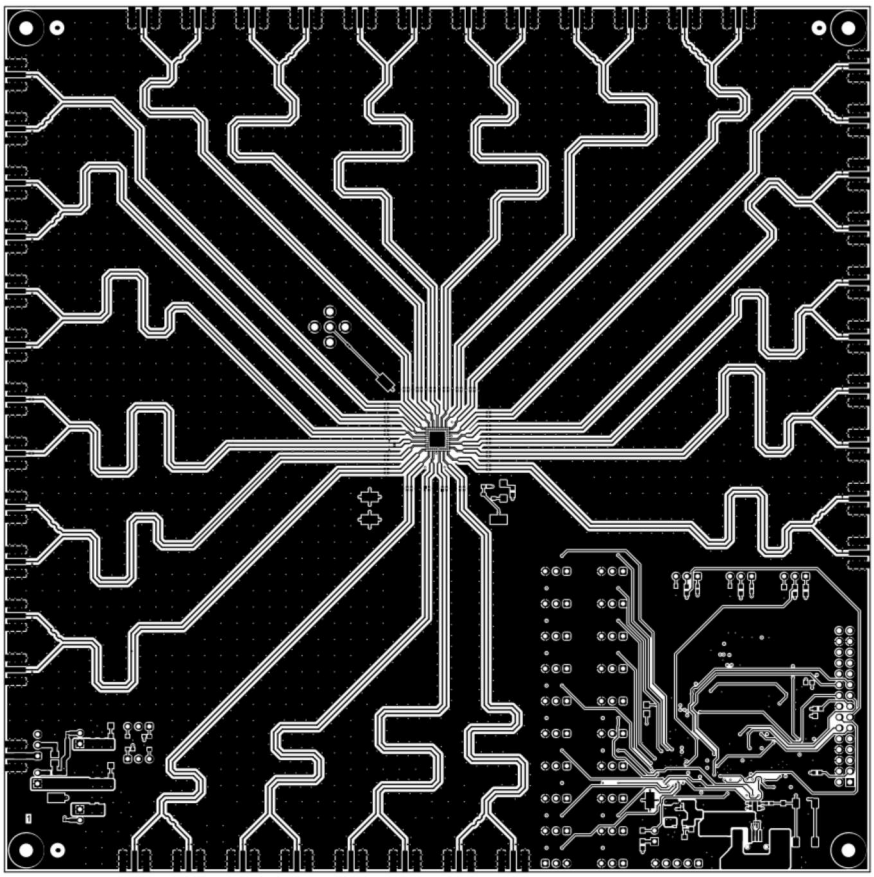


Figure 6-12. Top Layer (CLKIN / CLKOUT Signals)

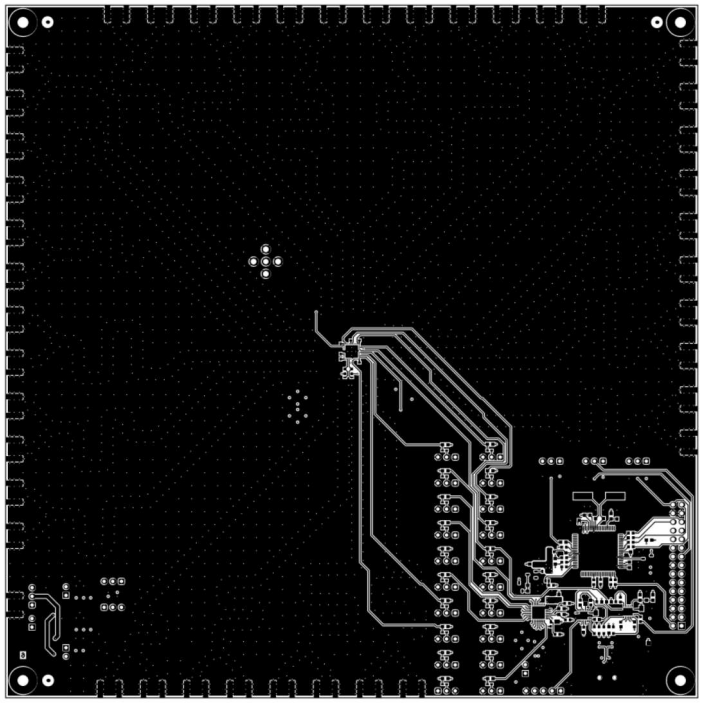


Figure 6-13. Bottom Layer

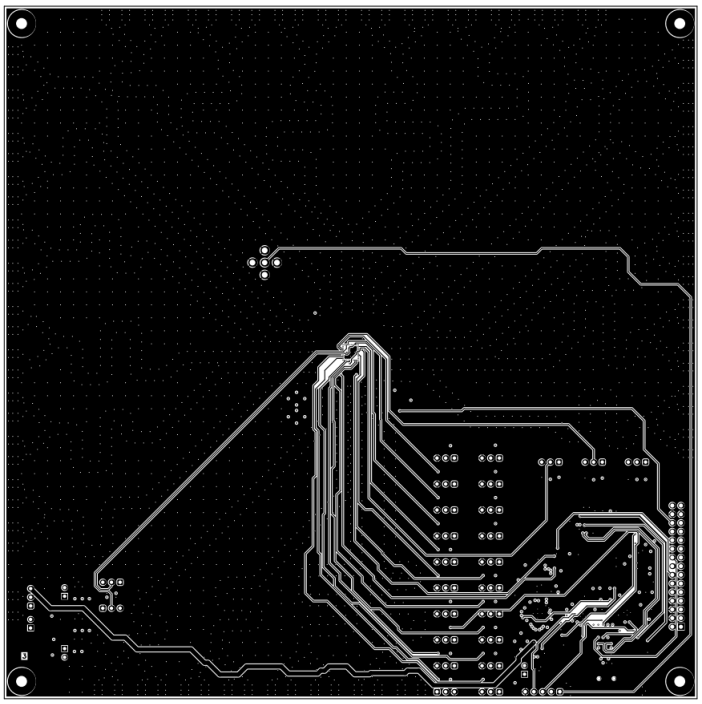


Figure 6-14. Signal 1 Layer

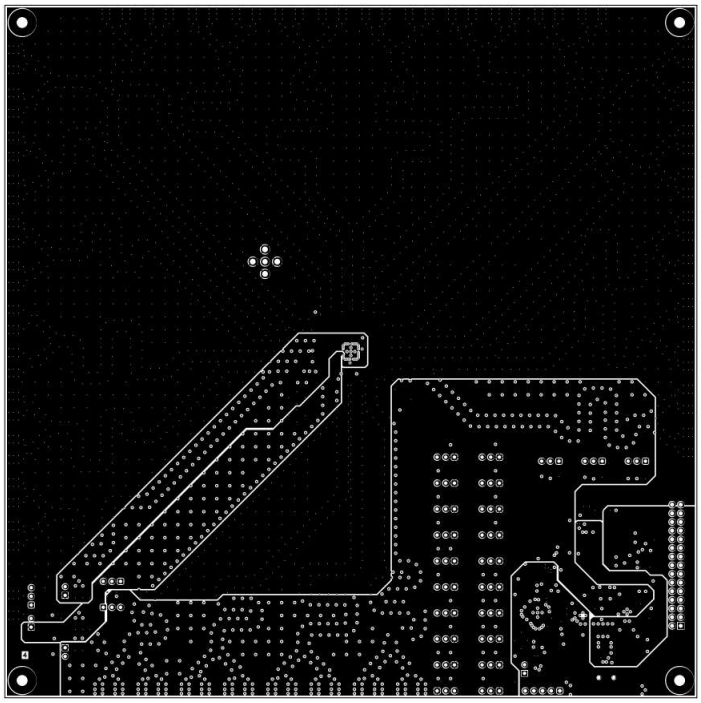


Figure 6-15. PWR Layer

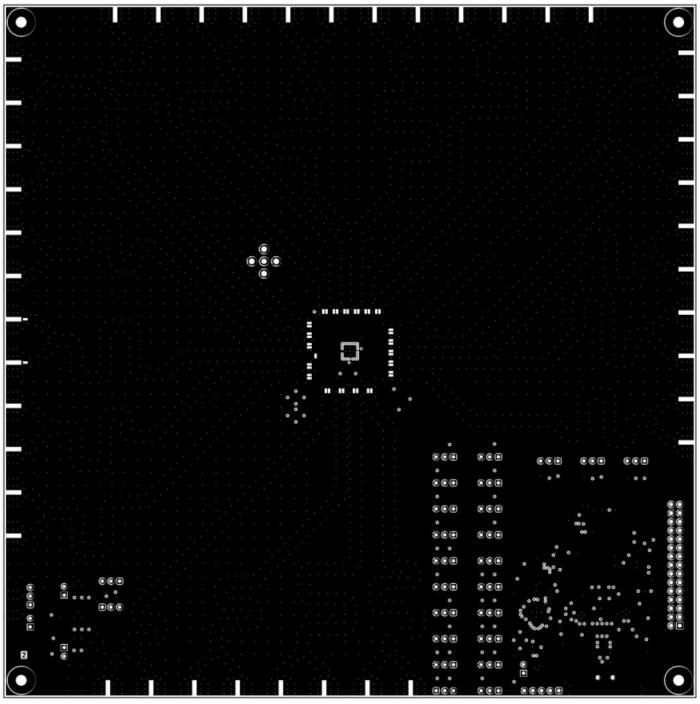


Figure 6-16. GND 1 Layer

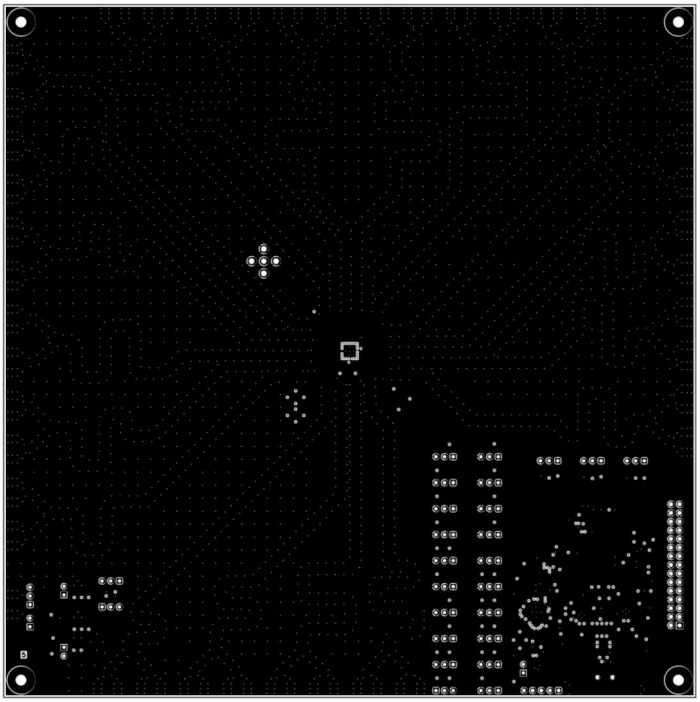


Figure 6-17. GND 2 Layer

6.3 Bill of Materials (BOM)

Table 6-1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C2	2	33pF	CAP, CERM, 33pF, 100V, +/- 5%, C0G/NP0, 0603	603	06031A330JAT2A	AVX
C3, C4, C5, C6, C7, C8	6	0.1uF	CAP, CERM, 0.1uF, 16V, +/- 10%, X7R, 0402	402	0402YC104KAT2A	AVX
C13, C14, C69	3	10uF	CAP, CERM, 10µF, 16V,+/- 20%, X6S, 0603	603	GRM188C81C106MA73D	MuRata
C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56	40	2pF	Ceramic Capacitor 2pF ±0.1pF 25V C0G 0201 (0603 Metric)	201	GJM0335C1E2R0BB01D	Murata
C57, C58	2	1uF	CAP, CERM, 1µF, 25V,+/- 20%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E1X7R1E105M080AC	TDK
C59, C60, C61, C62	4	0.1uF	CAP, CERM, 0.1uF, 50V, +/- 20%, X7R, 0805	805	08055C104MAT2A	AVX
C63, C64, C65, C72, C76, C77, C81, C82	8	0.1uF	CAP, CERM, 0.1uF, 16V, +/- 5%, X7R, 0603	603	C0603C104J4RACTU	Kemet
C66	1	0.47uF	CAP, CERM, 0.47µF, 6.3V,+/- 10%, X7R, 0603	603	0603B474K6R3CT	Walsin
C67, C75	2	220pF	CAP, CERM, 220pF, 50V, +/- 1%, C0G/NP0, 0603	603	06035A221FAT2A	AVX
C68	1	2200pF	CAP, CERM, 2200pF, 50V, +/- 10%, X7R, 0603	603	C0603C222K5RACTU	Kemet
C70, C71	2	30pF	CAP, CERM, 30pF, 50V, +/- 5%, C0G/NP0, 0603	603	06035A300JAT2A	AVX
C73	1	4.7uF	CAP, CERM, 4.7µF, 50V,+/- 10%, X7R, 1206	1206	C3216X7R1H475K160AE	TDK
C74	1	0.01uF	CAP, CERM, 0.01uF, 50V, +/- 5%, X7R, 0603	603	C0603C103J5RACTU	Kemet
C78, C79	2	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X6S, 0603	603	GRM188C81A106MA73D	MuRata
C80	1	22µF	Multilayer Ceramic Capacitor 22uF 6.3V X6S 20% SMD 0805 T/R	805	JMK212BC6226MG-T	Taiyo Yuden
D1	1	Green	LED, Green, SMD	1206	CTL1206FGR2T	Venkel

Table 6-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
D2, D3, D6	3	Red	LED, Red, SMD	Red 0805 LED	LTST-C170KRKT	Lite-On
D4	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On
D5	1	30V	Diode, Schottky, 30V, 0.2A, SOT-23	SOT-23	BAT54-7-F	Diodes Inc.
D7	1	7.5V	Diode, Zener, 7.5V, 500mW, SOD-123	SOD-123	MMSZ4693T1G	ON Semiconductor
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J2, J3, J4, J8, J12, J16, J20, J24, J28, J32, J36, J40, J44	13		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.
J5, J6, J7, J49	4		Header, 100mil, 2x1, Gold, TH	Header, 2x1, 100mil	5-146261-1	TE Connectivity
J48	1		Header, 2.54mm, 5x1, Gold, TH	Header, 2.54mm, 5x1, TH	61300511121	Wurth Elektronik
J51	1		Connector, Receptacle, USB Mini B 2.0, SMT	Connector, Receptacle, USB Mini B 2.0, 5 Position, SMT	65100516121	Wurth Elektronik
JP1, JP5, JP9, JP13, JP17, JP18, JP22, JP23, JP24, JP25, JP26	11		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
L1	1	330 ohm	Ferrite Bead, 330 ohm at 100MHz, 2A, 0805	805	742792037	Wurth Elektronik
L2	1	60 ohm	Ferrite Bead, 60 ohm at 100MHz, 3.5A, 0603	603	MPZ1608S600ATAH0	TDK
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
Q1, Q3	2	25V	MOSFET, N-CH, 25V, 0.22A, SOT-23	SOT-23	FDV301N	Fairchild Semiconductor
Q2	1	50V	MOSFET, N-CH, 50V, 0.22A, SOT-23	SOT-23	BSS138	Fairchild Semiconductor
R1, R5, R8, R12, R14, R16, R18, R20, R22, R24, R26, R28, R31, R35, R39, R41, R43, R45, R47, R50, R99, R100, R107, R108	24	22	RES, 22, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060322R0JNEA	Vishay-Dale
R2, R6, R9, R10, R13, R15, R17, R19, R21, R23, R25, R27, R29, R32, R36, R40, R42, R44, R46, R48, R51	21	1.00k	RES, 1.00 k, 1%, 0.1 W, 0402	402	ERJ-2RKF1001X	Panasonic

Table 6-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R3, R4, R121, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R143, R149, R150, R151, R153, R154, R155, R156, R159, R160, R161, R162, R165	32	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06030000Z0EA	Vishay-Dale
R7, R33, R37, R49, R52, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96	46	0	RES, 0, 5%, .05 W, AEC-Q200 Grade 0, 0201	201	ERJ-1GN0R00C	Panasonic
R11, R53, R54, R167	4	470	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603470RJNEA	Vishay-Dale
R55	1	2.2	RES, 2.20, 1%, 0.1 W, 0603	603	ERJ-3RQF2R2V	Panasonic
R97, R103, R116, R123	4	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060310K0JNEA	Vishay-Dale
R98, R102, R104, R105, R106, R110, R111, R112, R122	9	4.99k	RES, 4.99 k, 1%, 0.063 W, 0402	402	RC0402FR-074K99L	Yageo America
R120, R124	2	1.00k	RES, 1.00 k, 0.5%, 0.1 W, 0603	603	RT0603DRE071KL	Yageo America
R146, R171	2	33k	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060333K0JNEA	Vishay-Dale
R147	1	510	RES, 510, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603510RJNEA	Vishay-Dale
R152	1	100	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603100RJNEA	Vishay-Dale
R157, R158	2	9.1k	RES, 9.1 k, 5%, 0.1 W, 0603	603	RC0603JR-079K1L	Yageo
R163	1	110k	RES, 110 k, 1%, 0.25 W, 1206	1206	RC1206FR-07110KL	Yageo America
R164	1	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603100KJNEA	Vishay-Dale

Table 6-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R166	1	1.2Meg	RES, 1.2M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06031M20JNEA	Vishay-Dale
R168	1	1.5k	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04021K50JNED	Vishay-Dale
R169, R170	2	33	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW040233R0JNED	Vishay-Dale
S1	1		Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	SW, SPST 6x6 mm	FSM4JSMA	TE Connectivity
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15	15	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	8		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		PCIe Gen 1 to Gen 6 Ultra Low Jitter 1:20, LP-HCSL Clock Buffer and Clock MUX, TLGA80	TLGA80	LMKDB1120NPPT	Texas Instruments
U2	1		500mA, Low IQ, Small Size, Low Dropout Regulator, DQN0004A (X2SON-4)	DQN0004A	TLV75533PDQNR	Texas Instruments
U3	1		Quadruple Bus Buffer Gate With 3-State Outputs, RGY0014A, LARGE T&R	RGY0014A	SN74LVC125ARGYR	Texas Instruments
U4	1		Quadruple 2-Line To 1-Line Data Selector/Multiplexer With 3-State Outputs, RGY0016A (VQFN-16)	RGY0016A	SN74LVC257ARGYR	Texas Instruments
U5	1		Low-Voltage 24-Bit I2C and SMBus I/O Expander, 24 Outputs, 1.65 to 5.5V, -40 to 85 degC, 32-pin UQFN (RGJ), Green (RoHS & no Sb/Br)	RGJ0032A	TCA6424ARGJR	Texas Instruments
U6	1		Single 2-Input Exclusive-OR Gate, DBV0005A (SOT-23-5)	DBV0005A	SN74LVC1G86DBVR	Texas Instruments
U7	1		150mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	NGF0006A	LP5900SD-3.3/NOPB	Texas Instruments
U8	1		25MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	PN0080A	MSP430F5529IPN	Texas Instruments
U9	1		4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	DRY0006A	TPD4E004DRYR	Texas Instruments

Table 6-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
Y1	1		Crystal, 24.000MHz, 20pF, SMD	Crystal, 11.4x4.3x3.8mm	ECS-240-20-5PX-TR	ECS Inc.
C9, C11, C15	0	10uF	CAP, CERM, 10µF, 16V,+/- 20%, X6S, 0603	603	GRM188C81C106MA73D	MuRata
C10, C12, C16	0	1uF	CAP, CERM, 1µF, 25V,+/- 20%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E1X7R1E105M080AC	TDK
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J1	0		Connector, SMA, TH	SMA	142-0701-231	Cinch Connectivity
J9, J10, J11, J13, J14, J15, J17, J18, J19, J21, J22, J23, J25, J26, J27, J29, J30, J31, J33, J34, J35, J37, J38, J39, J41, J42, J43, J45, J46, J47	0		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.
J50	0		Header(shrouded), 2.54mm, 15x2, Gold, TH	Header(shrouded), 2.54mm, 15x2, TH	302-S301	On-Shore Technology
JP2, JP3, JP4, JP6, JP7, JP8, JP10, JP11, JP12, JP14, JP15, JP16, JP19, JP20, JP21	0		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
R30, R38	0	49.9	49.9 Ohms ±1% 0.05W, 1/20W Chip Resistor 0201 (0603 Metric) Automotive AEC-Q200 Thick Film	201	ERJ-1GNF49R9C	Panasonic Electronic Components
R34	0	100	RES, 100, 5%, 0.05 W, 0201	201	RC0201JR-07100RL	Yageo America
R101, R109, R141, R142	0	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060310K0JNEA	Vishay-Dale
R113, R114, R115, R117, R118, R119, R144, R145, R148	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06030000Z0EA	Vishay-Dale

7 Compliance Information

7.1 Compliance and Certifications

Refer to *LMKDB1120EVM EU Declaration of Conformity (DoC)*.

8 References

For additional information on LMKDB1120, refer to *LMKDB1120/1108/1104/1102/1204/1202 PCIe Gen 1 to Gen 6 Ultra Low Jitter 1:20, 1:8, 1:4, 1:2, 2:4, 2:2 LP-HCSL Clock Buffer and Clock MUX*

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2023) to Revision A (October 2024)	Page
• Added explanation for pin functionality when SBI Mode is enabled	7
• Updated resistor that needs to be populated when using a signal generator as clock input to EVM	9
• Added *Device Info* section	12
• Added newly exposed register and explanation for setup of controlling output slew rate control	14

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