User's Guide

CC35xxE Hardware Integration

ABSTRACT

This document provides the necessary WLAN and *Bluetooth*® Low Energy hardware operation information to aid in system design. This is a review of the integration process of TI's CC35xxE devices into final product PCB. When designing your own system around the TI chipset, it is recommended to step through the guidelines outlined below.

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1 Introduction

1.1 Overview

The SimpleLink™ Wi-Fi™ CC35xxE family of devices is where affordability meets reliability, enabling engineers to connect more applications with confidence. CC35xxE devices are available in a single-chip package, integrating both Wi-Fi 6 and Bluetooth Low Energy (BLE) 5.4. The following devices are also pin to pin compatible within their packaging family:

Table 1-1. CC35xxE Wireless MCU Device Comparison

Device	Feature			
	WLAN 2.4GHz	Bluetooth Low Energy 5.4	WLAN 5GHz	EXPANSION PSRAM
CC3500ENJARSHR	✓			
CC3501ENJARSHR	✓	✓		
CC3501ESIARSHR	✓	✓		2MB
CC3501ETIARSHR	✓	✓		8MB
CC3550ENJARSHR	✓		✓	
CC3551ENJARSHR	✓	✓	✓	
CC3551ESIARSHR	✓	✓	✓	2MB
CC3551ETIARSHR	✓	✓	✓	8MB

This guide walks through the hardware requirements and recommendations for integrating CC35xxE devices.

2 Schematic Considerations - CC35xxE IC

The CC35xxE SimpleLink™ Wi-Fi 6 and Bluetooth® Low Energy wireless MCUs are ideal for use in cost-sensitive embedded applications with RTOS software. CC35xxE brings the efficiency of Wi-Fi 6 to embedded device applications for the internet of things (IoT), with a small PCB footprint and highly optimized bill of materials. The combination of an Arm® Cortex®-M33 processing core at 160 MHz, RF core running WLAN/BLE, and a wide selection of peripherals makes the CC35xxE specifically designed for single-chip implementation of shared Wi-Fi and Bluetooth Low Energy communication.

The minimum requirements for optimized engine area schematic is explained in this section.

2.1 Schematic Reference Design

It is recommended to follow the provided CC35xxE reference design and guidelines as close as possible to achieve the capabilities of the CC35xxE listed in the device-specific data sheet as well as to pass certification. The recommended schematic designs for both the CC350xE and CC355xE can be accessed here:

LP-EM-CC35x1 Reference Design Files

The reference schematics for the CC350xE and CC355xE are shown below.

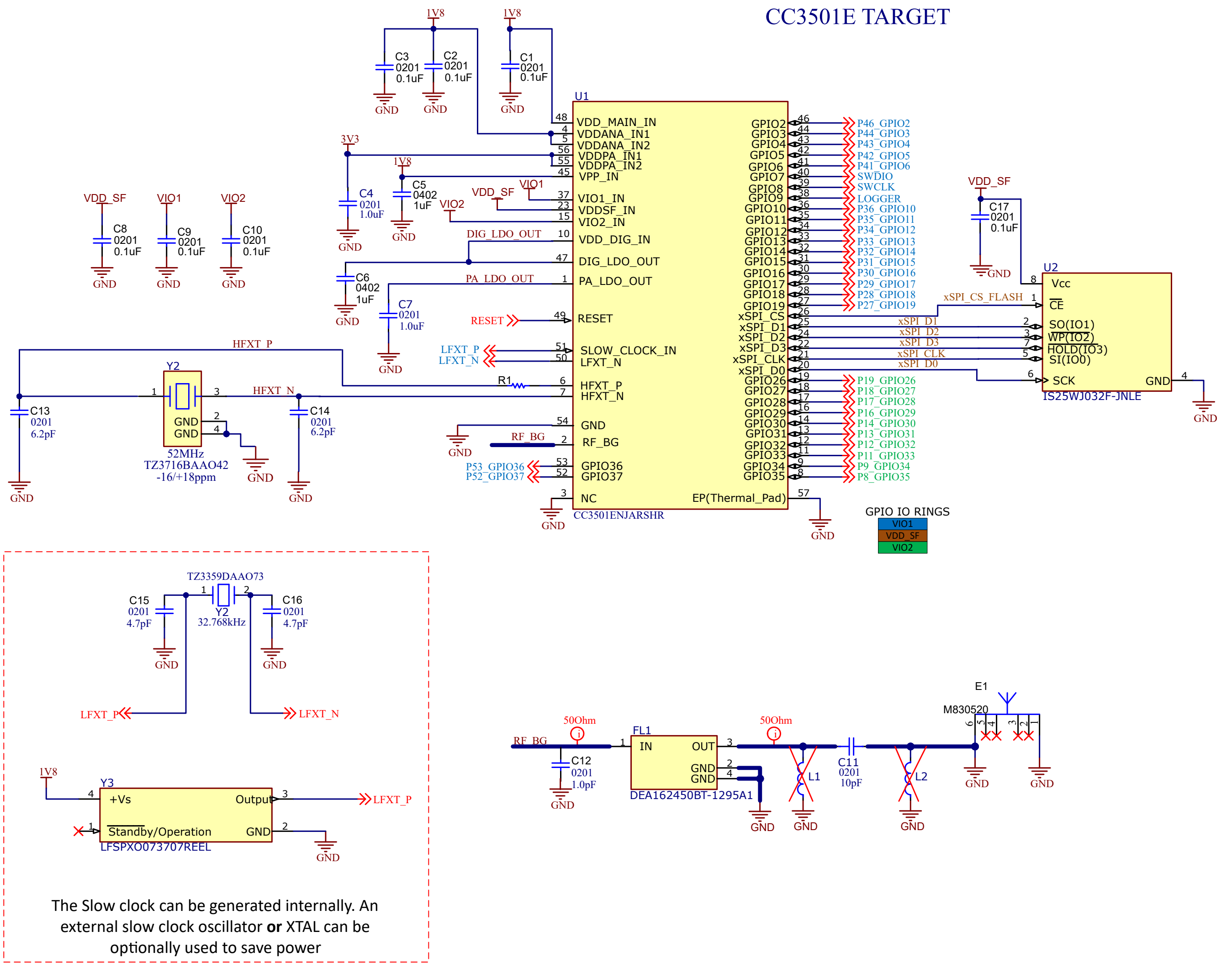

Figure 2-1. CC350xE Reference Schematic

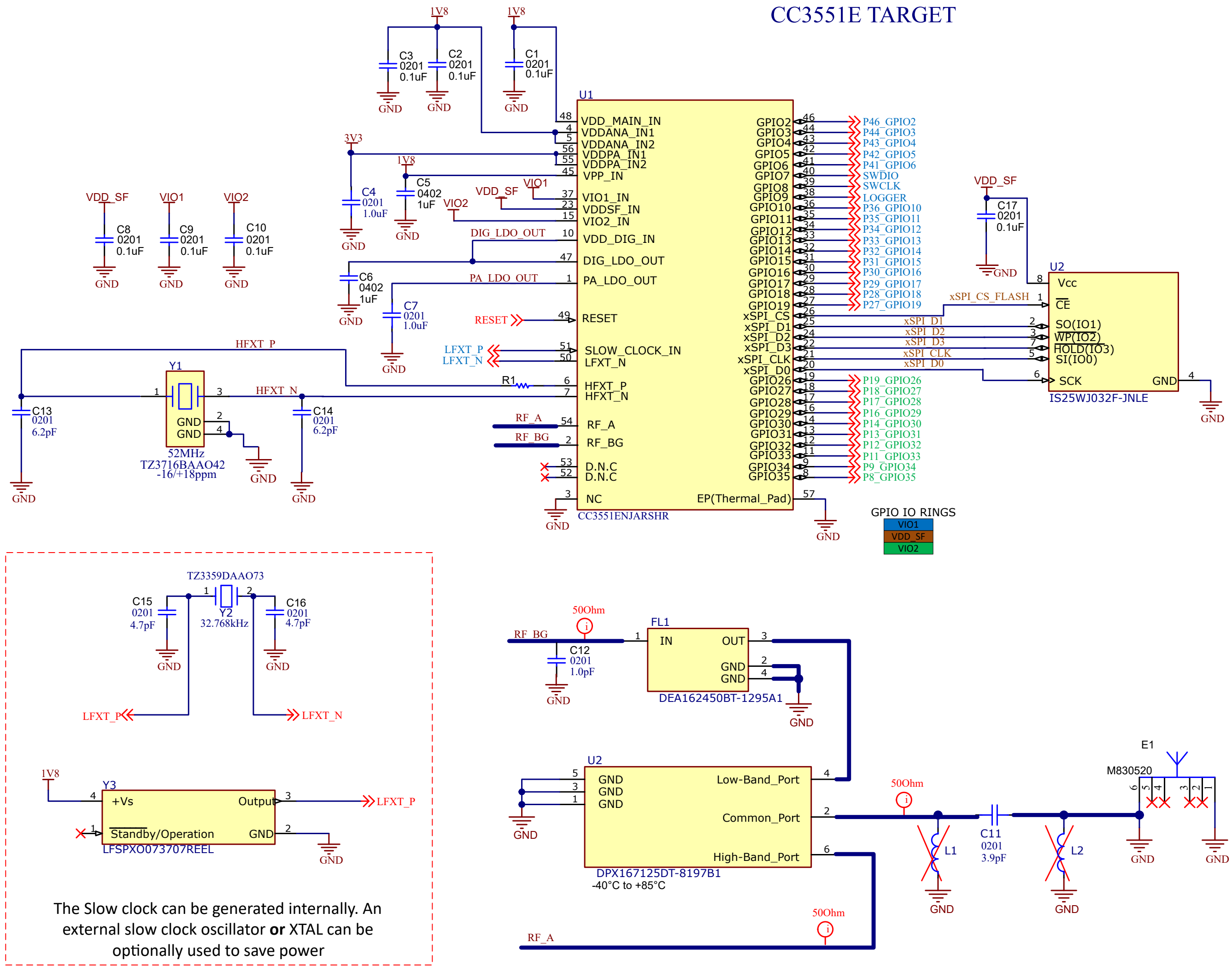

Figure 2-2. CC355xE Reference Schematic

1. RF Shield recommended for optimal regulatory compliance.

2. The only difference between the schematics for the CC350xE and CC355xE is the added diplexer U2 for 5GHz support in the CC355xE. For more information on the RF section of the schematic see Section 2.4.

Table 2-1. Bill of Materials

DESIGNATOR	QUANTITY	VALUE	PART NUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
C1, C2, C3, C8, C9,C10, C17	7	0.1µF	GRM033C71A104KE14D	Murata	CAP, CERM, 0.1µF, 10V, +/-10%, X7S, 0201	0201
C4, C7	2	1µF	GRM033D70J105ME01D	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 1.0µF, X7T, +22%/-33%, 20%, 6.3V	0201
C5, C6	2	1µF	GRM155R70J105MA12D	Murata	CAP, CERM, 1µF, 6.3V, +/-20%, X7R, 0402	0402
C11	1	3.9pF	GRM0335C1E3R9BA01	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 3.9pF, C0G	0201

Table 2-1. Bill of Materials (continued)

DESIGNATOR	QUANTITY	VALUE	PART NUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
C12	1	1.0pF	GRM0335C1E1R0CA01	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 1.0pF, C0G, 25V	0201
C13, C14	2	6.2pF	GRM0335C1E6R2BA01	Murata	CAP, CERM, 6.2pF, 25V, +/- 2%, C0G/NP0, 0201	0201
R1	1	150Ω	RC0201FR-7D150RL	Yageo America	RES, 150, 1%, 0.05W, 0201	0201
U1	1		CC3551ENJARSHR	Texas Instruments	CC355x 2.4GHz SimpleLink™ Wi-Fi 6 and Bluetooth Low Energy Wireless MCU	VQFN56
U2	1		DPX167125DT-8197B1	TDK	Multilayer Diplexer For 2.4-2.5GHz W-LAN and Bluetooth / 5-7GHz W-LAN	SMD6
U3	1		IS25WJ032F-JNLE [2]	ISSI	FLASH - NOR Memory IC 32Mbit SPI - Quad I/O, QPI, DTR 133MHz 6ns 8-SOP	SOIC8
Y1	1		TZ3716BAAO42	TAI-SAW TECHNOLOGY	Crystal Unit SMD 2.0x1.6 52.0MHz	SMT_XTAL_2MM05 _1MM65
FL1	1		DEA162450BT-1295A1	TDK	2.45GHz Center Frequency Band Pass RF Filter (Radio Frequency) 100MHz Bandwidth 1.8dB 0603 (1608 Metric), 3 PC Pad	SMT_FILTER_ 1MM60_0MM80
E1	1		M830520	Kyocera AVX	WLAN ANTENNA 802.11, SMD	A 802.11, SMD 8x3mm
Optional: Y2	1		TZ3359DAAO73	TAI-SAW TECHNOLOGY	Crystal Unit 1.6x1.0 Tuning Fork 32.768KHz	SMT2_1MM65_ 1MM05
Optional: C15,C16	2	4.7pF	GRM0335C1H4R7BA01 D	Murata	CAP, CERM, 4.7pF, 50V,+/- 3%, C0G/NP0, 0201	0201
Optional: Y3	1		LFSPXO073707REEL [(1)]	IQD Frequency Products	32.768kHz XO (Standard) CMOS Oscillator 1.8V Enable/Disable 4- SMD, No Lead	SMT4_2MM0_ 1MM6

(1) The slow clock can be generated internally. An external slow clock can be optionally used to consume less power than sourcing the slow clock internally.
(2) CC35xxE has dynamic support for different 1.8V flash types only. For more information, see Section 2.5.1.1

2.2 Power Supply

There are multiple voltage levels in use on the device to effectively optimize the power consumption of various modules operating in different power modes. Separate supplies allow users to use a DC/DC to source the 1.8V or an LDO depending on design focus (power efficiency or cost savings). The external power supplies are as follows:

- VDD_MAIN_IN, VDD_ANA_IN1, VDD_ANA_IN2, VPP: 1.8V
- VDDSF, V_{IO1}, V_{IO2}: 1.8V/ 3.3V
- V_{PA}: 3.3V

The VIO power supplies (VIO1, VIO2, VDDSF) provide split voltage rails for the device GPIOs. The VIO split rail I/O supply enables using a different I/O supply rail compared to the main VDDMAIN supply rail. This enables applications to interface with other system components at a different voltage level compared to the main VDDMAIN power supply level.

The VDDSF supply powers the IO supply for external Flash GPIOs only. VDDSF split rail I/O supply (independent from VIO1 + VIO2) enables using a different I/O supply rail compared to the main VDDMAIN supply rail. This enables applications to interface with external Flash at a different voltage level compared to the main VDDMAIN power supply level.

Note

Only 1.8V flashes are supported today. For more information, see Section 2.5.1.1

For further information on the operating conditions for the supply pins, see Table 2-2.

Table 2-2. Required Device Power

Pin	Signal	Dir (I/O)	Required Voltage (Typical)
1	PA_LDO_OUT	O	N/A
47	DIG_LDO_OUT	O	N/A
48	VDD_MAIN_IN	I	1.8V
4	VDD_ANA_IN1	I	1.8V
5	VDD_ANA_IN2	I	1.8V
45	VPP_IN	I	1.8V
23	VDDSF	I	1.8V/3.3V
55	PA_LDO_IN	I	3.3V
56	PA_LDO_IN	I	3.3V
37	VIO1	I	1.8V/3.3V
15	VIO2	I	1.8V/3.3V

Note

VIO2 and VDDSF must be set to 1.8V for **CC35x1ES** and **CC35x1ET** devices.

2.2.1 Power Input/Output Requirements

Supply connections are listed in descending order of criticality. Prioritize the bypass capacitor placements in this order to maximize RF performance.

- PA_LDO_OUT (pin 1) : Provide de-coupling capacitor (1.0uF)
- VDDA_IN1 (pin 4): Provide de-coupling capacitor (0.1uF)
- VDDA_IN2 (pin 5): Provide de-coupling capacitor (0.1uF)
- DIG_LDO_OUT (pin 47): Provide de-coupling capacitor (1.0uF)
- VPP_IN (pin 45): Provide de-coupling capacitor (1.0uF).
- VDD_MAIN_IN (pin 48): Provide de-coupling capacitor (0.1uF)
- VDDPA (pin 56): Provide de-coupling capacitor (1.0uF)
- VDDSF_IN (pin 23): Provide de-coupling capacitor (0.1uF)
- VIO1_IN (pin 37): Provide de-coupling capacitor (0.1uF)
- VIO2_IN (pin 15): Provide de-coupling capacitor (0.1uF)

2.2.1.1 LDO Recommendations

The recommendations for LDO selection are as follows:

- Sourcing minimum 500mA.
- Noise requirement does not exceed 500uVrms

2.2.2 Boot Sequence

For the CC35xxE to function correctly, the proper boot-up sequence should be followed. This boot sequence is dependent on how the CC35xxE device is configured in your system which can be in two modes:

2.2.2.1 Hosted Mode (Power up by reset pin)

CC35xxE device is controlled by an external host. In this configuration the following boot-up sequence should be followed:

Power Up by Reset Pin

The device is released from reset by de-asserting the reset pin. For proper operation of the device, perform the recommended power-up sequencing as follows:

1. All supplies (VDD_MAIN_IN, VDD_ANA_IN, V_{IO1}, V_{IO2}, VDDSF, V_{PA}) must be available before nReset is released.
2. For an external slow clock, ensure that the clock is stable before nReset is deasserted (high).
3. The nReset pin should be held low for at least 10 us after stabilization of the external power supplies.

2.2.2.2 Standalone Mode (Power up when supply above threshold)

CC35xxE device is the host in your system and not controlled by external MCU. In this configuration the following boot-up sequence should be followed:

Power Up by When Supply Above Threshold

In this configuration the VDD_ANA_IN pin and reset pin needs to be shorted to the VDD_MAIN_IN pin. The VDDSF needs to be shorted to either VDD_MAIN or V_{IO1} or V_{IO2}. When nRESET is shorted to the VMAIN supply, the CC35xxE device will recognize when the supply is stable (within recommended operating conditions). However, user must ensure that the VPA supply is within recommended operating conditions before enabling device either:

- 1ms after VDDMAIN/VIO/VDDSF are available
- Prior to or as soon as VDDMAIN is available

It is important to note:

- When either V_{IO1}, V_{IO2}, or VDDSF is 3.3V, it is important to ensure that the 3.3V is available <15ms after VDDMAIN reaches 1.8V. It is expected this will be the normal case in systems where the 1.8V supply is derived from the 3.3V supply.
- When reset is driven from an external source, it can be driven from 1.8V or 3.3V IO independently of V_{IO1} level.

Figure 2-3 shows the top-level block diagram for the CC35xxE in both configurations

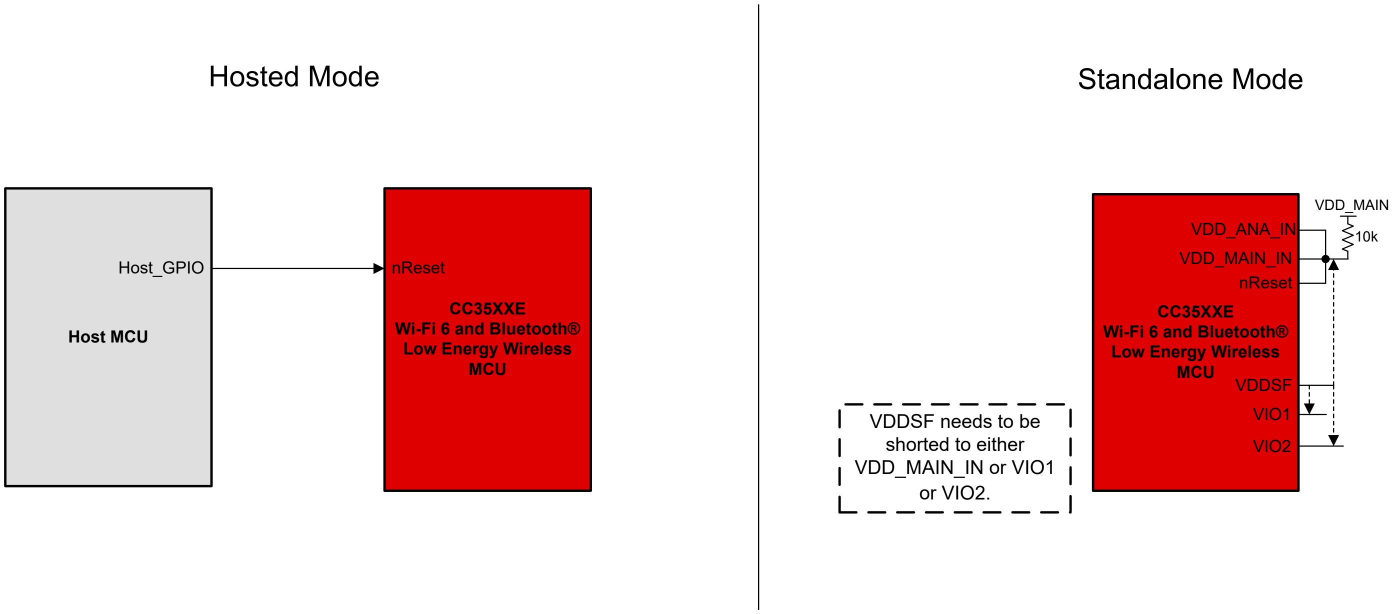

Figure 2-3. CC35xxE Configuration Options

2.2.2.3 SOP Modes

The Logger (pin 38) and GPIO_37 (pin 52) signals are considered to be Sense on Power pins. When connecting these pins, ensure GPIO_37 (pin 52) stay at logic level Low during power-up, and Logger (pin 38) stays at logic level High during power-up. If these pins are not used, there are no considerations as the CC35xxE device has these pins internally configured. For CC3551E users, Pin 52 and Pin 53 are "D.N.C". No considerations should be taken as the CC35xxE device has these pins internally configured.

2.3 Clock Source

The CC35xxE device uses two clocks for operation:

- A fast clock running at 52 MHz for WLAN/BLE and main MCU functions
- A slow clock running at 32.768 kHz for low power modes

The fast clock must be generated externally by an XTAL. The slow clock can be generated internally by the device or externally by an oscillator or XTAL.

It is important to note that a deviation in clock frequency is reflected as a deviation in radio frequency. For more information on doing frequency tuning with careful selection of external loading capacitors (C_L) depending on the layout, see *Simplelink Frequency Tuning*.

2.3.1 Fast Clock

The CC35xxE device supports a crystal-based fast clock (XTAL). The crystal is fed directly between HFXT_P and HFXT_M pins with appropriate loading capacitors and a 150Ω resistor. See the design requirements below:

1. Provide 150Ω resistor on HFXT_P (pin 6) close to the device and before the XTAL.
2. XTAL must be connected across HFXT_P (pin 6) and HFXT_N (pin 7).
3. Provide load capacitors (6.2pF) at both the pins of the XTAL. Note that the recommended load capacitor of 6.2pF is based on TI board layout.
4. Tuning of the load capacitance may be required depending on customer board layout.

   For further guidance on this topic, see *Simplelink Frequency Tuning*.

The Fast Clock component must meet the requirements shown in Table 2-3.

Table 2-3. External Fast Clock XTAL Specifications

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Supported frequencies			52		MHz

Table 2-3. External Fast Clock XTAL Specifications (continued)

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Frequency accuracy	Initial + temperature + aging			± 25/± 20 (2)	ppm
Load Capacitance, C_L (1)		5		13	pF
Equivalent series resistance, ESR				40	Ω
Drive level			100		µW

(1) Load capacitance, C_L= [C1*C2] / [C1 + C2] + C_P, where C1, C2 are the capacitors connected on HFXT_P and HFXT_M, respectively, and C_P is the parasitic capacitance (typically 1 to 2 pF). For example, for C1 = C2 = 6.2pF and C_P = 2pF, then C_L = 5pF.
(2) When choosing and XTAL in a design with CC350xE devices, the frequency accuracy requirement is ± 25 ppm. For CC355xE devices the requirement is ± 20 ppm.

2.3.2 Slow Clock

The slow clock is generated by the device internal oscillator, but an external oscillator or XTAL may be used as well.

2.3.2.1 Slow Clock Generated Internally

To minimize external components, the slow clock can be generated by an internal oscillator. However, this clock is less accurate and can lead to higher current consumption during Wi-Fi connected modes. For this scenario the SLOW_CLK_IN pin must be set to "Internal" in system configuration file (SYSCONFIG).

2.3.2.2 Slow Clock Using an External Oscillator

For optimal power consumption, the slow clock can be generated externally by an oscillator, XTAL, or sourced from elsewhere in the system. If using an oscialltor, the external source must meet the requirements listed below. This clock should be fed into the CC35xxE pin Slow_CLK_IN/ GPIO0 and should be stable before nReset is deasserted and device is enabled. The clock signal logic high should be the same voltage as VIO1 IO Ring.

Table 2-4. External Slow Clock Requirements

Parameter		Description	MIN	TYP	MAX	Unit
	Input slow clock frequency	Square wave		32.768		kHz
	Frequency accuracy	Inital + temperature + aging			±250	ppm
	Input Duty cycle		30%	50%	70%	
T_r/T_f	Rise and fall time	10% to 90% (rise) and 90% to 10% (fall) of digital signal level			100	ns
	Input impedence		1			MΩ
	Input capacitance				5	pF

2.3.2.3 Slow Clock Using an External Crystal (XTAL)

For optimal power consumption, the slow clock can be generated externally by an oscillator, XTAL, or sourced from elsewhere in the system. If using an XTAL, the external source must meet the requirements listed below. The crystal pins should be fed into the CC35xxE pins LFXT_P/ GPIO0 and LFXT_N/GPIO1.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supported frequencies			32.768		kHz
Frequency accuracy	Initial + temperature + aging	-250		250	ppm
Load Capacitance, C_L		3		12.5	pF
Equivalent series resistance, ESR				100	kΩ

2.4 Radio Frequency (RF)

For the CC350xE devices it is required to route out RF_BG (pin 2) for single band 2.4GHz for any radio frequency (RF) functionality. For the CC355xE devices the additional requirement is to route out RF_A (pin 54) for dual band 5GHz support.

On the RF_BG trace, a 1.0pF capacitor to ground, and a band pass filter (BPF) is required along this path before reaching any radiative or conductive component. For the recommended BPF, see Section 2.1. It is also recommended to implement an impedance matching network (such as a 'PI' or 'L' network) before the antenna for optimal RF performance.Figure 2-4 is an example of schematic design for the RF path when designing only for single band 2.4GHz (CC350xE). In this case you should ground pin 54 for optimal noise reduction.

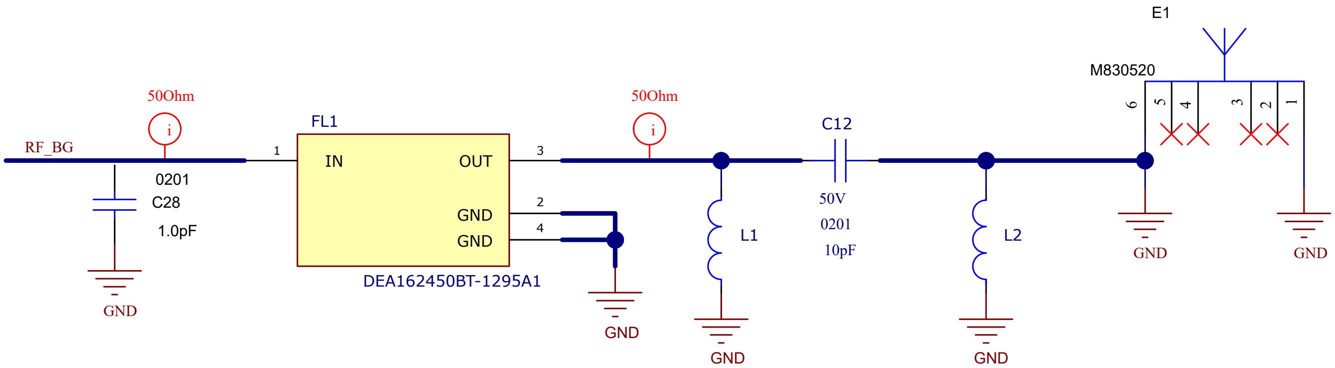

Figure 2-4. BG Band Reference Schematic

When designing with the CC355xE devices, additonal routing is needed for the RF_A pin (pin 54) to enable 5GHz RF with 2.4GHz RF band. In order to use both RF bands, a diplexer is needed. The RF_A pin should be connected directly to the High-Band port of the diplexer, while the RF_BG pin should be routed through a BPF (as described previously) then connected to the Low_Band port of the diplexer. For the recommended Diplexer, see Section 2.1.Figure 2-5 is an example of schematic design for the RF path when designing for dual band 2.4GHz + 5GHz (CC355xE).

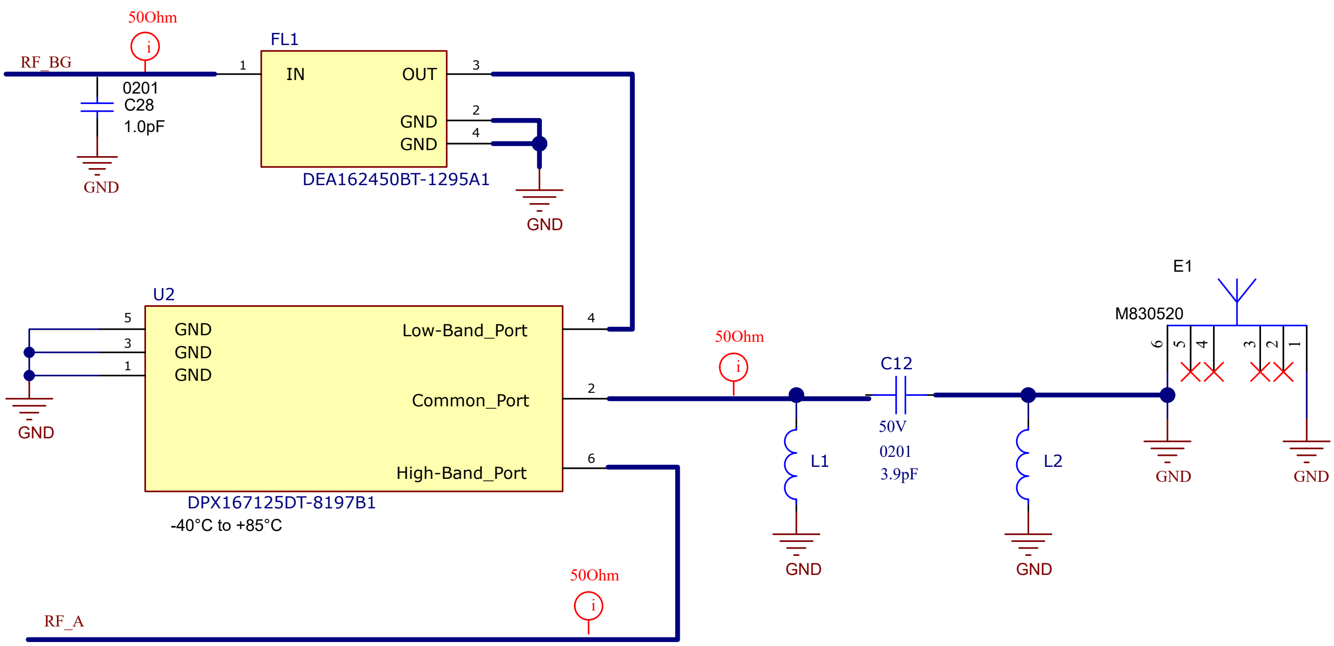

Figure 2-5. Dual Band RF Reference Schematic

Any deviation from these recommendations can cause performance to diverge from the data sheet specifications.

If implementing a RF switch (for utilizing antenna diversity), ensure that the input of the RF switch is the final filtered signal from the CC35xxE device. Specifically when designing dual band RF with the CC355xE, the input of the RF switch should be routed to the common port of the diplexer. When designing with the CC350xE for single band RF usage the input of the RF switch should be routed to the output of the BPF. ANT_SEL may be routed and used as the switching signal. As seen in Figure 2-6, the "RF_IN" signal should be connected to the output of the BPF when designing single band (CC350xE) and to the common port of the diplexer when designing dual band (CC355xE).

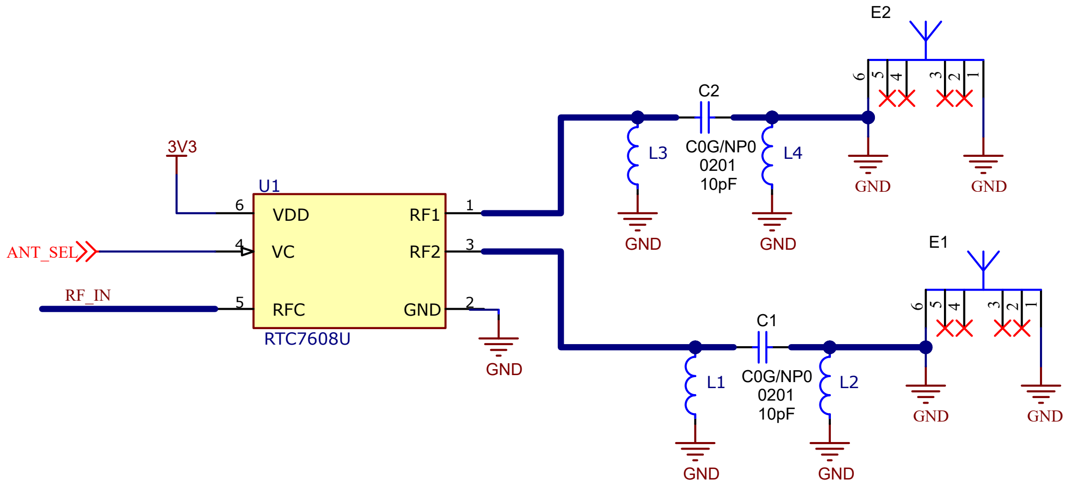

Figure 2-6. Antenna Diversity Reference Schematic

2.5 Digital Interfaces

All IO signals on CC35xxE can operate at 1.8V or 3.3V which is determined by VIO1 and VIO2. Take in consideration the use of level shifters if utilizing a higher voltage in your system.

2.5.1 xSPI

The xSPI Controller is a serial interface that allows communication on four data lines between the CC35xxE host MCU (M33) and an external Serial NOR flash device memory. The xSPI supports the QSPI mode which allows communication on 4 lines.

The xSPI supports the following features:

- XIP Mode selection and configuration
- Errors/events/status reports
- Data interface
  - Single/Burst incremental
  - Single outstanding transaction
  - Bus Master
  - Direct memory-mapped access only
- External Flash Interface:
  - SDR
  - 80MHz
  - Quad Data Lines

2.5.1.1 External Serial Flash

The external flash provides programmable, nonvolatile program memory for the device. Using the external flash allows the user to use saved network-specific data and avoids the need for a full start-up and network find-and-join process.

Figure 2-7 is sampled from the LP-EM-CC35X1 design files.

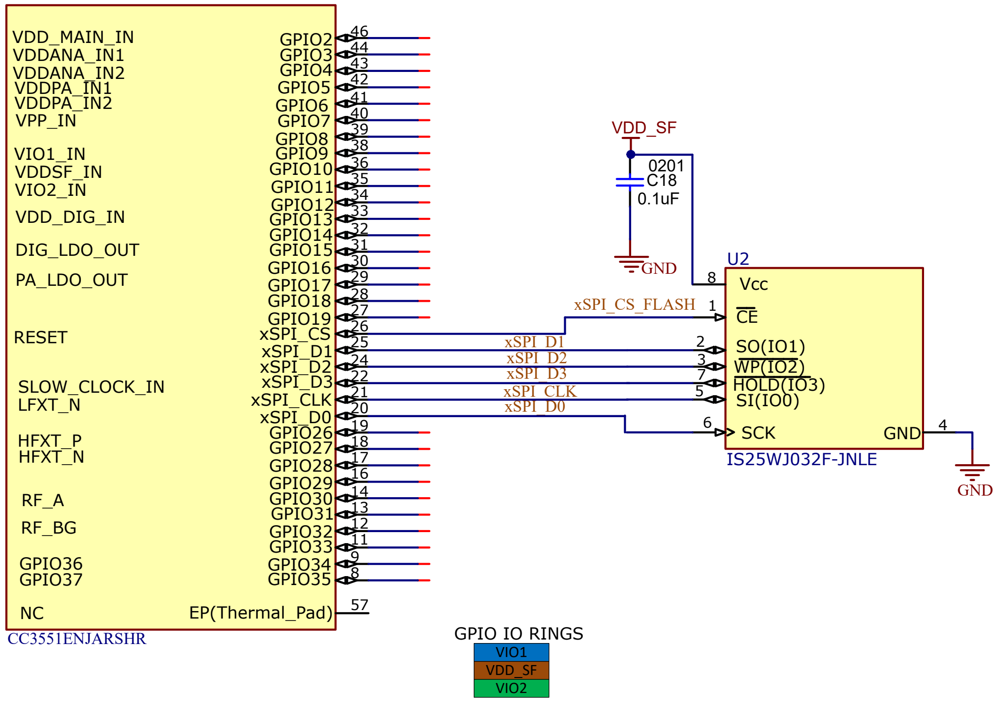

Figure 2-7. CC35xxE External Flash Recommendation

CC35xxE has dynamic support for different 1.8V flash types only. It is recommend to choose a flash from our dedicated list of supported flashes which can be found in the SDK release notes

2.5.2 Serial Wire Debug (SWD)

The two serial wire debug pins on CC35xxE include SWCLK (pin 39) and SWDIO (pin 40). These signals are used for used for programming, activation, debug, and non-signaling RF testing. These signals should be routed to headers.

2.5.3 Logger

The CC35xxE Logger pin (pin 38) is an output tracer for WLAN/BLE radio firmware logs. This is useful for in-depth debug of the firmware running on the CC35xxE, and TI provides parsers and documentaion for how to read these logs in the CC35xxE SDK release. There are other debugging tools as part of the driver, the firmware logs are normally not needed unless for deep debugging with TI. Connecting the Logger pin routed to a header is a good option for access in the event that these logs are needed.

2.5.4 Coexistence

The coexistence feature is a means to organize wireless packet traffic for communication protocols operating in the same frequency band. CC35xxE behaves as the Coex primary device and communicates to the Coex secondary device. CC35xxE supports a three-wire Packet Traffic Arbitration (PTA) interface for coexistence:

- COEX_GRANT - an input signal, controlled by the Coex primary device. Indicates the response of the PTA decision.
- COEX_PRIORITY - an output signal, controlled by the Coex secondary device. Indicates the priority of a request signal.
- COEX_REQ - an output signal, controlled by the Coex secondary device. Indicates a request to use the shared frequency band.

Please refer to the product data sheet for pin muxing options for Coexistence. These three signals on CC35xxE should be routed to the matching coexistence pins on the Coex secondary device. Coexistence is enabled by default and can be configured between internal and external in the INI file. Coexistence can be implemented with either one antenna (for both the primary and secondary device) or two antennas for each device. Figure 2-8 and Figure 2-9 provide visual examples of utilizing the coexistence feature.

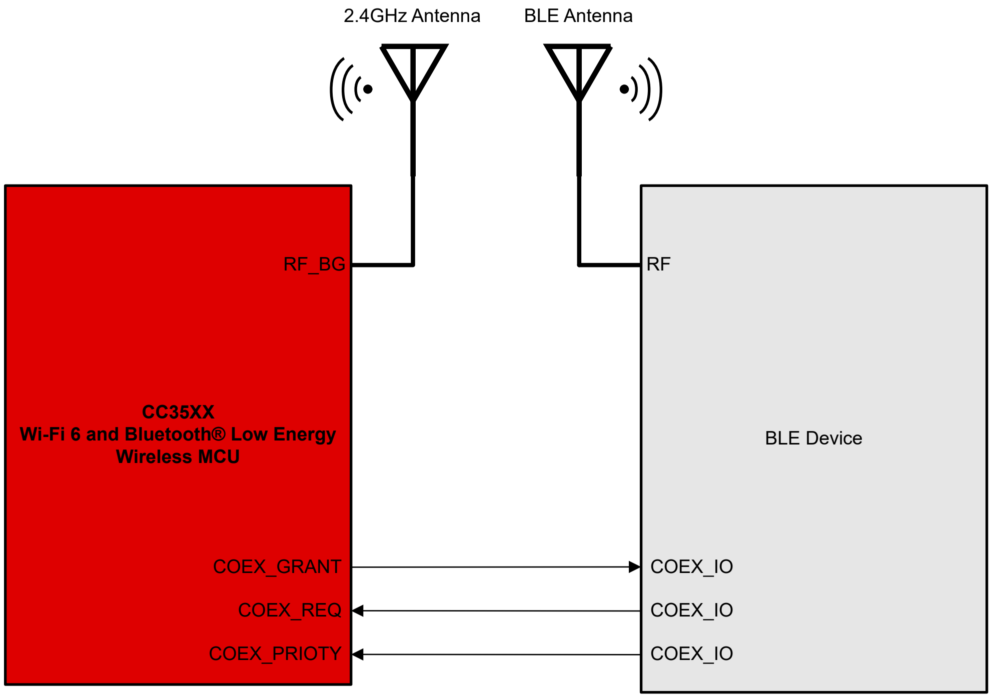

Figure 2-8. CC35xxE Coexistence With Dual Antennas

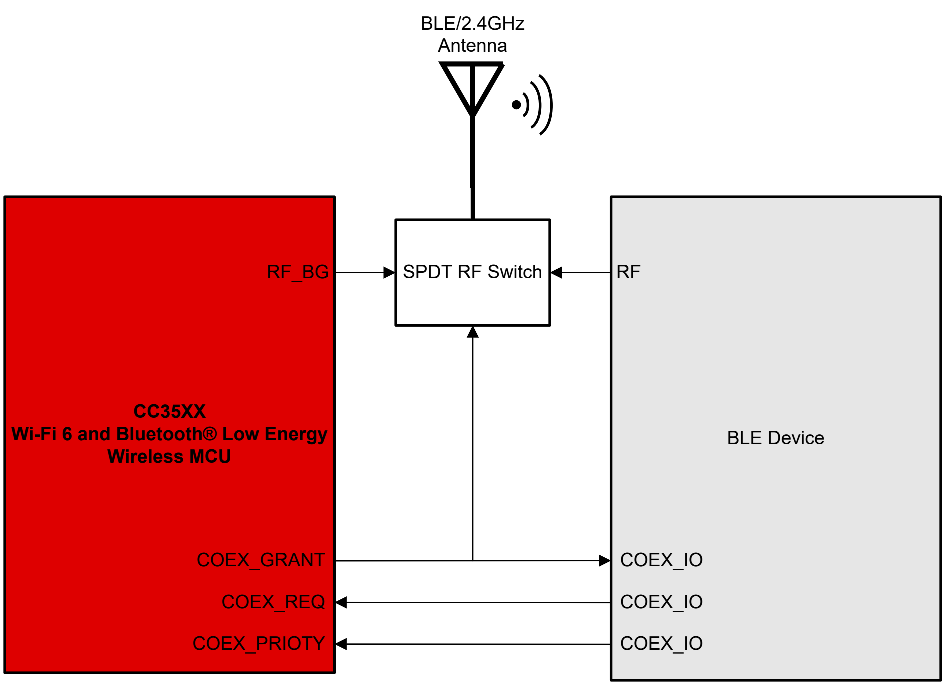

Figure 2-9. CC35xxE Coexistence With Single Antenna

2.6 Stacked PSRAM Variant

The stacked PSRAM variant (CC35x1ES/ET) a provides an extended RAM memory for the device. 2MB or 8MB of PSRAM is supported.

VIO2 and VDDSF must be set to 1.8V for **CC35x1ES** and **CC35x1ET** devices.

3 Layout Considerations - CC35xxE IC

The CC35xxE SimpleLink™ Wi-Fi 6 and Bluetooth® Low Energy wireless MCUs are ideal for use in cost-sensitive embedded applications with RTOS software. CC35xxE brings the efficiency of Wi-Fi 6 to embedded device applications for the internet of things (IoT), with a small PCB footprint and highly optimized bill of materials. The combination of an Arm® Cortex®-M33 processing core at 160 MHz, RF core running WLAN/BLE, and a wide selection of peripherals makes the CC35xxE specifically designed for single-chip implementation of shared Wi-Fi and Bluetooth Low Energy communication.

The minimum requirements for optimized engine area layout is explained in this section.

3.1 Layout Reference Design

It is recommended to follow the provided reference design and guidelines as close as possible in order to achieve the capabilities of the CC35xxE listed in the data sheet as well as to pass radio certification. These layout guidelines are especially important in the engine area, which includes the sensitive RF components and traces.

The following designs incorporate the layout guidelines given throughout this document. Refer to these as reference sources:

- LP-EM-CC35x1 Reference Design

The figures below include the engine area of CC35xxE on the top layer (layer 1) and ground layer (layer 2) for the designs. Note that the engine area as shown in the reference design can be rotated as necessary according to the design requirements.

Note

Before proceeding with any hardware build involving the CC35xxE, it is recommended to submit the design, both schematic and layout, for review.

3.1.1 Reference Design - CC355xE Dual Band Layout

Figure 3-1 is sampled from the LP-EM-CC35X1 design files.

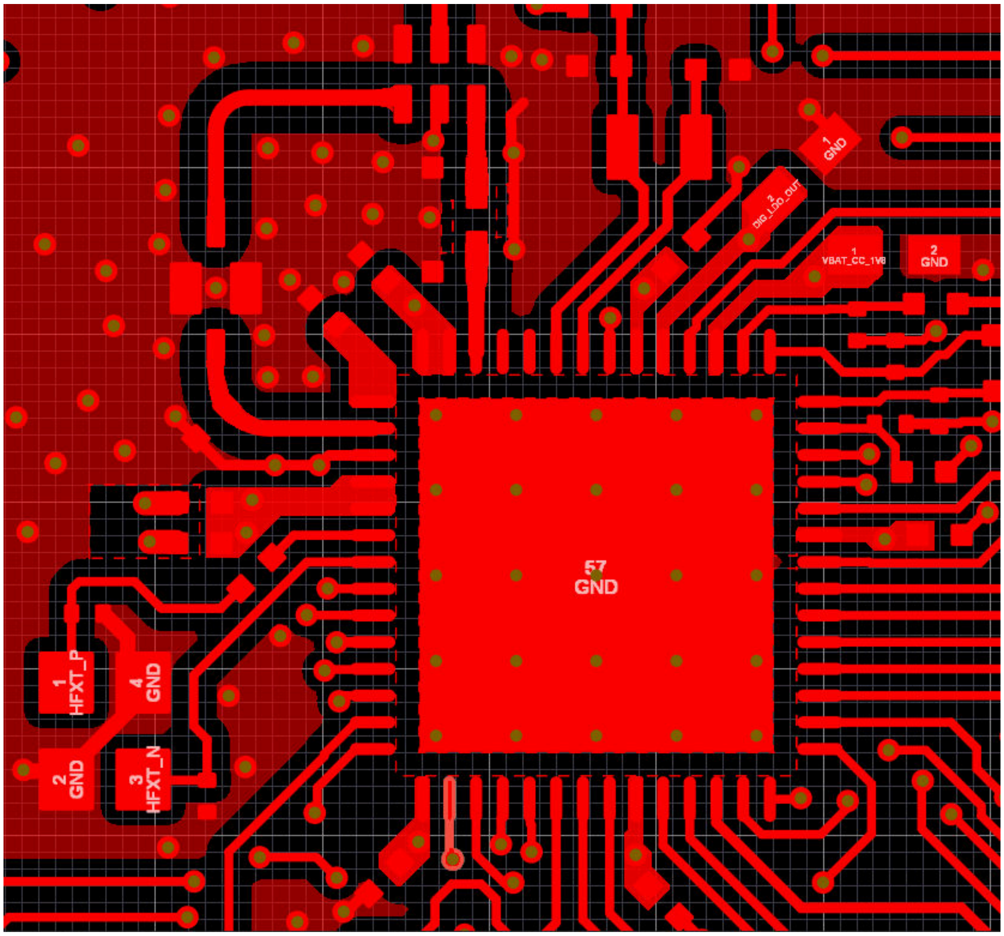

Figure 3-1. CC355xE Reference Design, Top (Layer 1)

Figure 3-2 is sampled from the LP-EM-CC35X1 design files.

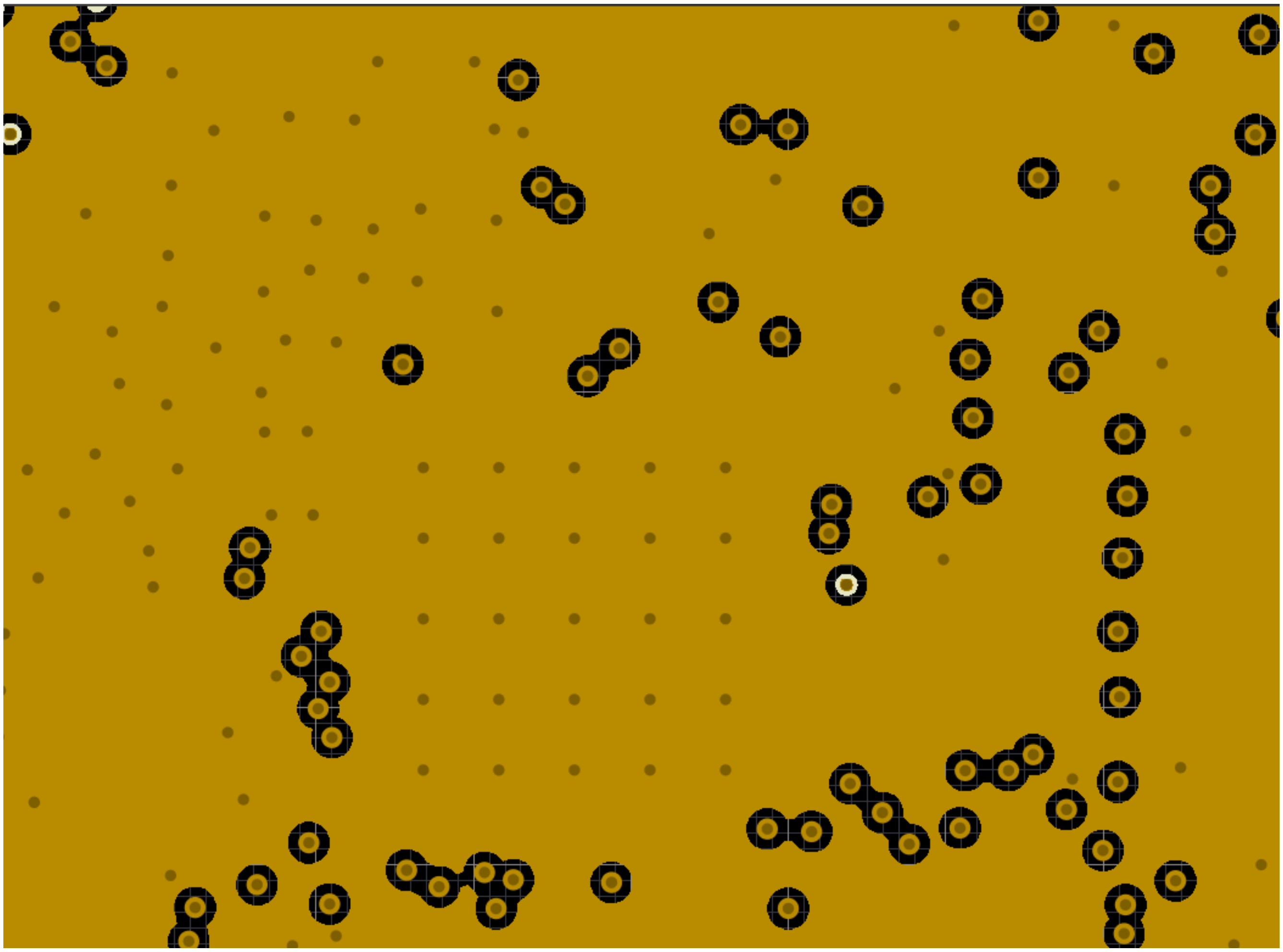

Figure 3-2. CC355xE Reference Design, Ground (Layer 2)

3.2 IC Thermal Pad

Underneath the IC, there should be one continuous ground plane on the top layer with 25 vias evenly distributed as shown in Figure 3-3. This is important for thermal dissipation and optimal RF performance.

Figure 3-3 is sampled from the LP-EM-CC35X1 reference design files.

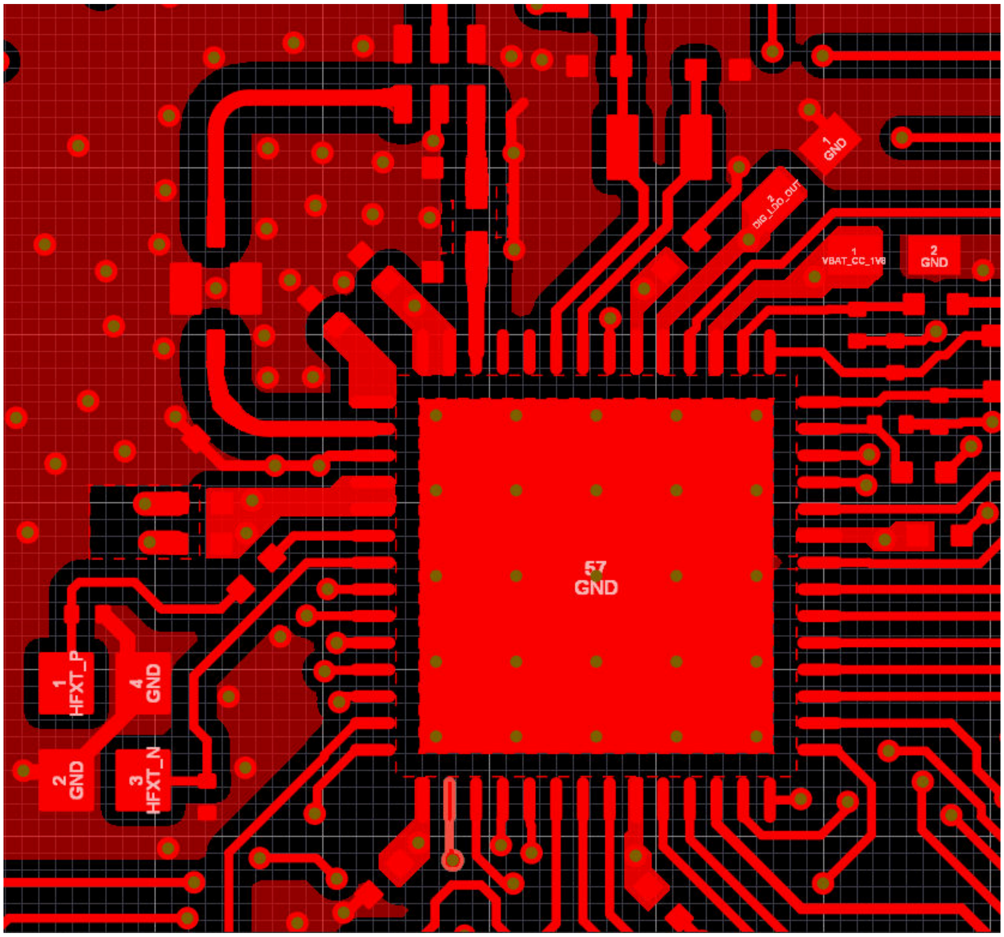

Figure 3-3. Reference Design Thermal Pad

3.3 Radio Frequency (RF)

The figure below show the RF section as it appears in the LP-EM-CC35x1 reference design. Special care must be taken when designing this area of the layout in order to achieve peak performance. A poor layout can cause performance degradation for the output power, EVM, sensitivity, and spectral mask.

Figure 3-4 is sampled from the LP-EM-CC35x1 reference design files. In the image below the blue traces are the RF_BG trace (2.4GHz), the yellow trace is the RF_A trace (5GHz), and the green trace is the combined RF trace connected to the common port of the diplexer, which should be routed to an antenna.

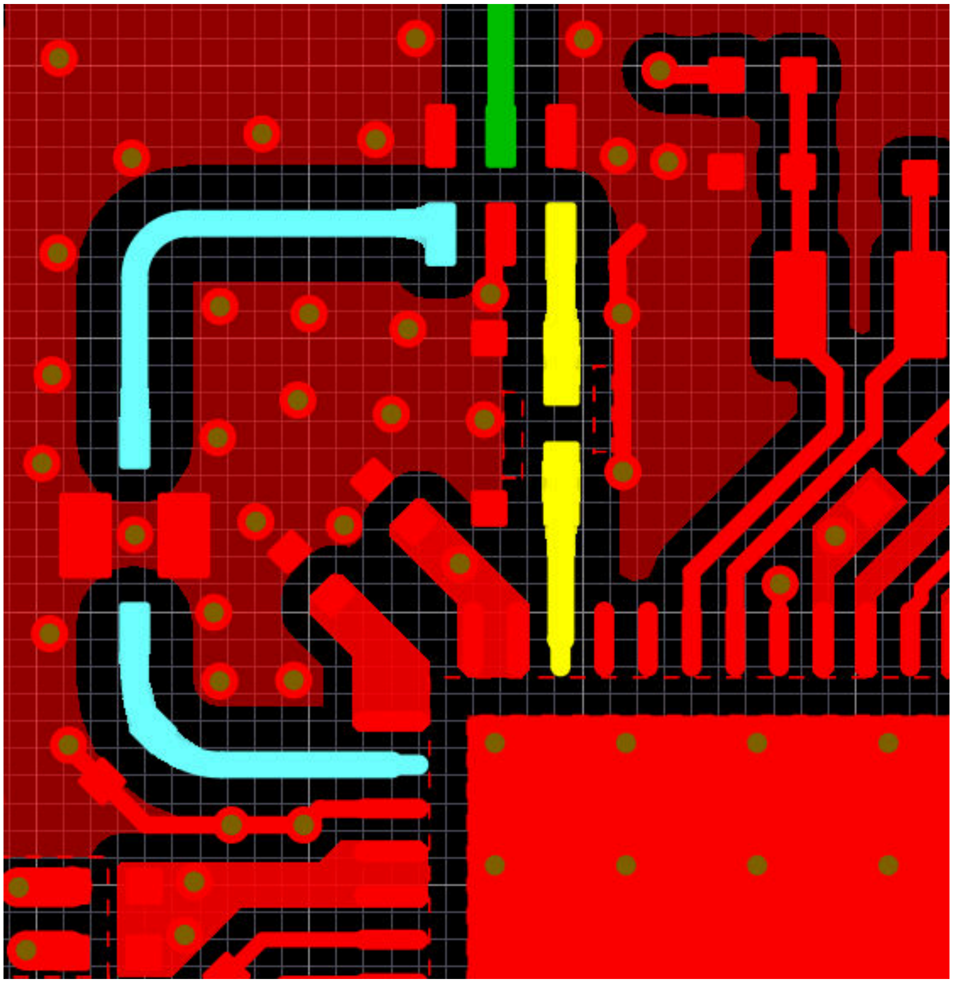

Figure 3-4. CC355xE Reference Design RF Path

In addition to following the reference design as close as possible, please comply with the guidelines listed below.

Note

The RF layout guidelines below are relevant for designs with the CC350xE and CC355xE, unless otherwise noted.

- The RF trace should have a constant 50 Ω characteristic impedance. This is achieved by matching the coplanar waveguide (CPWG) based on the dielectric, layer stackup, ground plane spacing, and trace thickness. These parameters should be consistent throughout the length of the trace.
- The entire RF trace should only be on the top layer of the PCB, and the layer immediately underneath should be one constant ground plane for the trace reference.
- The RF trace should be as clean and straight as possible with no components besides the band pass filter and matching filter before the antenna. This is to avoid unwanted component to component coupling. If a straight RF trace is not possible, rounded curves are acceptable.
- The RF trace should be as isolated as possible from other components to decrease noise. Ground planes should surround the RF trace, and distance between ground via stitching should be less than 1/8th of the minimum wavelength.
- The band pass filter should be as far as possible (within design space limits) from the RF_BG pin (pin 2) and the VDDA decoupling capacitors on pins 4 and 5.
- On the RF_BG (pin 2) trace, a 1.0pF capacitor to ground, should be place halfway between the band pass filter and IC pin.
- A ground via should be placed between the two ground pads for the band pass filter (BPF). The ground plane on both sides of the BPF should be connected to enable one common ground plane for the entire area.

There should be increased ground via stitching in the ground plane between the BPF and the PA_LDO_OUT decoupling capacitor (pin 1).

- There should be no high frequency signal traces or test points close to the RF trace.
- **CC355xE only:** The diplexer should be placed in such a way that the RF_A trace is as short as possible (the trace connecting the RF_A pin (pin 54) to the high port of the diplexer). The RF_A trace should take layout prioirty over the RF_BG trace when routing.

Another impactful factor in RF performance is the stackup. As an example, Table 3-1 contains the stackup (from top to bottom) used in the LP-EM-CC35X1 design.

Table 3-1. Stackup (from top to bottom) Used in all CC35xxE EVMs

Layer	Name	Thickness	ε_r
	Top Soldermask		
	Top Solder	1.00 mil	3.5
1	Top Layer	1.85 mil	
	Dielectric 1	5.48 mil	4.2
2	L02_GND	1.26 mil	
	Dielectric 2	42.82 mil	4.2
3	L03_PWR	1.26 mil	
	Dielectric 3	5.48 mil	4.2
4	Bottom Layer	1.85 mil	
	Bottom Solder	1.00 mil	3.5
	Bottom Soldermask		

The RF signal from the device is routed to the antenna using a CPWG structure. This structure offers the maximum isolation across the filter gap, and the best possible shielding to the RF lines. It is imperative to take in account the stackup and trace measurements in order to achieve a 50 ohm impedance. Figure 3-5 and Figure 3-6 illustrate examples of calculating trace impedance using the LP-EM-CC35X1 EVM as an example.

This image is sampled from the LP-EM-CC35X1 design files.

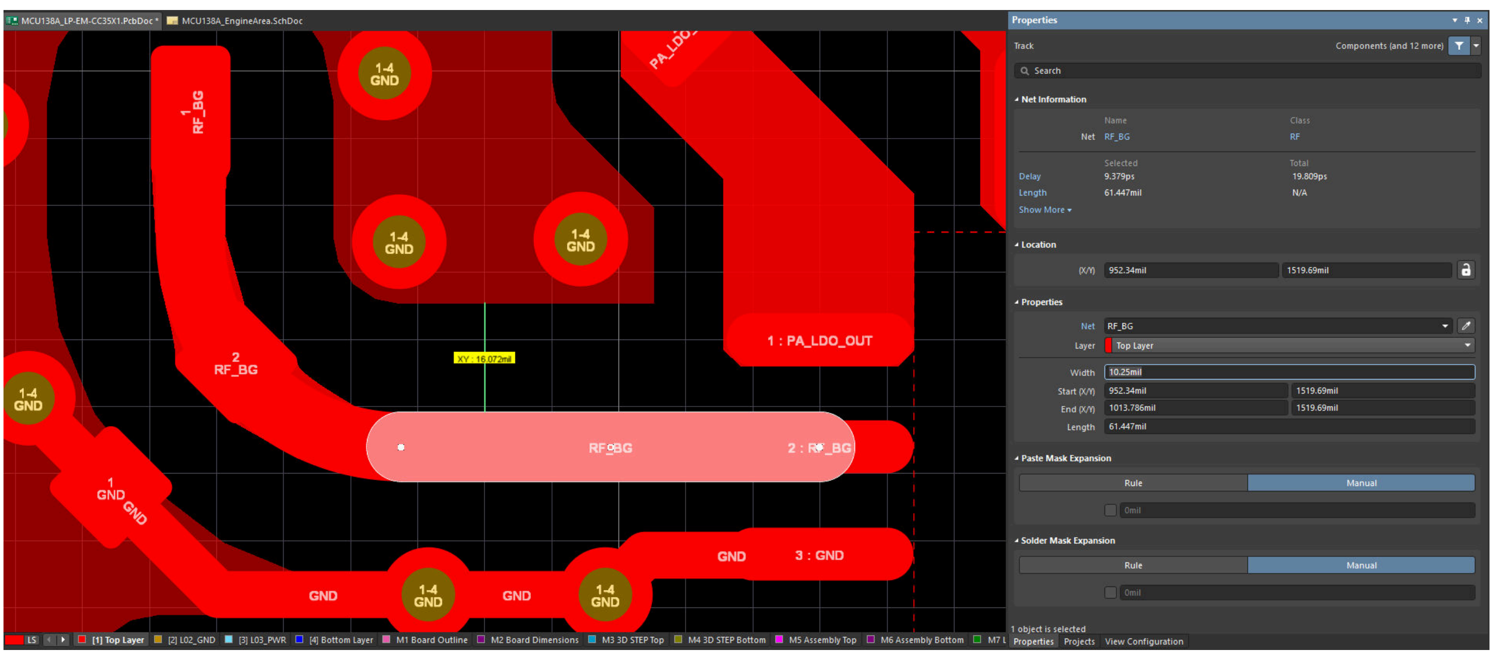

Figure 3-5. Example of Taking RF Trace Measurements

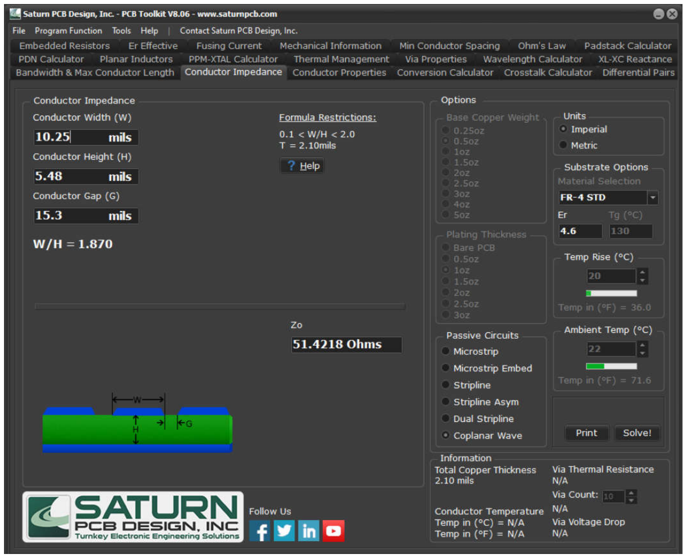

Figure 3-6. Example of Calculating Trace Impedance

3.4 XTAL

Figure 3-7 shows the placement and layout around the 52 MHz XTAL and its connections to the CC35xxE IC. Figure 3-7 is sampled from the LP-EM-CC35X1 design files.

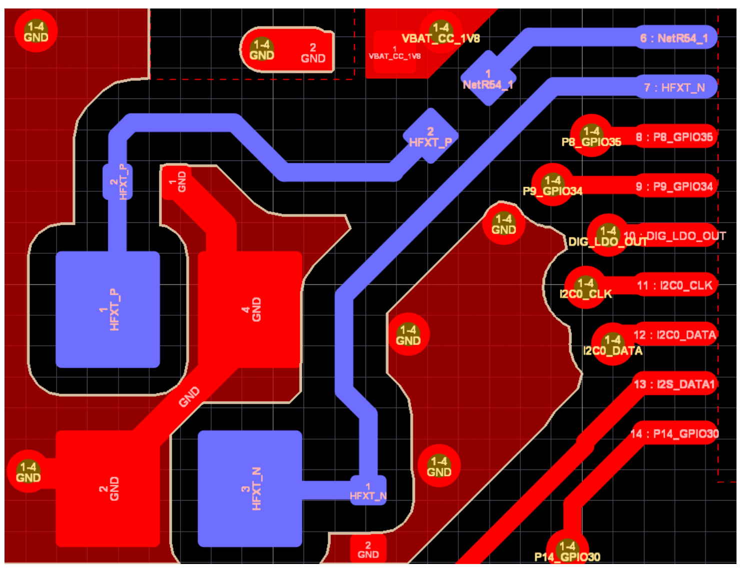

Figure 3-7. 52MHz XTAL From LP-EM-CC35X1

When integrating the XTAL, please follow these guidelines:

- The traces connecting the XTAL to the CC35xxE (XTAL_P and XTAL_M) be as short as possible with matching trace length.
- Place a 150 Ω resistor on the XTAL_P pin (pin 6) as close as possible to the CC35xxE.
- The two loading capacitors should be parallel to the edge of the XTAL.
- Wherever possible, there should be increased ground via stitching around the XTAL for optimal isolation.

3.5 Power Supplies

The power supplies, ground traces, and the decoupling capacitors are important for having an optimal layout. Since the decoupling capacitors can be close to the RF pins and traces of the device and power supplies, traces must be thick enough to support the necessary current to the device.

- PA_LDO_OUT (pin 1): It is suggested to have the decoupling capacitor close to the device pin, as well as a thick enough trace to have a low impedance path to the capacitor. For a visual representation, see Figure 3-8.
- VDD_ANA_IN1 and VDD_ANA_IN2 (pins 4 and 5): The supply side of the decoupling capacitors must be shorted together with a polygon region with two power vias (one for each decoupling capacitor). The ground side of each capacitor must go directly to ground by separate vias (not shorted together), and be isolated from the rest of the ground plane on the top layer.
- For the 1.8V power delivery, a thick trace or power plane must be used to carry the required amount of current consumption in VDD_MAIN_IN, VDD_ANA_IN1, VDD_ANA_IN2, and VPP_IN combined.
- VDD_DIG_IN (pin 10) and DIG_LDO_OUT (pin 47) must be shorted together on a layer that is not the top layer or ground layer (place it on layer 3 or 4).This way the power path cannot interrupt the RF trace on top layer (layer 1) or the continuous ground layer (layer 2). For a visual reference, see Figure 3-9. The decoupling capacitor should be close to pin 47.
- VDDSF (pin 23) must be configured to 1.8V. A thick trace or power plane must be used to carry the required amount of current consumption.
- VIO1 (pin 37) and VIO2 (pin 15) can be configured to 1.8V or 3.3V. A thick trace or power plane must be used to carry the required amount of current consumption.
- The 1.8V path must be located around the device on a layer that is not the top layer or ground layer (place it on layer 3 or 4). This way the power path cannot interrupt the RF trace on top layer (layer 1) or the continuous ground layer (layer 2). Only one via is used for each 1.8V power supply, the 1.8V supply currents must not flow under the device.
- For the 3.3V power delivery, a thick trace or a power plane must be used to carry the required amount of current consumption of the PA_LDO_IN. The power delivery must also be placed on a layer that is not top layer or ground layer (layer 3 or 4).
- PA_LDO_IN (pins 55 and 56): These two pins must be shorted together with a solid region. The decoupling capacitor should be placed close to the device. Use two vias if possible to deliver the 3.3V rail.

Figure 3-8 is sampled from the LP-EM-CC35X1 design files.

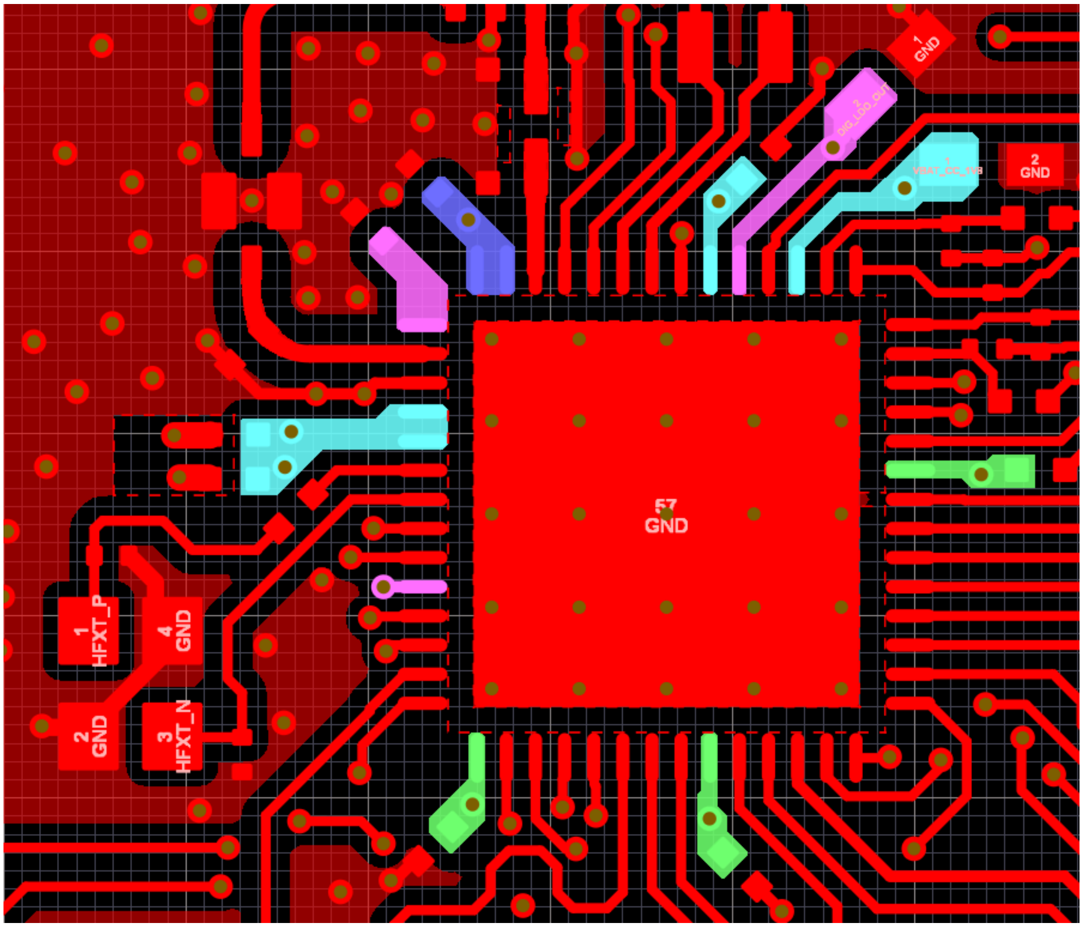

Figure 3-8. Reference Layout of CC35xxE Power Supplies

Figure 3-9 is sampled from the LP-EM-CC35X1 design files.

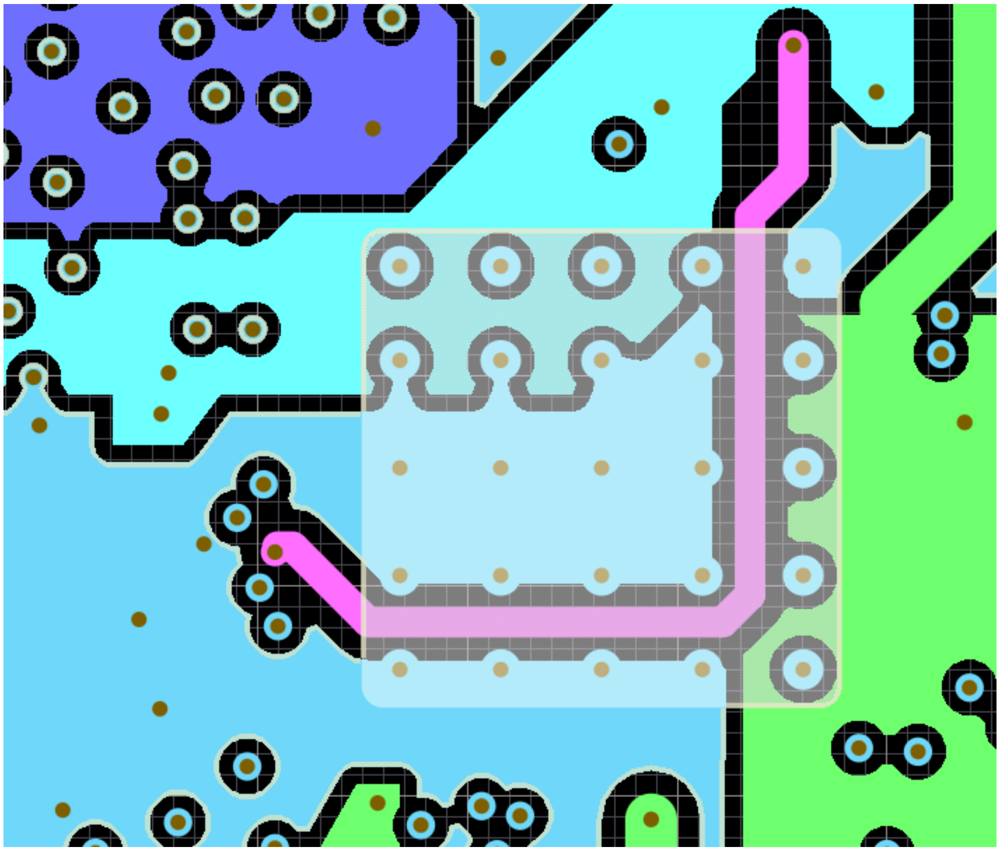

Figure 3-9. Reference Layout of the Power Layer (Layer 3)

3.6 External Flash Layout

The external flash provides programmable, nonvolatile program memory for the device. Up to 64MB of flash memory is supported. Using the external flash allows the user to use saved network-specific data and avoids the need for a full start-up and network find-and-join process. The CC35xxE device communicates to the external flash using xSPI.

The xSPI lines include xSPI_CLK, xSPI_CS_FLASH, xSPI_D0, xSPI_D1, xSPI_D2, and xSPI_D3. The xSPI_CLK signal in particular is very sensitive and should be regarded as such. In order to ensure reliable xSPI communication, the following layout considerations should be taken into account:

- Trace Length should be no more than 1000 mil (25.4 mm)
- The lengths of the traces must be length matched within 100 mil tolerance to provide the sampled data at the same time on all of the traces.

Figure 3-10 is sampled from the LP-EM_CC35X1 design files.

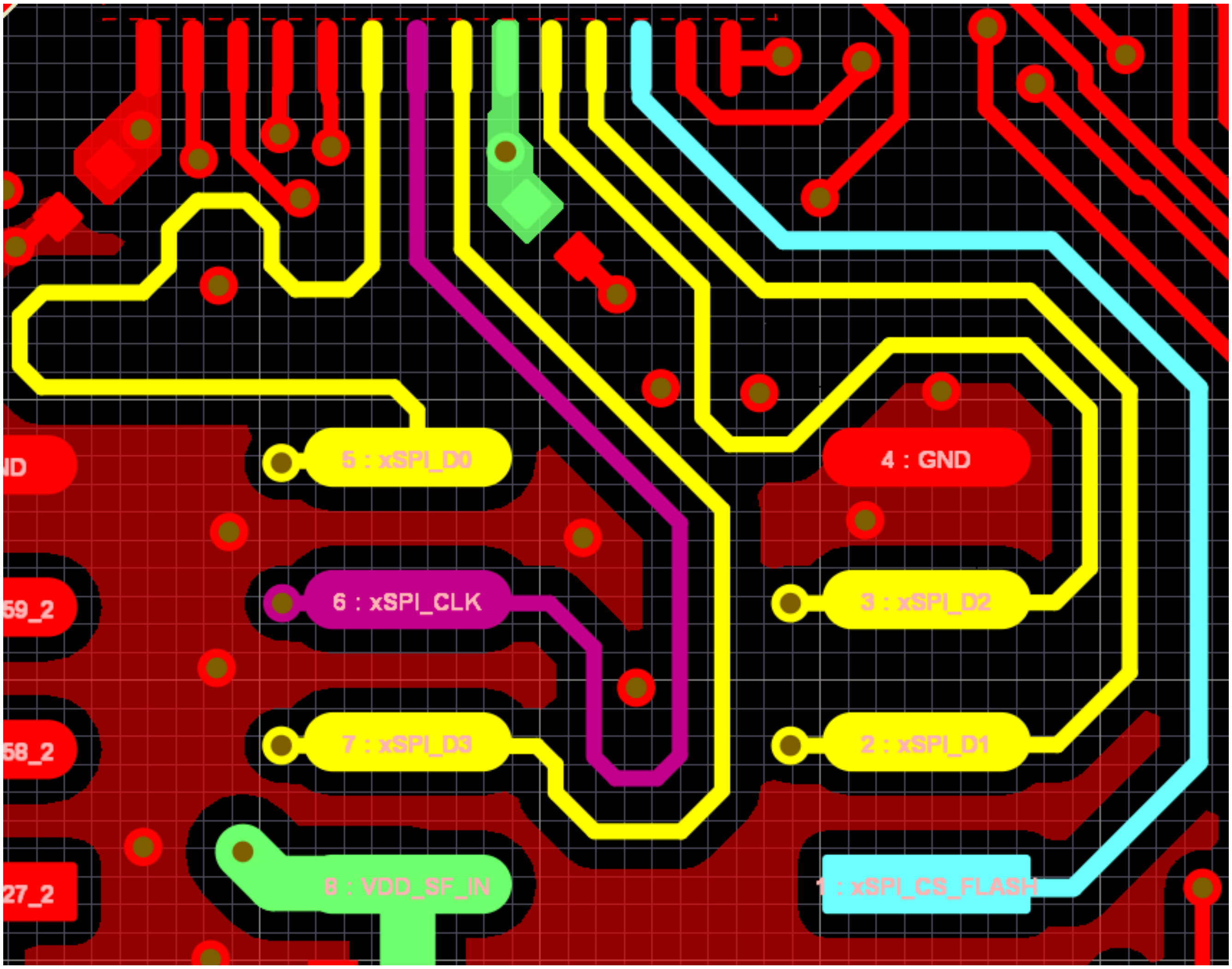

Figure 3-10. CC35xxE External Serial Flash

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