Application Brief

Inrush Current Reduction Considerations for UCC25800-Q1 in Parallel Startup Applications

Vincent Kwok, Robert Martinez

Introduction

Inrush current refers to the initial current surge that flows into a circuit when power is first applied. The cause of inrush current stems from the charging or energizing of capacitors and inductive components. In some cases, the transient current can be several times higher than the device's normal operating current. This is a common occurrence in the UCC25800-Q1, especially when devices are powered in parallel simultaneously, triggering overcurrent protection. For more information on the UCC25800-Q1, see *UCC25800-Q1 Ultra-low EMI Transformer Driver for Isolated Bias Supplies*

Given that the peak inrush current upon startup is given by the voltage supplied by the source and the impedance of the circuit, a logical conclusion is to simply increase the impedance to proportionally reduce inrush current. Theoretically, a sufficiently large resistance can reduce inrush to a near-zero. However this introduces trade-offs:

- Longer startup time due to increased RC time constant
- Power losses across the resistor, causing efficiency losses
- Potential undervoltage or functional delays in downstream devices and circuits during the longer startup time

This application brief discusses strategies to reduce inrush beyond increasing input impedance.

Changing Input Voltage Ramp Time

Input voltage ramp time refers to the rate at which the input voltage to a circuit rises from 0V to nominal operating level during startup. Increasing ramp time allows input capacitors to charge more slowly and reduce peak inrush current. However, this method introduces delay to full operation and is not designed for time critical applications. UCC25800-Q1 does not have a dedicated pin or feature to control an input voltage ramp. External slew control needs to be added to manipulate this.

If the ramp is too slow, the rising voltage does not reach a level sufficient enough to maintain sufficient headroom above the converter's UVLO (Undervoltage Lockout) threshold. For the UCC25800-Q1, this threshold typically lies at 8.6V (Figure 1). In this case, the device can shut down and cause a failed startup. Simulation of UCC25800-Q1 indicates the ramp time for UVLO to trigger a failed startup is around 0.8V/ms or greater. If such a case is observed, other inrush reduction methods can be used to avoid this problem.

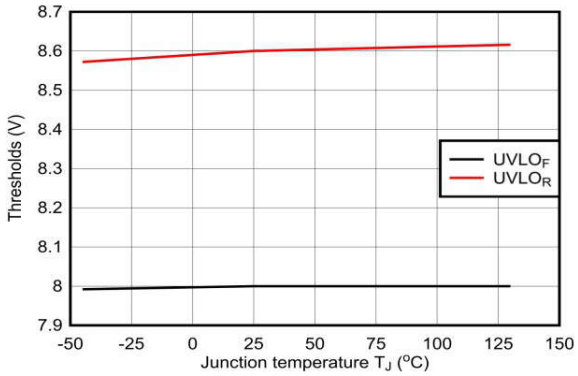

Figure 1. UVLO Threshold Relationship to Junction Temperature

Staggered Startup Sequencing Using RC Delay

When multiple identical devices with capacitive inputs stages are powered on simultaneously, the devices individual inrush currents combine. Figure 2 shows the inrush of 2 UCC25800-Q1 starting in parallel, Figure 3 shows the inrush of 4 parallel UCC25800-Q1 devices all starting up at the same time. As seen in the figures, this inrush created by combination usually increases linearly per parallel identical device added, though changing the power supply can also change the individual inrush each board contributes to the total current demand.

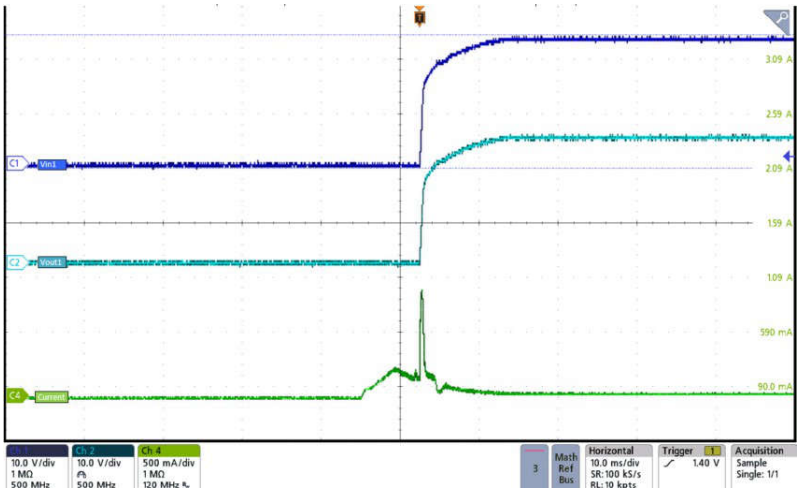

Figure 2. Two UCC25800-Q1 Devices Starting Simultaneously, Inrush Peak of 982mA

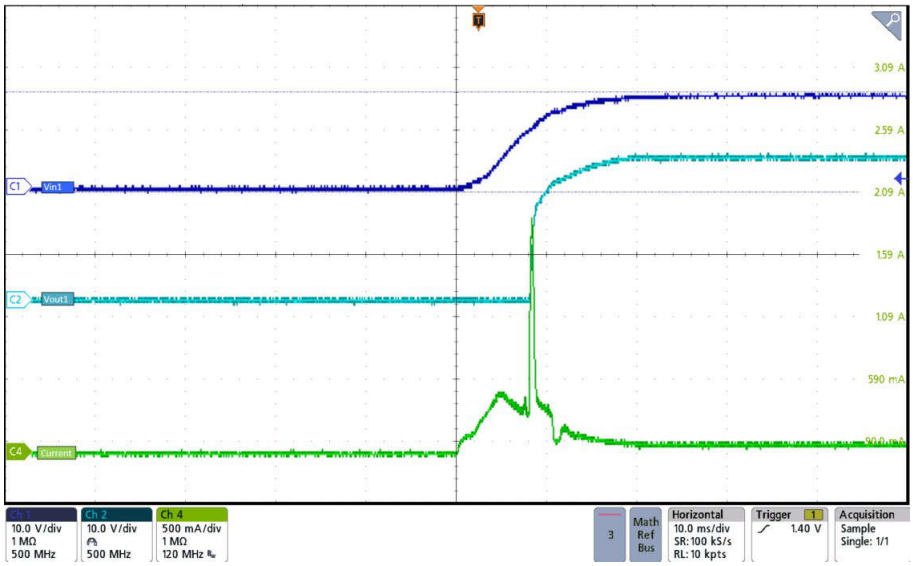

Figure 3. Four UCC25800-Q1 Devices Starting Simultaneously, Inrush Peak of 982mA

There is the option to remove a singular large spike of inrush by intentionally delaying the power-up of each device by a defined time interval. By chronologically isolating the inrush current of each stage, the peak aggregate current seen by the power source is significantly reduced to the inrush of a single stage at best. Having a staggered start-up control scheme improves power system stability during startup and prevents upstream overcurrent from creating protection tripping. A drawback of this strategy is the slower startup of the device which is caused by the defined delay time interval. This can be counteracted by activating multiple devices per delay stage though the number of devices that can be activated at the same time is dependent on the current output limit of the previous power stage.

There are many common ways to create a startup sequence that staggers the inrush current with similar outcome including the following:

- RC circuits connected to the same power source to trigger a threshold enable pin value for each device at a different time
- Microcontroller outputs set by firmware to create delay
- A discrete timer circuit where the output of one timer triggers the following timer after a delay
- A sequential power controller, such as the LM3880 or TPS38700-Q1, the latter of which is recommend to pair with UCC25800-Q1

Figure 4 and Figure 5 show the difference between staggered and simultaneous startup of 4 devices using an RC delay circuit. Voltage from one stage is not probed due to equipment limitations.

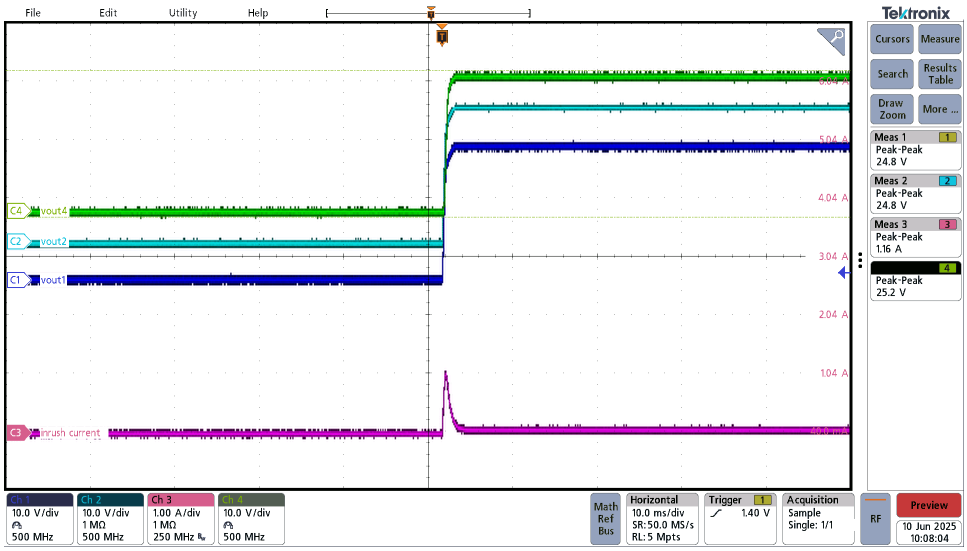

Figure 4. Simultaneous Startup, 1.16A Max Inrush

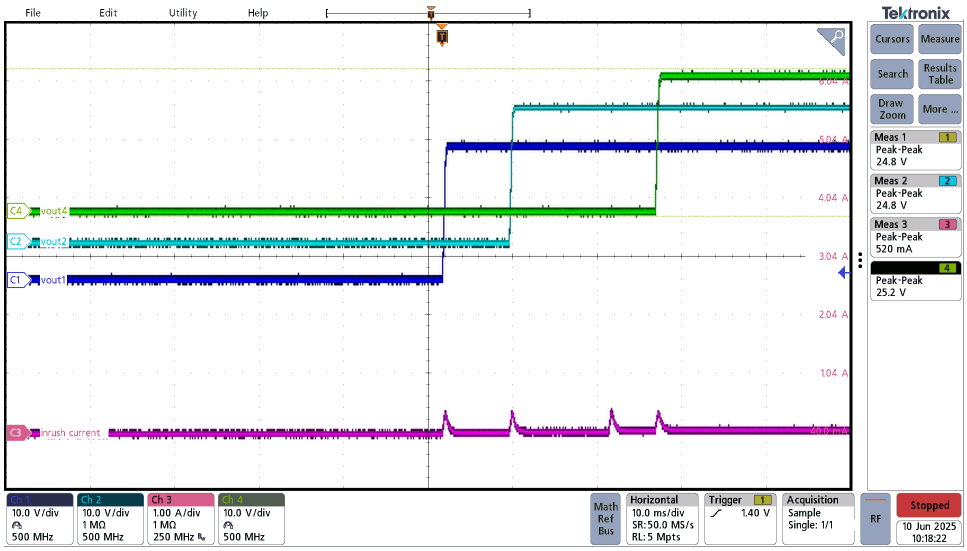

Figure 5. Staggered Startup Using RC Circuit, 528mA Max Inrush

Switching Frequency Control

In switching power converters, the switching frequency directly affects the energy transferred per cycle. By increasing the switching frequency using an appropriate resistance, inrush can be limited to protect the load and power stage.

However, this design of maintaining a high switching frequency during normal operation is not designed for as higher frequencies increase switching losses and reduce efficiency. As such, the preferred approach is to boost the switching frequency only at the moment of startup, then return to a standard frequency.

In Figure 6, UCC25800-Q1 includes an RT pin that sets the switching frequency. To create a temporary frequency boost, connect RT to the voltage of the enable with an RC circuit to force the rising edge of the enable to trigger the charging of the capacitor upon power up. As long as the enable rising edge is several volts larger than the maximum switching frequency voltage at 3V (Figure 6), the voltage provided can have time to decay at a rate inversely proportional to the capacitance value of the RC circuit. Increasing the capacitance value can stretch the duration of high switching frequency, creating a more gradual current ramp into the load. As the circuit stabilizes, the capacitor can discharge and the RT pin voltage decays to bring the switching frequency back to the connected resistor.

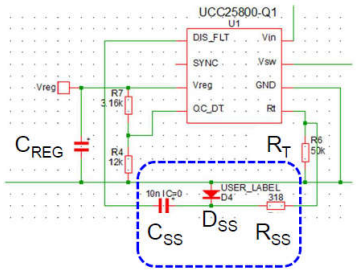

Figure 6. RCD Circuit Modification to Create a Temporary Frequency Boost

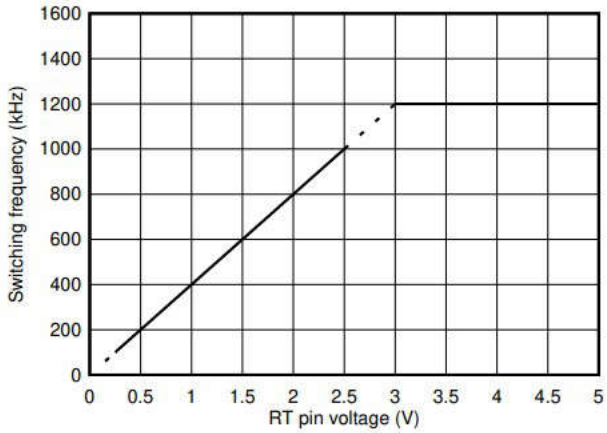

Figure 7. UCC25800-Q1 Relationship Between Switching Frequency and RT Pin Voltage

Summary

Transformer drivers play a key role in modern EV power architectures, especially in high-power subsystems like traction inverters and on-board chargers where efficient startup is critical. Inrush current management is essential, particularly for parallel startup applications including the UCC25800-Q1, where overcurrent protections can trip early. While resistive limiting can reduce this concern, this introduces losses and delays. More effective approaches include staggered startup methods such as RC delay, timers, or sequencers. For further refinement a temporary frequency boost via an RC circuit connected to a frequency controlling pin can limit inrush without efficiency penalties. Combining these techniques can significantly reduce inrush current and prevent overcurrent protections from tripping.

Table 1 lists each inrush reduction method mentioned in the application brief with the respective pros and cons.

Table 1. Inrush Reduction Method Pros and Cons

Inrush Reduction Method	Pro	Con
Increase Impedance	• Simple to implement • Can theoretically eliminate inrush	• Longer startup time • Power loss across resistor • Potential undervoltage issues
Increase Vin Ramp Time	• Reduces current surge • Can be simple to implement based off input power design	• Requires controlled source or active components • Slower system readiness • Requires external slew control
Staggering Using Enable/Disable Pins	• Reduces peak current demand potentially down to a single device • Easily scalable • Can be passive design with RC circuit implementation • Many methods of implementation	• Requires control signals and addition power sources • Increase in startup time
Switching Speed Frequency Boost	• Can reduce inrush of a standalone device • Improves soft-start behavior • Passive, compact design	• Frequency control must be supported by IC

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