Texas Instruments

Application Report

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Using ADS8411/ADS8412 as a Serial ADC

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ABSTRACT

This application report discusses how to use a parallel ADC as a serial ADC by using a low-cost CPLD. This concept is tested with a Texas Instruments ADS8411/12 (16-bit, 2 MSPS SAR ADC) and an Altera™ MAX 3000A CPLD. A full solution with schematic, layout, and software for programming the CPLD is presented at the end of the report. Project collateral discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/SLAA199.

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1 Introduction

The Texas Instruments ADS8411 is a 16-bit, 2 MSPS, unipolar single-ended ADC with parallel interface and internal reference. The ADS8412 is a 16-bit, 2 MSPS, unipolar differential ADC with parallel interface and internal reference. To complement the serial interface, this application report discusses how to use this ADC as a serial output ADC. To convert the parallel data to serial output, a CPLD (complex programmable logic device) is used. The same CPLD converts the serial control signals ($\overline{\text{CS}}$, FS, SCLK, etc.) to parallel control signals and sends them to the device. So, to the user, the ADC along with the CPLD (henceforth referred as a chipset) is a serial device. The user sends serial control signals to the chipset and receives serial data outputs. An Altera™ MAX 3000A-series CPLD is used.

2 Hardware

The hardware platform comprises the ADS8411 and the MAX 3000A CPLD. To program the one-time programmable CPLD, an Altera™ ByteBlasterMV cable can be used.

2.1 ADS8411

The ADS8411 is a 16-bit, 2-MHz A/D converter with an internal 4.096-V reference. The device includes a 16-bit, capacitor-based, SAR A/D converter with inherent sample and hold capability.

2.2 MAX 3000A CPLD

The Altera™ MAX 3000A-series CPLD was selected for this solution because of its low cost, ease of use, and does not need a configuration device. The MAX 3000A CPLD part number is EPM3032ATC44-10.

2.3 ByteBlasterMV Cable

The ByteBlasterMV parallel port download cable (ordering code: PL-BYTEBLASTERMV) connects to a standard PC parallel port (also known as an LPT port). This cable drives configuration data from the PC to MAX 3000A devices and configuration devices. Because design changes are downloaded directly to the CPLD, prototyping is easy, and multiple design iterations can be accomplished quickly.

2.4 Hardware Interface

The ADS8411 sends parallel data (D0-D15) to the CPLD (see Figure 1). SCLK and $\overline{\text{CS}}$ are sent to the CPLD from outside. The CPLD generates the $\overline{\text{CONVST}}$ signal to control the parallel device and also outputs the serial data. See the schematics in Appendix B for more detail.

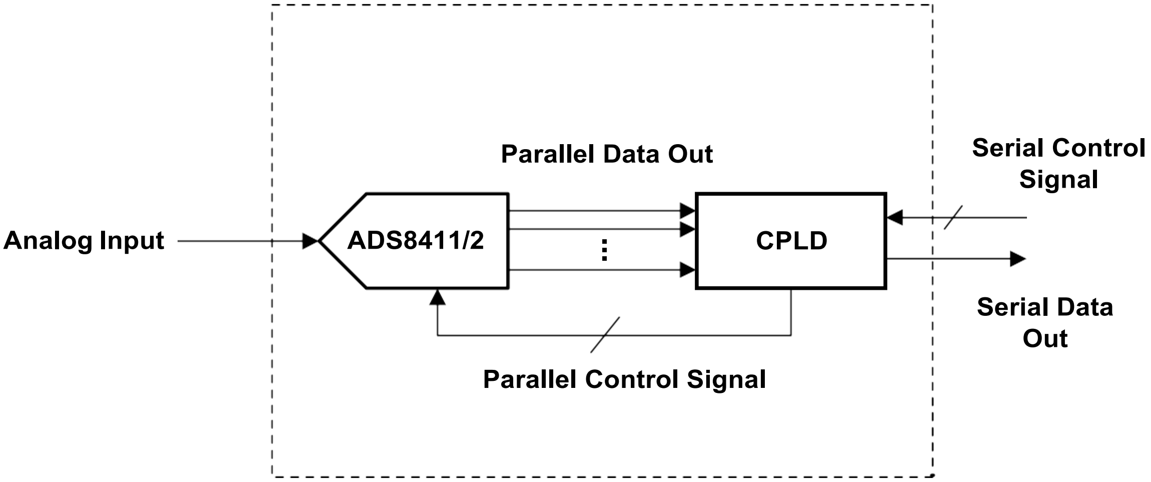


Figure 1. Simplified Block Diagram

The system inside the dashed line of Figure 1 works as a serial part.

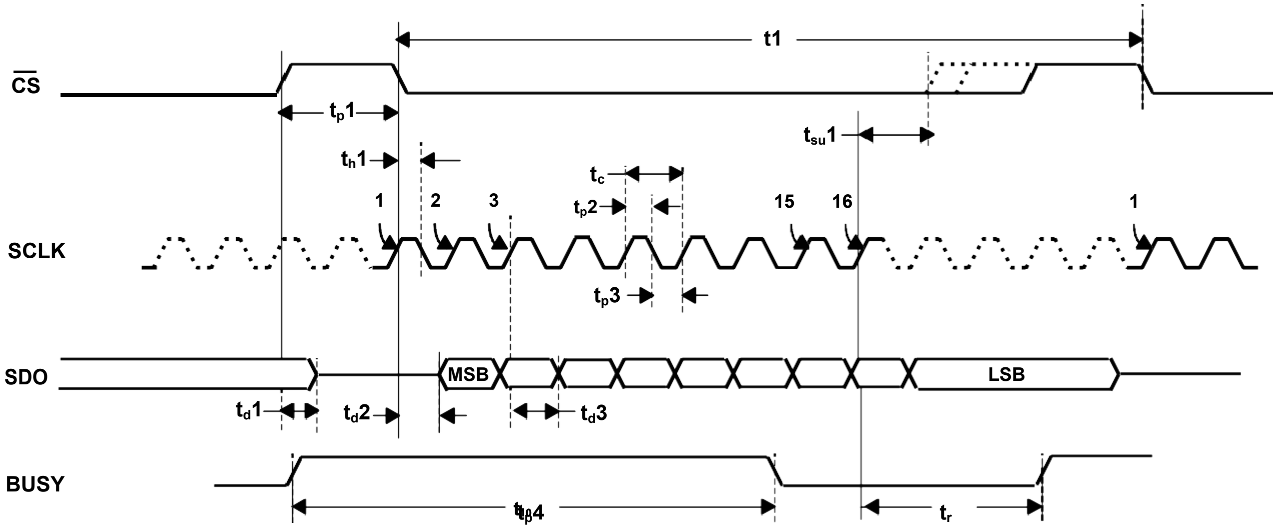


Figure 2. Timing Diagram at 2 MSPS

2.5 Timing

The serial interface used in this chipset is SPI (serial peripheral interface) compatible. The $\overline{CS}$ and SCLK signals control the chipset (see Figure 2). The data is only available in the bus when $\overline{CS}$ is low. Otherwise, the bus is in a 3-state mode. After the $\overline{CS}$ falling edge, the chipset waits for the falling edge of SCLK. This clock is counted as the first SCLK. The MSB of the data appears after the $\overline{CS}$ falling edge. Then, the next data appears after the rising edge of second SCLK. Only 16 clocks per frame are necessary for the chipset to work. After that, the clock can be free-running or withdrawn.

Table 1. Chipset Timings

Symbol	Parameter	MIN	MAX	Unit
t1	Width of a full frame	500		ns
t_p1	Pulse duration, $\overline{CS}$ high time	20		ns
t_h1	Hold time, $\overline{CS}$ falling edge (first SCLK falling edge after $\overline{CS}$ toggles from high to low) to SCLK falling edge	4		ns
$t_{su}1$	Setup time, 16th clock rising edge to $\overline{CS}$ rising edge	20		ns
t_c	Cycle time, SCLK	20		ns
t_p2	Pulse duration, SCLK high	8		ns
t_p3	Pulse duration, SCLK low	8		ns
t_d1	Delay, $\overline{CS}$ high to SDO 3-state		15.5	ns
t_d2	Delay, Falling edge of $\overline{CS}$ to SDO		15.5	ns
t_p4	Pulse duration, Busy high		360 [1]	ns
t_r	16th clock rising edge to Busy High		75	ns
t_d3	Delay, Rising edge of SCLK to SDO toggle		9.5	ns

[1] Maximum pulse duration data taken from ADS8411 data sheet (SLAS369).

2.6 Quartus™ II 3.0

The logic for converting parallel data to serial data and serial control signals to parallel control signals is written in Quartus II 3.0 software from Altera. Verilog HDL is used to write the hardware description. To program the CPLD, the user needs to download Quartus II 3.0 free evaluation version from www.altera.com. The program is downloaded by the ByteBlasterMV cable through the PC parallel port. The Verilog file and the schematics also are available in the appendixes.

Appendix A. Logic Diagram, Description, and Verilog Code of the CPLD Program

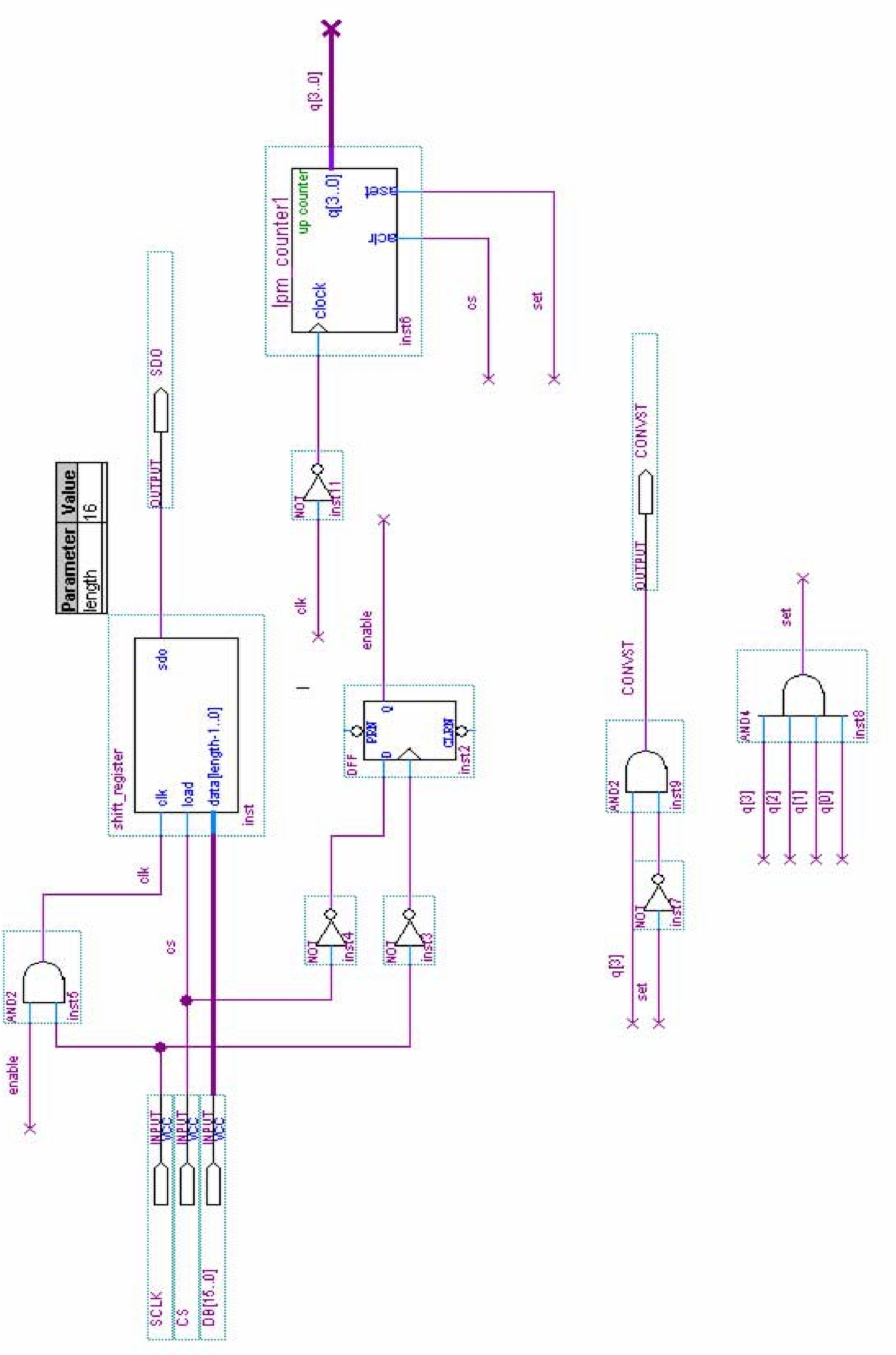


Figure A-1. Logic Diagram

A.1 CPLD Program Logic

A.1.1 Parallel Data to Serial Data

Shift_register (inst) is a 16-bit parallel-to-serial shift register (see Figure A-1). It loads 16-bit data when load = 1. Otherwise, it shifts the 16-bit data at every positive edge of the clock. Serial data is given out in MSB-first format.

When $\overline{\text{CS}}$ is high, the 16-bit data is loaded into the shift register, but SCLK is disabled until $\overline{\text{CS}}$ is low. After $\overline{\text{CS}}$ goes low, the chipset responds to the SCLK falling edge. To incorporate this $\overline{\text{CS}}$ logic, the inverted Chip Select signal is sent to the D input of the DFF (inst2), and the inverted SCLK signal is sent to the clock input of the DFF. The output of the DFF generates the enable signal for the clock and for the shift register.

A.2 $\overline{\text{CONVST}}$ Generation

The 3-bit counter (inst6) along with the gates (inst7, 8, 9, and 11) generates the $\overline{\text{CONVST}}$ for the parallel device. This is the conversion start signal required for the parallel device. $\overline{\text{CS}}$ resets the counter, and output of the 4-input AND gate sets the counter. It ensures that the counter is stopped after the 16th clock. Otherwise, the counter keeps producing $\overline{\text{CONVST}}$, even if the $\overline{\text{CS}}$ is not toggled. $\overline{\text{CONVST}}$ remains high from the 8th clock to the 15th clock. At the 16th clock, it falls to LOW and conversion starts.

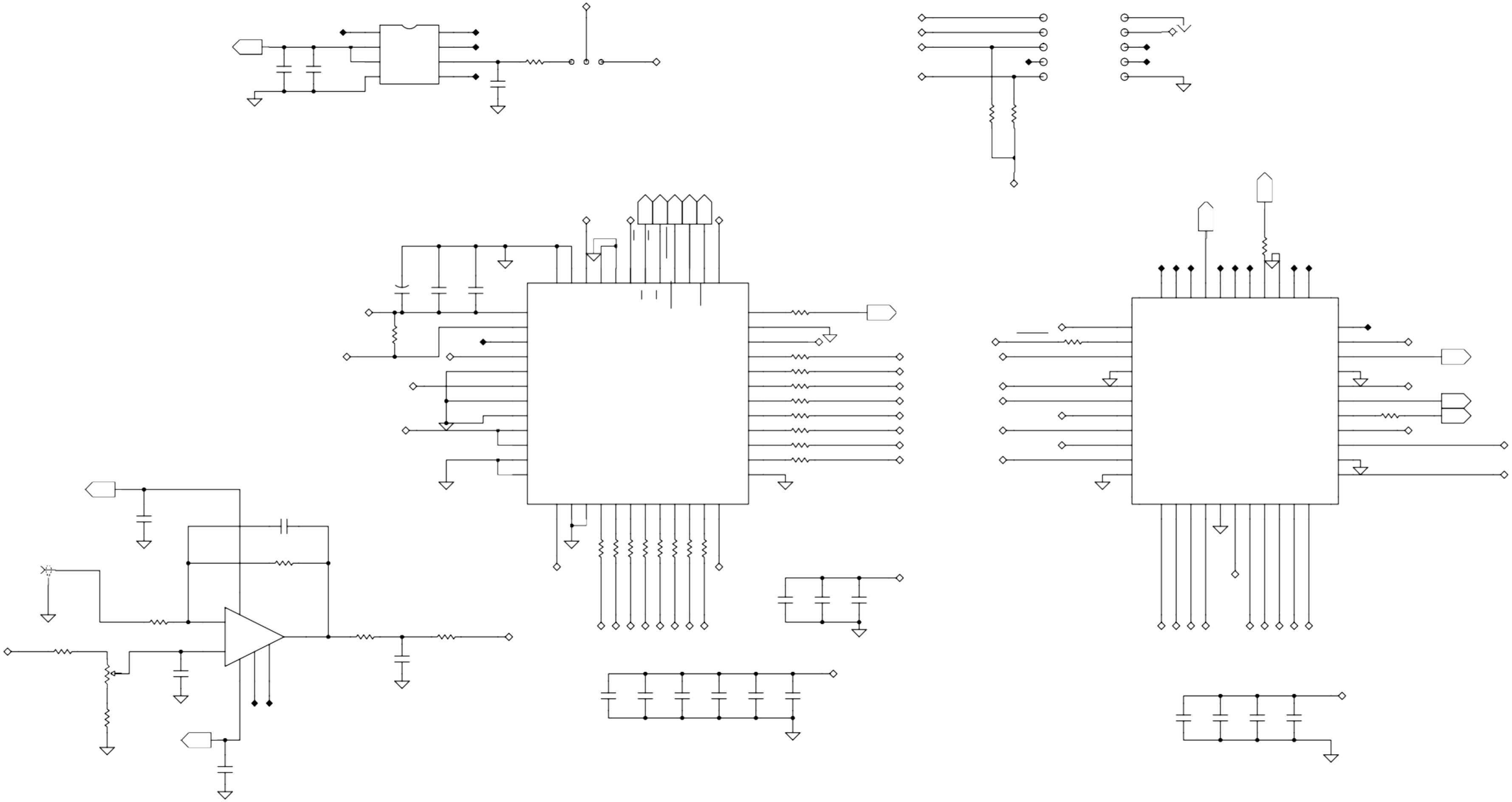
A.3 Verilog Code for the CPLD Program (File: shift_register.v)

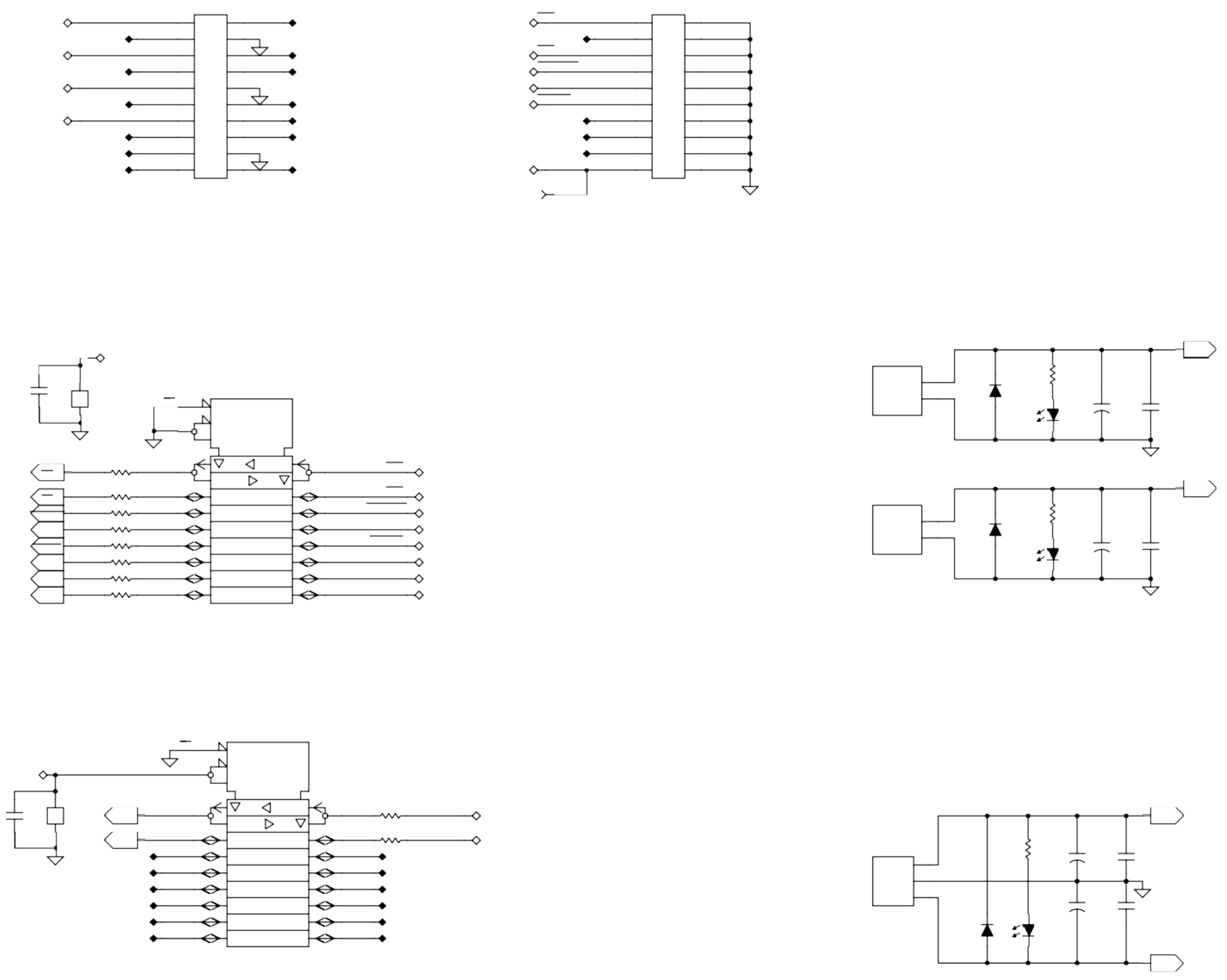
```
module shift_register(clk, load, data, sdo);

parameter length=16;

input clk, load;
input [length-1:0] data;
output sdo;
reg sdo;
reg [length-1:0] q;

always @ (posedge clk or posedge load)
 begin
   if(load)
   q<=data;
   else
    begin
     q[15]<=q[14];
                              q[14]<=q[13];
                              q[13]<=q[12];
                              q[12]<=q[11];
                              q[11]<=q[10];
                              q[10]<=q[9];
                              q[9]<=q[8];
```

```
                     q[8]<=q[7];
                     q[7]<=q[6];
                     q[6]<=q[5];
                     q[5]<=q[4];
                     q[4]<=q[3];
                     q[3]<=q[2];
                     q[2]<=q[1];
                     q[1]<=q[0];
                    end
  sdo<=q[length-1];

 end

endmodule
```

Appendix B. ADS8411 Schematic

Sheets 1 and 2 of the ADS8411 schematic follow.





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