Functional Safety Information

TPS1211x
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

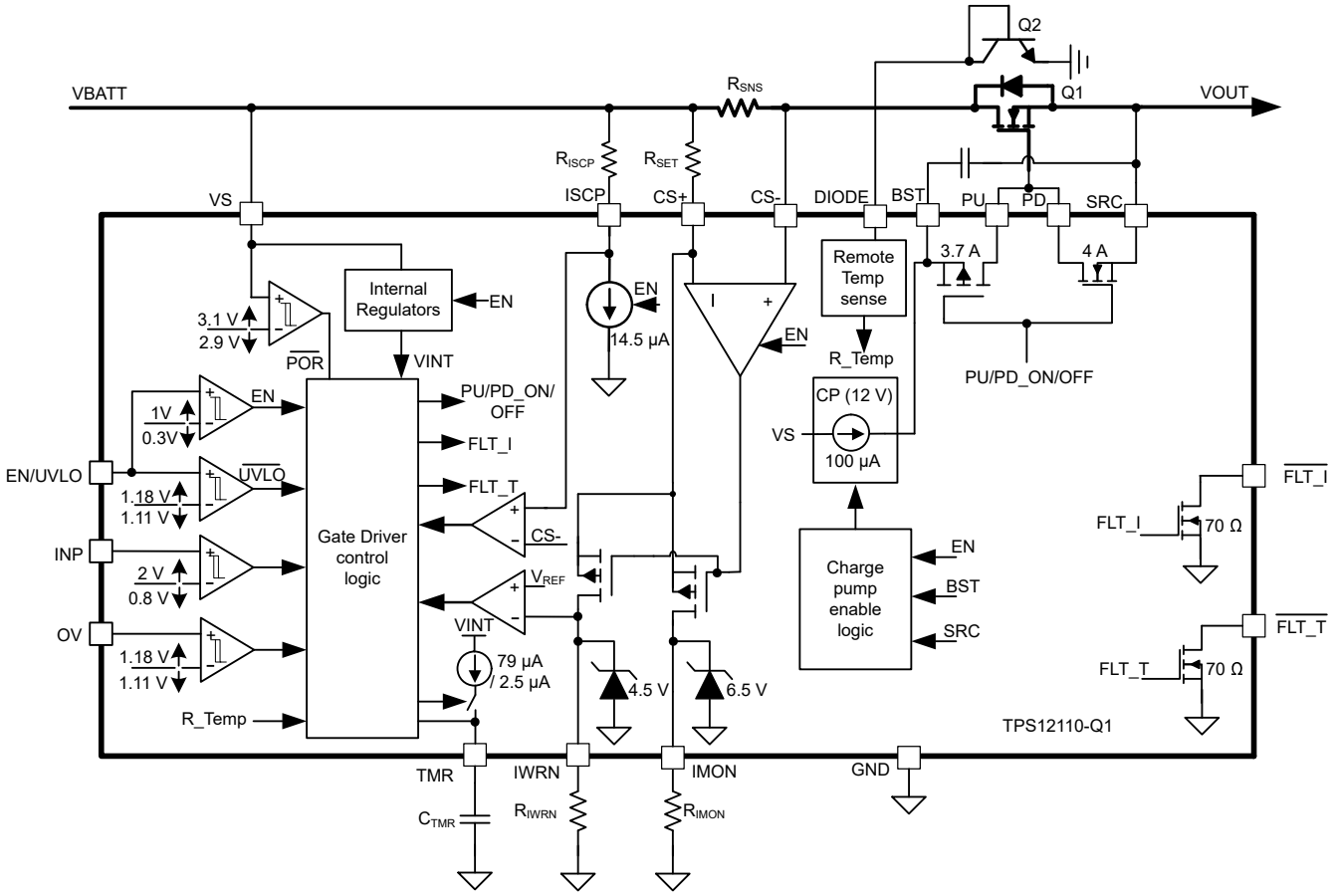
Trademarks

1 Overview

This document contains information for TPS1211x (VSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



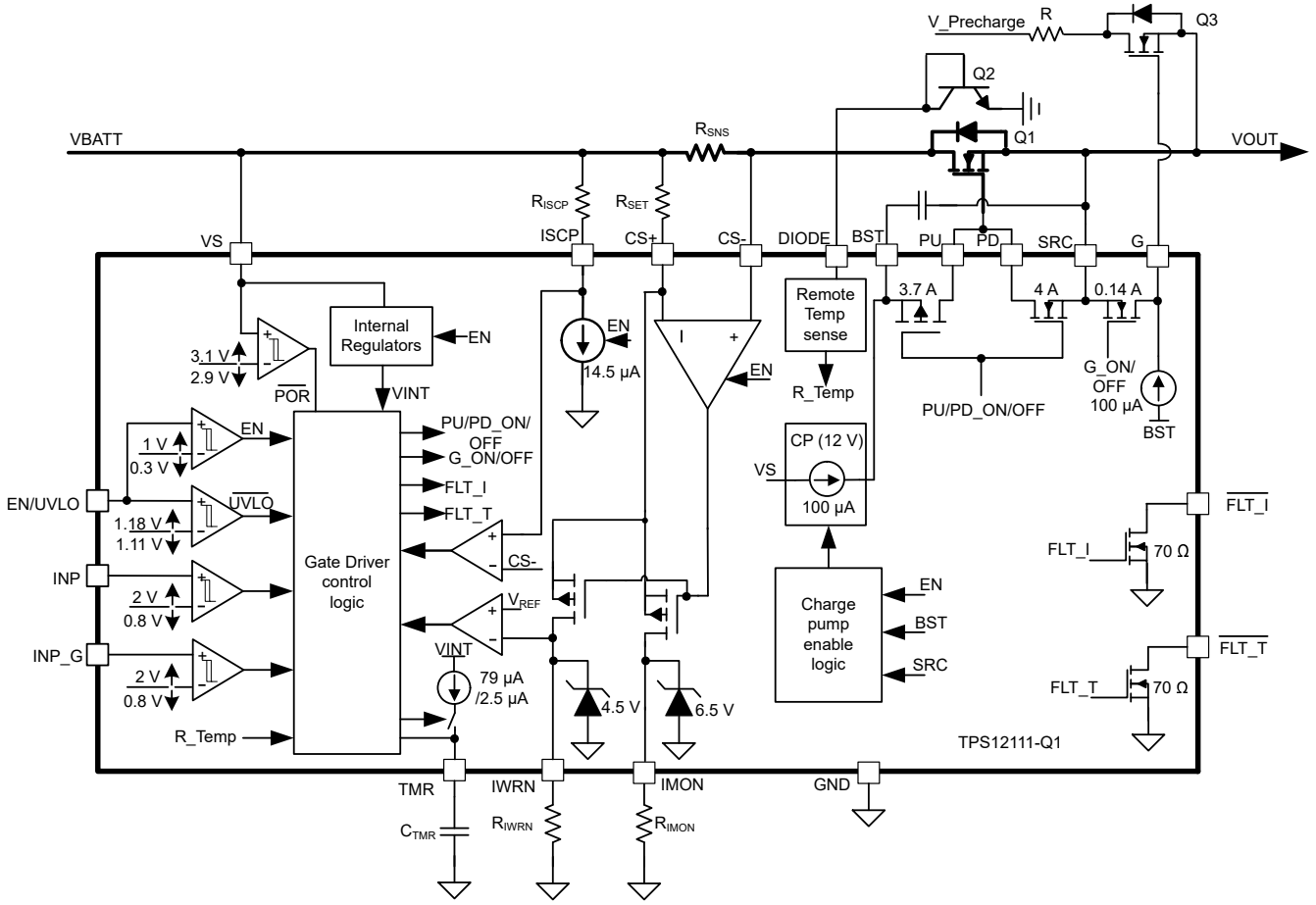


Figure 1-1. Functional Block Diagram

TPS1211x was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS1211x based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	3
Package FIT rate	6

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 27mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS1211x in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Gate output stuck high	13
Gate output stuck low	40
Gate output functional, not in specification – voltage or timing	33
Short circuit protection fails to trip or false trip	2
IMON not in specification – current or timing	5
UVLO, OV, TSD fails to trip or false trip	2
Pin-to-pin short any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS1211x. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS1211x pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS1211x datasheets.

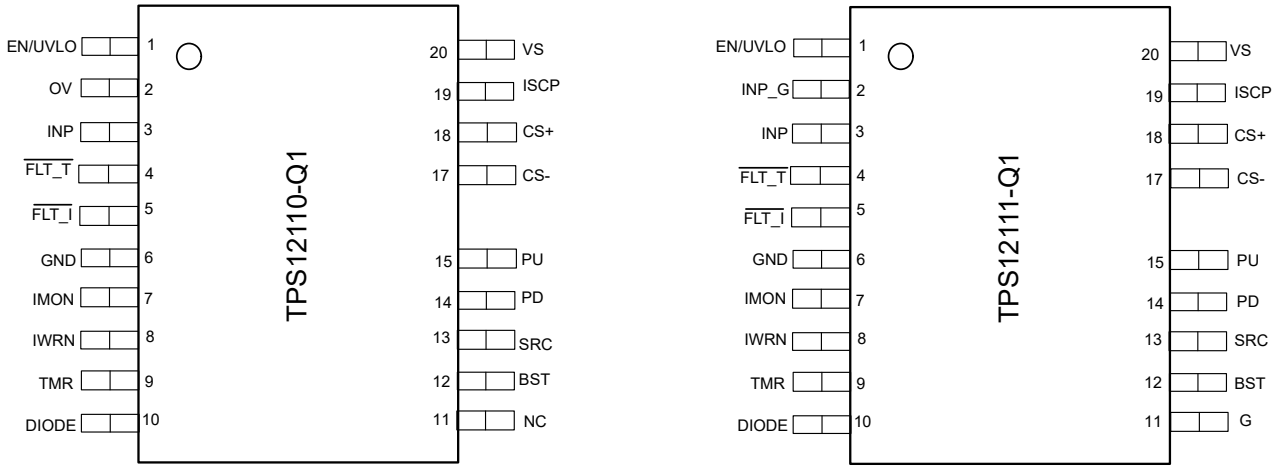


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The recommendations for operating conditions, external component selection, and PCB layout in the datasheet are followed.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	The device operates as normal. The device is disabled.	B
OV	2	Applies to TPS1210-Q1 only. The overvoltage functionality is disabled.	B
INP_G	2	Applies to TPS1211-Q1 only. The device operates as normal. The output of the G pin is low, and the external precharge FET is off.	B
INP	3	The device operates as normal. The output of the PD pin is low, and the external FET is off.	B
$\overline{\text{FLT\_T}}$	4	The overtemperature fault diagnostic cannot be reported.	B
$\overline{\text{FLT\_I}}$	5	The overtemperature fault diagnostic cannot be reported.	B
GND	6	The device operates as normal.	D
IMON	7	The output of the IMON pin cannot be reported.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IWRN	8	Overcurrent is not detected; hence, overcurrent protection is disabled.	B
TMR	9	Overcurrent is not detected; hence, overcurrent protection is disabled.	B
DIODE	10	Overtemperature is not detected; hence, overtemperature protection is disabled.	B
NC	11	Applies to TPS1210-Q1 only. There is no effect to the device.	D
G	11	Applies to TPS1211-Q1 only. With the G pin grounded, if the voltage between the SRC pin and G pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
BST	12	The gate driver supply does not come up. The FETs remain OFF.	B
SRC	13	Short to GND protection starts.	B
PD	14	With the PD pin grounded, if the voltage between the SRC pin and PD pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
PU	15	The gate driver supply gets short circuited. The FETs remain OFF.	B
CS–	17	The input supply gets short circuited.	B
CS+	18	With the CS+ pin grounded, if the voltage between the CS+ pin and CS– pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
ISCP	19	With the ISCP pin grounded, if the voltage between the ISCP pin and CS– pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
VS	20	The supply of the device is grounded. The device does not power up.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	Internal pulldown brings the EN/UVLO pin low, disabling the device.	B
OV	2	Applies to TPS1210-Q1 only. The overvoltage functionality is disabled as the overvoltage is internally pulled down to 0V.	B
INP_G	2	Applies to TPS1211-Q1 only. Internal pulldown brings the INP_G pin low, pulling the output of the G pin low.	B
INP	3	Internal pulldown brings the INP pin low, pulling the output of the PD pin low.	B
$\overline{\text{FLT\_T}}$	4	The overtemperature fault diagnostic cannot be reported.	B
$\overline{\text{FLT\_I}}$	5	The overcurrent fault diagnostic cannot be reported.	B
GND	6	The device does not power up and is disabled.	B
IMON	7	The voltage of the IMON pin can get clamped to the internal supply of 6.5V.	B
IWRN	8	The voltage of the IWRN pin can get clamped to the internal supply of 4.5V.	B
TMR	9	The overcurrent response time and automatic retry duration is reduced to the minimum setting of the device.	C
DIODE	10	Overtemperature protection can unintentionally trigger.	B
NC	11	There is no effect to the device.	D
G	11	The output of the G pin is not controlled.	B
BST	12	The external FET can turn ON and OFF repetitively due to no capacitor connection at the BST pin.	B
SRC	13	The external FET does not turn OFF as the FET source disconnects from the internal pulldown driver.	B
PD	14	The external FET does not turn OFF as the FET GATE disconnects from the internal pulldown driver.	B
PU	15	The external FET does not turn OFF as the FET GATE disconnects from the internal pulldown driver.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CS–	17	The CS– pin is internally clamped to the CS+ pin minus two diode drops. If the IWRN feature is used, then the external FET cannot turn ON due to a false overcurrent detection.	B
CS+	18	The IMON pin and overcurrent protection features are disabled.	B
ISCP	19	The short-circuit protection feature is disabled.	B
VS	20	The device does not power up and is disabled.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	2 (OV)	Applies to TPS1210-Q1 only. When the EN/UVLO pin is driven high, based on the voltage level of the EN/UVLO pin, the device can detect an overvoltage event and turn off the external FET.	B
EN/UVLO	1	2 (INP_G)	Applies to TPS1211-Q1 only. When the EN/UVLO pin is driven high, based on the voltage level of the EN/UVLO pin, the INP_G pin is detected high and the G goes high; turning ON the external precharge FET.	B
OV	2	3 (INP)	Applies to TPS1210-Q1 only. When INP is driven high then based on INP level the device can detect the OV event and turn off the external FET.	B
INP_G	2	3 (INP)	Applies to TPS1211-Q1 only. The PU and PD pins and the G pin are controlled together.	B
INP	3	4 ($\overline{\text{FLT\_T}}$)	When an overtemperature fault occurs, the INP pin is pulled low and the pin stays latched off in this state.	B
$\overline{\text{FLT\_T}}$	4	5 ($\overline{\text{FLT\_I}}$)	The $\overline{\text{FLT\_T}}$ and $\overline{\text{FLT\_I}}$ pins are ORed together.	B
$\overline{\text{FLT\_I}}$	5	6 (GND)	An overcurrent fault is not indicated.	B
GND	6	7 (IMON)	The output of the IMON pin is not reported.	B
IMON	7	8 (IWRN)	The output range of the IMON pin and the set point of the IWRN pin changes, based on the total bias currents flowing through the IMON and IWRN resistors.	C
IWRN	8	9 (TMR)	The thresholds of the TMR and IWRN pins are affected. The external FET shuts off at a different threshold than set by the IWRN pin. During an overcurrent fault, the TMR feature become inactive, and the device is in latch-off mode.	C
TMR	9	10 (DIODE)	The automatic retry feature is disabled. The overtemperature feature can give false errors and cause the external FET to turn OFF.	B
NC	11	12 (BST)	Applies to TPS1210-Q1 only. There is no effect to the device.	D
G	11	12 (BST)	Applies to TPS1211-Q1 only. When the INP_G pin is driven low, the BST pin (gate driver supply) is loaded through the internal G pulldown switch. The gate driver UVLO hits; resulting in turning off the external FETs.	B
BST	12	13 (SRC)	The gate drive supply is shorted and the external FETs do not turn ON.	B
SRC	13	14 (PD)	The pulldown switch (between PD and SRC) of the internal gate driver is shorted. The external FET remains OFF.	B
PD	14	15 (PU)	The turn ON and turn OFF speeds of the external FETs can be impacted.	C
CS–	17	18 (CS+)	The device bypasses the external current sense resistor. The IMON and OCP features are disabled.	B
CS+	18	19 (ISCP)	The short-circuit threshold is reduced.	C
ISCP	19	20 (VS)	The short-circuit protection is set to the minimum setting.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
OV	2	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
INP_G	2	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
INP	3	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
$\overline{\text{FLT\_T}}$	4	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
$\overline{\text{FLT\_I}}$	5	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
GND	6	The supply power is bypassed and the device does not turn on.	B
IMON	7	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
IWRN	8	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
TMR	9	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
DIODE	10	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
NC	11	Applies to TPS1210-Q1 only. There is no effect to the device.	D
G	11	Applies to TPS1211-Q1 only. If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
BST	12	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
SRC	13	The output is stuck onto the supply.	B
PD	14	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
PU	15	If the voltage of the pin exceeds the range for the pin, as indicated in the datasheet, the device can be damaged from voltage breakdown on the ESD circuit.	A
CS-	17	In the application, the external sense resistor is bypassed, and the IMON, overcurrent, and short-circuit protection does not work.	A
CS+	18	The outputs of the IMON and IWRN pins are saturated. The external FET can turn OFF.	B
ISCP	19	The short-circuit protection is set to the minimum setting.	C
VS	20	There is no effect to the device.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from July 14, 2022 to January 29, 2026 (from Revision * (July 2022) to Revision A (January 2026)) **Page**

- Updated generic part number throughout....2
- Corrected bullet regarding the assumptions of use....6
- Added clarity to the description of the potential failure effect for the DIODE pin in the *Pin FMA for Device Pins Open-Circuited* table....6
- Updated format and language to the current TI standard....6
- Removed the period from the no connection pin name....6

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025