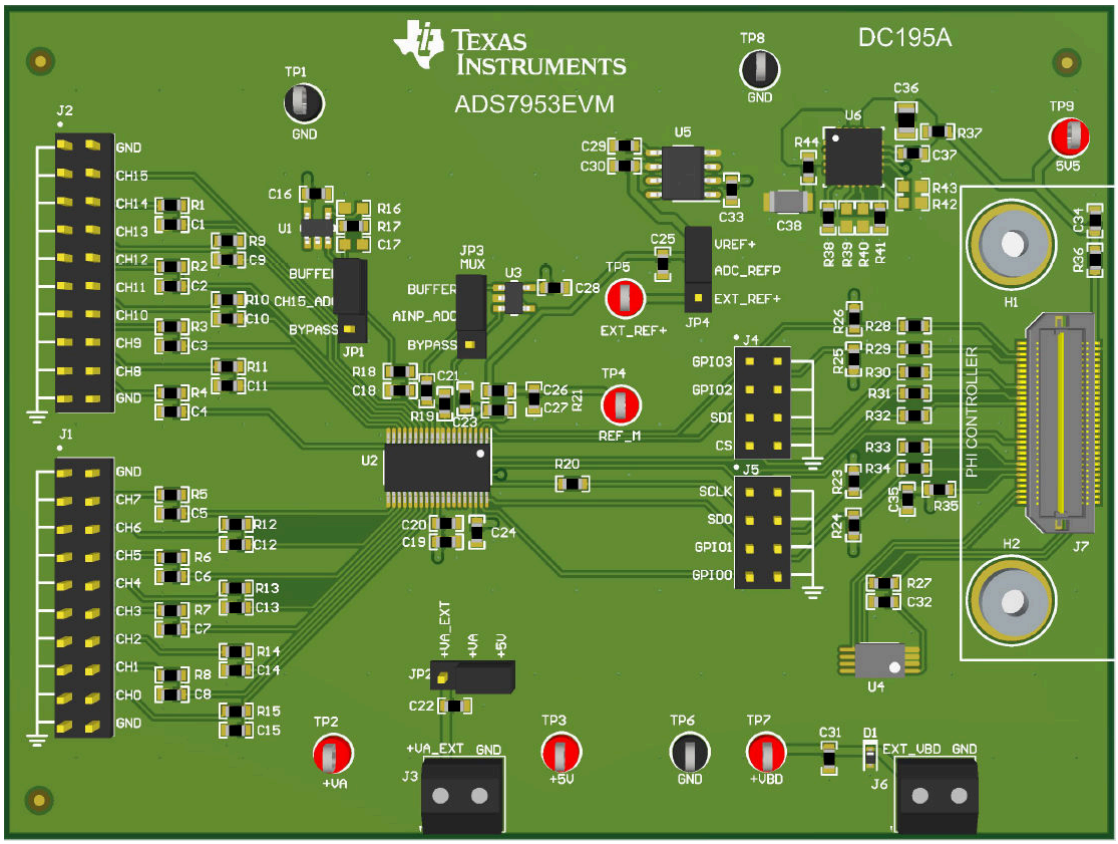
User's Guide

ADS7953EVM-PDK Evaluation Module

ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADS7953 evaluation module (EVM) performance demonstration kit (PDK). This kit is an evaluation platform for the ADS7953 device, which is a 12-bit, 16-channel, 1-MSPS, single-ended analog input, successive approximation register (SAR) analog-to-digital converter (ADC) that features an easy-to-use serial programming interface (SPI). The ADS7953EVM-PDK eases evaluation with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials (BOM).

Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the ADS7953EVM-PDK.



ADS7953EVM-PDK Evaluation Module

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1 Overview

The ADS7953EVM-PDK evaluation kit includes the ADS7953EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis.

The ADS7953EVM board includes the ADS7953 SAR ADC, all the peripheral analog circuits, and the components required to achieve optimum performance from the ADC.

The PHI controller board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS7953 device
- Supplies power to all active circuitry on the ADS7953EVM board

Along with the ADS7953EVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

The following related documents are available through the Texas Instruments web site.

Table 1-1. Related Documentation

Device	Literature Number
ADS7953	SLAS605
OPA192	SBOS620
REF5025	SBOS410
TPS7A47	SBVS204

1.1 ADS7953EVM-PDK Features

The ADS7953EVM-PDK showcases the following features:

- Hardware and software required for diagnostic testing and accurate performance evaluation of the ADS7953 ADC
- USB powered: No external power supply is required
- The PHI controller board provides a convenient communication interface to the ADS7953 ADC over USB 2.0 (or higher) for power delivery and digital inputs and outputs
- Easy-to-use evaluation software for Microsoft® Windows® 10, 64-bit operating systems

1.2 ADS7953EVM Features

The ADS7953EVM showcases the following features:

- Onboard low-noise, low-distortion ADC input driver optimized to meet ADC performance available on channel 15 pin and the MXO-AINP pin
- RC charge-bucket filter on all 16 channels
- Onboard ultra-low noise, low-dropout (LDO) regulator generate supplies for the operational amplifier and ADC

2 Analog Interface

The ADS7953 is a low-power, 16-channel, SAR ADC that supports single-ended analog inputs. The ADS7953EVM uses an OPA192 to drive optional paths such as channel 15 and the AINP pin of the ADC. The ADS7953EVM is designed for easy interfacing to various analog sources. This section describes the front-end driver circuitry details, including jumper configurations for the analog input signal source.

2.1 Connectors for Analog Inputs

The ADS7953EVM is designed to interface to an external, analog source through 100-mil headers. Analog sources can be connected to pins 4 to 18 of connectors J1 and J2 using 100-mil jumper cables or mini grabbers. Table 2-1 and Table 2-2 list the analog input connectors.

Table 2-1. Analog Input J1 Header Description

Pin Number	Signal	Description
J1.18	CH0	Channel 0 analog input
J1.16	CH1	Channel 1 analog input
J1.14	CH2	Channel 2 analog input
J1.12	CH3	Channel 3 analog input
J1.10	CH4	Channel 4 analog input
J1.8	CH5	Channel 5 analog input
J1.6	CH6	Channel 6 analog input
J1.4	CH7	Channel 7 analog input
J1.1-19 (odd), J1.2, J1.20	AGND	Analog ground connections

Table 2-2. Analog Input J2 Header Description

Pin Number	Signal	Description
J2.18	CH8	Channel 8 analog input
J2.16	CH9	Channel 9 analog input
J2.14	CH10	Channel 10 analog input
J2.12	CH11	Channel 11 analog input
J2.10	CH12	Channel 12 analog input
J2.8	CH13	Channel 13 analog input
J2.6	CH14	Channel 14 analog input
J2.4	CH15	Channel 15 analog input
J2.1-19 (odd), J2.2, J2.20	AGND	Analog ground connections

2.2 ADC Input Signal Driver

The SAR ADC inputs terminate in switched-capacitor networks that create large instantaneous current loads when the switches are closed, which effectively makes the ADC inputs dynamically low impedance. The analog inputs of the ADC are therefore driven by an OPA192 used in a unity-gain buffer configuration to maintain ADC performance with maximum loading (1 MSPS) at full device throughput of the ADS7953.

2.2.1 Input Signal Path

Figure 2-1 shows the signal path for the analog inputs applied to the ADS7953EVM. A separate OPA192 amplifier is used in a unity-gain buffer configuration to drive the individual analog input of channel 15 (CH15). An additional OPA192 is connected from the internal multiplexer output (MXO) to the ADC input (AINP). Onboard provisioning enables both OPA192 amplifiers to be bypassed with configurable jumper options listed in Table 5-1 . An RC filter with values of 33 Ω and 270 pF was selected to achieve a optimal performance at full throughput (1 MSPS) of the ADS7953.

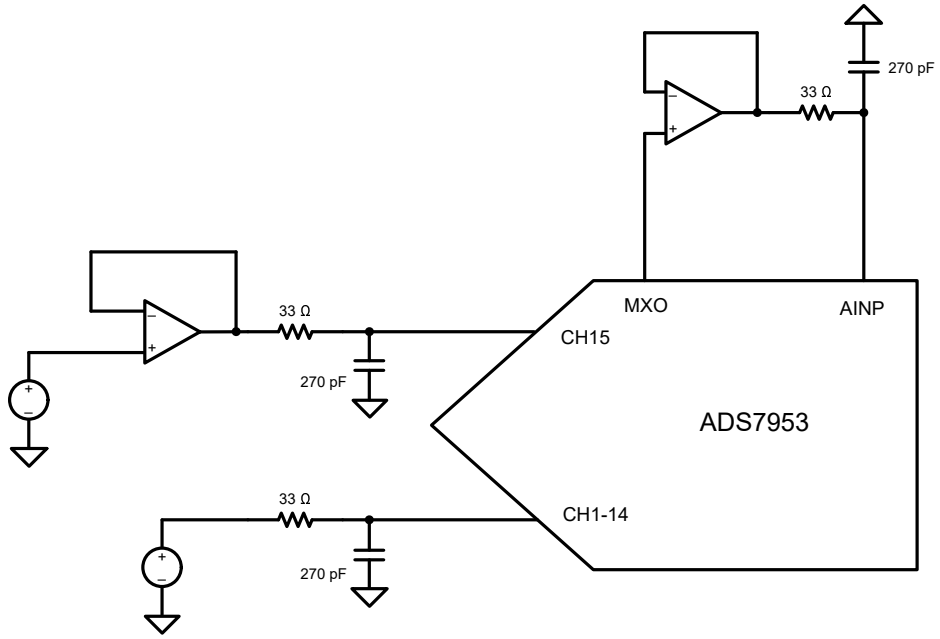

Figure 2-1. ADS7953 Analog Input Path

3 Digital Interfaces

As discussed in Section 1, the ADS7953EVM interfaces with the PHI, which in turn communicates with the computer over the USB. The two devices on the EVM that the PHI communicates with are the ADS7953 ADC (over the SPI) and the EEPROM (over the I^2C interface). The electrically erasable programmable read-only memory (EEPROM) comes preprogrammed with the information required to configure and initialize the ADS7953EVM-PDK platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 SPI for the ADC Digital I/O

The ADS7953EVM-PDK supports the interface and ADC input modes detailed in the ADS7953 data sheet. The PHI is capable of operating at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC.

4 Power Supplies

The ADS7953 supports a wide range of operation on the analog supplies. The analog supply (+VA) operates from 2.7 V to 5.25 V. The same supply is used to power the two OPA192 amplifiers. The digital supply (+VBD) operates from 1.7 V to 5.25 V, independent of the analog supply.

The analog portion of the ADS7953EVM operates from a 5-V supply (+5V) generated using the TPS7A47 low-noise, low-dropout regulator. The analog supply can be configured to run off an external power supply provided on the terminal block J3. For an external analog supply, short JP2 with a shunt in positions 2-3. Otherwise, keep the shunt on the default positions 1-2 for the on-board TPS7A47 generated supply.

The digital portion of the ADC and EEPROM operates from a 3.3-V supply sourced from the PHI. If the PHI is not connected to the ADS7953EVM, an external digital supply can be provided through the terminal block J6.

4.1 ADC Voltage Reference Configuration

The ADS7953 operates off of an external 2.5-V voltage reference. By default, the ADS7953 EVM is configured to work with an onboard 2.5-V reference voltage supplied by the REF5025. By default, a shunt is applied on positions 1-2 on JP4.

There is also a provision to bypass the onboard voltage reference and supply an external voltage reference to the ADS7953 REFP pin. When supplying the board with an external reference, the onboard voltage reference must be disabled by adding a shunt across position 2-3 on JP4 and the external reference can be applied on TP5. Supplying an external voltage reference to the EVM allows for the 2 × V_{REF} mode of the ADS7953.

The ADS7953 REFM pin is set to ground by default. However, a different voltage can be used by removing R21 and applying the desired REF_M voltage to TP4.

5 ADS7953EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for proper operation of the ADS7953EVM-PDK.

5.1 Default Jumper Settings

Figure 5-1 details the jumper locations for the ADS7953EVM-PDK.

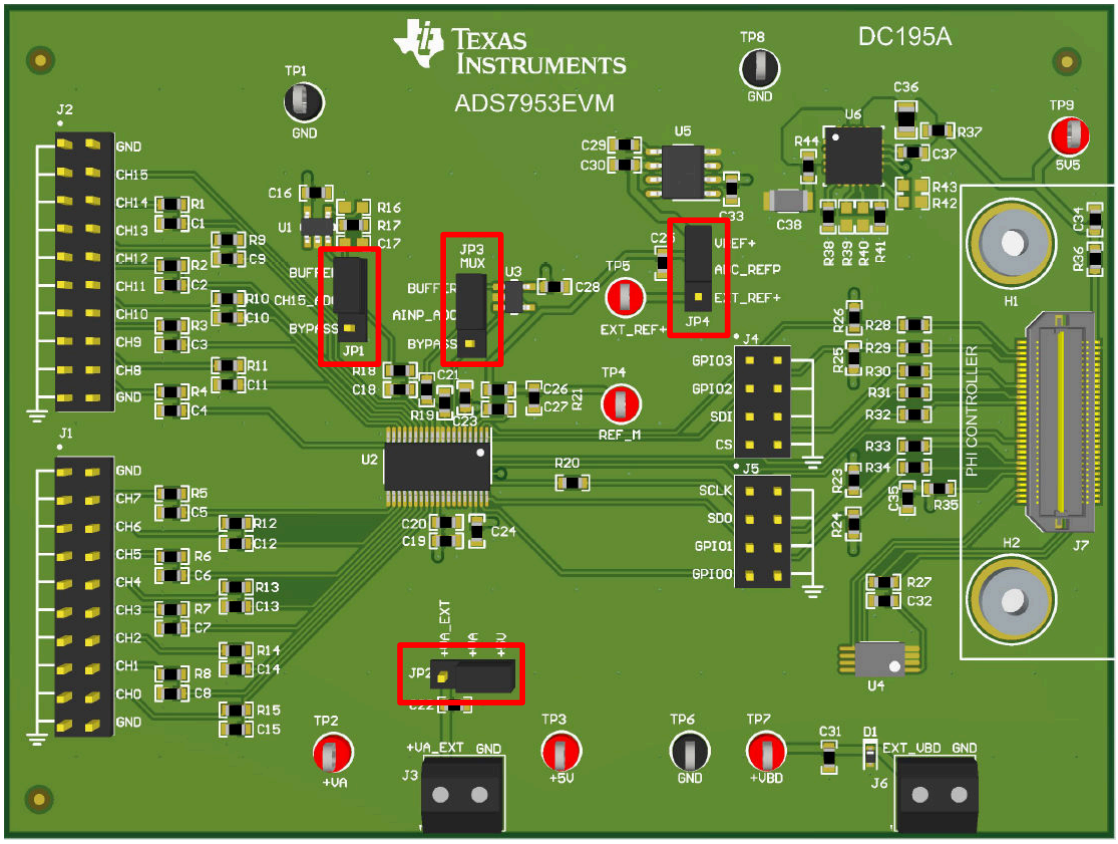

Figure 5-1. Default Jumper Settings

Table 5-1 lists the functionality and default configuration of each jumper.

Table 5-1. Default Jumper Configurations

Reference Designator	Default Configuration	Description
JP1 and JP3	1-2	Amplifiers are used in this position. Place jumper on pins 2-3 on JP1 or JP3 to bypass the amplifier in the circuit.
JP2	1-2	Onboard +VA supply is used in this position. Place the jumper in position 2-3 to connect an external supply.
JP4	1-2	Onboard reference is used in this position. Place the jumper in position 2-3 to connect an external reference.

5.2 EVM Graphical User Interface Software Installation

The following steps describe how to install the software for the ADS7953 EVM graphical user interface (GUI).

1. Download the latest version of the EVM GUI installer from the *Order & Start development* section of the ADS7953EVM-PDK Tool Folder and run the GUI installer to install the EVM GUI software on your computer.
2. Accept the license agreements (Figure 5-2) and follow the on-screen instructions to complete the installation.

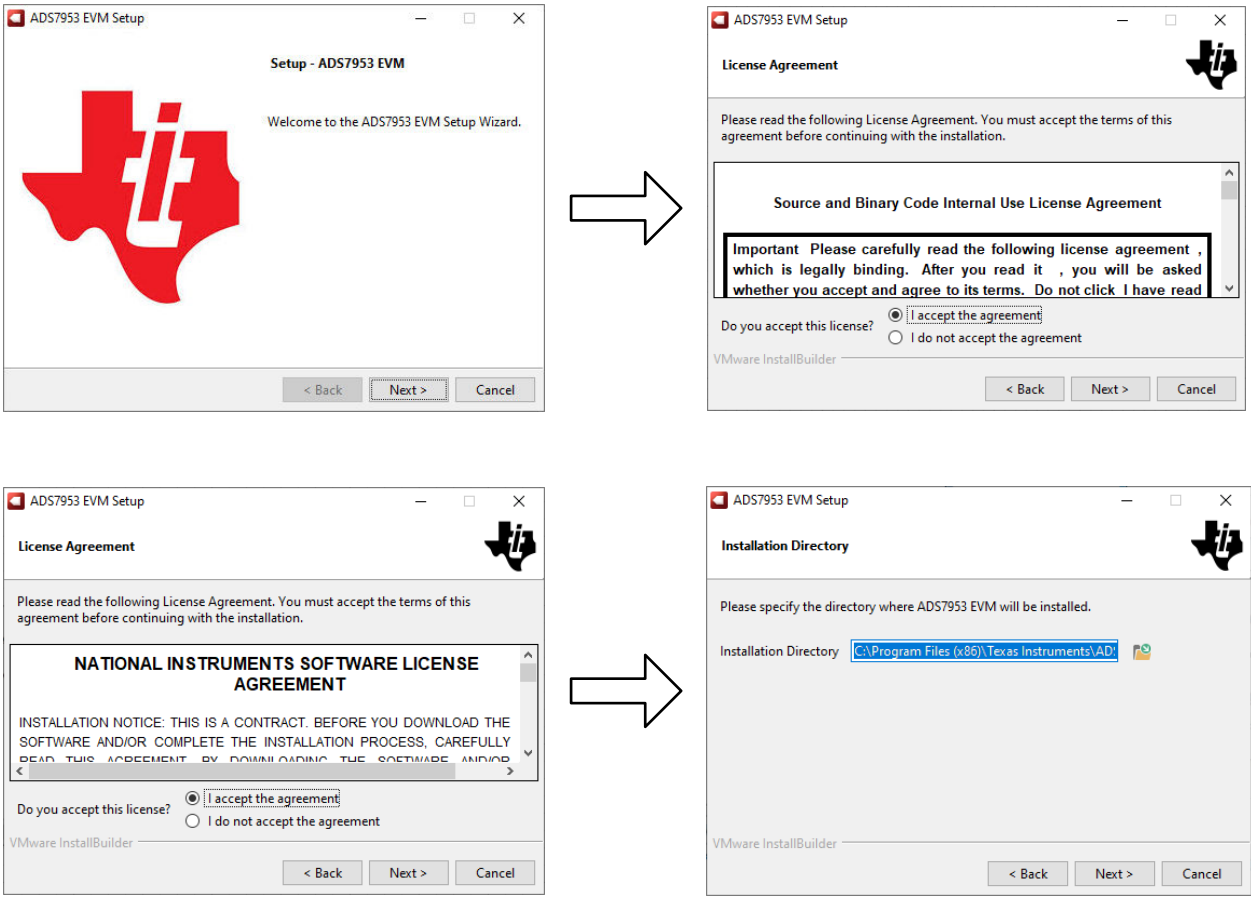

Figure 5-2. Software Installation Prompts

3. As a part of the ADS7953EVM GUI installation, a prompt with a Device Driver Installation Wizard (Figure 5-3) appears on the screen. Click the *Next* button to proceed, then click the *Finish* button when the installation is complete.

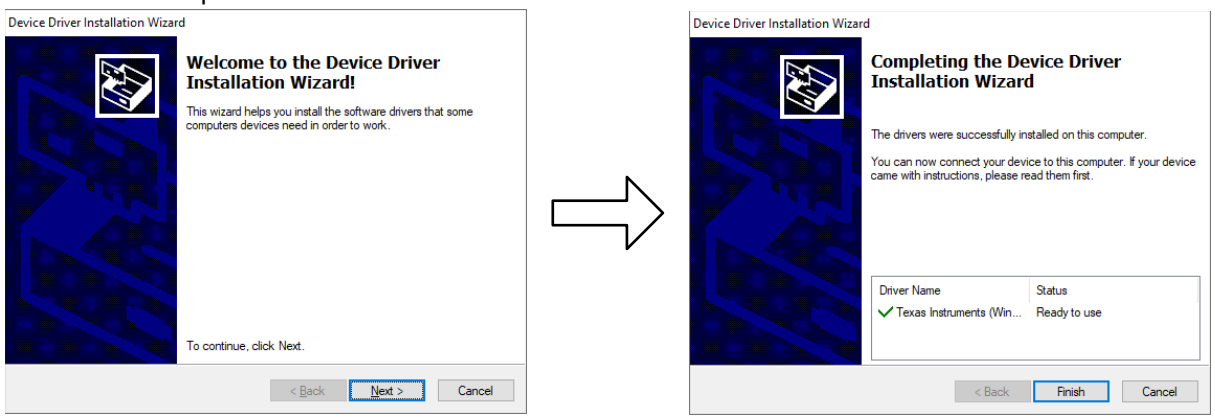

Figure 5-3. Device Driver Installation Wizard

Note

A notice can appear on the screen stating that Windows cannot verify the publisher of this driver software. Select the *Install this driver software anyway* option.

The device requires the LabVIEW™ Run-Time Engine and does not prompt for the installation of this software.

4. Check the *Create Desktop Shortcut* box, as Figure 5-4 shows, after these installations.

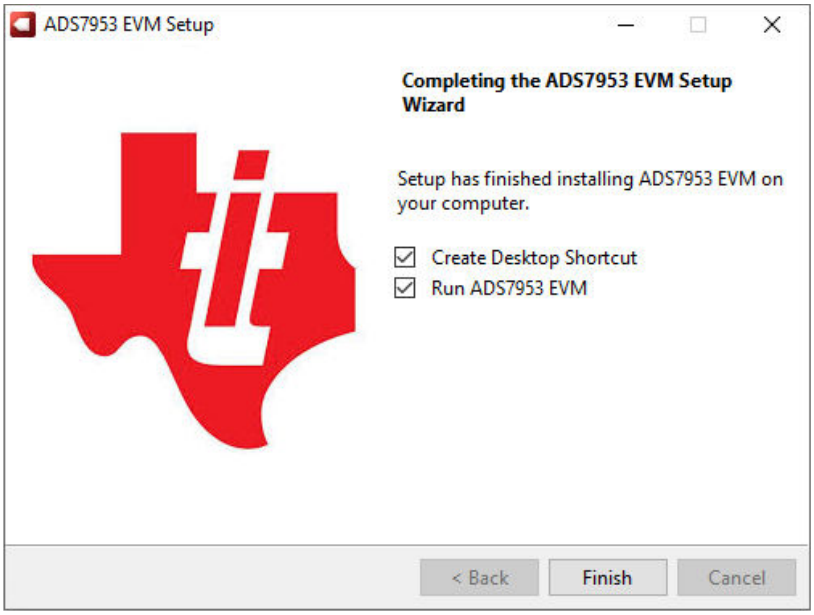

Figure 5-4. Software Installation Final Step

6 ADS7953EVM-PDK Operation

The following instructions are a step-by-step guide for connecting the device to a computer and evaluating the performance of the device.

1. Connect the device EVM to the PHI board.
2. Use the provided USB cable to connect the PHI to the computer.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up.
   - LEDs D1 and D2 on the PHI start flashing, indicating that the PHI is booted up and communicating with the PC.
3. Launch the device EVM GUI software from the installed path, as Figure 6-1 shows, or by using the desktop shortcut created during installation.

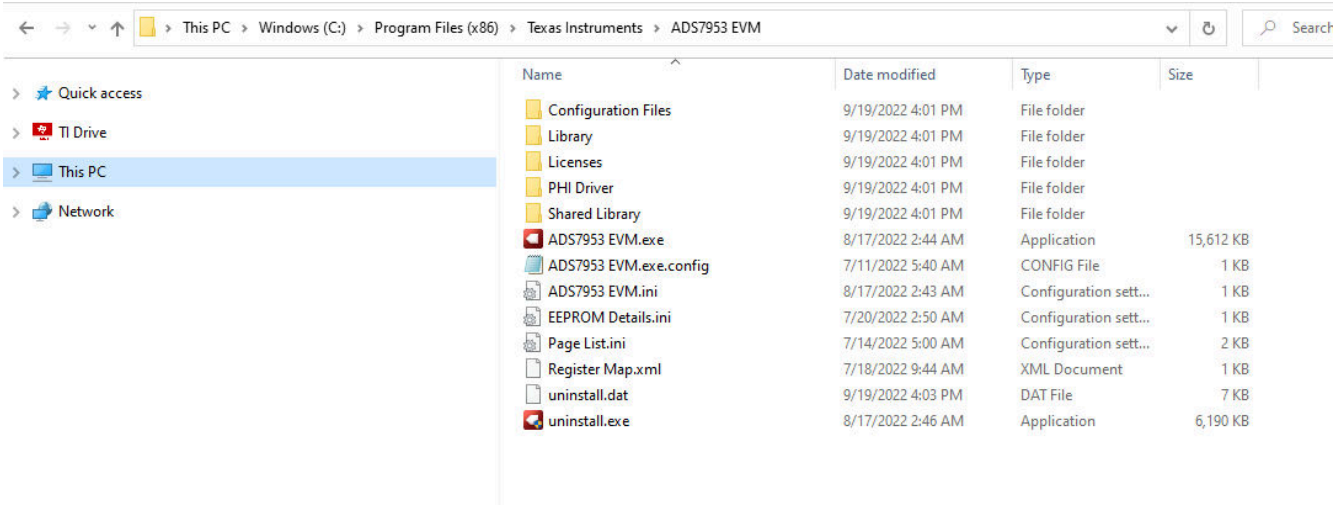

Figure 6-1. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Figure 6-2 shows the input parameters of the GUI (and the default values), through which the various functions of the ADS7953EVM-PDK can be exercised. These settings are global and persist across the GUI tools listed in the top left pane (or from one page to another).

Figure 6-2. EVM GUI Global Input Parameters

The ADS7953 interface configurations can be selected on this page. The GUI lets the user select the ADC input range, mode of operation (manual, Auto 1, and Auto 2), ADC voltage reference, and ADC channel selection using a drop-down menu.

The *SCLK Frequency* and *Sampling Rate* settings are selected on this page. The GUI lets the user enter the target values for these two parameters, and the GUI computes the closest value that can be achieved, considering the timing constraints of the device.

Specify a target SCLK frequency (Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI phase-locked loop (PLL) settings; however, the achievable frequency can differ from the target value entered. Similarly, the sampling rate of the ADC can be adjusted by modifying the *Target Sampling Rate* argument (Hz). The achievable ADC sampling rate can differ from the target value, depending on the applied SCLK frequency and the closest match achievable is displayed. This page, therefore, allows various settings available on the device to be tested in a repetitive fashion until arriving at the best settings for the corresponding test scenario.

6.2 Time Domain Display Tool

The *Time Domain Display* tool provides a visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or front-end drive circuits.

As per the selected interface mode settings using the *Capture* button indicated in Figure 6-3, the user can trigger a data capture of the selected number of samples from the ADS7953EVM-PDK. The sample indices are on the x-axis, and two y-axes show the corresponding output codes and the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections triggers calculations to be performed on the same set of data.

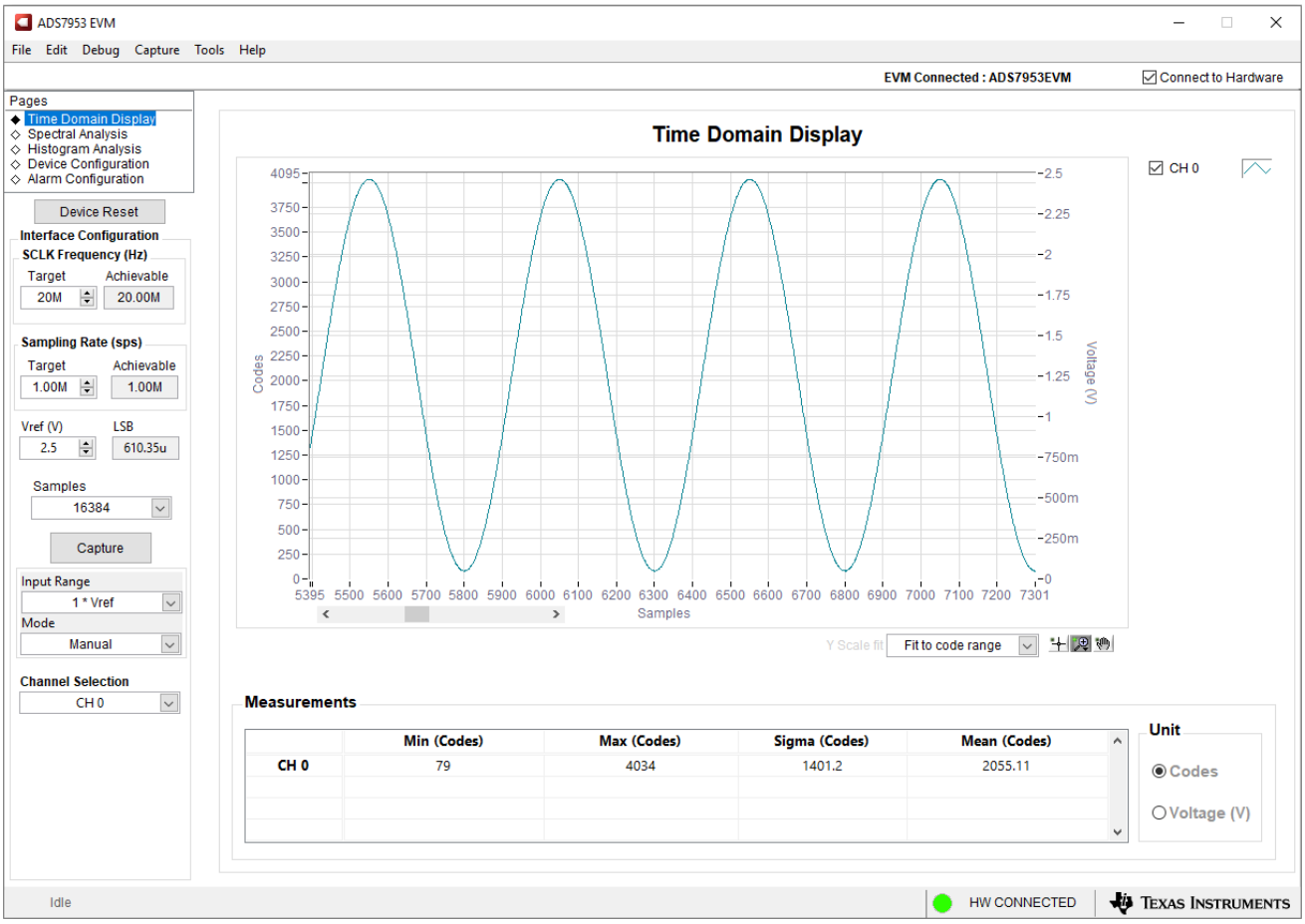

Figure 6-3. Time Domain Display Tool

6.3 Spectral Analysis Tool

The *Spectral Analysis* tool (Figure 6-4) is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS7953 SAR ADC through the use of a single-tone, sinusoidal signal fast Fourier transform (FFT) analysis, using the 7-term Blackman-Harris window setting. Alternatively, the window setting of *None* can be used to search for noise spurs over frequency in DC inputs.

For dynamic performance evaluation, the external, single-ended source must have better specifications than the ADC to make sure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements listed in Table 6-1. Alternately, the user can use the Precision Signal Injector EVM that provides a low-distortion, low-noise, 2-kHz input signal for driving the input of the ADC, and pairs with most of the TI SAR ADC evaluation modules (EVMs). The board is powered over a USB, which also provides a user-interface connection to a PC.

Table 6-1. External Source Requirements for Device Evaluation (SNR and THD)

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Single-ended
Minimum SNR	90 dB
Minimum THD	–100 dB

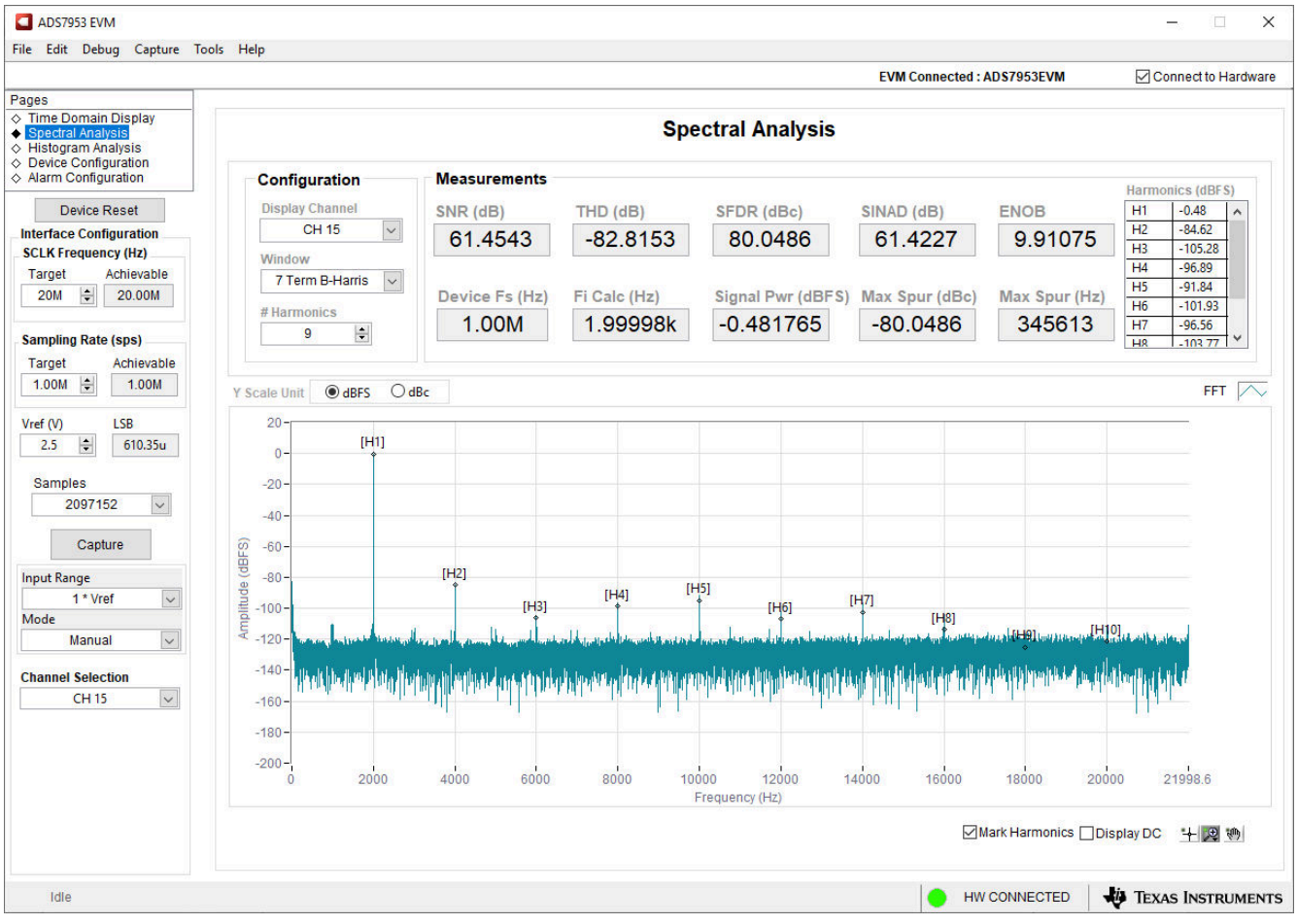

Figure 6-4. Spectral Analysis Tool

6.4 Histogram Analysis Tool

The *Histogram Analysis* tool can be used to estimate the effective resolution of the ADC resulting from performance degradation caused by noise. Effective resolution is an indicator of the number of bits of ADC measurement resolution resulting from performance losses caused by noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output (from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC) is reflected in the standard deviation of the ADC output code histogram obtained by performing multiple conversions of a DC input applied to a given channel.

The histogram corresponding to a DC input is displayed by clicking the *Capture* button. The example capture shown in Figure 6-5 is captured with the ADC configured in single-ended and 1 × V_{REF} mode and with the AINP pin driven with +1 V.

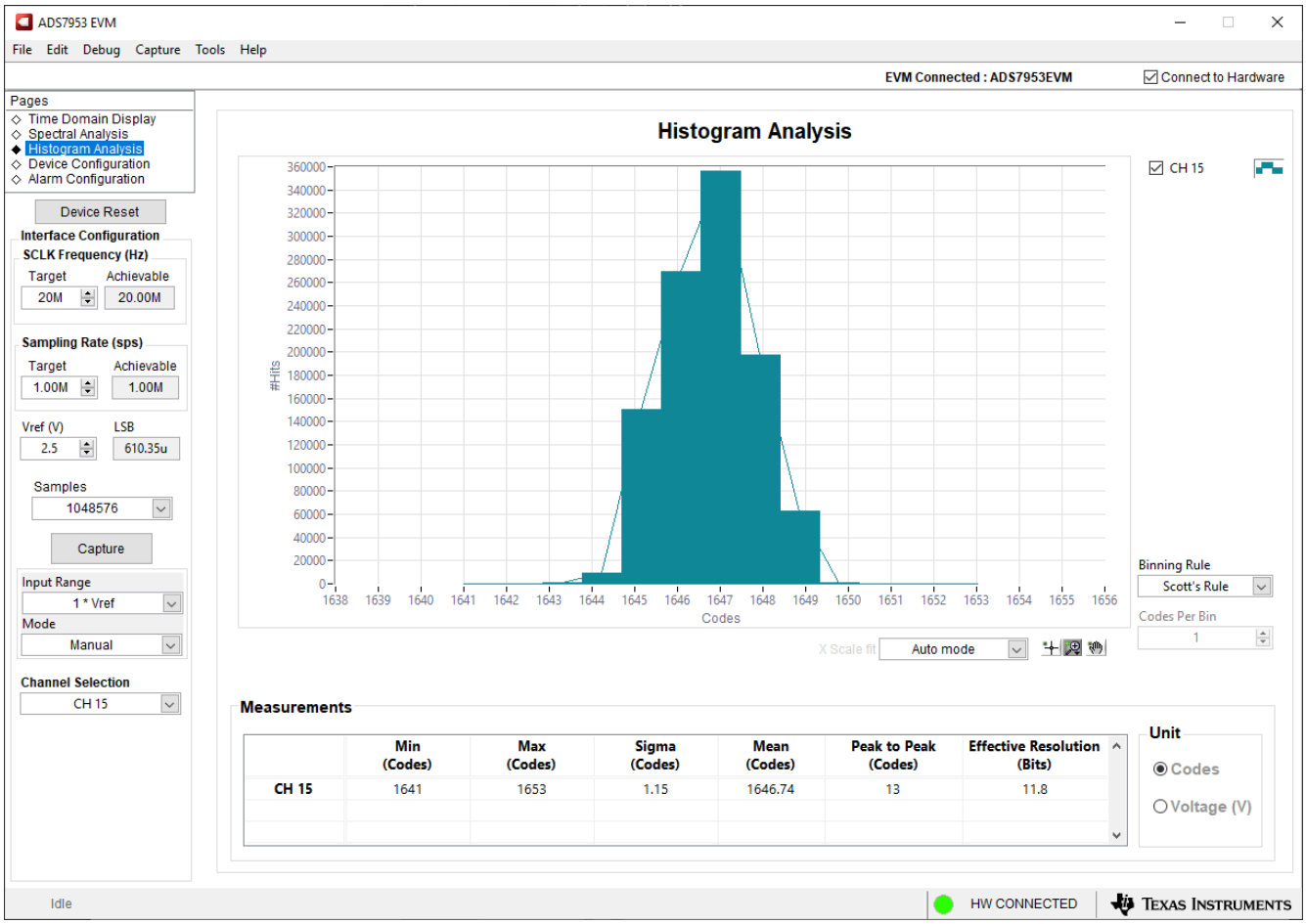

Figure 6-5. Histogram Analysis Tool

6.5 Device Configuration

The *Device Configuration* page configures the GPIO and general settings that the ADS7953 ADC offers. The ADS7953 device has four GPIO pins that can be independently configured for various functions, such as general-purpose input (GPI), general-purpose output (GPO), power-down input, device range input, and alarm thresholds. Not all GPIOs are capable of each function. See the *GPIO Registers* section in the ADS7953 data sheet for additional details. These GPIO functions can be selected using drop-down menus. The GPIO direction can also be configured as an input or output. These GPIO settings are programmed to the ADC by clicking on the button shown in Figure 6-6 .

The general settings shown in Figure 6-6 can also be configured in this page. If a GPIO is configured as a GPO, then the output can be user controlled as either a logic *0* or *1*. Below the general settings are four visual GPIO alerts that illuminate when the GPI input value is equal to a logic *1*.

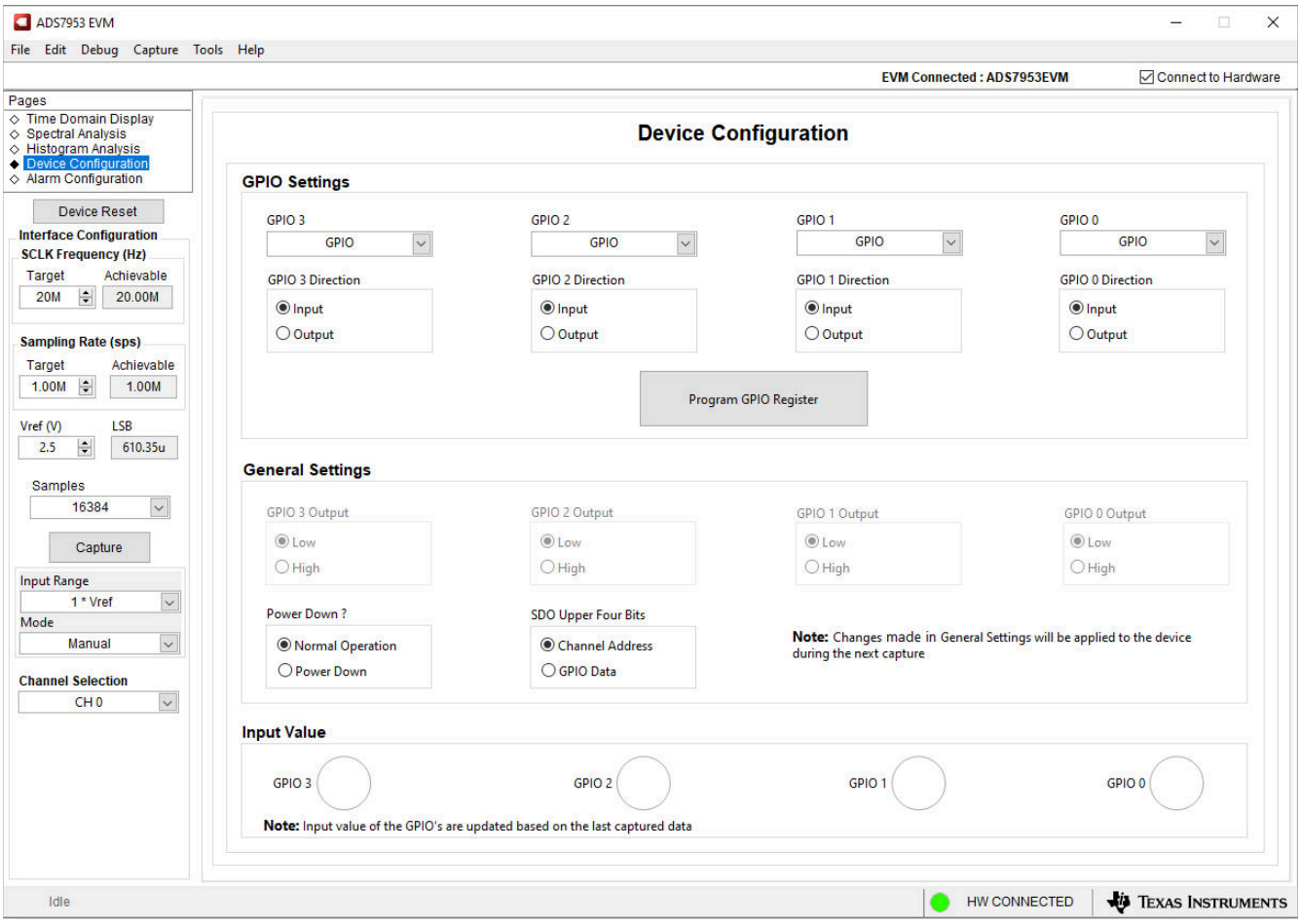

Figure 6-6. Device Configuration Page

6.6 Alarm Configuration

The *Alarm Configuration* page (Figure 6-7) sets the alarm thresholds of the ADS7953 ADC. The device has an alarm feature that allows GPIO0 to be configured as either a *high or low* or just as a *low* alarm threshold and GPIO1 to be configured as a *low* alarm threshold. These GPIO configurations can be set by going to the *Device Configuration* page and using the drop-down menu to select the appropriate function for the two GPIOs. In the GUI, these thresholds are set using a 12-bit hexadecimal value and are available on all 16 channels. If a threshold is crossed, the bell under GPIO0 or GPIO1 illuminates depending on which threshold is crossed and the configuration of the two GPIOs. To program the values, enter the appropriate threshold value and click on the *Program Alarm Registers* button. Only channels 0 to 7 are displayed by default. To set the thresholds for the other eight channels, click the **CH8-CH15** button next to *Select Page* at the bottom right corner of the window.

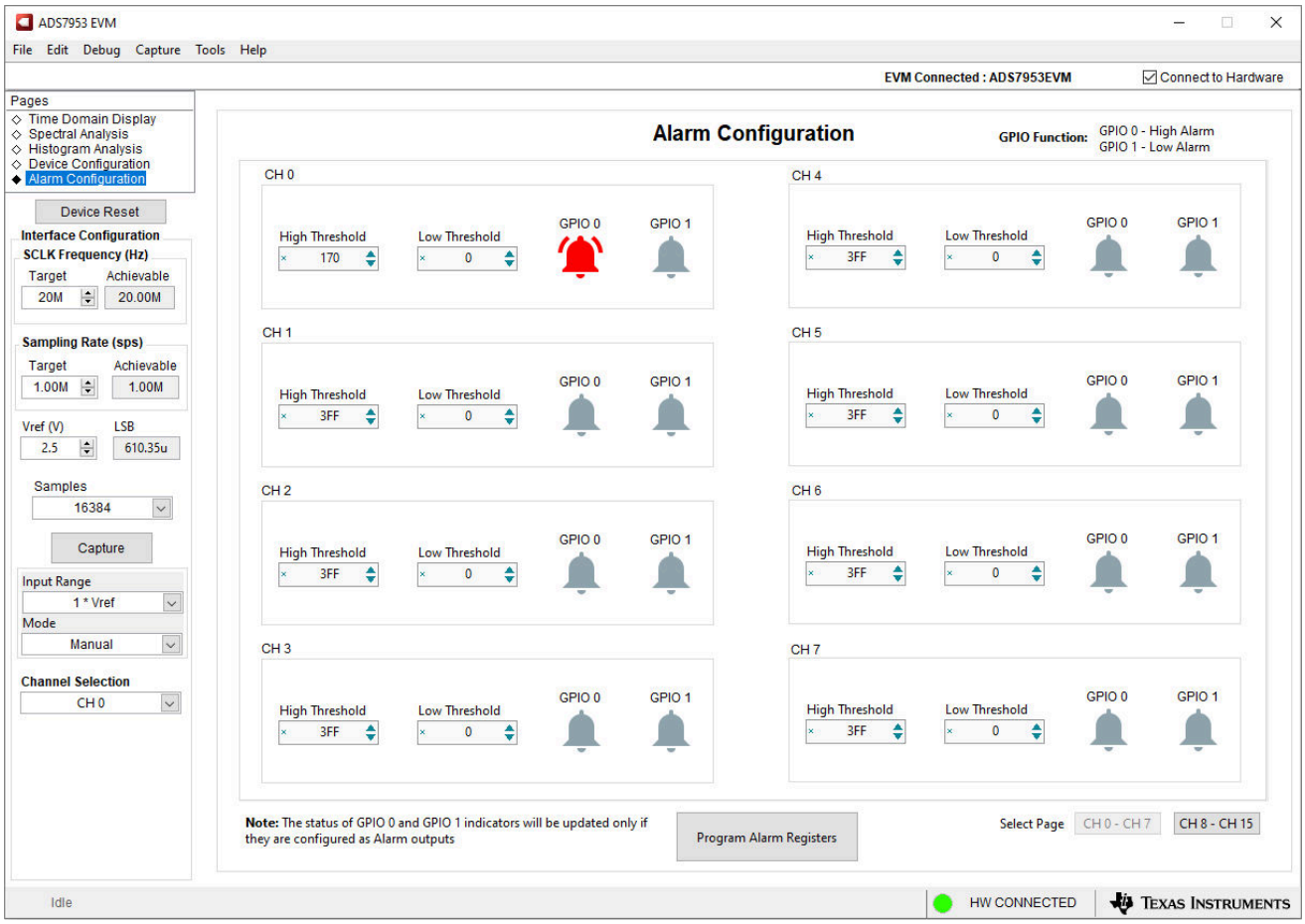

Figure 6-7. Alarm Configuration Page

7 Schematic, Bill of Materials, and Printed-Circuit Board Layout

This section contains the ADS7953EVM schematic, bill of materials, and printed-circuit board layout.

7.1 Schematic

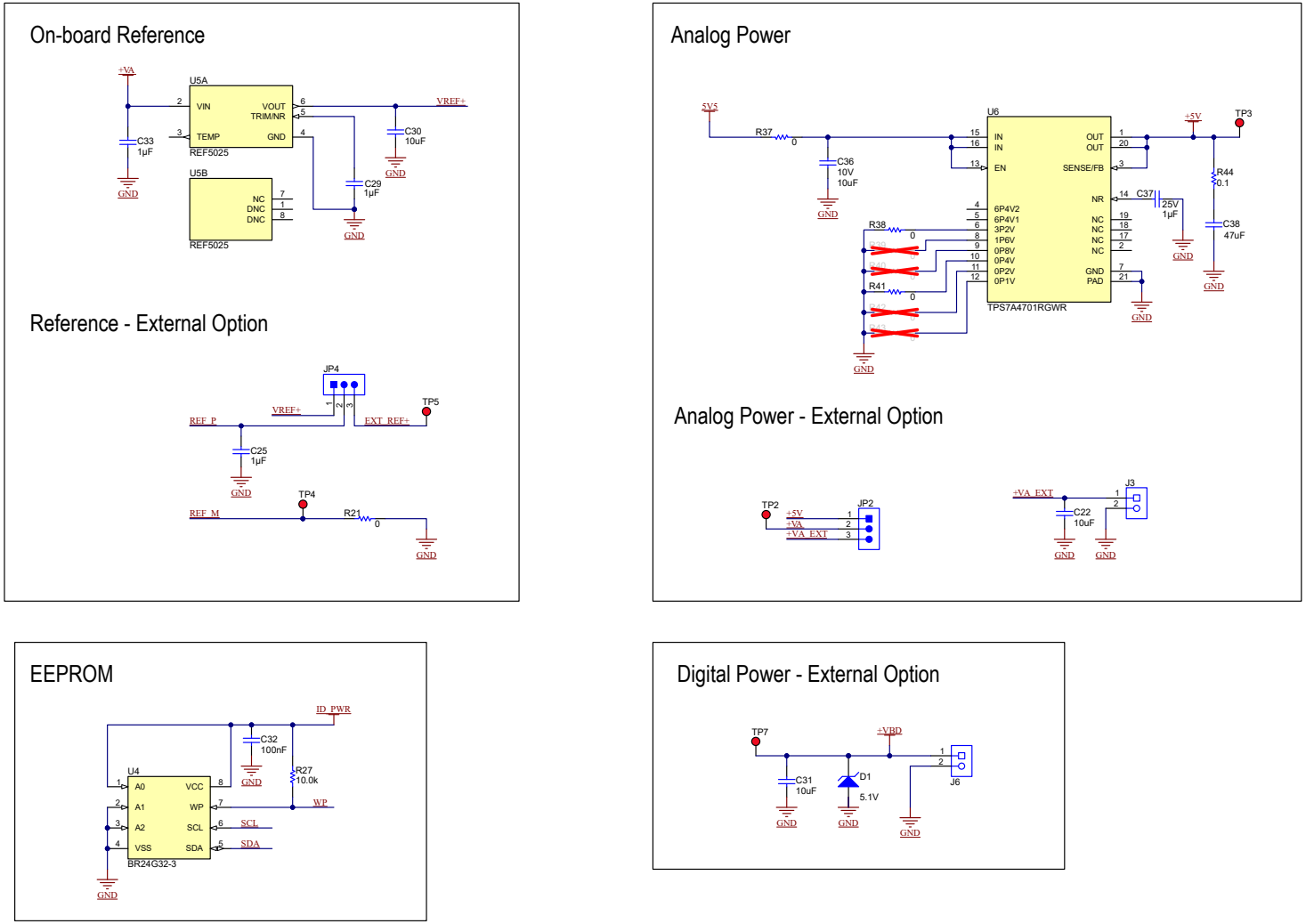

Figure 7-1. Schematic Diagram (Page 1): Reference, EEPROM, Power Supplies

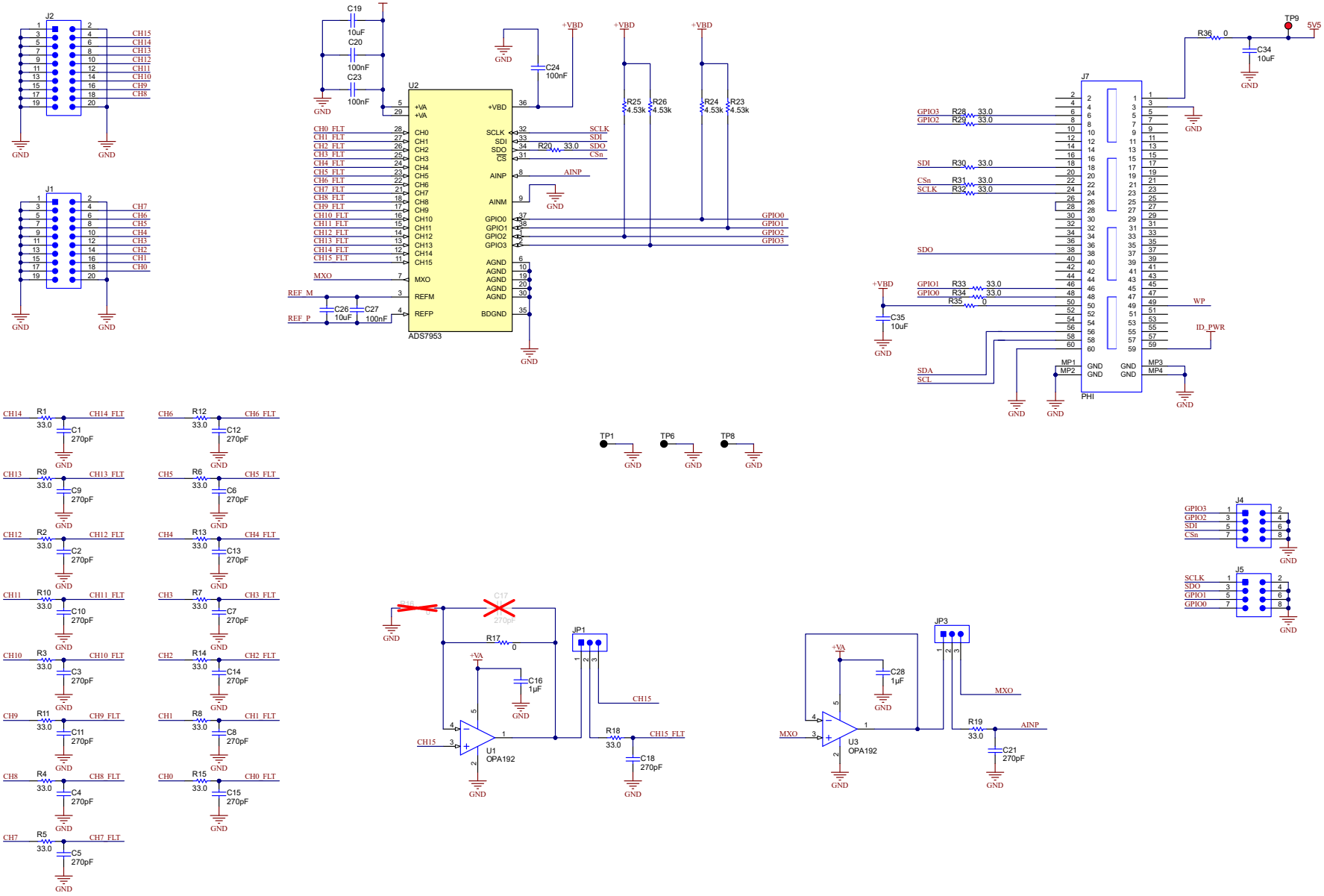

Figure 7-2. Schematic Diagram (Page 2): Analog Inputs, ADC Main, PHI Connector

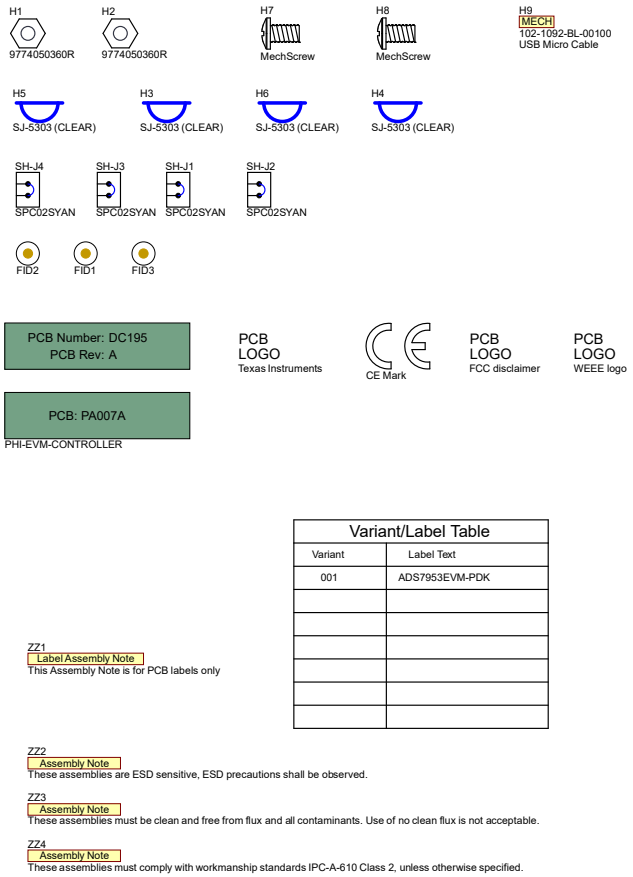

Figure 7-3. Schematic Diagram (Page 3): Hardware Components

7.2 Bill of Materials

Table 7-1 lists the ADS7953EVM BOM.

Table 7-1. ADS7953EVM Bill of Materials

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
GRM1885C1H271JA01D	17	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C18, C21	MuRata	CAP, CERM, 270 pF, 50 V, +/- 5%, C0G/NP0, 0603
EMK107B7105KA-T	5	C16, C25, C28, C29, C33	Taiyo Yuden	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603
GRM188R61C106MAALD	7	C19, C22, C26, C30, C31, C34, C35	MuRata	CAP, CERM, 10 uF, 16 V, +/- 20%, X5R, 0603
C1608X7R1E104K080AA	5	C20, C23, C24, C27, C32	TDK	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603
C0805C106K8PACTU	1	C36	Kemet	CAP, CERM, 10 uF, 10 V, +/- 10%, X5R, 0805
CGA3E1X7R1E105K080AD	1	C37	TDK	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603
C3216X5R1E476M160AC	1	C38	TDK	CAP, CERM, 47 uF, 25 V, +/- 20%, X5R, 1206_190
BZX585-C5V1,115	1	D1	NXP Semiconductor	Diode, Zener, 5.1 V, 300 mW, SOD-523
N/A	3	FID1, FID2, FID3	N/A	Fiducial mark. There is nothing to buy or mount.
9774050360R	2	H1, H2	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5 MM
SJ-5303 (CLEAR)	4	H3, H4, H5, H6	3M	Bumpon, Hemisphere, 0.44 X 0.20, Clear
RM3X4MM 2701	2	H7, H8	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
TSW-110-07-G-D	2	J1, J2	Samtec	Header, 100mil, 10x2, Gold, TH
ED555/2DS	2	J3, J6	On-Shore Technology	Terminal Block, 3.5mm Pitch, 2x1, TH
TSW-104-07-G-D	2	J4, J5	Samtec	Header, 100mil, 4x2, Gold, TH
QTH-030-01-L-D-A	1	J7	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
TSW-103-07-G-S	4	JP1, JP2, JP3, JP4	Samtec	Header, 100mil, 3x1, Gold, TH
RC0603FR-0733RL	25	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R18, R19, R20, R28, R29, R30, R31, R32, R33, R34	Yageo	RES, 33.0, 1%, 0.1 W, 0603
CRCW06030000Z0EA	4	R17, R21, R35, R36	Vishay-Dale	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
RC0603FR-074K53L	4	R23, R24, R25, R26	Yageo	RES, 4.53 k, 1%, 0.1 W, 0603
RCG060310K0FKEA	1	R27	Vishay Draloric	RES, 10.0 k, 1%, 0.1 W, 0603
ERJ-3GEY0R00V	1	R37	Panasonic	RES, 0, 5%, 0.1 W, 0603
ERJ-3GEY0R00V	2	R38, R41	Panasonic	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3RSFR10V	1	R44	Panasonic	RES, 0.1, 1%, 0.1 W, 0603
SPC02SYAN	4	SH-J1, SH-J2, SH-J3, SH-J4	Sullins Connector Solutions	Shunt, 100mil, Flash Gold, Black
5011	3	TP1, TP6, TP8	Keystone	Test Point, Multipurpose, Black, TH
5010	6	TP2, TP3, TP4, TP5, TP7, TP9	Keystone Electronics	Test Point, Multipurpose, Red, TH
OPA192IDBVT	2	U1, U3	Texas Instruments	Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with E-trim, 4.5 to 36 V, 8-Pin SOT-23 (DBV)
ADS7953SBDBTR	1	U2	Texas Instruments	12-Bit, 1-MSPS, 16-Channel, Single-Ended, microPower SAR ADC with Serial I/F, DBT0038A (TSSOP-38)
BR24G32FVT-3AGE2	1	U4	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
REF5025ID	1	U5	Texas Instruments	Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin SOIC (D)
TPS7A4701QRGWR	1	U6	Texas Instruments	35 V, 1 A, 4.2µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)

7.3 PCB Layout

Figure 7-4 through Figure 7-7 show the EVM PCB layout.

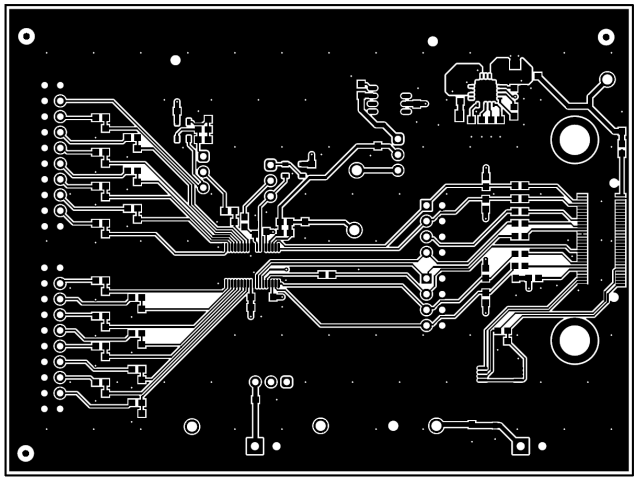

Figure 7-4. Layer 1: Top Layer

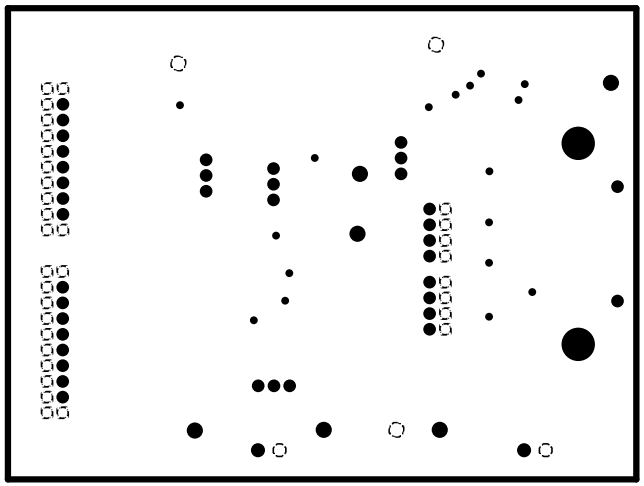

Figure 7-5. Layer 2: GND Plane

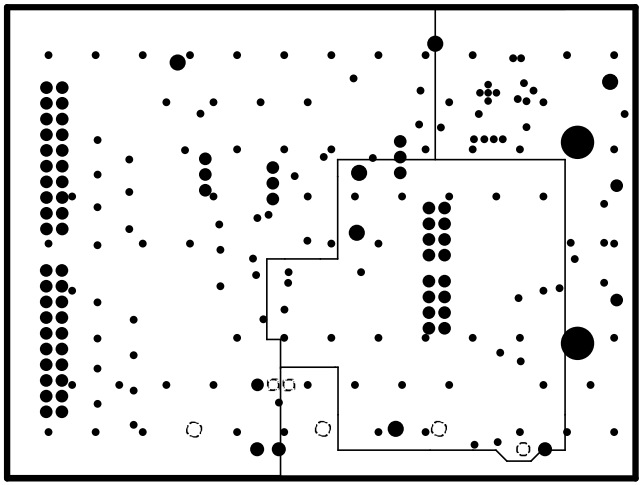

Figure 7-6. Layer 3: Power Plane

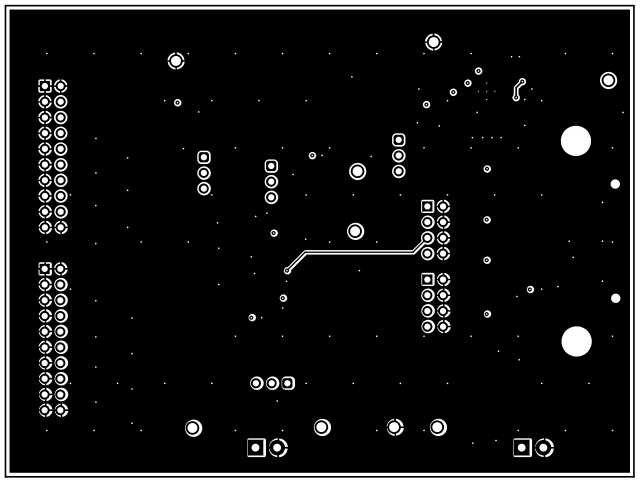

Figure 7-7. Layer 4: Bottom Layer

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