Application Note

Powering Noise Sensitive LIDAR ADC Designs With TPS62913 Low-Ripple and Low-Noise Buck Converter

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ABSTRACT

- The power supply design demonstrates a simplified and efficient implementation of the TPS62913 low ripple and low noise buck converter to power an ADC12QJ1600-Q1, reducing power consumption by 1.908W (32% power savings).
- The Analog, Digital, and Clock rails are all supplied using the switching regulator without the need for a low-dropout linear regulator (LDO) while maintaining the same performance as the original design.
- Design is applicable for ADC12QJ1600-Q1 and other ADCs that require low noise power supplies that are size constrained and thermal constrained.
- Short description of ADC12QJ1600-Q1 and overview of the EVM modifications to use a switching supply only, without the need for LDOs.
- Key measurement results and comparison with and without spread specturm to previous implementation, including output noise density, SNR, and SFDR.

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Trademarks

1 Introduction and System Description

1.1 Introduction

High speed analog to digital converters are notoriously sensitive to power supply noise. The most common solution to minimize that noise is to use linear power supplies, or a switch mode power supply (SMPS) from the main bus rail followed by a low dropout regulator. Compared to a linear supply, there are two big advantages of being able to use a SMPS alone: the reduction in power loss and the size of the power supply. To use a SMPS alone requires careful consideration of the switching supply selected, as well as the design and layout of the SMPS to achieve the desired results of the same performance with lower power dissipation and smaller board space.

This application note uses the ADC12QJ1600-Q1 as an example of a high performance ADC where the supplies have been changed from a SMPS+LDO approach to a SMPS-only approach. This methodology can be used for many other noise sensitive applications as well. The TPS62913 low-ripple and low-noise buck converter used in this application note is specifically designed to help engineers design power supplies that meet the noise and ripple requirements for noise sensitive applications.

1.1.1 ADC12QJ1600-Q1 Noise and Ripple Requirements

The ADC12QJ1600-Q1 is a family of quad, dual and single channel, 12bit, 1.6 GSPS analog-to-digital converter (ADC). Low power consumption and high sample rate make the ADC12QJ1600-Q1 an ideal suite for light detection and ranging (LiDAR) systems. The ADC12QJ1600-Q1 uses a high-speed JESD204C output interface with up to 8 serialized lanes supporting up to 17.16 Gbps line rate. Deterministic latency and multi-device synchronization is supported through JESD204C subclass-1 and is compatible with JESD204B receivers. Innovative synchronization features, including SYSREF windowing, internal PLL with internal voltage-controlled oscillator (VCO), multi clock outputs for logic and Serdes of FPGA or ASIC, simplify system design for multi-device applications.

The original product evaluation module (EVM) implements low-noise LDOs in addition to the DC/DC buck regulators to minimize any impairments from the supply network. While the DC accuracy of the supply rail is specified for the ADC12QJ1600-Q1, there is no specification on supply voltage noise and supply voltage ripple. Any supply ripple or noise appears attenuated on the output spectrum of the ADC. This attenuation can be expressed as Power Supply Rejection Ration (PSRR) and $PSRR_{MOD}$ (or PSMR) as shown in Figure 1-1.

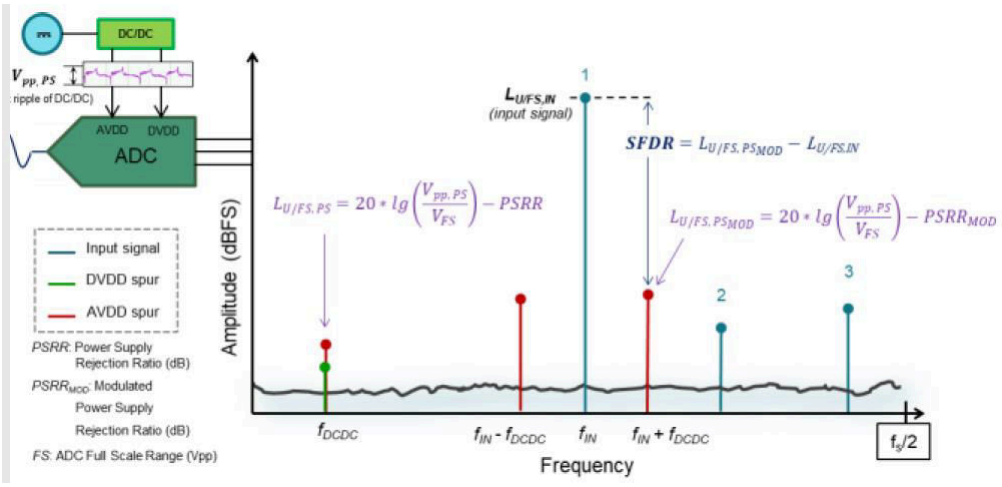


Figure 1-1. Power Supply Noise and Ripple in the ADC Output Spectrum

PSRR is the attenuation of the ADC input supply ripple to the ADC output spectrum at the switching frequency fundamental of the DC-DC converter (f_{DCDC}). $PSRR_{MOD}$ (or PSMR) is the attenuation from the ADC input to the modulated spur in the output spectrum (f_{in} - f_{DCDC}, f_{in} + f_{DCDC}).

PSRR is usually less of a concern since it is typically >40 dB and outside of the frequency of interest, however some analog rails can have PSRR of <40 dB, as shown in Figure 1-2. Most sensitive supplies of the ADC12QJ1600-Q1 are the analog supply rails of VA11 and VA19. More important is PSMR, since the attenuation from the supply rail to the modulated spur can be low for sensitive analog rails such as VA11 and VA19 on the ADC12QJ1600-Q1.

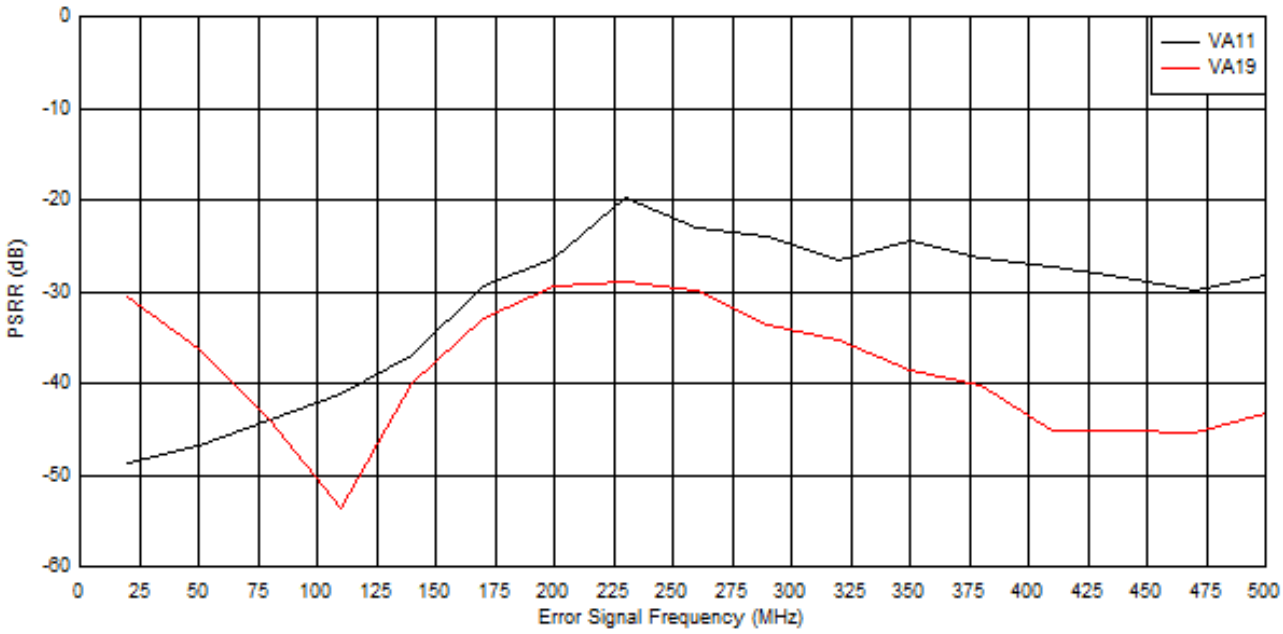


Figure 1-2. ADC12QJ1600-Q1 PSRR of the VA11 and VA19 Supplies

1.1.2 Power Supply Requirements for Clocks

On the ADC12QJ1600-Q1 evaluation module, an external clock is provided to an ultra low noise PLL which is used for clocking the ADC. Similar to high speed ADCs, higher frequencies command larger supply currents. At the same time, higher frequencies require lower clock jitter and therefore lower phase noise. Phase noise is directly impacted by the power supply noise and ripple. The performance of the TPS62913 is shown in Figure 1-3.

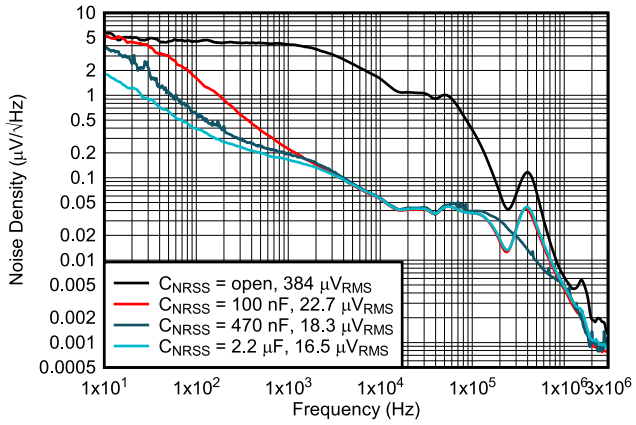


Figure 1-3. TPS62913 Output Noise Density vs Frequency for 12Vin to 3.3Vout at 2.2 MHz

Note

BW = 100 Hz to 100 kHz

The TPS62913 has been designed specifically for low noise with the addition of an external noise reduction filter cap, which also provides the means to adjust the softstart time. Using a 470 nF $C_{NR/SS}$ cap provide the noise performance desired and a 5 ms softstart time.

1.1.3 TPS62913 Low-Noise and Low-Ripple Buck Converter

The TPS62912 and TPS62913 devices are a family of high-efficiency, low-noise and low-ripple synchronous buck converters. The devices are ideal for noise sensitive applications that would normally use an LDO for post regulation such as high-speed ADCs, Clock and Jitter Cleaner, Serializer, De-serializer, LIDAR and RADAR applications. The device operates at a fixed switching frequency of 2.2 MHz or 1 MHz, and can be synchronized to an external clock. To further reduce the output voltage ripple, the device integrates loop compensation to operate with an optional second-stage ferrite bead L-C filter. This allows an output voltage ripple below 10 µVRMS. Low-frequency noise levels, similar to a low-noise LDO, are achieved by filtering the internal voltage reference with a capacitor connected to the NR/SS pin. The optional spread spectrum modulation scheme spreads the DC/DC switching frequency over a wider span, which lowers the mixing spurs.

1.2 Block Diagram

The original ADC12QJ1600-Q1 Rev A evaluation module used several SMPS with LDO followers to provide power to the ADC and clock rails. The 3.3 V clock rails require low phase noise and low jitter. The 1.1 V analog rail (VA11) and digital rail (VD11) are supplied through one LDO and each rail is split with a feed through filter capacitor to ensure low noise requirements for both analog and digital rails. The 1.9 V supplies are also supplied through one LDO with each rail having a split that connects to a feed through filter capacitor as shown in Figure 1-4.

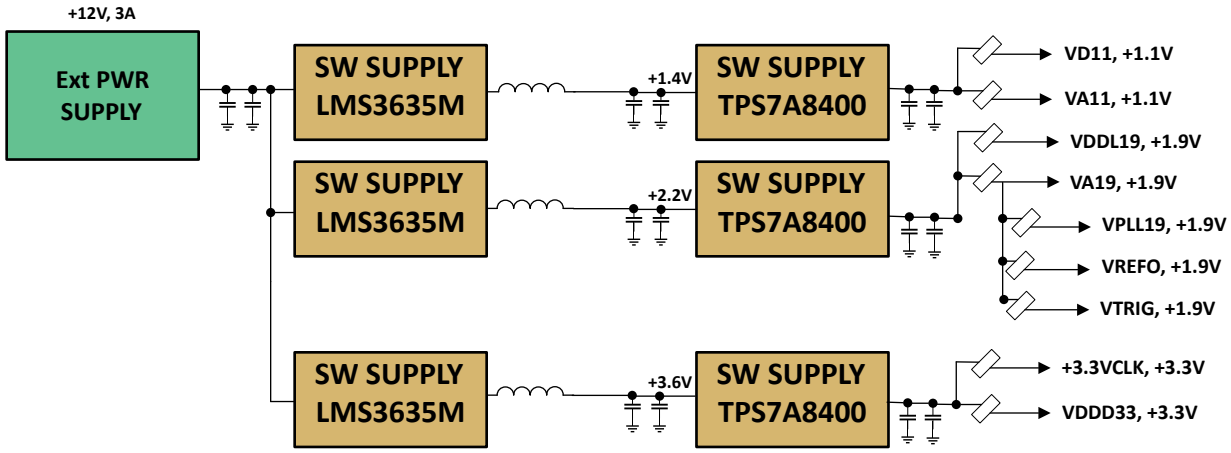


Figure 1-4. Original Power Block Diagram for ADC12QJ1600-Q1 Rev A Evaluation Module

The original EVM power supply is outlined in blue and shown in Figure 1-5.

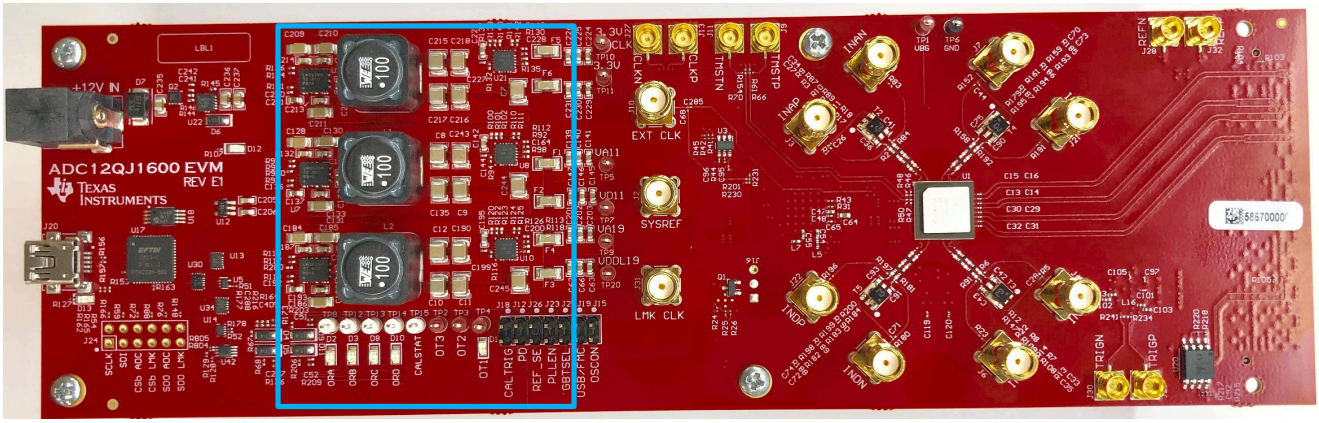


Figure 1-5. Image of Board With Switchers and LDO's Outlined in Blue

In the revised design, the LDOs are removed and the TPS62913 low-ripple, low-noise SMPS is used instead. This design presents a simplified power supply network for the ADC, where all three power domains are supplied from a DC/DC regulator as shown in Figure 1-6. This implementation improves the efficiency and reduces the part count in comparison to a solution using LDOs while maintaining the output voltage ripple and noise requirements of the ADC and clock for good performance.

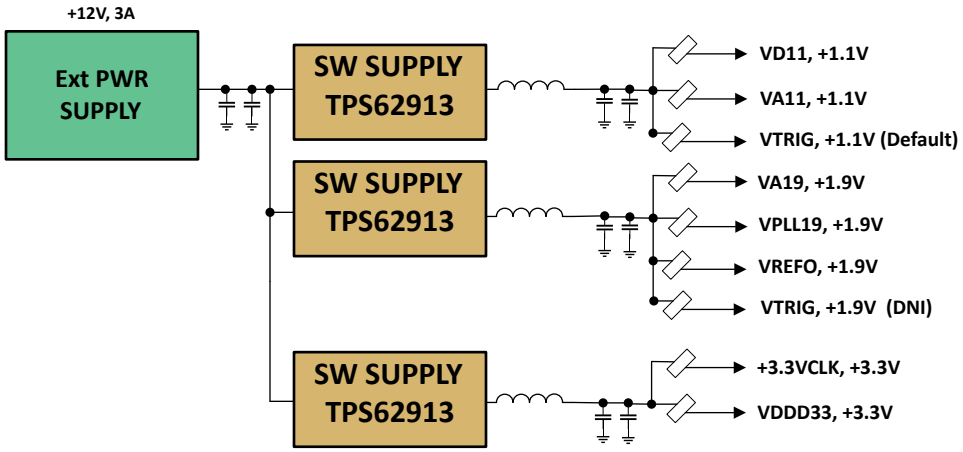


Figure 1-6. Power Block Diagram for ADC12QJ1600-Q1 Rev E2 Evaluation Module With TPS62913

The updated EVM power supply with the TPS62913 is outlined in blue and shown in Figure 1-7.

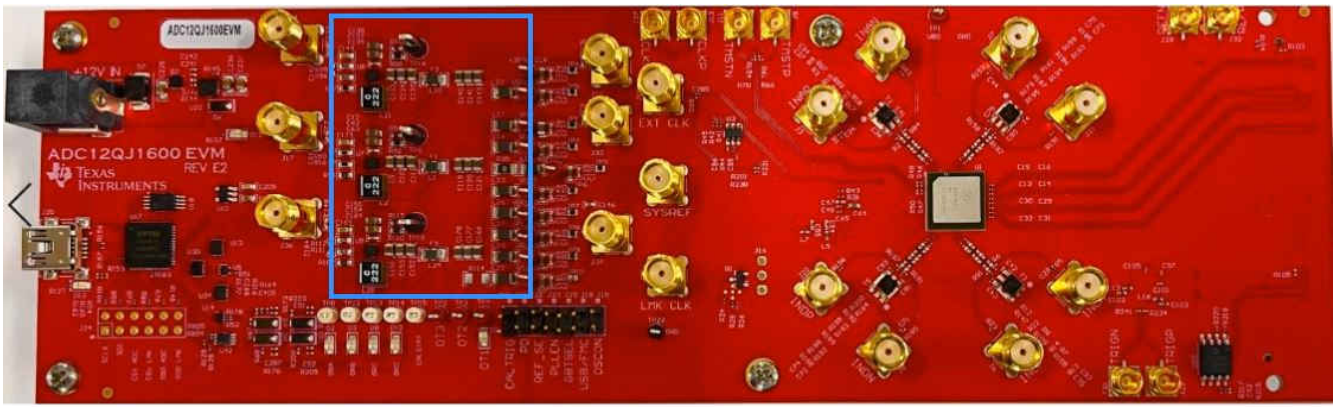


Figure 1-7. Image of Board With TPS62913 Switchers Outlined in Blue

The schematics for the 3.3-V, 1.1-V, and 1.9-V rails can be found in the Appendix A.

Table 1-1. ADC12QJ1600-Q1 Evaluation Module Component Comparison

Component	Original Rev C	Rev C with TPS62913
Switching Power Supplies	3 x LMS3635M (4mm x 5mm ea)	3 x TPS62913 (2mm x 2mm ea)
LDO's	3 x TPS7A8400 (3.5mm x 3.5mm ea)	None
Size of Power Supplies	96.75 sqmm + passives	12 sqmm + passives

1.3 Design Considerations

The ADC12QJ1600-Q1 is a high performance giga sample per second (GSPS) ADC and is sensitive to noise and spurious contents that result from high current in the switching elements, output capacitor ESL, and the magnetics involved when using a standard DC/DC converter. Utilizing the TPS62913 low-ripple, low-noise converter enables a significant reduction in noise and ripple without using a post-regulation LDO through the converters' unique low-ripple and low-noise design features.

The converter’s analog and clock inputs often get most of the scrutiny when it comes to addressing low noise on their inputs. Keep in mind that power supplies are inputs too. Because we think of them as DC biasing circuits we often don’t think of them as relating to RF performance. However, this is not true. When designing power supply domains for any high-speed converter, here are some useful tips in maximizing power supply noise immunity:

- Decouple all power supply rails and bus voltages as they come onto the system board and near/at the ADC itself.
- Remember that approximately 20 dB/decade noise suppression is gained for each additional filtering stage.
- Decouple for both high and low frequencies, which might require multiple capacitor values.
- Series ferrite beads are commonly used at the power entry point. just before the decoupling capacitor to ground. This should be done for each individual supply voltage coming in on the system board whether it comes from an LDO or switcher regulator.
- For added capacitance, use tightly stacked power and ground plane pairs (≤4 mil spacing) this adds inherent high-frequency (>500MHz) decoupling to the PCB design.
- Keep supplies away from sensitive analog circuitry such as the front-end stage of the ADC and clocking circuits if possible.
- Some components could be located on the opposite side of the PCB for added isolation.
- Follow the IC manufacture recommendations; if they are not directly stated in the application note or data sheet, then study the evaluation board. These are great vehicles to learn from.

Applying these points above can help provide a solid power supply design yielding datasheet performance in many applications.

2 Tests and Results

2.1 Test Methodology

Power Supply Rejection Ratio (PSRR)

The PSRR is typically measured as shown in Figure 2-1using HSDC-Pro software to display and measure the digital output FFT spectrum. Each supply is tested individually, using a bias T, which can be purchased off the shelf from various companies. The bias T is used to combine the AC and DC signal to the individual supply under test. It’s worth noting that the bias T must have a high enough current rating to supply enough bias to the supply under test. If not, the measurement could produce unreliable results.

After setting up the EVM or system board as you normally would, next, isolate the supply under test. Then apply the bias T to that supply, setting the appropriate DC voltage using an external lab bench power supply. Apply power to the rest of the board’s power supplies as you normally would, keeping those supplies at nominal. Next, select a low frequency, 10 MHz or less to start and inject the sinewave signal source to the bias T. This is called the error signal. It is also important to use a signal generator that is used for the applied error signal, is clean with low phase noise. This is so that the converter’s inherent performance is not otherwise degraded during testing. The signal generator should also be able to provide enough power to accommodate for the losses through the cabling, bias T and pcb.

Start the signal low in amplitude, slowly bringing the amplitude up until a spur comes out of the noise floor, the error spur should be high enough in the FFT spectrum where it is repeatable. The error spur should show at the error test frequency injected. Lets say the error spur amplitude captured is -85 dB.

Next use an oscilloscope or spectrum analyzer to note the level of the error signal injected. Make sure the error signal amplitude reading is taken at the ADC’s power pin and note the peak to peak voltage injected at that pin. Once this is found, PSRR can be found using some simple math.

For example, if the voltage measured was 10mVpp and the converter's fullscale voltage is 1.2 Vpp. Then simply take the ratio of those two numbers or 20*log(10m/1.2) = -41.6 dB. To find PSRR, subtract this number from the error spur amplitude found previously in the FFT spectrum or PSRR = -85 - -41.6 = -43.4 dB.

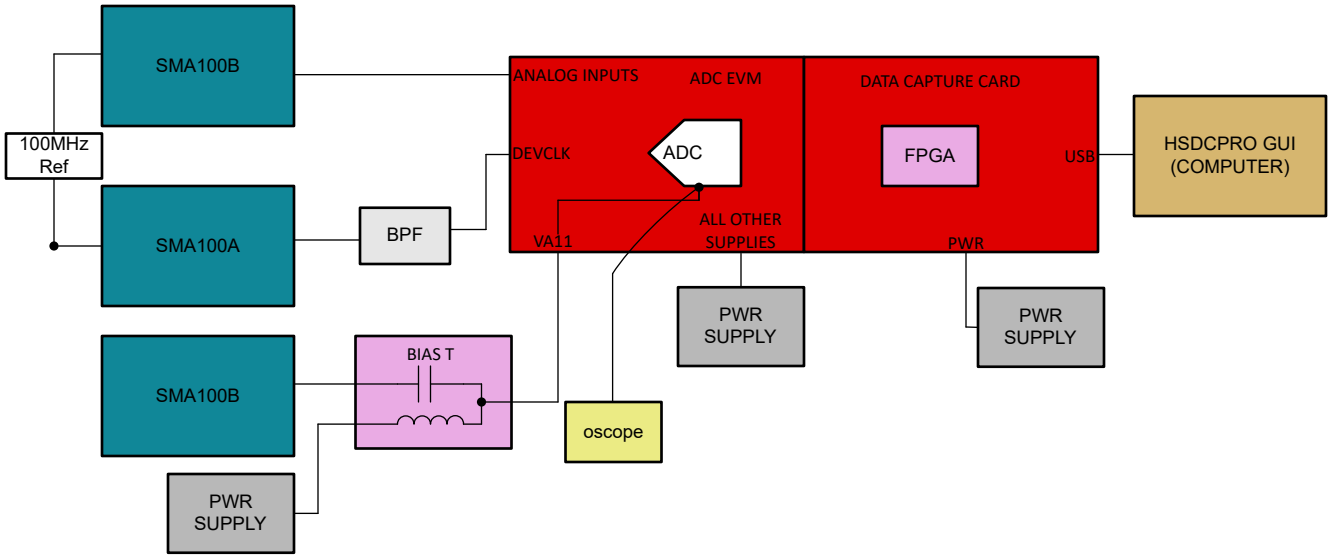


Figure 2-1. Test Configuration for PSRR and PSMR Measurement

An example of PSRR, with a forced error signal injected on the VA11 supply at 290 MHz with a -1 dBm amplitude level from the signal generator is shown in Figure 2-2.

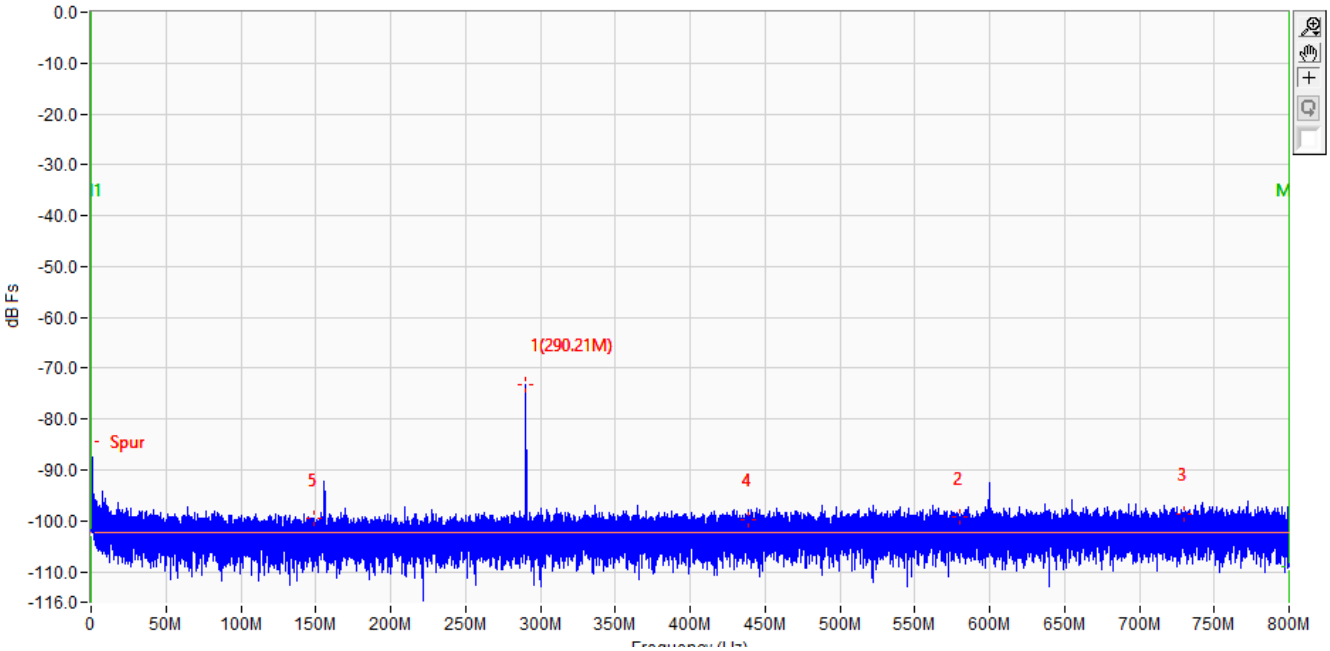


Figure 2-2. Example of Power Supply Rejection Ratio With Forced Error Signal

An example of PSMR, with a forced error signal injected at 10 MHz with a -1 dBm amplitude level from the signal generator is shown in Figure 2-3. This figure proves how leaky spurs through a power supply can modulate. With 10 MHz as the error frequency in this example, with the analog input signal frequency of 347 MHz, notice the intermodulation spurs(Fin+/- Error Frequency).

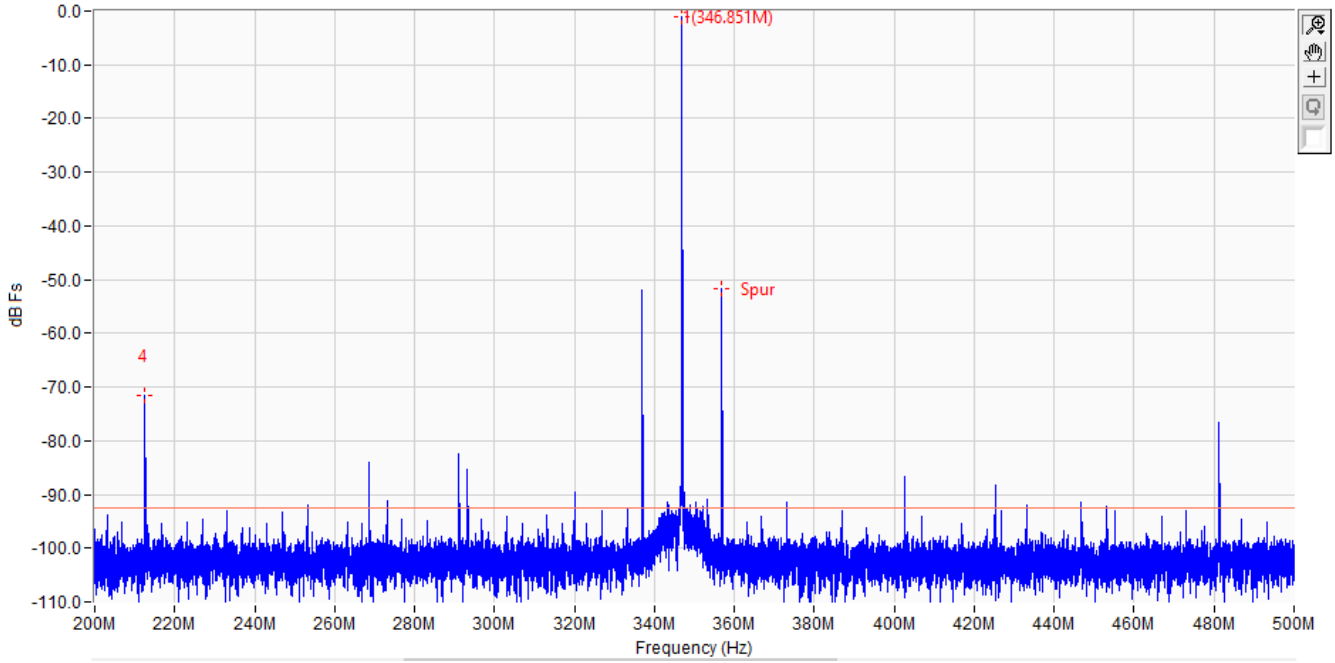


Figure 2-3. Example of Power Supply Modulation Ratio With Forced Error Signal

Signal-to-Noise Ratio (SNR, dBFS)

The SNR is the ratio of the rms signal amplitude to the rms value of the sum of all spectral components excluding DC, HD2 to HD9. The difference between SNR (dBc) and SNR (dBFS) is the difference between the fundamental amplitude and full scale.

Harmonic Distortion (dBc or dBFS)

A harmonic is a spectral component that is an integer multiple of the driven analog input frequency. For example, the frequency of the second harmonic is twice the analog input. Most ADCs have specifications for one or more harmonics. Typically, the second and third harmonics are singled out because they account for the worst performance of all the harmonics. Harmonic distortion, no matter the order, is the ratio of the rms signal amplitude to the rms value of the specified harmonic component, reported in dBc or dBFS. ADCs are nonlinear devices, therefore output FFT captured will be rich in spectral components.

Spurious-Free Dynamic Range (SFDR, dBc or dBFS)

The SFDR is the ratio of the rms value of the signal to the rms value of the peak spurious spectral component for the analog input frequency that produces the worst result. In most cases, SFDR is either the second or third harmonic (HD2 or HD3) of the input signal applied to the ADC.

Noise Spectral Density (NSD, dBFS/Hz)

The NSD is defined the entire noise power, per unit of bandwidth, sampled at an ADC's input. NSD is effectively the ADCs' SNR plus the power of the noise spread across the entire Nyquist band, which is equal to half the sample frequency, or Fs/2. Therefore, NSD = SNR + 10*log(Fs/2).

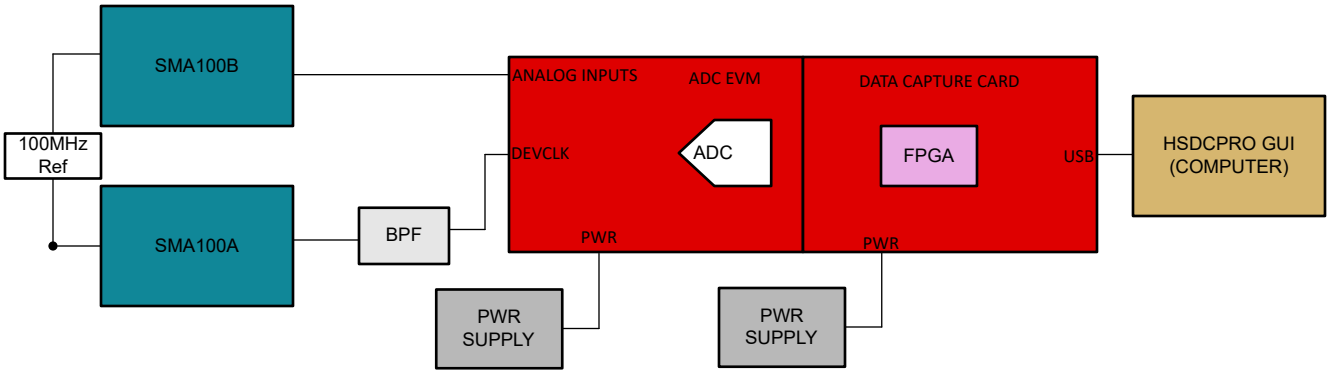


Figure 2-4. Test Configuration for SNR, SFDR, HD, and NSD Measurement

2.2 Test Conditions

The original design and the new design with the TPS62913 were tested in identical conditions for comparison.

AC or dynamic single tone FFT tests are are made with the analog signal applied to the A/D converter at a specific set of frequencies across the converter's analog input bandwidth. A signal of -1dB below full scale (or dBFS) is used for these frequency tested at the maximum rated sampling value or 1.6 GSPS. The input supply is 12V nominal, and the ambient temperature is 25 C nominal.

The ADC is operated at the sampling clock frequency of 1.6 GHz, which is derived from an external signal generator. The test results are shown using an external clock to LMK which then feeds into the ADC clock. The device register settings are set per the ADC12QJ1600-Q1 data sheet, using the GUI available on the product page, to JMODE0. The FFT is set to 65536 points with no averaging.

2.3 Test Results

Performance tables and graphs comparing the original ADC12QJ1600-Q1 Original EVM with TPS62913 spread spectrum on and off modified board are shown below.

Table 2-1. Signal to Noise (SNR) Comparison Table

Frequency (MHz)	Original QJ EVM (dBFS)	TPS62913 W/O SS (dBFS)	TPS62913 W/ SS (dBFS)
97	57.473	57.35	57.4
397	57.171	57.14	57.08
597	56.814	56.66	56.7
797	56.501	56.36	56.4
997	55.967	55.98	55.977
1497	54.765	55.02	55.01

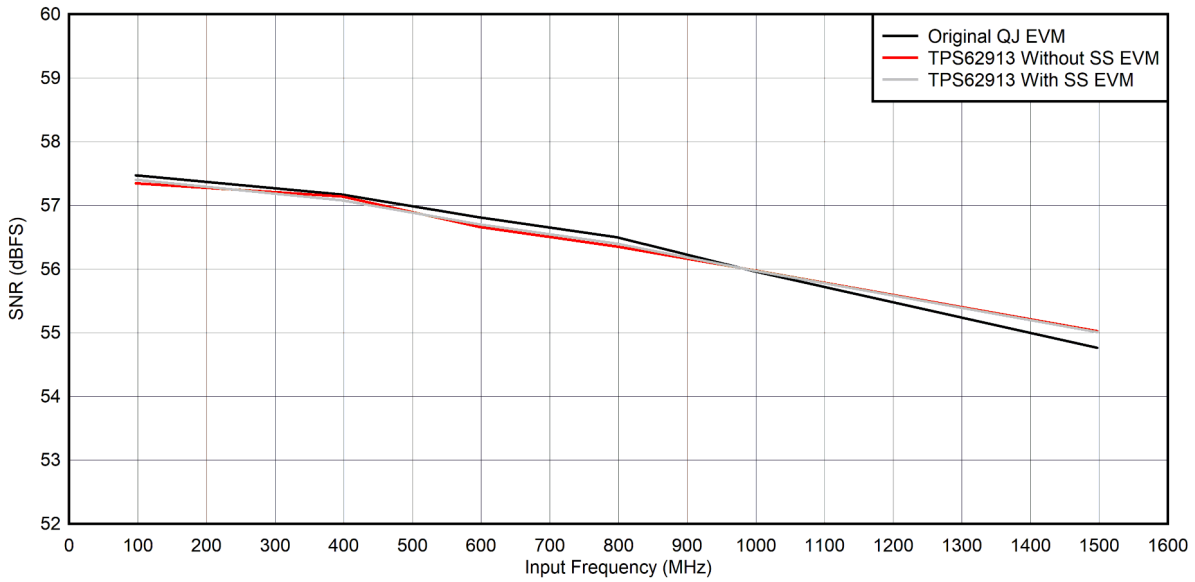


Figure 2-5. Signal to Noise (SNR) Comparison Graph

Table 2-2. Spurious-Free Dynamic Range (SFDR) Comparison Table

Frequency (Hz)	Original QJ EVM (dBFS)	TPS62913 W/O SS (dBFS)	TPS62913 W/ SS (dBFS)
97	67.92	67.41	67.28
397	70.799	70.91	69.95
597	64.663	65.57	65.6
797	65.847	65.42	65.51
997	64.302	64.14	64.2
1497	63.485	63.46	63.4

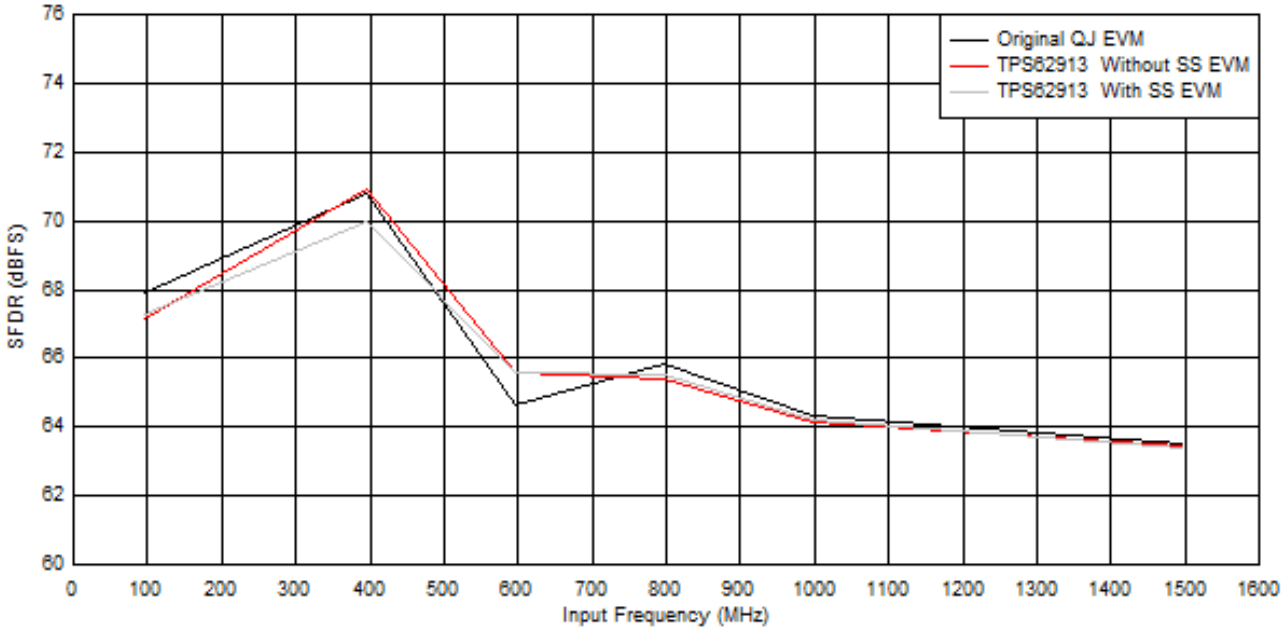


Figure 2-6. Spurious-Free Dynamic Range Comparison Graph

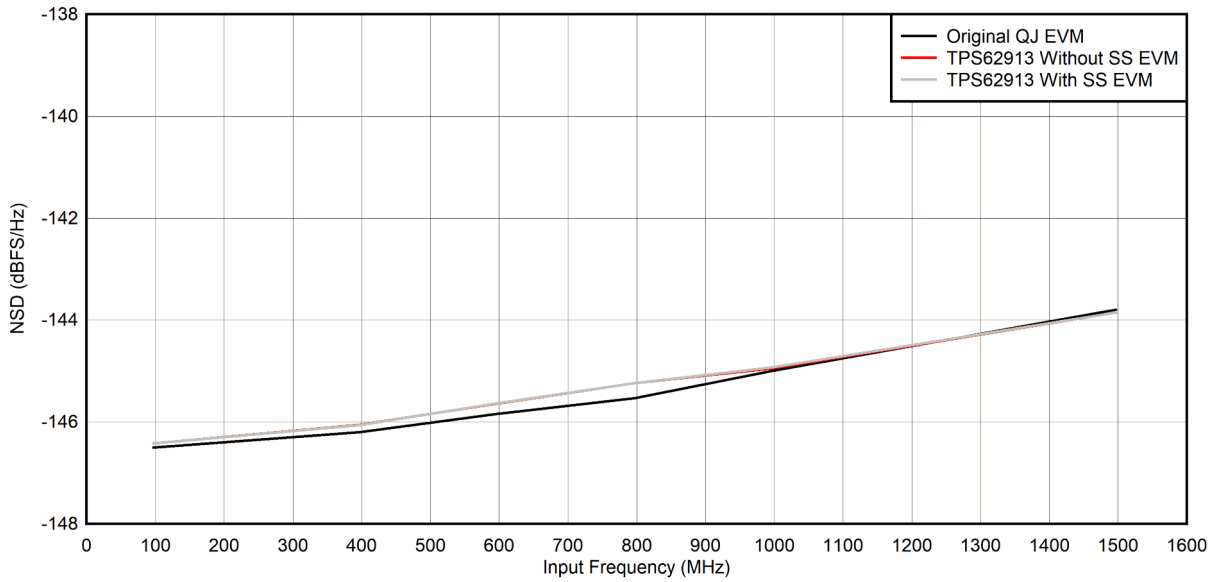


Figure 2-7. Noise Spectral Density Comparison Graph

The next plot, Figure 2-8, shows how no PSMR is observed with an analog input signal frequency of 347 MHz applied when using the original power design with SMPS and LDO, and the TPS62913 switching supply with and without spread sprectrum enabled.

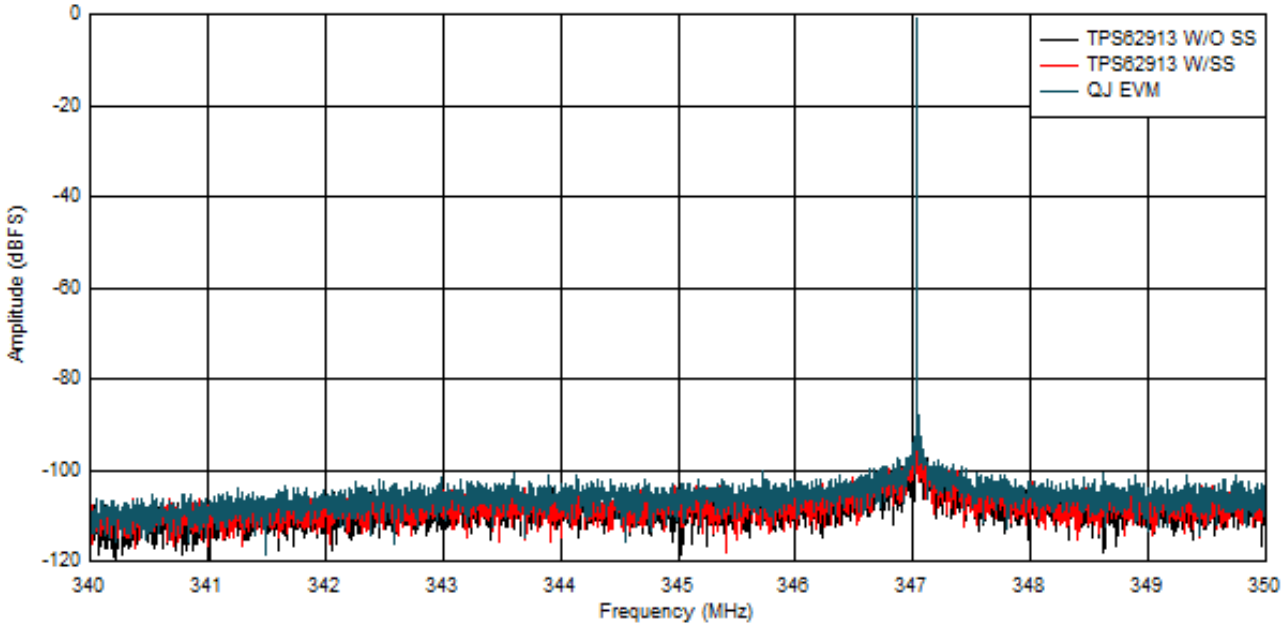


Figure 2-8. PSMR Comparison of Original and TPS62913

Additionally, no visible modulation of the switcher power supply spur is seen around the carrier and at DC as seen in Figure 2-9.

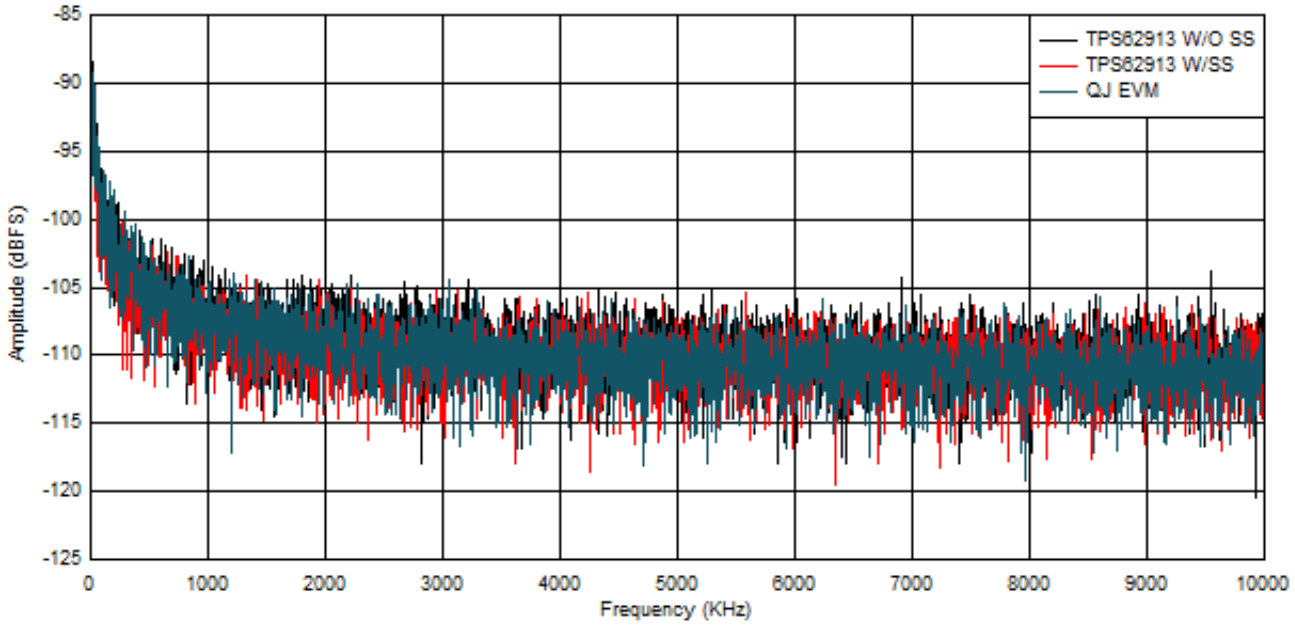
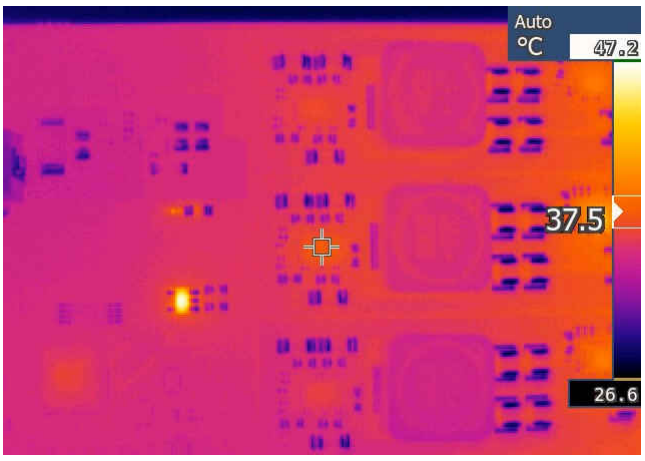


Figure 2-9. PSMR Comparison of Original and TPS62913 at DC

Table 2-3. Power Loss Comparison

Configuration	Input Current	Input Power
Original Power Supply Configuration with SMPSs + LDOs	486 mA	5.832 W
TPS62913 Power Supplies only-UPDATE	327 mA	3.924 W
Input Current and Power Savings-UPDATE	159 mA	1.908W

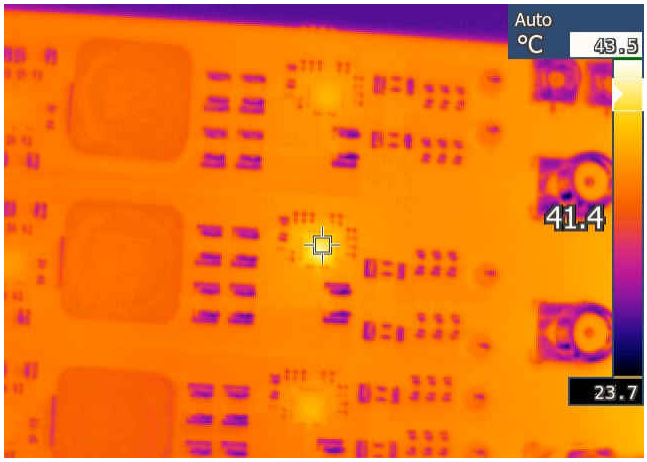
Figure 2-10 through Figure 2-12 are thermal images of the power supplies running when taking data for the performance comparison tables.



Note

Original Board DC/DC Max Temp is 37.5 C

Figure 2-10. Original Switching Converters



Note

Original Board LDO Max Temp is 41.4 C

Figure 2-11. Original LDOs

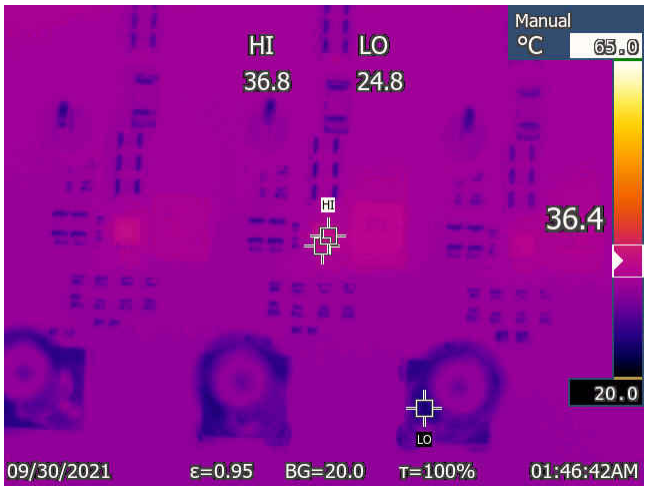


Figure 2-12. TPS62913 Switching Converters

Note

TPS62913 Max Temp is 36.8 C

3 Conclusion

As shown by the test results, a simplified power supply design using the TPS62913 low-ripple and low-noise buck converts can provide similar performance to the traditional SMPS + LDO approach. The Analog, Digital, and Clock rails are all supplied using the switching regulator without the need for a low-dropout linear regulator (LDO) while maintaining the same performance as the original design. The SNR, SFDR, and NSD performance with spread spectrum and without spread spectrum is similar to the SMPS + LDO approach. Use of the TPS62913 design reduces the power consumption by 1.908W (32% power savings), reduces the size of the design, and reduces the temperature rise of the power supply components.

Although this design used the ADC12QJ1600-Q1, other ADCs that require low noise power supplies that are size constrained and thermal constrained can also use this approach.

4 References

- Texas Instruments, ADC12QJ1600-Q1, Automotive. 4-ch, 12-bit. 1.6-GSPS ADC with JESD204C interface and integrated sample clock generator
- Texas Instruments, TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter with Integrated Ferrite Bead Filter Compensation

A Appendix

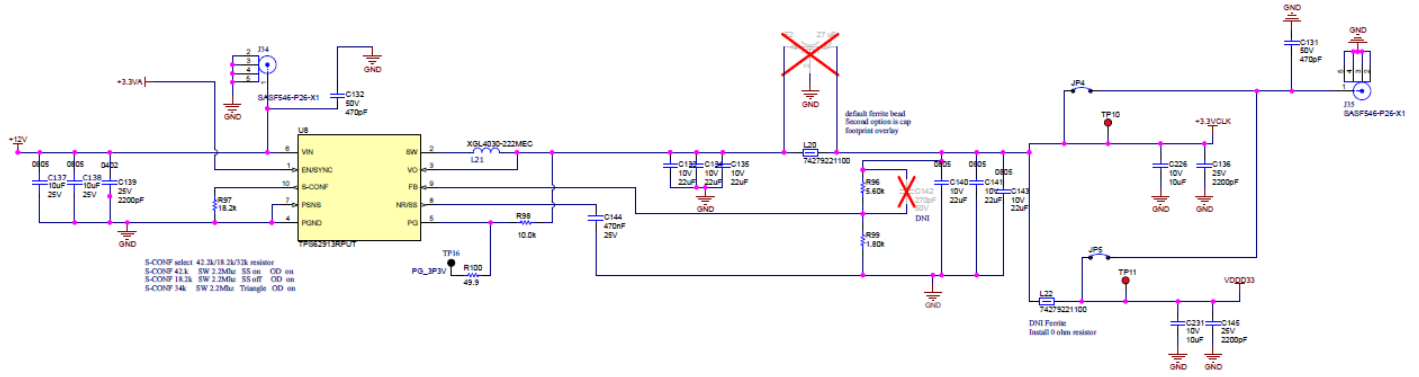


Figure A-1. TPS62913 3.3V Clock Power Schematic

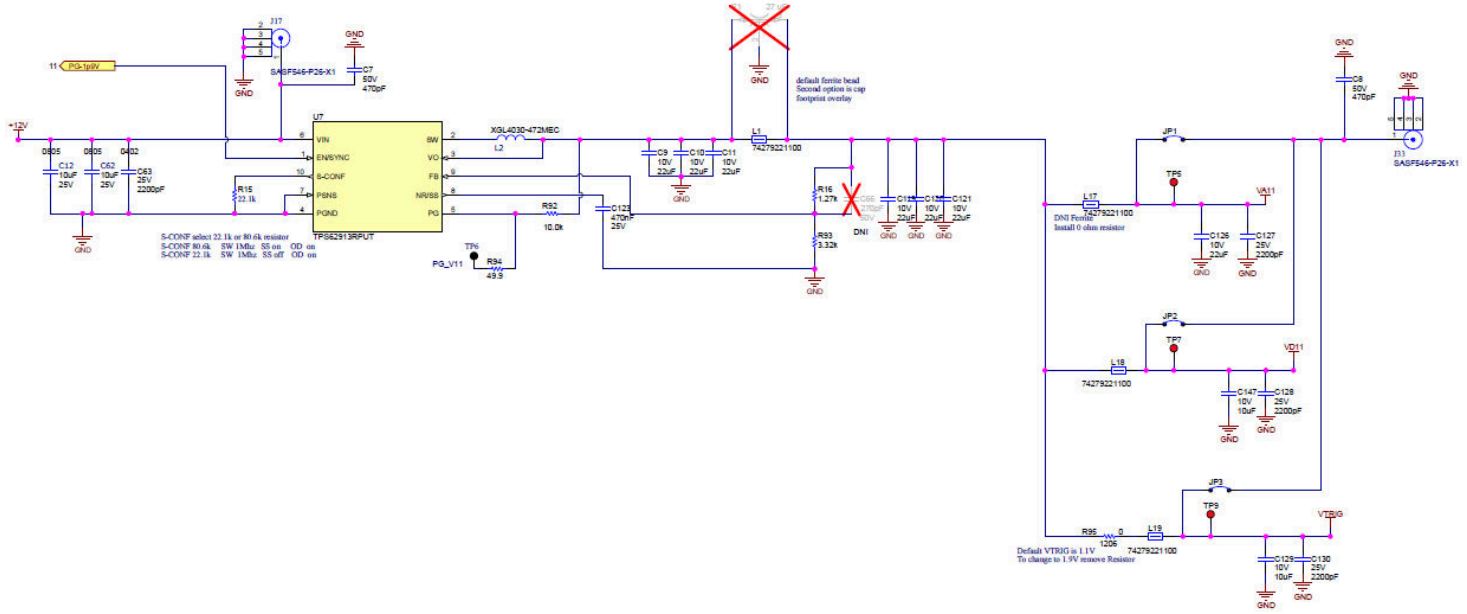


Figure A-2. TPS6913 1.1V ADC Power Schematic

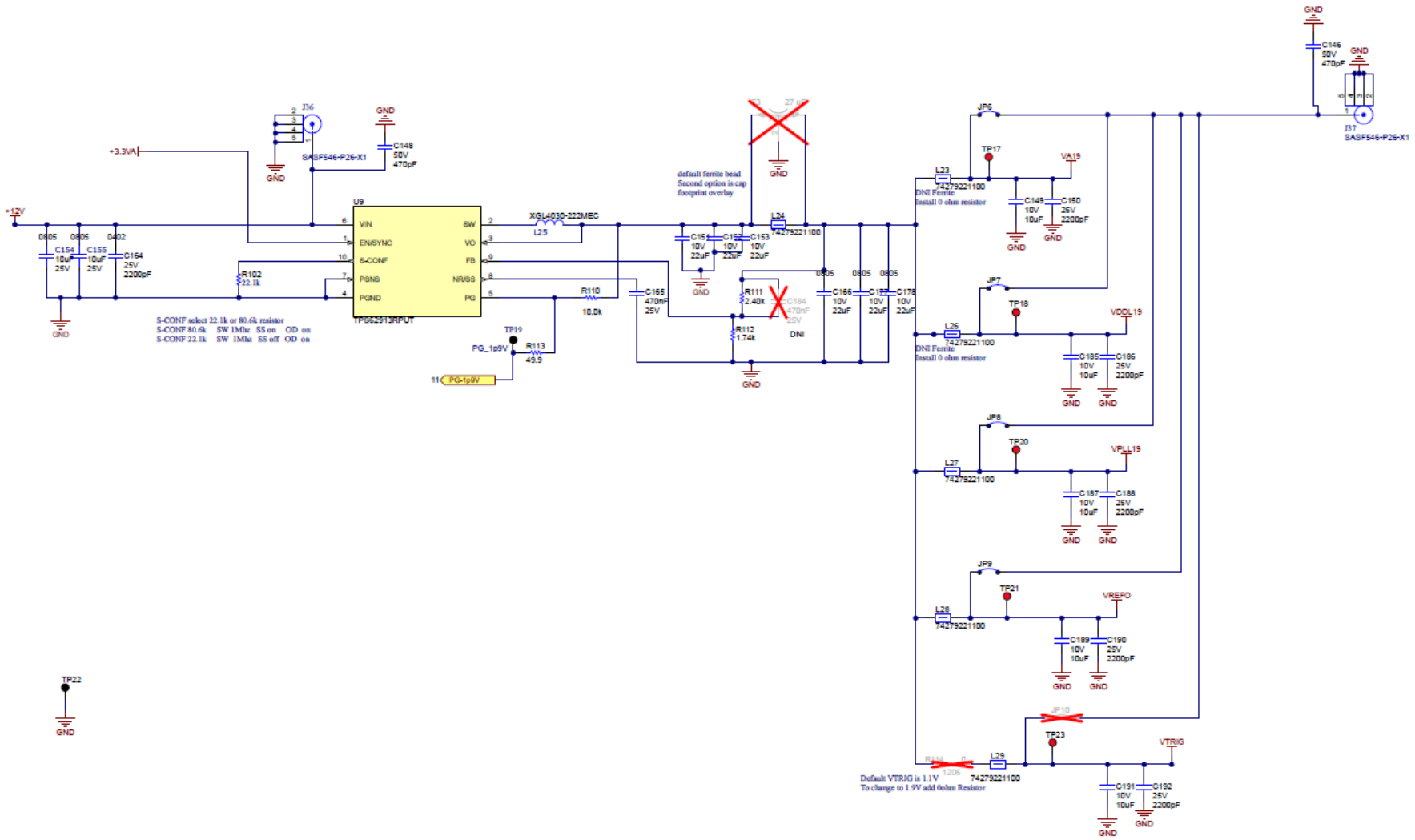


Figure A-3. TPS62913 1.9V ADC Power Schematic

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