

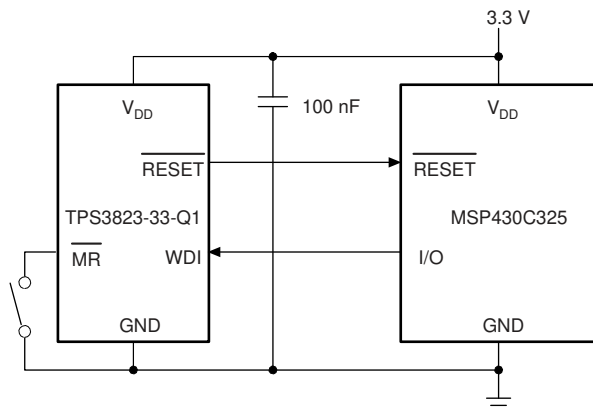
## TPS382x-xx-Q1 Voltage Monitor With Watchdog Timer

### 1 Features

- Qualified for automotive applications
- AEC-Q100 Qualified With the Following Results:
  - Device temperature grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- ESD protection exceeds 2000V Per MIL-STD-883, Method 3015; using human body model ( $C = 100\text{pF}$ ,  $R = 1500\Omega$ )
- Power-on reset generator with fixed delay time of 200ms (TPS3823/4/5/8-xx-Q1) or 25ms (TPS3820-xx-Q1)
- Manual reset input (TPS3820/3/5/8-xx-Q1)
- Reset output available in active-low (TPS3820/3/4/5-xx-Q1), Active-High (TPS3824/5-xx-Q1), and open drain (TPS3828-xx-Q1)
- Supply voltage supervision range: 2.5V, 3V, 3.3V, 5V
- Watchdog timer (TPS3820/3/4/8-xx-Q1)
- Supply current of  $15\mu\text{A}$  (typical)
- 5-Pin SOT-23 package
- Temperature range:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$

### 2 Applications

- Automotive DSPs, microcontrollers, or microprocessors
- Industrial equipment
- Programmable controls
- Automotive systems
- Portable and battery-powered equipment
- Intelligent instruments
- Wireless communications systems



Typical Application Schematic

### 3 Description

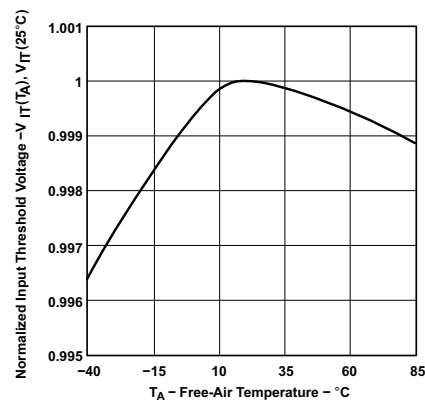
For all new designs with TPS3820-xx-Q1, use the TPS3820-xxQPDBVRQ1 part number. The TPS3820-xxQP is functionally equivalent and a replacement to the TPS3820xxQ. The TPS3820-xxQDBVRQ1 is not recommended for new designs (NRND).

The TPS382x-xx-Q1 family of supervisors provide circuit initialization and timing supervision, primarily for DSP and processor-based systems. During power on,  $\overline{\text{RESET}}$  asserts when the supply voltage  $V_{\text{DD}}$  becomes greater than 1.1V. Thereafter, the supply voltage supervisor monitors  $V_{\text{DD}}$  and keeps  $\overline{\text{RESET}}$  active low as long as  $V_{\text{DD}}$  remains below the threshold voltage,  $V_{\text{IT-}}$ . An internal timer delays the return of the output to the inactive state (high) to verify a proper system reset. The delay time,  $t_d$ , starts after  $V_{\text{DD}}$  has risen above the threshold voltage  $V_{\text{IT-}}$ . When the supply voltage drops below the threshold voltage  $V_{\text{IT-}}$ , the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage,  $V_{\text{IT-}}$ , set by an internal voltage divider. The TPS382x-xx-Q1 family also offers watchdog time out options of 200ms (TPS3820-xx-Q1) and 1.6s (TPS3823/4/8-xx-Q1).

#### Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TPS382x-xx-Q1	SOT-23 (5)	2.90mm × 1.60mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Normalized Input Threshold Voltage vs Free-Air Temperature



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## 4 Device Comparison Table

DEVICE	RESET	RESET	WDI	MR	FIXED DELAY TIME
TPS3820-xx-Q1		Push-pull	X	X	25ms
TPS3823-xx-Q1		Push-pull	X	X	200ms
TPS3824-xx-Q1	Push-pull		X		200ms
TPS3825-xx-Q1	Push-pull	Push-pull		X	200ms
TPS3828-xx-Q1		Open-drain	X	X	200ms

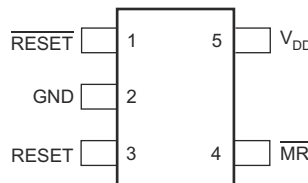
## 5 Pin Configuration and Functions



**Figure 5-1. TPS3820-xx-Q1, TPS3823-xx-Q1, TPS3828-xx-Q1: DBV PACKAGE 5-Pin SOT-23 Top View**



**Figure 5-2. TPS3824-xx-Q1: DBV PACKAGE 5-Pin SOT-23 Top View**



**Figure 5-3. TPS3825-xx-Q1: DBV PACKAGE 5-Pin SOT-23 Top View**

## Pin Functions

NAME	PIN			I/O	DESCRIPTION
	TPS3820-xx-Q1, TPS3823-xx-Q1, TPS3828-xx-Q1	TPS3824-xx-Q1	TPS3825-xx-Q1		
GND	2	2	2	—	Ground connection
MR	3	—	4	I	Manual-reset input. Pull low to force a reset. RESET remains low as long as MR is low and for the time-out period after MR goes high. Leave unconnected or connect to V <sub>DD</sub> when unused.
RESET	—	3	3	O	Active-high reset output. Either push-pull or open-drain output stage.
RESET	1	1	1	O	Active-low reset output. Either push-pull or open-drain output stage.
V <sub>DD</sub>	5	5	5	I	Supply voltage. Powers the device and monitors the voltage.
WDI	4	4	—	I	Watchdog timer input. If WDI remains high or low longer than the time-out period, then reset is triggered. The timer clears when reset is asserted or when WDI sees a falling edge. If left floating, the device generates pulses internally to prevent watchdog reset event. WDI must be driven low or high for watchdog error to assert output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	VDD	-0.3	6	V
	RESET, $\overline{\text{RESET}}$ , $\overline{\text{MR}}$ , WDI	-0.3	$V_{\text{DD}} + 0.3$	V
Current	Maximum low output, $I_{\text{OL}}$	-5	5	mA
	Maximum high output, $I_{\text{OH}}$	-5	5	mA
	Output range ( $V_{\text{O}} < 0$ or $V_{\text{O}} > V_{\text{DD}}$ ), $I_{\text{OK}}$	-10	10	mA
Temperature	Operating free-air temperature, $T_{\text{A}}$	-40	125	°C
	Storage temperature range, $T_{\text{stg}}$	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{\text{(ESD)}}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±750	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process  
 (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{\text{DD}}$	Supply voltage	1.1		5.5	V
$V_{\text{I}}$	Input voltage	0		$V_{\text{DD}} + 0.3$	V
$V_{\text{IH}}$	High level input voltage at $\overline{\text{MR}}$ and WDI	$0.7 \times V_{\text{DD}}$			V
$V_{\text{IL}}$	Low level input voltage			$0.3 \times V_{\text{DD}}$	V
$\Delta t/\Delta V$	Input transition rise and fall rate at $\overline{\text{MR}}$ or WDI			100	ns/V
$T_{\text{A}}$	Operating free-air temperature range	-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS382x-xx-Q1
		DBV (SOT-23)
		5 PINS
$R_{\theta\text{JA}}$	Junction-to-ambient thermal resistance	185
$R_{\theta\text{JC(top)}}$	Junction-to-case (top) thermal resistance	83.3
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance	52.4
$\Psi_{\text{JT}}$	Junction-to-top characterization parameter	20.4
$\Psi_{\text{JB}}$	Junction-to-board characterization parameter	52.0
$R_{\theta\text{JC(bot)}}$	Junction-to-case (bottom) thermal resistance	n/a

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT			
V <sub>OH</sub>	High-level output voltage	RESET	TPS382x-25-Q1	V <sub>DD</sub> = V <sub>IT-</sub> + 0.2V, I <sub>OH</sub> = –20µA	0.8 × V <sub>DD</sub>	V <sub>DD</sub> – 1.5V	V			
			TPS382x-30-Q1							
			TPS382x-33-Q1							
			TPS382x-50-Q1							
		RESET	TPS3824-25-Q1 TPS3825-25-Q1	V <sub>DD</sub> ≥ 1.8V, I <sub>OH</sub> = –100µA	0.8 × V <sub>DD</sub>	V <sub>DD</sub> – 1.5V		V		
			TPS3824-30-Q1 TPS3825-30-Q1							
			TPS3824-33-Q1 TPS3825-33-Q1							
			TPS3824-50-Q1 TPS3825-50-Q1							
V <sub>OL</sub>	Low-level output voltage	RESET	TPS3824-25-Q1 TPS3825-25-Q1	V <sub>DD</sub> = V <sub>IT-</sub> + 0.2V, I <sub>OL</sub> = 1mA	0.4	V				
			TPS3824-30-Q1 TPS3825-30-Q1							
			TPS3824-33-Q1 TPS3825-33-Q1							
			TPS3824-50-Q1 TPS3825-50-Q1							
		RESET	TPS382x-25-Q1	V <sub>DD</sub> = V <sub>IT-</sub> – 0.2V, I <sub>OL</sub> = 1mA	0.45	V				
			TPS382x-30-Q1							
			TPS382x-33-Q1							
			TPS382x-50-Q1							
V <sub>POR</sub>	Power-up reset voltage <sup>(1)</sup>		V <sub>OL(max)</sub> = 0.4V, I <sub>OL(Sink)</sub> = 20µA			0.9	V			
V <sub>IT-</sub>	Negative-going input threshold voltage <sup>(2)</sup>	TPS382x-25-Q1	TPS382x-30-Q1	TPS382x-33-Q1	TPS382x-50-Q1	T <sub>A</sub> = 0°C to 85°C	V			
								2.21	2.25	2.3
								2.59	2.63	2.69
								2.88	2.93	3
		4.49	4.55	4.64						
		TPS382x-25-Q1	TPS382x-30-Q1	TPS382x-33-Q1	TPS382x-50-Q1	T <sub>A</sub> = –40°C to 125°C	V			
								2.19	2.25	2.3
								2.55	2.63	2.69
2.84	2.93							3		
4.44	4.55	4.64								
V <sub>HYS</sub>	Hysteresis at V <sub>DD</sub> input	TPS382x-25-Q1	TPS382x-30-Q1	TPS382x-33-Q1	TPS382x-50-Q1					
				30						
				50						
I <sub>IH(AV)</sub>	Average high-level input current	WDI	WDI = V <sub>DD</sub> , time average (DC = 88%)		120		µA			
I <sub>IL(AV)</sub>	Average low-level input current		WDI = 0.3V, V <sub>DD</sub> = 5.5V, time average (DC = 12%)		–15		µA			
I <sub>IH</sub>	High-level input current	WDI	WDI = V <sub>DD</sub>		140	190	µA			
		MR	MR = 0.7 × V <sub>DD</sub> , V <sub>DD</sub> = 5.5V		–40	–60	µA			
I <sub>IL</sub>	Low-level input current	WDI	WDI = 0.3V, V <sub>DD</sub> = 5.5V		140	190	µA			
		MR	MR = 0.3V, V <sub>DD</sub> = 5.5V		–110	–160	µA			
I <sub>OS</sub>	Output short-circuit current <sup>(3)</sup>	RESET	TPS382x-25-Q1	V <sub>DD</sub> = V <sub>IT-,max</sub> + 0.2V, V <sub>O</sub> = 0V		–400	µA			
			TPS382x-30-Q1							
			TPS382x-33-Q1							
			TPS382x-50-Q1							
						–800				

## 6.5 Electrical Characteristics (continued)

over operating temperature range (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$I_{DD}$	Supply current	WDI, $\overline{MR}$ and outputs unconnected		15	25	$\mu\text{A}$
$R_{MR}$	Internal pullup resistor at $\overline{MR}$			90		$\text{k}\Omega$
$C_i$	Input capacitance at $\overline{MR}$ , WDI	$V_i = 0\text{V to } 5.5\text{V}$		5		$\text{pF}$

- (1) The lowest supply voltage at which  $\overline{\text{RESET}}$  becomes active.  $t_r, V_{DD} \geq 15\mu\text{s/V}$ .
- (2) To make sure best stability of the threshold voltage, place a bypass capacitor (ceramic,  $0.1\mu\text{F}$ ) near the supply terminal.
- (3) The  $\overline{\text{RESET}}$  short-circuit current is the maximum pullup current when  $\overline{\text{RESET}}$  is driven low by a microprocessor bidirectional reset pin.

### 6.6 Timing Requirements

at  $R_L = 1M\Omega$ ,  $C_L = 50pF$  and  $T_J = 25^\circ C$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT	
$t_W$	Pulse width	At $V_{DD}$	$V_{DD} = V_{IT-} + 0.2V$ , $V_{DD} = V_{IT-} - 0.2V$			6	$\mu s$
		At $\overline{MR}$	$V_{DD} \geq V_{IT-} + 0.2V$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$			1	$\mu s$
		At $WDI$				100	ns

### 6.7 Switching Characteristics

at  $R_L = 1M\Omega$ ,  $C_L = 50pF$  and  $T_J = 25^\circ C$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT			
$t_{out}$	Watchdog time out	TPS3820-xx-Q1	$V_{DD} \geq V_{IT-} + 0.2V$ , See timing diagram			112	200	300	ms
		TPS3823/4/8-xx-Q1				0.9	1.6	2.5	s
$t_d$	Delay time	TPS3820-xx-Q1	$V_{DD} \geq V_{IT-} + 0.2V$ , See timing diagram			15	25	37	ms
		TPS3823/4/5/8-xx-Q1				120	200	300	
$t_{PHL}$	Propagation delay time, high-to-low output	$\overline{MR}$ to RESET delay (TPS3820/3/5/8-xx-Q1)	$V_{DD} \geq V_{IT-} + 0.2V$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$					0.1	$\mu s$
		$V_{DD}$ to RESET delay				$V_{IL} = V_{IT-} - 0.2V$ , $V_{IH} = V_{IT-} + 0.2V$			
$t_{PLH}$	Propagation delay time, low-to-high output	$\overline{MR}$ to RESET delay (TPS3824/5-xx-Q1)	$V_{DD} \geq V_{IT-} + 0.2V$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$					0.1	$\mu s$
		$V_{DD}$ to RESET delay (TPS3824/5-xx-Q1)				$V_{IL} = V_{IT-} - 0.2V$ , $V_{IH} = V_{IT-} + 0.2V$			

### 6.8 Timing Diagram

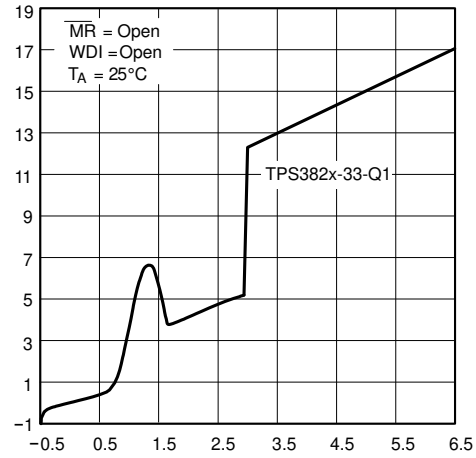


Figure 6-1. Delay and Time Out Timing Diagram

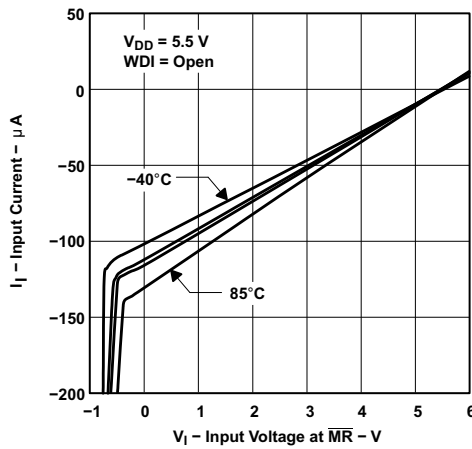
## 6.9 Typical Characteristics



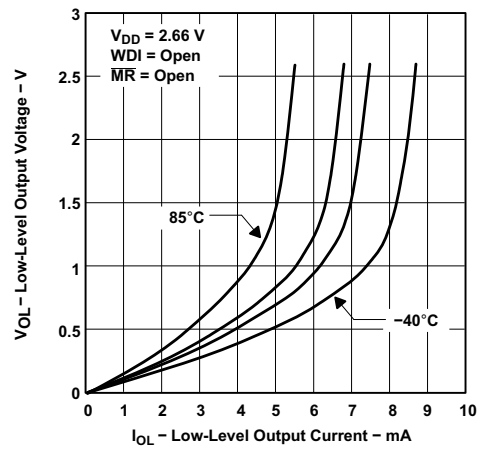
**Figure 6-2. Normalized Input Threshold Voltage vs Free-Air Temperature at  $V_{DD}$**



**Figure 6-3. Supply Current vs Supply Voltage**



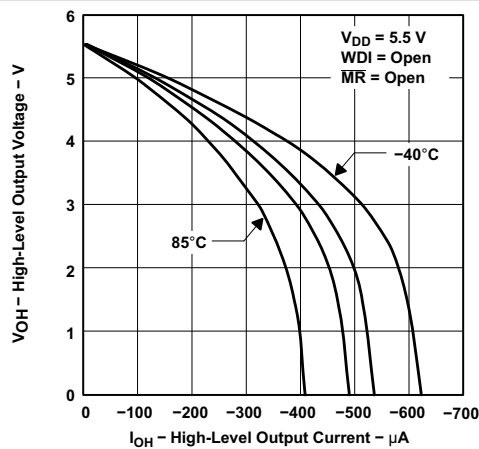
**Figure 6-4. Input Current vs Input Voltage at  $\overline{MR}$**



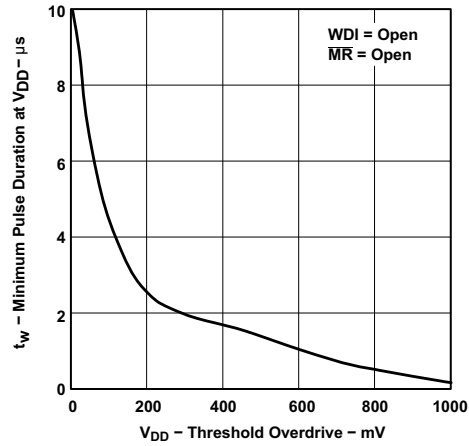
**Figure 6-5. Low-Level Output Voltage vs Low-Level Output Current**



**Figure 6-6. High-Level Output Voltage vs High-Level Output Current**



**Figure 6-7. High-Level Output Voltage vs High-Level Output Current**



**Figure 6-8. Minimum Pulse Duration at V<sub>DD</sub> vs V<sub>DD</sub> Threshold Overdrive**

## 7 Detailed Description

### 7.1 Overview

The TPS382x-xx-Q1 family of supervisors provide circuit initialization and timing supervision. Optional configurations include devices with active-high and active-low output signals (TPS3824/5-xx-Q1), devices with a watchdog timer (TPS3820/3/4/8-xx-Q1), and devices with manual reset ( $\overline{MR}$ ) pins (TPS3820/3/5/8-xx-Q1).  $\overline{RESET}$  asserts when the supply voltage,  $V_{DD}$ , rises above 1.1V. For devices with active-low output logic, the device monitors  $V_{DD}$  and keeps  $\overline{RESET}$  low as long as  $V_{DD}$  remains below the negative threshold voltage,  $V_{IT-}$ . For devices with active-high output logic,  $RESET$  remains high as long as  $V_{DD}$  remains below  $V_{IT-}$ . An internal timer delays the return of the output to the inactive state (high) to make sure proper system reset. The delay time,  $t_d$ , starts after  $V_{DD}$  rises above the positive threshold voltage ( $V_{IT-} + V_{HYS}$ ). When the supply voltage drops below  $V_{IT-}$ , the output becomes active (low) again. All the devices of this family have a fixed-sense threshold voltage,  $V_{IT-}$ , set by an internal voltage divider, so no external components are required.

The TPS382x-xx-Q1 family is designed to monitor supply voltages of 2.5V, 3V, 3.3V, and 5V. The devices are available in a 5-pin SOT-23 package and are characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , and are qualified in accordance with AEC-Q100 stress test qualification for integrated circuits.

### 7.2 Functional Block Diagram



- A. TPS3824/5-xx-Q1
- B. TPS3820/3/5/8-xx-Q1
- C. TPS3820/3/4/8-xx-Q1

### 7.3 Feature Description

#### 7.3.1 Manual Reset ( $\overline{MR}$ )

The  $\overline{MR}$  input allows an external logic signal from processors, logic circuits, and/or discrete sensors to force a reset signal regardless of  $V_{DD}$  with respect to  $V_{IT-}$  or the state of the watchdog timer. A low level at  $\overline{MR}$  causes the reset signals to become active.

#### 7.3.2 Active High or Active Low Output

All TPS382x-xx-Q1 devices have an active-low logic output ( $\overline{RESET}$ ), while the TPS3824/5-xx-Q1 devices also include an active-high logic output ( $RESET$ ).

#### 7.3.3 Push-Pull or Open-Drain Output

All TPS382x-xx-Q1 devices, except for TPS3828-xx-Q1, have push-pull outputs. TPS3828-xx-Q1 devices have an open-drain output.

### 7.3.4 Watchdog Timer (WDI)

TPS3820/3/4/8-xx-Q1 devices have a watchdog timer that must be periodically triggered by negative transition at WDI to avoid a reset signal being issued. When the supervising system fails to retrigger the watchdog circuit within the time-out interval,  $t_{\text{out}}$ ,  $\overline{\text{RESET}}$  becomes active for the time period  $t_d$ . This event also reinitializes the watchdog timer.

The watchdog timer can be disabled by disconnecting the WDI pin from the system. If the WDI pin detects a high-impedance state the TPS3820/3/4/8-xx-Q1 generates a WDI pulse to make sure that  $\overline{\text{RESET}}$  does not assert. If this behavior is not desired place a 1k $\Omega$  resistor from WDI to ground. This resistor makes sure that the TPS3820/3/4/8-xx-Q1 detects that WDI is not in a high-impedance state.

In applications where the input to the WDI pin is active (transitioning high and low) when the TPS3820/3/4/8-xx-Q1 is asserting  $\overline{\text{RESET}}$ ,  $\overline{\text{RESET}}$  is stuck at a logic low after the input voltage returns above  $V_{IT-}$ . If the application requires that input to WDI be active when the reset signal is asserted, then use a FET to decouple the WDI signal. An external FET decouples the WDI signal by disconnecting the WDI input when  $\overline{\text{RESET}}$  is asserted. For more details on this, see [Section 8.2.2](#) for more details.

### 7.4 Device Functional Modes

The device functions according to the inputs and outputs in [Table 7-1](#).

**Table 7-1. Function Table**

INPUTS		OUTPUTS	
$\overline{\text{MR}}$ <sup>(1)</sup>	$V_{DD} > V_{IT}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ <sup>(2)</sup>
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

(1) TPS3820/3/5/8-xx-Q1

(2) TPS3824/5-xx-Q1

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

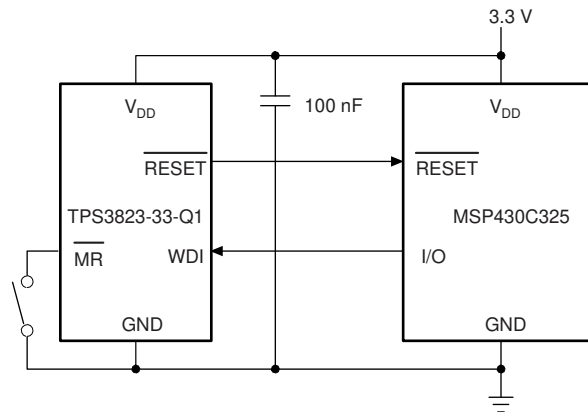
The TPS382x-xx-Q1 family of devices are very small supervisory circuits that monitor fixed supply voltages of 2.5V, 3V, 3.3V, and 5V. The TPS382x-xx-Q1 family operates from 1.1V to 5.5V. Orderable options include versions with either push-pull or open-drain outputs, versions that use active-high or active-low logic for output signals, versions with a manual reset pin, and versions with a watchdog timer. See the [Section 4](#) for an overview of device options.

### 8.2 Typical Applications

#### 8.2.1 Supply Rail Monitoring with Watchdog Time-out and 200ms Delay

The TPS3823-xx-Q1 can be used to monitor the supply rail for devices such as microcontrollers. The downstream device is enabled by the TPS3823-xx-Q1 once the voltage on the supply pin ( $V_{DD}$ ) is above the internal threshold voltage ( $V_{IT-} + V_{HYS}$ ). The downstream device is disabled by the TPS3823-xx-Q1 when  $V_{DD}$  falls below the threshold voltage minus the hysteresis voltage ( $V_{IT-}$ ). The TPS3823-xx-Q1 also issues a reset signal if the WDI input is not periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval,  $t_{out}$ ,  $\overline{RESET}$  becomes active for the time period  $t_d$ .

Some applications require a shorter reset signal than the 200ms that most of the TPS382x-xx-Q1 family provide. In these cases, the TPS3820-xx-Q1 is a good choice because the device has a delay time of only 25ms. If an open-drain output is needed, replace the TPS3823-xx-Q1 with the TPS3828-xx-Q1 (if the WDI input must be active while  $\overline{RESET}$  is low, see [Section 8.2.2](#)). [Figure 8-1](#) shows the TPS3823-33-Q1 in a typical application.



**Figure 8-1. Supply Rail Monitoring With Watchdog Time-out**

#### 8.2.1.1 Design Requirements

The TPS3823-33-Q1 must drive the enable pin of a MSP430C325 using a logic-high signal to signify that the supply voltage is above the minimum operating voltage of the device and monitor the I/O pin to determine if the microcontroller is operating correctly.

### 8.2.1.2 Detailed Design Procedure

Determine which version of the TPS382x-xx-Q1 family best works for the functional performance required. If the input supply is noisy, include an input capacitor to help avoid unwanted changes to the reset signal.

### 8.2.1.3 Application Curve

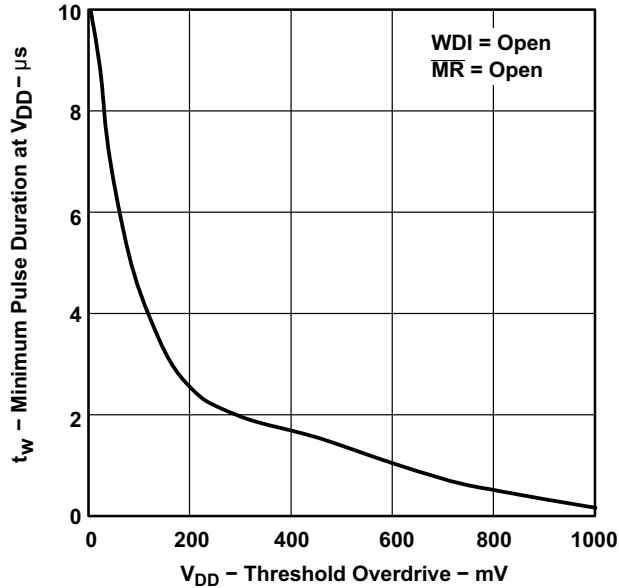


Figure 8-2. Minimum Pulse Duration at V<sub>DD</sub> vs V<sub>DD</sub> Threshold Overdrive

### 8.2.2 Decoupling WDI During Reset Event

If the application requires that the input to WDI is active when the reset signal is asserted, Figure 8-3 shows how to decouple WDI from the active signal using an N-channel FET. The N-channel FET is placed in series with the WDI pin, with the gate of the FET connected to the  $\overline{\text{RESET}}$  output.

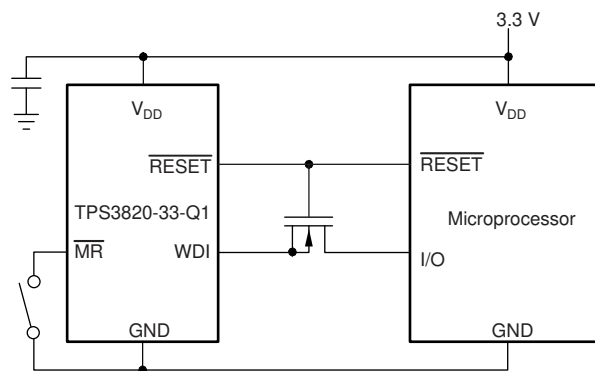


Figure 8-3. WDI Example

## 8.3 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 1.1V to 5.5V. Though not required, good analog design is to place a 0.1μF ceramic capacitor close to the V<sub>DD</sub> pin if the input supply is noisy.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Follow these guidelines to lay out the printed-circuit-board (PCB) that is used for the TPS382x-xx-Q1 family of devices.

- Place the  $V_{DD}$  decoupling capacitor ( $C_{VDD}$ ) close to the device.
- Avoid using long traces for the  $V_{DD}$  supply node. The  $V_{DD}$  capacitor ( $C_{VDD}$ ), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum  $V_{DD}$  voltage.

### 8.4.2 Layout Example



Figure 8-4. Example Layout (DBV Package)

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

- [Latching a Voltage Supervisor \(Reset IC\)](#)
- [Voltage Supervisors \(Reset ICs\): Frequently Asked Questions \(FAQs\)](#)
- [Disabling the Watchdog Timer for TI's Family of Supervisors](#)

#### 9.1.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 9-1. Related Links**

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS3820-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS3823-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS3824-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS3825-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS3828-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

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All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2019) to Revision E (March 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated thermal parameters.....	4
• Clarify VPOR test conditions.....	5
• Updated MR resistance typical value.....	5

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<b>Changes from Revision C (December 2015) to Revision D (July 2019)</b>	<b>Page</b>
• For all new designs, use the TPS3820-33QPDBVRQ1 and TPS3820-50QPDBVRQ1. TPS3820-xxQP is functionally equivalent and a replacement to the TPS3820xxQ.....	1

---

<b>Changes from Revision B (June 2008) to Revision C (December 2015)</b>	<b>Page</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes, Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Added AEC-Q100 Qualified information and Temperature Range to <i>Features</i> .....	1
• Added -Q1 to all applicable part numbers .....	1
• Added FIXED DELAY TIME column to table .....	3

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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3820-33QDBVRQ1	NRND	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDEQ
TPS3820-33QDBVRQ1.A	NRND	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDEQ
<a href="#">TPS3820-33QPDBVRQ1</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	33PQ
TPS3820-33QPDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	33PQ
TPS3820-50QDBVRQ1	NRND	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDDQ
TPS3820-50QDBVRQ1.A	NRND	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDDQ
<a href="#">TPS3820-50QPDBVRQ1</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	50PQ
TPS3820-50QPDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	50PQ
<a href="#">TPS3823-25QDBVRQ1</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	PAPQ
TPS3823-25QDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PAPQ
<a href="#">TPS3823-33QDBVRQ1</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	PARQ
TPS3823-33QDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PARQ
<a href="#">TPS3823-50QDBVRQ1</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	PASQ
TPS3823-50QDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PASQ
<a href="#">TPS3824-33QDBVRQ1</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAVQ
TPS3824-33QDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAVQ
<a href="#">TPS3824-50QDBVRQ1</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	PAWQ
TPS3824-50QDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PAWQ
<a href="#">TPS3825-33QDBVRQ1</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	PDGQ
TPS3825-33QDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PDGQ
<a href="#">TPS3828-33QDBVRQ1</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	PDIQ
TPS3828-33QDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PDIQ
<a href="#">TPS3828-50QDBVRG4Q</a>	NRND	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDHQ

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TPS3820-Q1, TPS3823-Q1, TPS3824-Q1, TPS3825-Q1, TPS3828-Q1 :**

- Catalog : [TPS3820](#), [TPS3823](#), [TPS3824](#), [TPS3825](#), [TPS3828](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3820-33QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3820-33QPDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3820-33QPDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3820-50QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3820-50QPDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3820-50QPDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3823-25QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3823-25QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3823-33QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3823-33QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3823-50QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3823-50QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3824-33QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3824-50QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3824-50QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3825-33QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3828-33QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3828-33QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3828-50QDBVRG4Q	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3820-33QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3820-33QPDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3820-33QPDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3820-50QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3820-50QPDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3820-50QPDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3823-25QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3823-25QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3823-33QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3823-33QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3823-50QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3823-50QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3824-33QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3824-50QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3824-50QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3825-33QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3828-33QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3828-33QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3828-50QDBVRG4Q	SOT-23	DBV	5	3000	182.0	182.0	20.0



# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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