TMS320VC5407/TMS320VC5404 Fixed-Point Digital Signal Processors

Data Manual

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TEXAS INSTRUMENTS

REVISION HISTORY

This data sheet revision history highlights the technical changes made to the SPRS007D device-specific data sheet to make it an SPRS007E revision.

Scope: This document has been reviewed for technical accuracy; the technical content is up-to-date as of the specified release date with the following changes.

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
18	Table 2−2, Signal Descriptions: − Added “TEST PINS” pin group title − Updated DESCRIPTION of $\overline{\text{TRST}}$ − Added footnote about $\overline{\text{TRST}}$
109	Section 6, Mechanical Data: − Moved “Package Thermal Resistance Characteristics” section (Section 5.4 in SPRS007D) to this section − Added Section 6.2, Packaging Information − Mechanical drawings will be appended to this document via an automated process

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1 TMS320VC5407/TMS320VC5404 Features

- Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus
- 40-Bit Arithmetic Logic Unit (ALU) Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators
- 17- × 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation
- Compare, Select, and Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator
- Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)
- Data Bus With a Bus Holder Feature
- Extended Addressing Mode for 8M × 16-Bit Maximum Addressable External Program Space
- On-Chip ROM
  - 128K × 16-Bit (5407) Configured for Program Memory
  - 64K × 16-Bit (5404) Configured for Program Memory
- On-Chip RAM
  - 40K x 16-Bit (5407) Composed of Five Blocks of 8K × 16-Bit On-Chip Dual-Access Program/Data RAM
  - 16K x 16-Bit (5404) Composed of Two Blocks of 8K × 16-Bit On-Chip Dual-Access Program/Data RAM
- Enhanced External Parallel Interface (XIO2)
- Single-Instruction-Repeat and Block-Repeat Operations for Program Code
- Block-Memory-Move Instructions for Better Program and Data Management
- Instructions With a 32-Bit Long Word Operand
- Instructions With Two- or Three-Operand Reads
- Arithmetic Instructions With Parallel Store and Parallel Load
- Conditional Store Instructions
- Fast Return From Interrupt
- On-Chip Peripherals
  - Software-Programmable Wait-State Generator and Programmable Bank-Switching
  - On-Chip Programmable Phase-Locked Loop (PLL) Clock Generator With External Clock Source
  - Two 16-Bit Timers
  - Six-Channel Direct Memory Access (DMA) Controller
  - Three Multichannel Buffered Serial Ports (McBSPs)
  - 8/16-Bit Enhanced Parallel Host-Port Interface (HPI8/16)
  - Universal Asynchronous Receiver/ Transmitter (UART) With Integrated Baud Rate Generator
- Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes
- CLKOUT Off Control to Disable CLKOUT
- On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG) Boundary Scan Logic
- 144-Pin Ball Grid Array (BGA) (GGU Suffix)
- 144-Pin Low-Profile Quad Flatpack (LQFP) (PGE Suffix)
- 8.33-ns Single-Cycle Fixed-Point Instruction Execution Time (120 MIPS)
- 3.3-V I/O Supply Voltage
- 1.5-V Core Supply Voltage

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

2 Introduction

This data manual discusses features and specifications of the TMS320VC5407 and TMS320VC5404 (hereafter referred to as the 5407/5404 unless otherwise specified) digital signal processors (DSPs). The 5407 and 5404 are essentially the same device except for differences in their memory maps.

This section lists the pin assignments and describes the function of each pin. This data manual also provides a detailed description section, electrical specifications, parameter measurement information, and mechanical data about the available packaging.

NOTE: This data manual is designed to be used in conjunction with the *TMS320C54x™ DSP Functional Overview* (literature number SPRU307).

2.1 Description

The 5407/5404 are based on an advanced modified Harvard architecture that has one program memory bus and three data memory buses. These processors provide an arithmetic logic unit (ALU) with a high degree of parallelism, application-specific hardware logic, on-chip memory, and additional on-chip peripherals. The basis of the operational flexibility and speed of these DSPs is a highly specialized instruction set.

Separate program and data spaces allow simultaneous access to program instructions and data, providing a high degree of parallelism. Two read operations and one write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions can fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that can all be performed in a single machine cycle. These DSPs also include the control mechanisms to manage interrupts, repeated operations, and function calls.

2.2 Pin Assignments

Figure 2−1 illustrates the ball locations for the 144-pin ball grid array (BGA) package and is used in conjunction with Table 2−1 to locate signal names and ball grid numbers. Figure 2−2 provides the pin assignments for the 144-pin low-profile quad flatpack (LQFP) package.

TMS320C54x is a trademark of Texas Instruments.

2.2.1 Terminal Assignments for the GGU Package

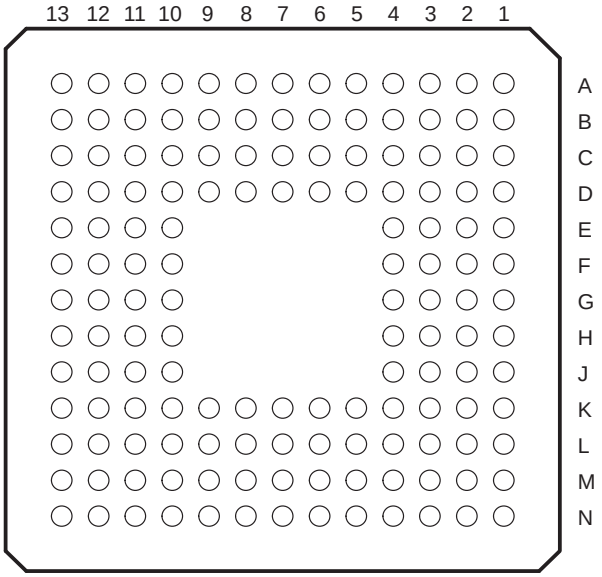


Figure 2−1. 144-Ball GGU MicroStar BGA™ (Bottom View)

Table 2−1 lists each signal name and BGA ball number for the 144-pin TMS320VC5407/ TMS320VC5404GGU package. Table 2−2 lists each terminal name, terminal function, and operating modes for the TMS320VC5407/TMS320VC5404.

MicroStar BGA is a trademark of Texas Instruments.

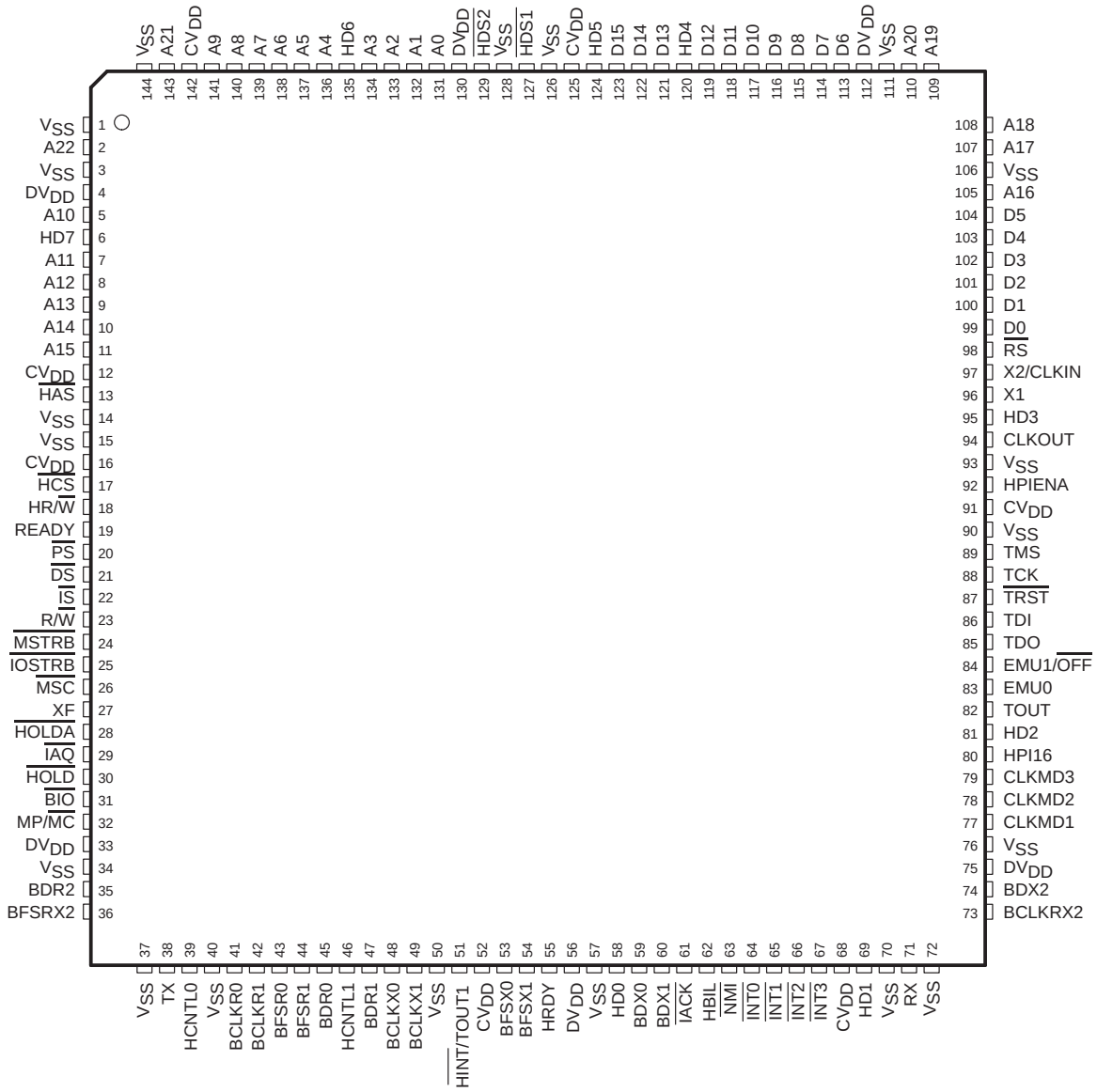
Table 2−1. Terminal Assignments for the 144-Pin BGA Package†

SIGNAL QUADRANT 1	BGA BALL #	SIGNAL QUADRANT 2	BGA BALL #	SIGNAL QUADRANT 3	BGA BALL #	SIGNAL QUADRANT 4	BGA BALL #
V_{SS}	A1	BCLKRX2	N13	V_{SS}	N1	A19	A13
A22	B1	BDX2	M13	TX	N2	A20	A12
V_{SS}	C2	DV_{DD}	L12	HCNTL0	M3	V_{SS}	B11
DV_{DD}	C1	V_{SS}	L13	V_{SS}	N3	DV_{DD}	A11
A10	D4	CLKMD1	K10	BCLKR0	K4	D6	D10
HD7	D3	CLKMD2	K11	BCLKR1	L4	D7	C10
A11	D2	CLKMD3	K12	BFSR0	M4	D8	B10
A12	D1	HPI16	K13	BFSR1	N4	D9	A10
A13	E4	HD2	J10	BDR0	K5	D10	D9
A14	E3	TOUT	J11	HCNTL1	L5	D11	C9
A15	E2	EMU0	J12	BDR1	M5	D12	B9
CV_{DD}	E1	EMU1/$\overline{OFF}$	J13	BCLKX0	N5	HD4	A9
$\overline{HAS}$	F4	TDO	H10	BCLKX1	K6	D13	D8
V_{SS}	F3	TDI	H11	V_{SS}	L6	D14	C8
V_{SS}	F2	$\overline{TRST}$	H12	$\overline{HINT}$/TOUT1	M6	D15	B8
CV_{DD}	F1	TCK	H13	CVDD	N6	HD5	A8
$\overline{HCS}$	G2	TMS	G12	BFSX0	M7	CV_{DD}	B7
HR/$\overline{W}$	G1	V_{SS}	G13	BFSX1	N7	V_{SS}	A7
READY	G3	CV_{DD}	G11	HRDY	L7	$\overline{HDS1}$	C7
$\overline{PS}$	G4	HPIENA	G10	DV_{DD}	K7	V_{SS}	D7
$\overline{DS}$	H1	V_{SS}	F13	V_{SS}	N8	$\overline{HDS2}$	A6
$\overline{IS}$	H2	CLKOUT	F12	HD0	M8	DV_{DD}	B6
R/$\overline{W}$	H3	HD3	F11	BDX0	L8	A0	C6
$\overline{MSTRB}$	H4	X1	F10	BDX1	K8	A1	D6
$\overline{IOSTRB}$	J1	X2/CLKIN	E13	$\overline{IACK}$	N9	A2	A5
$\overline{MSC}$	J2	$\overline{RS}$	E12	HBIL	M9	A3	B5
XF	J3	D0	E11	$\overline{NMI}$	L9	HD6	C5
$\overline{HOLDA}$	J4	D1	E10	$\overline{INT0}$	K9	A4	D5
$\overline{IAQ}$	K1	D2	D13	$\overline{INT1}$	N10	A5	A4
$\overline{HOLD}$	K2	D3	D12	$\overline{INT2}$	M10	A6	B4
$\overline{BIO}$	K3	D4	D11	$\overline{INT3}$	L10	A7	C4
MP/$\overline{MC}$	L1	D5	C13	CV_{DD}	N11	A8	A3
DV_{DD}	L2	A16	C12	HD1	M11	A9	B3
V_{SS}	L3	V_{SS}	C11	V_{SS}	L11	CV_{DD}	C3
BDR2	M1	A17	B13	RX	N12	A21	A2
BFSRX2	M2	A18	B12	V_{SS}	M12	V_{SS}	B2

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

2.2.2 Pin Assignments for the PGE Package

The TMS320VC5407/TMS320VC5404PGE 144-pin low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2−2.



NOTE A: DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

Figure 2−2. 144-Pin PGE Low-Profile Quad Flatpack (Top View)

2.3 Signal Descriptions

Table 2−2 lists each signal, function, and operating mode(s) grouped by function. See Section 2.2 for exact pin locations based on package type.

Table 2−2. Signal Descriptions

TERMINAL NAME	I/O†	DESCRIPTION		
EXTERNAL MEMORY INTERFACE PINS				
A22 (MSB) A21 A20 A19 A18 A17 A16	O/Z	Parallel address bus A22 (MSB) through A0 (LSB). The lower sixteen address pins—A0 to A15—are multiplexed to address all external memory (program, data) or I/O, while the upper seven address pins—A22 to A16—are only used to address external program space. These pins are placed in the high-impedance state when the hold mode is enabled, or when $\overline{OFF}$ is low.		
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)		A15 (MSB) A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)	I	These pins can be used to address internal memory via the HPI when the HPI16 pin is high.
D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O/Z	D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O	Parallel data bus D15 (MSB) through D0 (LSB). The sixteen data pins, D0 to D15, are multiplexed to transfer data between the core CPU and external data/program memory, I/O devices, or HPI in 16-bit mode. The data bus is placed in the high-impedance state when not outputting or when $\overline{RS}$ or $\overline{HOLD}$ is asserted. The data bus also goes into the high-impedance state when $\overline{OFF}$ is low. The data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external bias resistors on unused pins. When the data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The data bus holders of the DSP are disabled at reset, and can be enabled/disabled via the BH bit of the BSCR.

† I = Input, O = Output, Z = High-impedance, S = Supply

‡ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{TRST}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

Table 2−2. Signal Descriptions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
INITIALIZATION, INTERRUPT, AND RESET PINS		
$\overline{IACK}$	O/Z	Interrupt acknowledge signal. $\overline{IACK}$ Indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–0. $\overline{IACK}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{INT3}$	I	External user interrupt inputs. $\overline{INT0-3}$ are prioritized and maskable via the interrupt mask register and interrupt mode bit. The status of these pins can be polled by way of the interrupt flag register.
$\overline{NMI}$	I	Nonmaskable interrupt. $\overline{NMI}$ is an external interrupt that cannot be masked by way of the INTM or the IMR. When $\overline{NMI}$ is activated, the processor traps to the appropriate vector location.
$\overline{RS}$	I	Reset input. $\overline{RS}$ causes the DSP to terminate execution and causes a re-initialization of the CPU and peripherals. When $\overline{RS}$ is brought to a high level, execution begins at location 0FF80h of program memory. $\overline{RS}$ affects various registers and status bits.
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select pin. If active low at reset, microcomputer mode is selected, and the internal program ROM is mapped into the upper 16K words of program memory space. If the pin is driven high during reset, microprocessor mode is selected, and the on-chip ROM is removed from program space. This pin is only sampled at reset, and the MP/$\overline{MC}$ bit of the PMST register can override the mode that is selected at reset.
MULTIPROCESSING AND GENERAL PURPOSE PINS		
$\overline{BIO}$	I	Branch control input. A branch can be conditionally executed when $\overline{BIO}$ is active. If low, the processor executes the conditional instruction. The $\overline{BIO}$ condition is sampled during the decode phase of the pipeline for XC instruction, and all other instructions sample $\overline{BIO}$ during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or as a general-purpose output pin. XF goes into the high-impedance state when $\overline{OFF}$ is low, and is set high at reset.
MEMORY CONTROL PINS		
$\overline{DS}$ $\overline{PS}$ $\overline{IS}$	O/Z	Data, program, and I/O space select signals. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ are always high unless driven low for accessing a particular external memory space. Active period corresponds to valid address information. Placed into a high-impedance state in hold mode. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ also go into the high-impedance state when $\overline{OFF}$ is low.
MSTRB	O/Z	Memory strobe signal. MSTRB is always high unless low-level asserted to indicate an external bus access to data or program memory. Placed in high-impedance state in hold mode. MSTRB also goes into the high-impedance state when $\overline{OFF}$ is low.
READY	I	Data ready input. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/$\overline{W}$	O/Z	Read/write signal. R/$\overline{W}$ indicates transfer direction during communication to an external device. Normally in read mode (high), unless asserted low when the DSP performs a write operation. Placed in high-impedance state in hold mode. R/$\overline{W}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{IOSTRB}$	O/Z	I/O strobe signal. $\overline{IOSTRB}$ is always high unless low level asserted to indicate an external bus access to an I/O device. Placed in high-impedance state in hold mode. $\overline{IOSTRB}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{HOLD}$	I	Hold input. $\overline{HOLD}$ is asserted to request control of the address, data, and control lines. When acknowledged by the C54x™ DSP, these lines go into high-impedance state.
$\overline{HOLDA}$	O/Z	Hold acknowledge signal. $\overline{HOLDA}$ indicates that the DSP is in a hold state and that the address, data, and control lines are in a high-impedance state, allowing the external memory interface to be accessed by other devices. $\overline{HOLDA}$ also goes into the high-impedance state when is $\overline{OFF}$ low.

† I = Input, O = Output, Z = High-impedance, S = Supply

‡ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{TRST}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

C54x is a trademark of Texas Instruments.

Table 2−2. Signal Descriptions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
MEMORY CONTROL PINS (CONTINUED)		
$\overline{\text{MSC}}$	O/Z	Microstate complete. $\overline{\text{MSC}}$ indicates completion of all software wait states. When two or more software wait states are enabled, the $\overline{\text{MSC}}$ pin goes active at the beginning of the first software wait state, and goes inactive (high) at the beginning of the last software wait state. If connected to the ready input, $\overline{\text{MSC}}$ forces one external wait state after the last internal wait state is completed. $\overline{\text{MSC}}$ also goes into the high impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{IAQ}}$	O/Z	Instruction acquisition signal. $\overline{\text{IAQ}}$ is asserted (active low) when there is an instruction address on the address bus and goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
OSCILLATOR/TIMER PINS		
CLKOUT	O/Z	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of this signal. CLKOUT also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
CLKMD1 CLKMD2 CLKMD3	I	Clock mode external/internal input signals. CLKMD1−CLKMD3 allows you to select and configure different clock modes such as crystal, external clock, various PLL factors.
X2/CLKIN	I	Input pin to internal oscillator from the crystal. If the internal oscillator is not being used, an external clock source can be applied to this pin. The internal machine cycle time is determined by the clock operating mode pins (CLKMD1, CLKMD2 and CLKMD3).
X1	O	Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when $\overline{\text{OFF}}$ is low. (This is revision depended, see Section 3.10 for additional information.)
TOUT	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT cycle wide. TOUT also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
TOUT1	I/O/Z	Timer1 output. TOUT1 signals a pulse when the on-chip timer1 counts down past zero. The pulse is a CLKOUT cycle wide. The TOUT1 output is multiplexed with the $\overline{\text{HINT}}$ pin of the HPI, and TOUT1 is only available when the HPI is disabled.
MULTICHANNEL BUFFERED SERIAL PORT PINS		
BCLKR0 BCLKR1 BCLKRX2	I/O/Z	Receive clock input. BCLKR serves as the serial shift clock for the buffered serial port receiver. BCLKRX2 is McBSP2 transmit AND receive clock.
BDR0 BDR1 BDR2	I	Serial data receive input.
BFSR0 BFSR1 BFSRX2	I/O/Z	Frame synchronization pulse for receive input. The BFSR pulse initiates the receive data process over BDR. BFSRX2 is McBSP2 transmit AND receive frame sync.
BCLKX0 BCLKX1	I/O/Z	Transmit clock. BCLKX serves as the serial shift clock for the buffered serial port transmitter. The BCLKX pins are configured as inputs after reset. BCLKX goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
BDX0 BDX1 BDX2	O/Z	Serial data transmit output. BDX is placed in the high-impedance state when not transmitting, when $\overline{\text{RS}}$ is asserted or when $\overline{\text{OFF}}$ is low.
BFSX0 BFSX1	I/O/Z	Frame synchronization pulse for transmit output. The BFSX pulse initiates the transmit data process over BDX. The BFSX pins are configured as inputs after reset. BFSX goes into the high-impedance state when $\overline{\text{OFF}}$ is low.

† I = Input, O = Output, Z = High-impedance, S = Supply

‡ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{\text{TRST}}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

Table 2−2. Signal Descriptions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
UART		
TX	O	UART asynchronous serial transmit data output.
RX	I	UART asynchronous serial receive data input.
HOST PORT INTERFACE PINS		
A0−A15	I	These pins can be used to address internal memory via the HPI when the HPI16 pin is HIGH.
D0−D15	I/O	These pins can be used to read/write internal memory via the HPI when the HPI16 pin is high. The sixteen data pins, D0 to D15, are multiplexed to transfer data between the core CPU and external data/program memory, I/O devices, or HPI in 16-bit mode. The data bus is placed in the high-impedance state when not outputting or when $\overline{RS}$ or $\overline{HOLD}$ is asserted. The data bus also goes into the high-impedance state when $\overline{OFF}$ is low. The data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external bias resistors on unused pins. When the data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The data bus holders of the DSP are disabled at reset, and can be enabled/disabled via the BH bit of the BSCR.
HD0−HD7	I/O/Z	Parallel bi-directional data bus. These pins can also be used as general-purpose I/O pins when the HPI16 pin is high. HD0−HD7 is placed in the high-impedance state when not outputting data or when $\overline{OFF}$ is low. The HPI data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. When the HPI data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The HPI data bus holders are disabled at reset, and can be enabled/disabled via the HBH bit of the BSCR.
HCNTL0 HCNTL1	I	Control inputs. These inputs select a host access to one of the three HPI registers. (Pullup only enabled when HPIENA=0, HPI16=1)
HBIL	I	Byte identification input. Identifies first or second byte of transfer. (Pullup only enabled when HPIENA=0, invalid when HPI16 = 1)
$\overline{HCS}$	I	Chip select input. This pin is the select input for the HPI, and must be driven low during accesses. (Pullup only enabled when HPIENA = 0, or HPI16 = 1)
$\overline{HDS1}$ $\overline{HDS2}$	I	Data strobe inputs. These pins are driven by the host read and write strobes to control transfers. (Pullup only enabled when HPIENA = 0)
$\overline{HAS}$	I	Address strobe input. Address strobe input. Hosts with multiplexed address and data pins require this input, to latch the address in the HPIA register. (Pull-up only enabled when HPIENA = 0)
HR/$\overline{W}$	I	Read/write input. This input controls the direction of an HPI transfer. (Pullup only enabled when HPIENA=0)
HRDY	O/Z	Ready output. The ready output informs the host when the HPI is ready for the next transfer. HRDY goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{HINT}$	O/Z	Interrupt output. This output is used to interrupt the host. When the DSP is in reset, this signal is driven high. $\overline{HINT}$ can also be used for timer 1 output (TOUT1), when the HPI is disabled. The signal goes into the high-impedance state when $\overline{OFF}$ is low. (invalid when HPI16=1)
HPIENA	I	HPI enable input. This pin must be tied directly to DV_{DD} to enable the HPI. An internal pulldown resistor is always active and the HPIENA pin is sampled on the rising edge of $\overline{RS}$. If HPIENA is left open or driven low during reset, the HPI module is disabled. Once the HPI is disabled, the HPIENA pin has no effect until the DSP is reset.
HPI16	I	HPI 16-bit select pin. This pin must be tied directly to DV_{DD} to enable HPI16 mode. This input pin has an internal pulldown resistor which is always active. If HPI16 is left open or driven low, HPI16 mode is disabled. The non-multiplexed mode allows hosts with separate address/data buses to access the HPI address range via the 16 address pins A0−A15. 16-bit Data is also accessible through pins D0−D15. HOST-to-DSP and DSP-to-HOST interrupts are not supported. There are no HPIC and HPIA registers in the non-multiplexed mode since there are HCNTRL0,1 signals available.

† I = Input, O = Output, Z = High-impedance, S = Supply

‡ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{TRST}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

Table 2−2. Signal Descriptions (Continued)

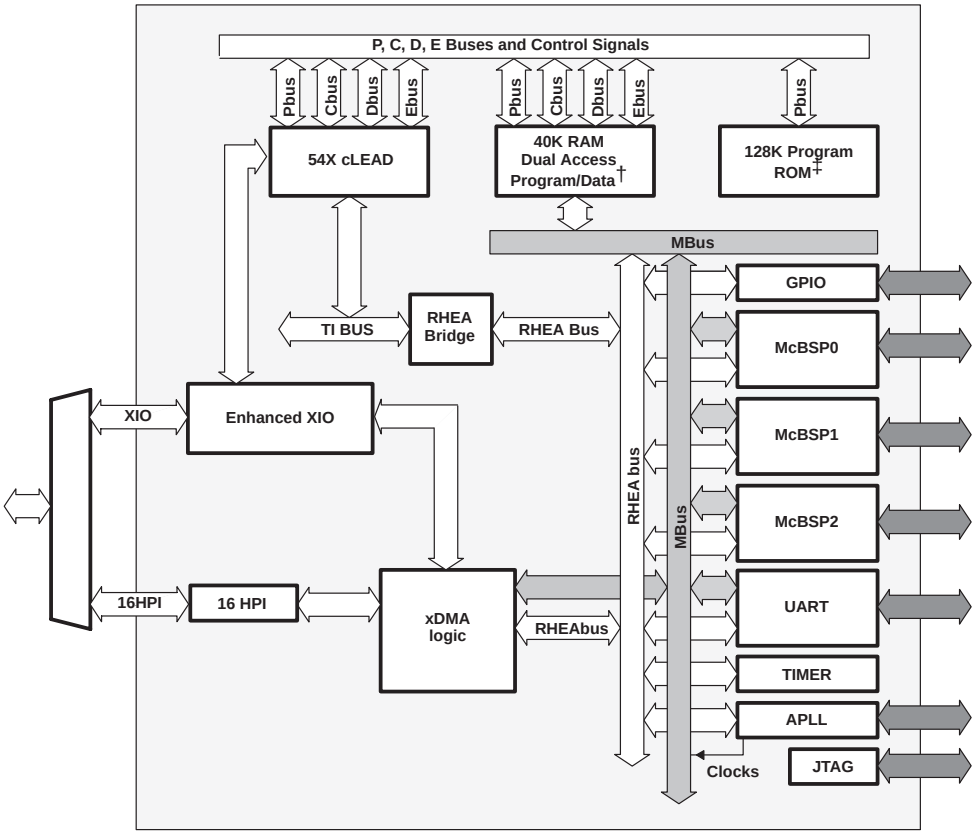
TERMINAL NAME	I/O†	DESCRIPTION
SUPPLY PINS		
CV_{DD}	S	$+V_{DD}$. Dedicated 1.5V power supply for the core CPU.
DV_{DD}	S	$+V_{DD}$. Dedicated 3.3V power supply for I/O pins.
V_{SS}	S	Ground.
TEST PINS		
TCK	I	IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	IEEE standard 1149.1 test data input, pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. TDO also goes into the high-impedance state when $\overline{OFF}$ is low.
TMS	I	IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the test access port (TAP) controller on the rising edge of TCK.
$\overline{TRST}$‡	I	IEEE standard 1149.1 test reset. $\overline{TRST}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{TRST}$ is driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pulldown device.
EMU0	I/O/Z	Emulator 0 pin. When $\overline{TRST}$ is driven low, EMU0 must be high for activation of the $\overline{OFF}$ condition. When $\overline{TRST}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of IEEE standard 1149.1 scan system. Should be pulled up to DV_{DD} with a separate 4.7-kΩ resistor.
EMU1/$\overline{OFF}$	I/O/Z	Emulator 1 pin/disable all outputs. When $\overline{TRST}$ is driven high, EMU1/$\overline{OFF}$ is used as an interrupt to or from the emulator system and is defined as input/output via IEEE standard 1149.1 scan system. When $\overline{TRST}$ is driven low, EMU1/$\overline{OFF}$ is configured as $\overline{OFF}$. The EMU1/$\overline{OFF}$ signal, when active low, puts all output drivers into the high-impedance state. Note that $\overline{OFF}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Thus, for the $\overline{OFF}$ feature, the following conditions apply: $\overline{TRST}$ = low, EMU0 = high, EMU1/$\overline{OFF}$ = low. Should be pulled up to DV_{DD} with a separate 4.7-kΩ resistor.

† I = Input, O = Output, Z = High-impedance, S = Supply

‡ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{TRST}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

3 Functional Overview

The following functional overview is based on the block diagram in Figure 3−1.



† 16K for 5404
‡ 64K for 5404

Figure 3−1. TMS320VC5407/TMS320VC5404 Functional Block Diagram

3.1 Memory

The 5407/5404 device provides both on-chip ROM and RAM memories to aid in system performance and integration.

3.1.1 Data Memory

The data memory space addresses up to 64K of 16-bit words. The device automatically accesses the on-chip RAM when addressing within its bounds. When an address is generated outside the RAM bounds, the device automatically generates an external access.

The advantages of operating from on-chip memory are as follows:

- Higher performance because no wait states are required
- Higher performance because of better flow within the pipeline of the central arithmetic logic unit (CALU)
- Lower cost than external memory
- Lower power than external memory

The advantage of operating from off-chip memory is the ability to access a larger address space.

3.1.2 Program Memory

Software can configure their memory cells to reside inside or outside of the program address map. When the cells are mapped into program space, the device automatically accesses them when their addresses are within bounds. When the program-address generation (PAGEN) logic generates an address outside its bounds, the device automatically generates an external access. The advantages of operating from on-chip memory are as follows:

- Higher performance because no wait states are required
- Lower cost than external memory
- Lower power than external memory

The advantage of operating from off-chip memory is the ability to access a larger address space.

3.1.3 Extended Program Memory

The 5407/5404 uses a paged extended memory scheme in program space to allow access of up to 8192K of program memory. In order to implement this scheme, the 5407/5404 includes several features which are also present on C548/549/5410:

- Twenty-three address lines, instead of sixteen
- An extra memory-mapped register, the XPC
- Six extra instructions for addressing extended program space

Program memory in the 5407/5404 is organized into 128 pages that are each 64K in length.

The value of the XPC register defines the page selection. This register is memory-mapped into data space to address 001Eh. At a hardware reset, the XPC is initialized to 0.

3.2 On-Chip ROM With Bootloader

The 5407 features a 128K-word $\times$ 16-bit on-chip maskable ROM that is mapped into program memory space, but 16K words of which can also optionally be mapped into data memory. The 5404 features a 64K-word $\times$ 16-bit on-chip maskable ROM that is mapped into program memory space.

Customers can also arrange to have the ROM of the 5407/5404 programmed with contents unique to any particular application.

A bootloader is available in the standard 5407/5404 on-chip ROM. This bootloader can be used to automatically transfer user code from an external source to anywhere in the program memory at power up. If MP/$\overline{\text{MC}}$ of the device is sampled low during a hardware reset, execution begins at location FF80h of the on-chip ROM. This location contains a branch instruction to the start of the bootloader program.

The standard 5407/5404 devices provide different ways to download the code to accommodate various system requirements:

- Parallel from 8-bit or 16-bit-wide EPROM
- Parallel from I/O space, 8-bit or 16-bit mode
- Serial boot from serial ports, 8-bit or 16-bit mode
- UART boot mode
- Host-port interface boot
- Warm boot

The standard on-chip ROM layout is shown in Table 3−1.

Table 3−1. Standard On-Chip ROM Layout†

ADDRESS RANGE	DESCRIPTION
C000h−D4FFh	ROM tables for the GSM EFR speech codec
D500h−F7FFh	Reserved
F800h−FBFFh	Bootloader
FC00h−FCFFh	μ-Law expansion table
FD00h−FDFFh	A-Law expansion table
FE00h−FEFFh	Sine look-up table
FF00h−FF7Fh	Reserved†
FF80h−FFFFh	Interrupt vector table

† In the 5407/5404 ROM, 128 words are reserved for factory device-testing purposes. Application code to be implemented in on-chip ROM must reserve these 128 words at addresses FF00h−FF7Fh in program space.

3.3 On-Chip RAM

The 5407 device contains 40K-words × 16-bit of on-chip dual-access RAM (DARAM), while the 5404 device contains 16K-words x 16-bit of DARAM.

The DARAM is composed of five blocks of 8K words each. Each block in the DARAM can support two reads in one cycle, or a read and a write in one cycle. The five blocks of DARAM on the 5407 are located in the address range 0080h−9FFFh in data space, and can be mapped into program/data space by setting the OVLY bit to one.

On the 5404, the two blocks of DARAM are located at 0080h−3FFFh in data space and can also be mapped into data space by setting OVLY to one.

3.4 On-Chip Memory Security

The 5407/5404 device provides maskable options to protect the contents of on-chip memories. When the ROM protect option is selected, no externally originating instruction can access the on-chip ROM; when the RAM protect option is selected, HPI RAM is protected; HPI writes are not restricted, but HPI reads are restricted to 2000h − 3FFFh.

3.5 Memory Maps

3.5.1 5407 Memory Map

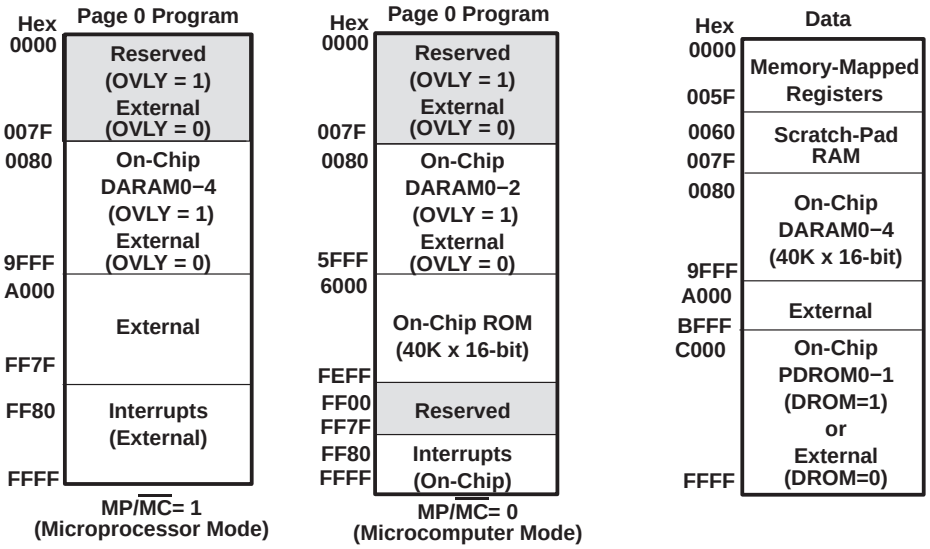
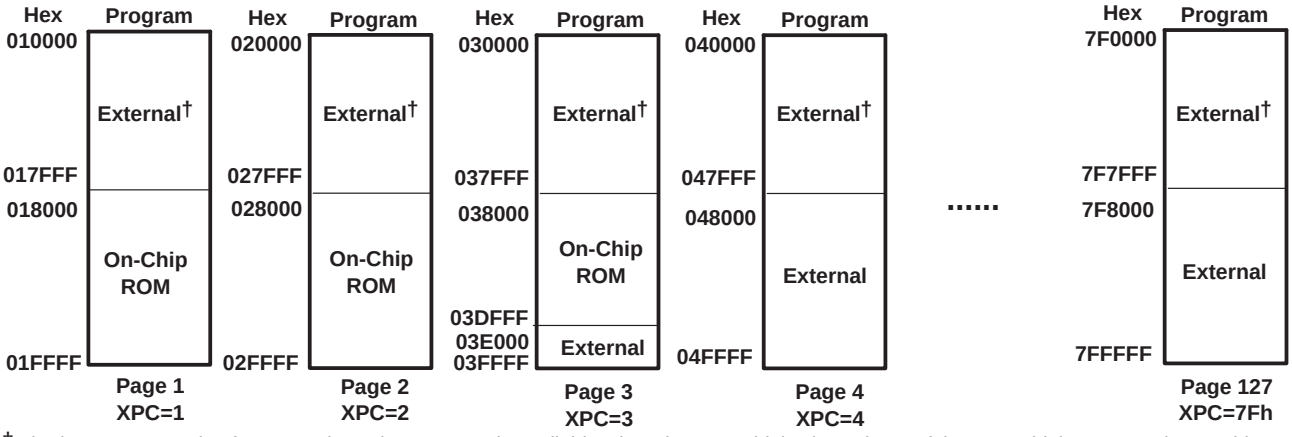


Figure 3−2. 5407 Program and Data Memory Map



† The lower 32K words of pages 1 through 127 are only available when the OVLY bit is cleared to 0. If the OVLY bit is set to 1, the on-chip memory is mapped to the lower 32K words of all program space pages.

Figure 3−3. 5407 Extended Program Memory Map

3.5.2 5404 Memory Map

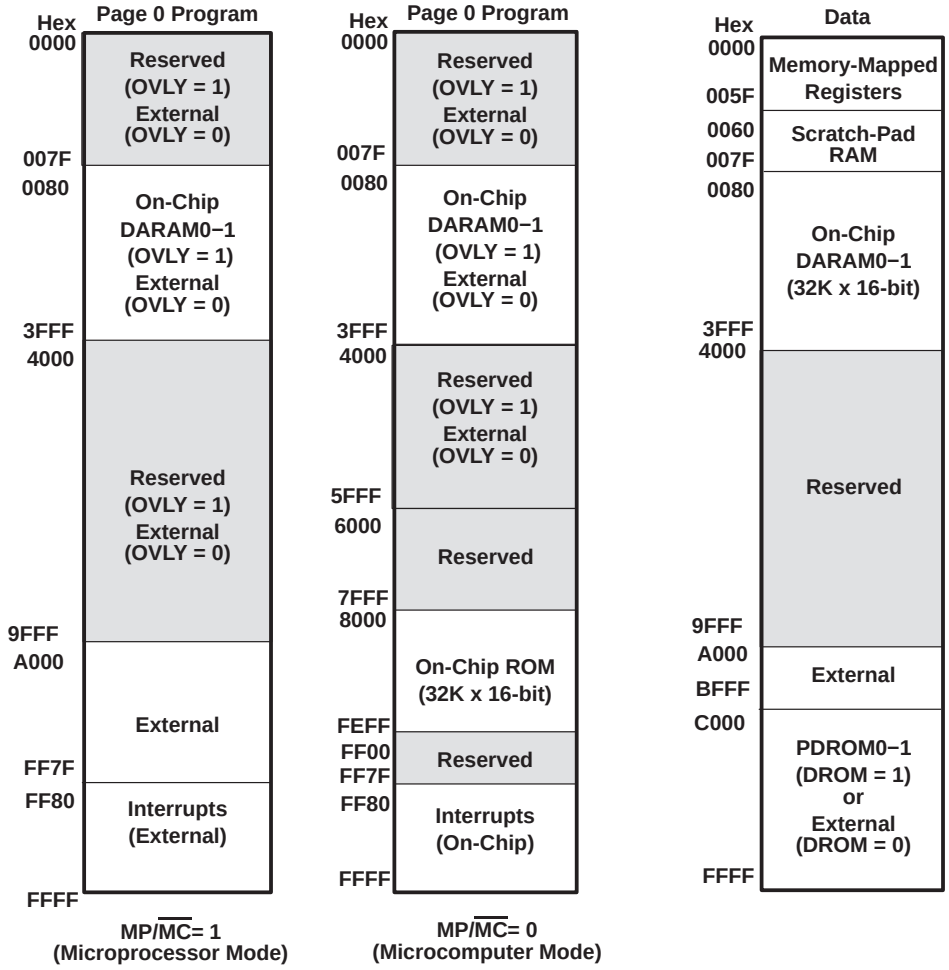
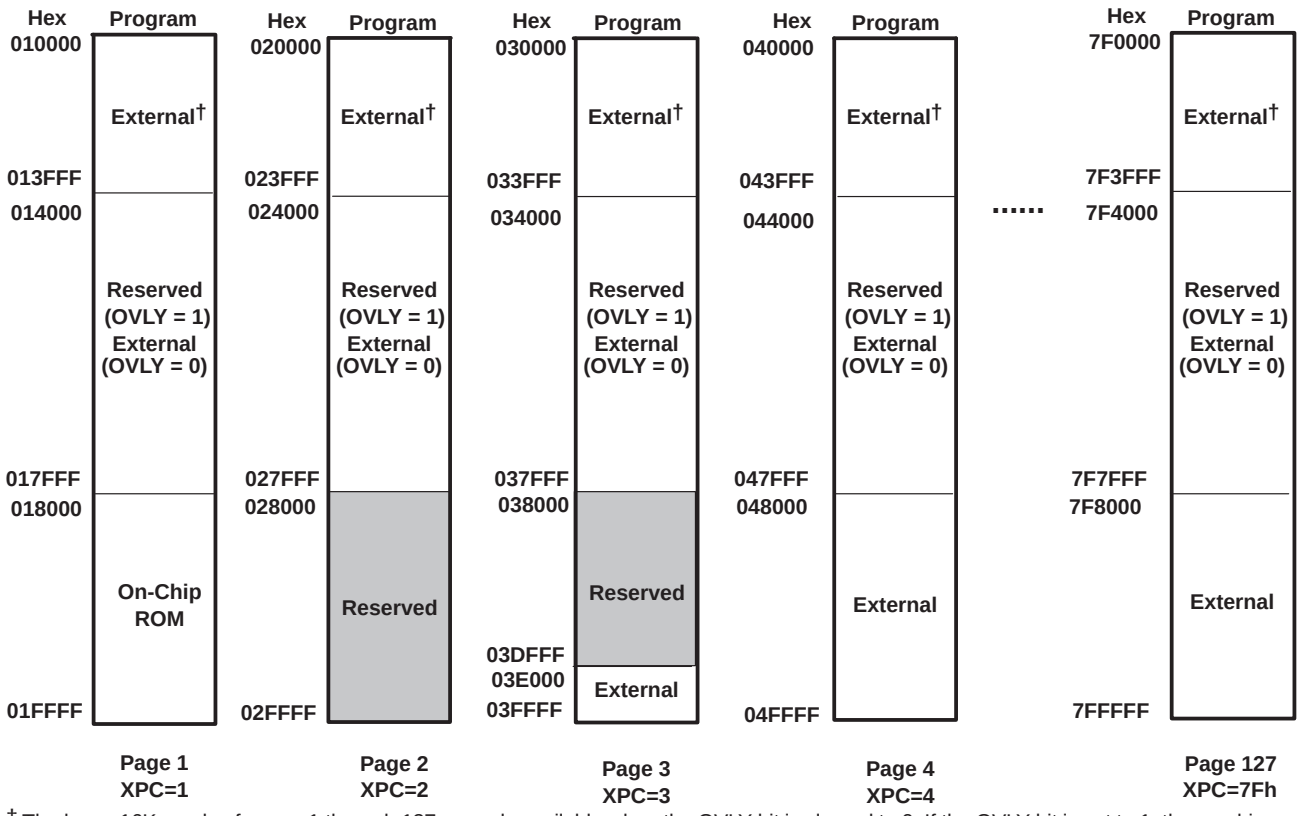


Figure 3−4. 5404 Program and Data Memory Map



† The lower 16K words of pages 1 through 127 are only available when the OVLY bit is cleared to 0. If the OVLY bit is set to 1, the on-chip memory is mapped to the lower 16K words of all program space pages.

Figure 3−5. 5404 Extended Program Memory Map

3.5.3 Relocatable Interrupt Vector Table

The reset, interrupt, and trap vectors are addressed in program space. These vectors are soft — meaning that the processor, when taking the trap, loads the program counter (PC) with the trap address and executes the code at the vector location. Four words, either two 1-word instructions or one 2-word instruction, are reserved at each vector location to accommodate a delayed branch instruction which allows branching to the appropriate interrupt service routine without the overhead.

At device reset, the reset, interrupt, and trap vectors are mapped to address FF80h in program space. However, these vectors can be remapped to the beginning of any 128-word page in program space after device reset. This is done by loading the interrupt vector pointer (IPTR) bits in the PMST register with the appropriate 128-word page boundary address. After loading IPTR, any user interrupt or trap vector is mapped to the new 128-word page.

NOTE: The hardware reset ($\overline{RS}$) vector cannot be remapped because the hardware reset loads the IPTR with 1s. Therefore, the reset vector is always fetched at location FF80h in program space.

15							
IPTR							
R/W-1FF							

7	6	5	4	3	2	1	0
IPTR	MP/$\overline{MC}$	OVLY	AVIS	DROM	CLKOFF	SMUL	SST
	MP/$\overline{MC}$ Pin	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read, W = Write, *n* = *value after reset*

Figure 3−6. Processor Mode Status Register (PMST)

Table 3−2. Processor Mode Status Register (PMST) Field Descriptions

BIT	FIELD	VALUE	DESCRIPTION
15−7	IPTR		Interrupt vector pointer. The 9-bit IPTR field points to the 128-word program page where the interrupt vectors reside. The interrupt vectors can be remapped to RAM for boot-loaded operations. At reset, these bits are all set to 1; the reset vector always resides at address FF80h in program memory space. The RESET instruction does not affect this field.
6	MP/$\overline{MC}$		Microprocessor/microcomputer mode. MP/$\overline{MC}$ enables/disables the on-chip ROM to be addressable in program memory space.
		0	The on-chip ROM is enabled and addressable.
		1	The on-chip ROM is not available.
			MP/$\overline{MC}$ is set to the value corresponding to the logic level on the MP/$\overline{MC}$ pin when sampled at reset. This pin is not sampled again until the next reset. The RESET instruction does not affect this bit. This bit can also be set or cleared by software.
5	OVLY		RAM overlay. OVLY enables on-chip dual-access data RAM blocks to be mapped into program space. The values for the OVLY bit are:
		0	The on-chip RAM is addressable in data space but not in program space.
		1	The on-chip RAM is mapped into program space and data space. Data page 0 (addresses 0h to 7Fh), however, is not mapped into program space.
4	AVIS		Address visibility mode. AVIS enables/disables the internal program address to be visible at the address pins.
		0	The external address lines do not change with the internal program address. Control and data lines are not affected and the address bus is driven with the last address on the bus.
		1	This mode allows the internal program address to appear at the pins of the 5407/5404 so that the internal program address can be traced. Also, it allows the interrupt vector to be decoded in conjunction with $\overline{IACK}$ when the interrupt vectors reside on on-chip memory.
3	DROM		Data ROM. DROM enables on-chip ROM to be mapped into data space. The DROM bit values are:
		0	The on-chip ROM is not mapped into data space.
		1	A portion of the on-chip ROM is not mapped into data space.
			The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
2	CLKOFF		CLOCKOUT off. When the CLKOFF bit is 1, the output of CLKOUT is disabled and remains at a high level.
1	SMUL		Saturation on multiplication. When SMUL = 1, saturation of a multiplication result occurs before performing the accumulation in a MAC of MAS instruction. The SMUL bit applies only when OVM = 1 and FRCT = 1.
0	SST		Saturation on store. When SST = 1, saturation of the data from the accumulator is enabled before storing in memory. The saturation is performed after the shift operation.

3.6 On-Chip Peripherals

The 5407/5404 device has the following peripherals:

- Software-programmable wait-state generator
- Programmable bank-switching
- A host-port interface (HPI8/16)
- Three multichannel buffered serial ports (McBSPs)
- Two hardware timers
- A clock generator with a multiple phase-locked loop (PLL)
- Enhanced external parallel interface (XIO2)
- A DMA controller (DMA)
- A UART with an integrated baud rate generator

3.6.1 Software-Programmable Wait-State Generator

The software wait-state generator of the 5407/5404 can extend external bus cycles by up to fourteen machine cycles. Devices that require more than fourteen wait states can be interfaced using the hardware READY line. When all external accesses are configured for zero wait states, the internal clocks to the wait-state generator are automatically disabled. Disabling the wait-state generator clocks reduces the power consumption of the 5407/5404.

The software wait-state register (SWWSR) controls the operation of the wait-state generator. The 14 LSBs of the SWWSR specify the number of wait states (0 to 7) to be inserted for external memory accesses to five separate address ranges. This allows a different number of wait states for each of the five address ranges. Additionally, the software wait-state multiplier (SWSM) bit of the software wait-state control register (SWCR) defines a multiplication factor of 1 or 2 for the number of wait states. At reset, the wait-state generator is initialized to provide seven wait states on all external memory accesses. The SWWSR bit fields are shown in Figure 3−7 and described in Table 3−3.

15	14	12	11	9	8
XPA	I/O		DATA		DATA
R/W-0	R/W-111		R/W-111		

6	5	3	2	0
DATA	PROGRAM		PROGRAM	
R/W-111	R/W-111		R/W-111	

LEGEND: R = Read, W = Write, *n* = *value after reset*

Figure 3−7. Software Wait-State Register (SWWSR) [Memory-Mapped Register (MMR) Address 0028h]

Table 3−3. Software Wait-State Register (SWWSR) Field Descriptions

BIT	FIELD	VALUE	DESCRIPTION
15	XPA	0	Extended program address control bit. XPA is used in conjunction with the program space fields (bits 0 through 5) to select the address range for program space wait states.
14−12	I/O	111	I/O space. The field value (0−7) corresponds to the base number of wait states for I/O space accesses within addresses 0000−FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
11−9	Data	111	Upper data space. The field value (0−7) corresponds to the base number of wait states for external data space accesses within addresses 8000−FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
8−6	Data	111	Lower data space. The field value (0−7) corresponds to the base number of wait states for external data space accesses within addresses 0000−7FFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
5−3	Program	111	Upper program space. The field value (0−7) corresponds to the base number of wait states for external program space accesses within the following addresses: ❑ XPA = 0: xx8000 − xxFFFFh ❑ XPA = 1: 400000h − 7FFFFFh The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
2−0	Program	111	Lower program space. The field value (0−7) corresponds to the base number of wait states for external program space accesses within the following addresses: ❑ XPA = 0: xx0000 − xx7FFFh ❑ XPA = 1: 000000 − 3FFFFFh The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.

The software wait-state multiplier bit of the software wait-state control register (SWCR) is used to extend the base number of wait states selected by the SWWSR. The SWCR bit fields are shown in Figure 3−8 and described in Table 3−4.

15															
Reserved															
R/W-0															

1	0
Reserved	SWSM
R/W-0	R/W-0

LEGEND: R = Read, W = Write, *n* = *value after reset*

Figure 3−8. Software Wait-State Control Register (SWCR) [MMR Address 002Bh]

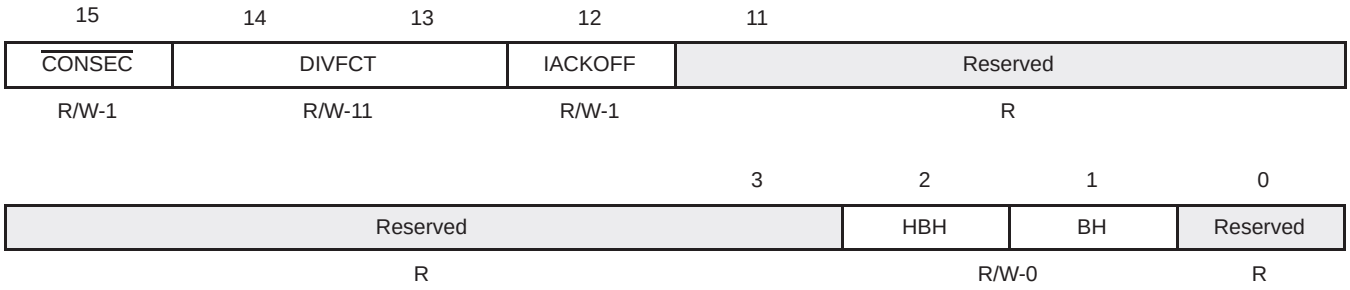
Table 3−4. Software Wait-State Control Register (SWCR) Field Descriptions

BIT	FIELD	VALUE	DESCRIPTION
15−1	Reserved		These bits are reserved and are unaffected by writes.
0	SWSM		Software wait-state multiplier. Used to multiply the number of wait states defined in the SWWSR by a factor of 1 or 2.
		0	Wait-state base values are unchanged (multiplied by 1).
		1	Wait-state base values are multiplied by 2 for a maximum of 14 wait states.

3.6.2 Programmable Bank-Switching

Programmable bank-switching logic allows the 5407/5404 to switch between external memory banks without requiring external wait states for memories that need additional time to turn off. The bank-switching logic automatically inserts one cycle when accesses cross a 32K-word memory-bank boundary inside program or data space.

Bank-switching is defined by the bank-switching control register (BSCR), which is memory-mapped at address 0029h. The bit fields of the BSCR are shown in Figure 3−9 and are described in Table 3−5.



LEGEND: R = Read, W = Write, *n* = *value after reset*

Figure 3−9. Bank-Switching Control Register (BSCR) [MMR Address 0029h]

Table 3−5. Bank-Switching Control Register (BSCR) Field Descriptions

BIT	FIELD	VALUE	DESCRIPTION
15	$\overline{\text{CONSEC}}$†		Consecutive bank-switching**.** Specifies the bank-switching mode.
		0	Bank-switching on 32K bank boundaries only. This bit is cleared if fast access is desired for continuous memory reads (i.e., no starting and trailing cycles between read cycles).
		1	Consecutive bank switches on external memory reads. Each read cycle consists of 3 cycles: starting cycle, read cycle, and trailing cycle.
13−14	DIVFCT		CLKOUT output divide factor**.** The CLKOUT output is driven by an on-chip source having a frequency equal to 1/(DIVFCT+1) of the DSP clock.
		00	CLKOUT is not divided.
		01	CLKOUT is divided by 2 from the DSP clock.
		10	CLKOUT is divided by 3 from the DSP clock.
		11	CLKOUT is divided by 4 from the DSP clock (default value following reset).
12	IACKOFF		$\overline{\text{IACK}}$ signal output off**.** Controls the output of the $\overline{\text{IACK}}$ signal. IACKOFF is set to 1 at reset.
		0	The $\overline{\text{IACK}}$ signal output off function is disabled.
		1	The $\overline{\text{IACK}}$ signal output off function is enabled.
11−3	Reserved		Reserved
2	HBH		HPI bus holder. Controls the HPI bus holder. HBH is cleared to 0 at reset**.**
		0	The bus holder is disabled except when HPI16=1.
		1	The bus holder is enabled. When not driven, the HPI data bus, HD[7:0] is held in the previous logic level.
1	BH		Bus holder. Controls the bus holder. BH is cleared to 0 at reset.
		0	The bus holder is disabled.
		1	The bus holder is enabled. When not driven, the data bus, D[15:0] is held in the previous logic level.
0	Reserved		Reserved

† For additional information, see Section 3.11 of this document.

The 5407/5404 has an internal register that holds the MSB of the last address used for a read or write operation in program or data space. In the non-consecutive bank switches ($\overline{\text{CONSEC}}$ = 0), if the MSB of the address used for the current read does not match that contained in this internal register, the $\overline{\text{MSTRB}}$ (memory strobe) signal is not asserted for one CLKOUT cycle. During this extra cycle, the address bus switches to the new address. The contents of the internal register are replaced with the MSB for the read of the current address. If the MSB of the address used for the current read matches the bits in the register, a normal read cycle occurs.

In non-consecutive bank switches ($\overline{\text{CONSEC}}$ = 0), if repeated reads are performed from the same memory bank, no extra cycles are inserted. When a read is performed from a different memory bank, memory conflicts are avoided by inserting an extra cycle. For more information, see Section 3.11 of this document.

The bank-switching mechanism automatically inserts one extra cycle in the following cases:

- A memory read followed by another memory read from a different memory bank.
- A program-memory read followed by a data-memory read.
- A data-memory read followed by a program-memory read.
- A program-memory read followed by another program-memory read from a different page.

3.6.3 Bus Holders

The 5407/5404 has two bus holder control bits, BH (BSCR[1]) and HBH (BSCR[2]), to control the bus keepers of the address bus (A[17−0]), data bus (D[15−0]), and the HPI data bus (HD[7−0]). Bus keeper enabling/disabling is described in Table 3−5.

Table 3−6. Bus Holder Control Bits

HPI16 PIN	BH	HBH	D[15−0]	A[17−0]	HD[7−0]
0	0	0	OFF	OFF	OFF
0	0	1	OFF	OFF	ON
0	1	0	ON	OFF	OFF
0	1	1	ON	OFF	ON
1	0	0	OFF	OFF	ON
1	0	1	OFF	ON	ON
1	1	0	ON	OFF	ON
1	1	1	ON	ON	ON

3.7 Parallel I/O Ports

The 5407/5404 has a total of 64K I/O ports. These ports can be addressed by the PORTR instruction or the PORTW instruction. The $\overline{IS}$ signal indicates a read/write operation through an I/O port. The 5407/5404 can interface easily with external devices through the I/O ports while requiring minimal off-chip address-decoding circuits.

3.7.1 Enhanced 8-/16-Bit Host-Port Interface (HPI8/16)

The 5407/5404 host-port interface, also referred to as the HPI8/16, is an enhanced version of the standard 8-bit HPI found on earlier TMS320C54x™ DSPs (542, 545, 548, and 549). The 5407/5404 HPI can be used to interface to an 8-bit or 16-bit host. When the address and data buses for external I/O is not used (to interface to external devices in program/data/IO spaces), the 5407/5404 HPI can be configured as an HPI16 to interface to a 16-bit host. This configuration can be accomplished by connecting the HPI16 pin to logic “1”.

When the HPI16 pin is connected to a logic “0”, the 5407/5404 HPI is configured as an HPI8. The HPI8 is an 8-bit parallel port for interprocessor communication. The features of the HPI8 include:

Standard features:

- Sequential transfers (with autoincrement) or random-access transfers
- Host interrupt and C54x™ interrupt capability
- Multiple data strobes and control pins for interface flexibility

The HPI8 interface consists of an 8-bit bidirectional data bus and various control signals. Sixteen-bit transfers are accomplished in two parts with the HBIL input designating high or low byte. The host communicates with the HPI8 through three dedicated registers — the HPI address register (HPIA), the HPI data register (HPID), and the HPI control register (HPIC). The HPIA and HPID registers are only accessible by the host, and the HPIC register is accessible by both the host and the 5407/5404.

Enhanced features:

- Access to entire on-chip RAM through DMA bus
- Capability to continue transferring during emulation stop

The HPI16 is an enhanced 16-bit version of the TMS320C54x™ DSP 8-bit host-port interface (HPI8). The HPI16 is designed to allow a 16-bit host to access the DSP on-chip memory, with the host acting as the master of the interface. Some of the features of the HPI16 include:

- 16-bit bidirectional data bus
- Multiple data strobes and control signals to allow glueless interfacing to a variety of hosts
- Only nonmultiplexed address/data modes are supported
- 18-bit address bus used in nonmultiplexed mode to allow access to all internal memory (including internal extended address pages)
- HRDY signal to hold off host accesses due to DMA latency
- The HPI16 acts as a slave to a 16-bit host processor and allows access to the on-chip memory of the DSP.

  NOTE: Only the nonmultiplexed mode is supported when the 5407/5404 HPI is configured as a HPI16 (see Figure 3−10).

The 5407/5404 HPI functions as a slave and enables the host processor to access the on-chip memory. A major enhancement to the 5407/5404 HPI over previous versions is that it allows host access to the entire on-chip memory range of the DSP. The host and the DSP both have access to the on-chip RAM at all times and host accesses are always synchronized to the DSP clock. If the host and the DSP contend for access to the same location, the host has priority, and the DSP waits for one cycle. Note that since host accesses are always synchronized to the 5407/5404 clock, an active input clock (CLKIN) is required for HPI accesses during IDLE states, and host accesses are not allowed while the 5407/5404 reset pin is asserted.

3.7.2 HPI Nonmultiplexed Mode

In *nonmultiplexed* mode, a host with separate address/data buses can access the HPI16 data register (HPID) via the HD 16-bit bidirectional data bus, and the address register (HPIA) via the 23-bit HA address bus. The host initiates the access with the strobe signals ($\overline{HDS1}$, $\overline{HDS2}$, $\overline{HCS}$) and controls the direction of the access with the HR/$\overline{W}$ signal. The HPI16 can stall host accesses via the HRDY signal. Note that the HPIC register is not available in *nonmultiplexed* mode since there are no HCNTL signals available. All host accesses initiate a DMA read or write access. Figure 3−10 shows a block diagram of the HPI16 in *nonmultiplexed* mode.

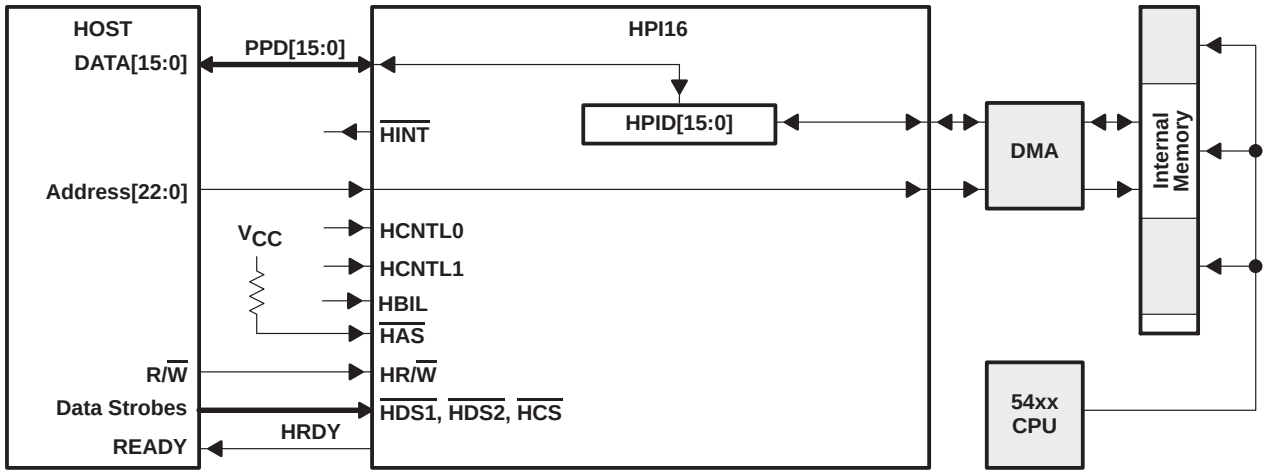
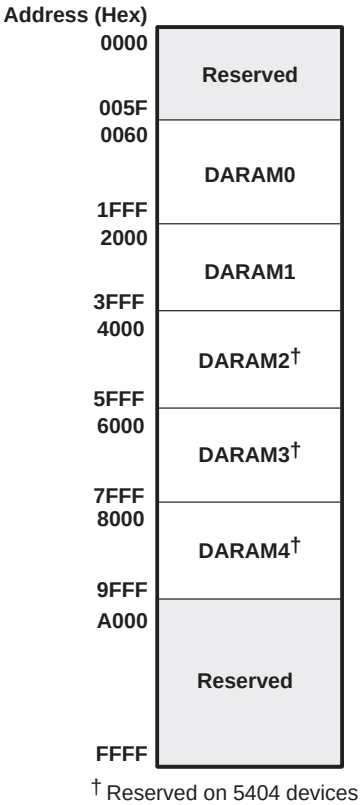


Figure 3−10. Host-Port Interface — Nonmultiplexed Mode



† Reserved on 5404 devices

Figure 3−11. HPI Memory Map

3.8 Multichannel Buffered Serial Ports (McBSPs)

The 5407/5404 device provides three high-speed, full-duplex, multichannel buffered serial ports that allow direct interface to other C54x/LC54x devices, codecs, and other devices in a system. The McBSPs are based on the standard serial-port interface found on other 54x devices. Like their predecessors, the McBSPs provide:

- Full-duplex communication
- Double-buffer data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit

In addition, the McBSPs have the following capabilities:

- Direct interface to:
  - T1/E1 framers
  - MVIP switching compatible and ST-BUS compliant devices
  - IOM-2 compliant devices
  - AC97-compliant devices
  - IIS-compliant devices
  - Serial peripheral interface
- Multichannel transmit and receive of up to 128 channels
- A wide selection of data sizes, including 8, 12, 16, 20, 24, or 32 bits
- μ-law and A-law companding
- Programmable polarity for both frame synchronization and data clocks
- Programmable internal clock and frame generation

The McBSP consists of a data path and control path. The six pins, BDX, BDR, BFSX, BFSR, BCLKX, and BCLKR, connect the control and data paths to external devices. The implemented pins can be programmed as general-purpose I/O pins if they are not used for serial communication. Note that on McBSP2, the transmit and receive clocks and the transmit and receive frame sync have been combined.

The data is communicated to devices interfacing to the McBSP by way of the data transmit (BDX) pin for transmit and the data receive (BDR) pin for receive. The CPU or DMA reads the received data from the data receive register (DRR) and writes the data to be transmitted to the data transmit register (DXR). Data written to the DXR is shifted out to BDX by way of the transmit shift register (XSR). Similarly, receive data on the BDR pin is shifted into the receive shift register (RSR) and copied into the receive buffer register (RBR). RBR is then copied to DRR, which can be read by the CPU or DMA. This allows internal data movement and external data communications simultaneously.

Control information in the form of clocking and frame synchronization is communicated by way of BCLKX, BCLKR, BFSX, and BFSR. The device communicates to the McBSP by way of 16-bit-wide control registers accessible via the internal peripheral bus.

The control block consists of internal clock generation, frame synchronization signal generation, and their control, and multichannel selection. This control block sends notification of important events to the CPU and DMA by way of two interrupt signals, XINT and RINT, and two event signals, XEVT and REVT.

The on-chip companding hardware allows compression and expansion of data in either μ-law or A-law format. When companding is used, transmitted data is encoded according to the specified companding law and received data is decoded to 2s complement format.

The sample rate generator provides the McBSP with several means of selecting clocking and framing for both the receiver and transmitter. Both the receiver and transmitter can select clocking and framing independently.

The McBSP allows the multiple channels to be independently selected for the transmitter and receiver. When multiple channels are selected, each frame represents a time-division multiplexed (TDM) data stream. In using time-division multiplexed data streams, the CPU may only need to process a few of them. Thus, to save memory and bus bandwidth, multichannel selection allows independent enabling of particular channels for transmission and reception. All 128 channels in a bit stream consisting of a maximum of 128 channels can be enabled.

15					10	9	8
Reserved						XMCME	XPBBLK
R						R/W	R/W

7	6	5	4		2	1	0
XPBBLK	XPABLK		XCBLK			XMCM	
R/W	R/W		R			R/W	

LEGEND: R = Read, W = Write

Figure 3−12. Multichannel Control Register (MCR1)

15					10	9	8
Reserved						RMCME	RPBBLK
R						R/W	R/W

7	6	5	4		2	1	0
RPBBLK	RPABLK		RCBLK			Reserved	RMCM
R/W	R/W		R			R	R/W

LEGEND: R = Read, W = Write

Figure 3−13. Multichannel Control Register (MCR2)

The 5407/5404 McBSP has two working modes:

- In the first mode, when (R/X)MCME = 0, it is comparable with the McBSPs used in the 5410 where the normal 32-channel selection is enabled (default).
- In the second mode, when (R/X)MCME = 1, it has 128-channel selection capability. Multichannel control register Bit 9, (R/X)MCME, is used as the 128-channel selection enable bit. Once (R/X)MCME = 1, twelve new registers ((R/X)CERC − (R/X)CERH) are used to enable the 128-channel selection.

The clock stop mode (CLKSTP) in the McBSP provides compatibility with the serial port interface protocol. Clock stop mode works with only single-phase frames and one word per frame. The word sizes supported by the McBSP are programmable for 8-, 12-, 16-, 20-, 24-, or 32-bit operation. When the McBSP is configured to operate in SPI mode, both the transmitter and the receiver operate together as a master or as a slave.

Although the BCLKS pin is not available on the 5407/5404 PGE and GGU packages, the 5407/5404 is capable of synchronization to external clock sources. BCLKX or BCLKR can be used by the sample rate generator for external synchronization. The sample rate clock mode extended (SCLKME) bit field is located in the PCR to accommodate this option.

15	14	13	12	11	10	9	8
Reserved		XIOEN	RIOEN	FSXM	FSRM	CLKXM	CLKRM
R/W		R/W	R/W	R/W	R/W	R/W	R/W

7	6	5	4	3	2	1	0
SCLKME	CLKS STAT	DX STAT	DR STAT	FSXP	FSRP	CLKXP	CLKRP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R = Read, W = Write

Figure 3−14. Pin Control Register (PCR)

The selection of sample rate input clock is made by the combination of the CLKSM (bit 13 in SRGR2) bit value and the SCLKME bit value as shown in Table 3−7.

Table 3−7. Sample Rate Input Clock Selection

SCLKME	CLKSM	SAMPLE RATE CLOCK MODE
0	0	Reserved (CLKS pin unavailable)
0	1	CPU clock
1	0	BCLKR
1	1	BCLKX

When the SCLKME bit is cleared to 0, the CLKSM bit is used, as before, to select either the CPU clock or the CLKS pin (not bonded out on the 5407/5404 device package) as the sample rate input clock. Setting the SCLKME bit to 1 enables the CLKSM bit to select between the BCLKR pin or BCLKX pin for the sample rate input clock.

When either the BCLKR or CLKX is configured this way, the output buffer for the selected pin is automatically disabled. For example, with SCLKME = 1 and CLKSM = 0, the BCLKR pin is configured as the input of the sample rate generator. Both the transmitter and receiver circuits can be synchronized to the sample rate generator output by setting the CLKXM and CLKRM bits of the pin configuration register (PCR) to 1. Note that the sample rate generator output will only be driven on the BCLKX pin since the BCLKR output buffer is automatically disabled.

The McBSP is fully static and operates at arbitrary low clock frequencies. For maximum operating frequency, see Section 5.13.

3.9 Hardware Timers

The 5407/5404 device features two 16-bit timing circuits with 4-bit prescalers. The timer counters are decremented by one every CPU clock cycle. Each time the counter decrements to 0, a timer interrupt is generated. The timer can be stopped, restarted, reset, or disabled by specific status bits.

Both timers can be use to generate interrupts to the CPU, however, the second timer (Timer1) has its interrupt combined with external interrupt 3 ($\overline{INT3}$) in the interrupt flag register. Therefore, to use the Timer1 interrupt, the $\overline{INT3}$ input should be disabled (tied high), and to use the $\overline{INT3}$ input, the timer should be disabled (placed in reset).

Since the Timer1 output is multiplexed externally with the $\overline{HINT}$ output, the HPI must be disabled (HPIENA input pin = 0) if the Timer1 output is to be used. The Timer1 output also has a dedicated enable bit in the General Purpose I/O Control Register (GPIOCR) located at data memory address 003Ch. If the external Timer1 output is to be used, in addition to disabling the HPI, the TOUT1 bit in the GPIOCR must also be set to 1.

3.10 Clock Generator

The clock generator provides clocks to the 5407/5404 device, and consists of a phase-locked loop (PLL) circuit. The clock generator requires a reference clock input, which can be provided from an external clock source. The reference clock input is then divided by two (DIV mode) to generate clocks for the 5407/5404 device, or the PLL circuit can be used (PLL mode) to generate the device clock by multiplying the reference clock frequency by a scale factor, allowing use of a clock source with a lower frequency than that of the CPU. The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal.

When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. Once the PLL is locked, it continues to track and maintain synchronization with the input signal. Then, other internal clock circuitry allows the synthesis of new clock frequencies for use as master clock for the 5407/5404 device.

This clock generator allows system designers to select the clock source. The sources that drive the clock generator are:

- A crystal resonator circuit. The crystal resonator circuit is connected across the X1 and X2/CLKIN pins of the 5407/5404 to enable the internal oscillator.
- An external clock. The external clock source is directly connected to the X2/CLKIN pin, and X1 is left unconnected.

The software-programmable PLL features a high level of flexibility, and includes a clock scaler that provides various clock multiplier ratios, capability to directly enable and disable the PLL, and a PLL lock timer that can be used to delay switching to PLL clocking mode of the device until lock is achieved. Devices that have a built-in software-programmable PLL can be configured in one of two clock modes:

- PLL mode. The input clock (X2/CLKIN) is multiplied by 1 of 31 possible ratios.
- DIV (divider) mode. The input clock is divided by 2 or 4. Note that when DIV mode is used, the PLL can be completely disabled in order to minimize power dissipation.

The software-programmable PLL is controlled using the 16-bit memory-mapped (address 0058h) clock mode register (CLKMD). The CLKMD register is used to define the clock configuration of the PLL clock module. Note that upon reset, the CLKMD register is initialized with a predetermined value dependent only upon the state of the CLKMD1 − CLKMD3 pins. For more programming information, see the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (literature number SPRU131). The CLKMD pin configured clock options are shown in Table 3−8.

Table 3−8. Clock Mode Settings at Reset

CLKMD1	CLKMD2	CLKMD3	CLKMD RESET VALUE	CLOCK MODE†
0	0	0	0000h	1/2 (PLL and oscillator disabled)
0	0	1	9007h	PLL x 10
0	1	0	4007h	PLL x 5
1	0	0	1007h	PLL x 2
1	1	0	F007h	PLL x 1
1	0	1	F000h	1/4 (PLL disabled)
1	1	1	0000h	1/2 (PLL disabled)
0	1	1	—	Reserved

† The external CLKMD1−CLKMD3 pins are sampled to determine the desired clock generation mode while $\overline{RS}$ is low. Following reset, the clock generation mode can be reconfigured by writing to the internal clock mode register in software.

3.11 Enhanced External Parallel Interface (XIO2)

The 5407/5404 external interface has been redesigned to include several improvements, including: simplification of the bus sequence, more immunity to bus contention when transitioning between read and write operations, the ability for external memory access to the DMA controller, and optimization of the power-down modes.

The bus sequence on the 5407/5404 still maintains all of the same interface signals as on previous 54x devices, but the signal sequence has been simplified. Most external accesses now require 3 cycles composed of a leading cycle, an active (read or write) cycle, and a trailing cycle. The leading and trailing cycles provide additional immunity against bus contention when switching between read operations and write operations. To maintain high-speed read access, a consecutive read mode that performs single-cycle reads as on previous 54x devices is available.

Figure 3−15 shows the bus sequence for three cases: all I/O reads, memory reads in nonconsecutive mode, or single memory reads in consecutive mode. The accesses shown in Figure 3−15 always require 3 CLKOUT cycles to complete.

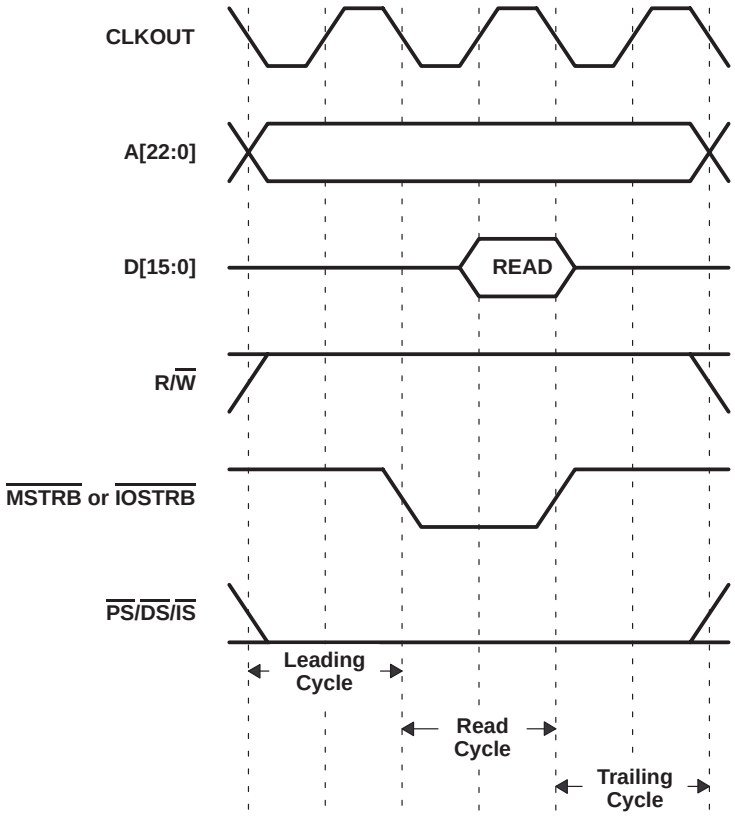


Figure 3−15. Nonconsecutive Memory Read and I/O Read Bus Sequence

Figure 3−16 shows the bus sequence for repeated memory reads in consecutive mode. The accesses shown in Figure 3−16 require (2+n) CLKOUT cycles to complete, where n is the number of consecutive reads performed.

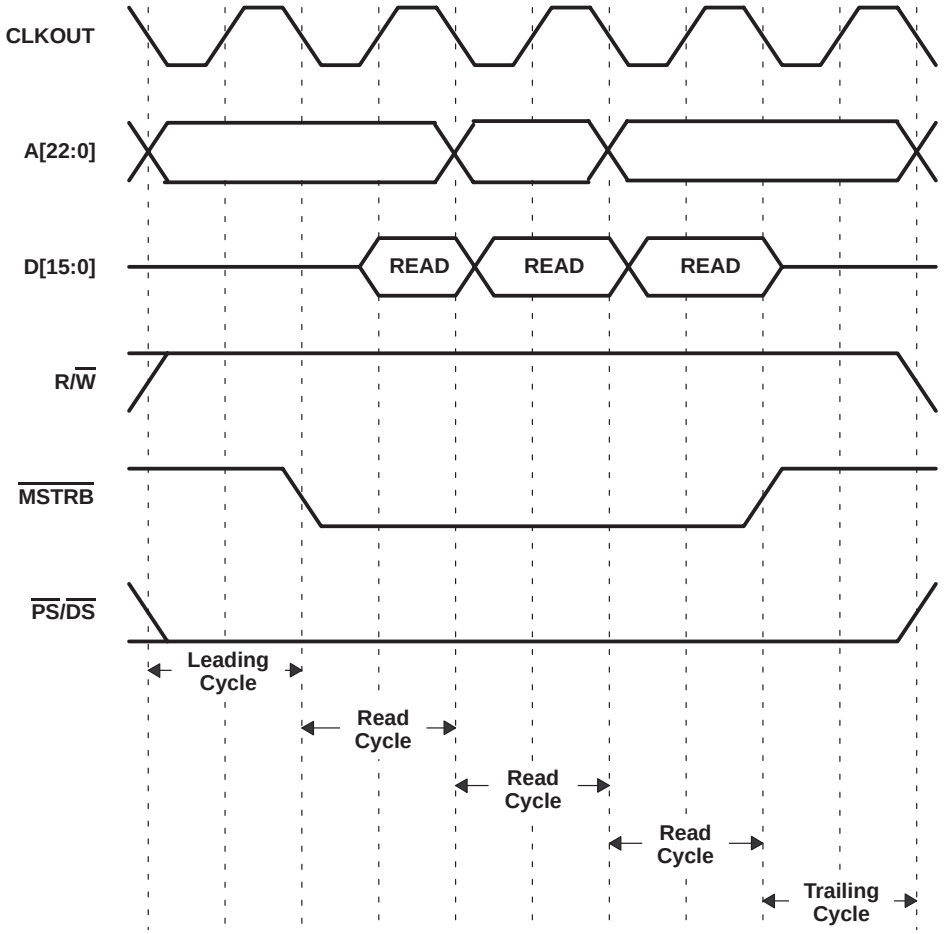


Figure 3−16. Consecutive Memory Read Bus Sequence (n = 3 reads)

Figure 3−17 shows the bus sequence for all memory writes and I/O writes. The accesses shown in Figure 3−17 always require 3 CLKOUT cycles to complete.

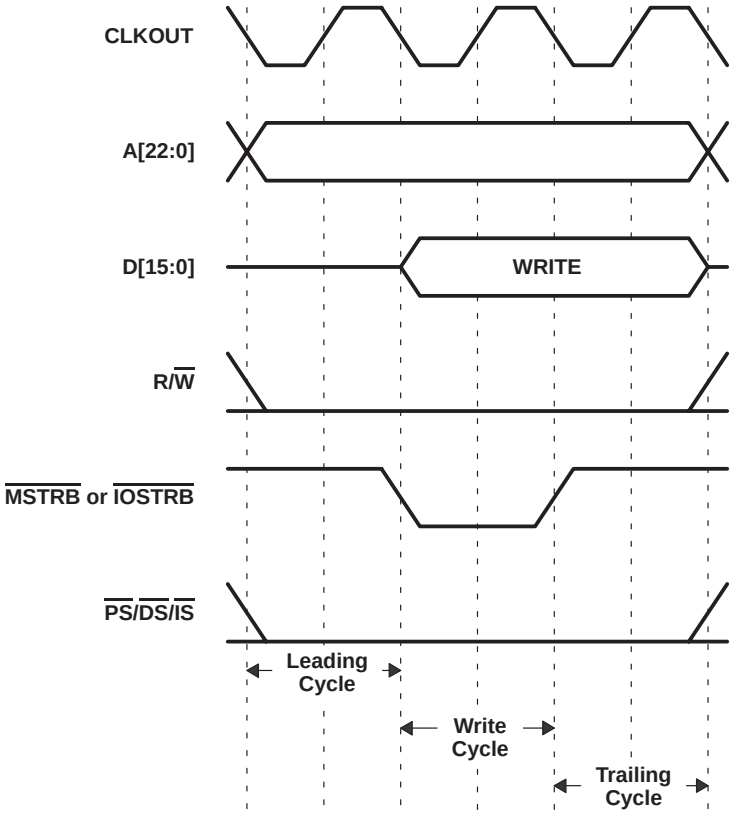


Figure 3−17. Memory Write and I/O Write Bus Sequence

The enhanced interface also provides the ability for DMA transfers to extend to external memory. For more information on DMA capability, see the DMA sections that follow.

The enhanced interface improves the low-power performance already present on the TMS320C5000™ DSP platform by switching off the internal clocks to the interface when it is not being used. This power-saving feature is automatic, requires no software setup, and causes no latency in the operation of the interface.

Additional features integrated in the enhanced interface are the ability to automatically insert bank-switching cycles when crossing 32K memory boundaries (see Section 3.6.2), the ability to program up to 14 wait states through software (see Section 3.6.1), and the ability to divide down CLKOUT by a factor of 1, 2, 3, or 4. Dividing down CLKOUT provides an alternative to wait states when interfacing to slower external memory or peripheral devices. While inserting wait states extends the bus sequence during read or write accesses, it does not slow down the bus signal sequences at the beginning and the end of the access. Dividing down CLKOUT provides a method of slowing the entire bus sequence when necessary. The CLKOUT divide-down factor is controlled through the DIVFCT field in the bank-switching control register (BSCR) (see Table 3−5).

3.12 DMA Controller

The 5407/5404 direct memory access (DMA) controller transfers data between points in the memory map without intervention by the CPU. The DMA allows movements of data to and from internal program/data memory, internal peripherals (such as the McBSPs, but not the UART), or external memory devices to occur in the background of CPU operation. The DMA has six independent programmable channels, allowing six different contexts for DMA operation.

TMS320C5000 is a trademark of Texas Instruments.

3.12.1 Features

The DMA has the following features:

- The DMA operates independently of the CPU.
- The DMA has six channels. The DMA can keep track of the contexts of six independent block transfers.
- The DMA has higher priority than the CPU for both internal and external accesses.
- Each channel has independently programmable priorities.
- Each channel's source and destination address registers can have configurable indexes through memory on each read and write transfer, respectively. The address may remain constant, be post-incremented, be post-decremented, or be adjusted by a programmable value.
- Each read or write internal transfer may be initialized by selected events.
- On completion of a half- or entire-block transfer, each DMA channel may send an interrupt to the CPU.
- The DMA can perform double-word internal transfers (a 32-bit transfer of two 16-bit words).

3.12.2 DMA External Access

The 5407/5404 DMA supports external accesses to extended program, extended data, and extended I/O memory. These overlay pages are only visible to the DMA controller. A maximum of two DMA channels can be used for external memory accesses. The DMA external accesses require a minimum of 8 cycles for external writes and a minimum of 11 cycles for external reads assuming the XIO02 is in consecutive mode ($\overline{\text{CONSEC}}$ = 1), wait state is set to two, and CLKOUT is not divided (DIVFCT = 00).

The control of the bus is arbitrated between the CPU and the DMA. While the DMA or CPU is in control of the external bus, the other will be held-off via wait states until the current transfer is complete. The DMA takes precedence over XIO requests.

- Only two channels are available for external accesses. (One for external reads and one for external writes.)
- Single-word (16-bit) transfers are supported for external accesses.
- The DMA does not support transfers from the peripherals to external memory.
- The DMA does not support transfers from external memory to the peripherals.
- The DMA does not support external-to-external transfers.
- The DMA does not support synchronized external transfers.

15	14	13	12	11	10		8
AUTOINIT	DINM	IMOD	CTMOD	SLAXS	SIND		
7	6	5	4		2	1	0
DMS		DLAXS	DIND			DMD	

Figure 3−18. DMA Transfer Mode Control Register (DMMCRn)

These new bit fields were created to allow the user to define the space-select for the DMA (internal/external). Also, a new extended destination data page (XDSTDP[6:0], subaddress 029h) and extended source data page (XSRCDP[6:0], subaddress 028h) have been created. The functions of the DLAXS and SLAXS bits are as follows:

DLAXS(DMMCRn[5]) Destination	0 = No external access (default internal)
	1 = External access
SLAXS(DMMCRn[11]) Source	0 = No external access (default internal)
	1 = External access

Table 3−9 lists the DMD bit values and their corresponding destination space.

Table 3−9. DMD Section of the DMMCRn Register

DMD	DESTINATION SPACE
00	PS
01	DS
10	I/O
11	Reserved

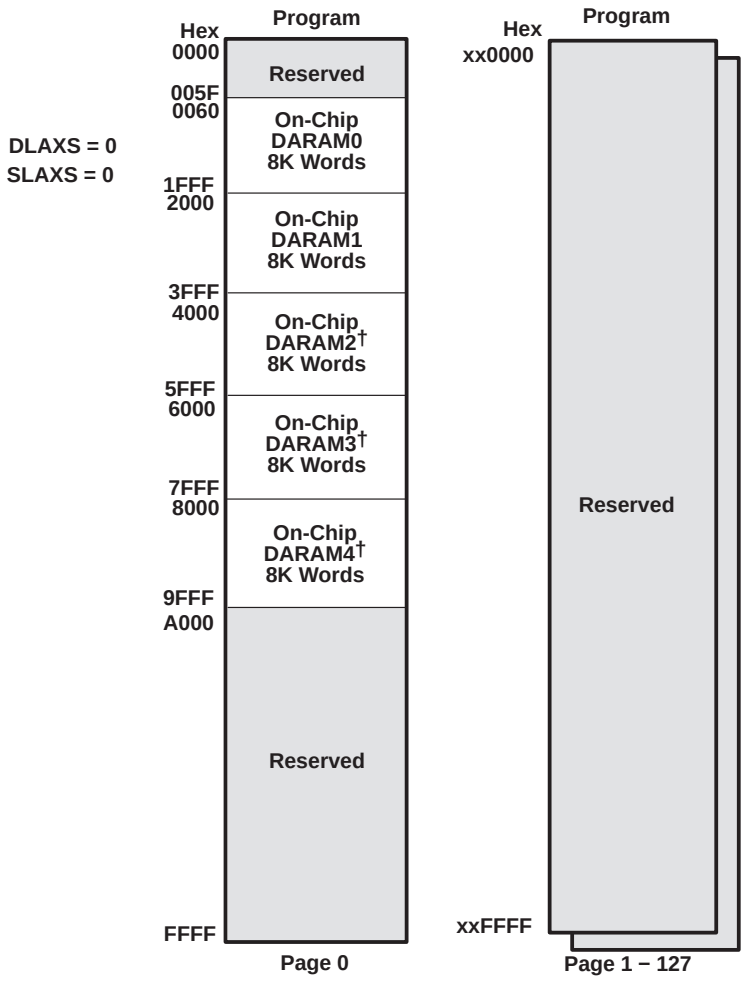
For the CPU external access, software can configure the memory cells to reside inside or outside the program address map. When the cells are mapped into program space, the device automatically accesses them when their addresses are within bounds. When the address generation logic generates an address outside its bounds, the device automatically generates an external access.

Two new registers are added to the 5407/5404 DMA to support DMA accesses to/from DMA extended data memory, page 1 to page 127.

- The DMA extended source data page register (XSRCDP[6:0]) is located at subbank address 028h.
- The DMA extended destination data page register (XDSTDP[6:0]) is located at subbank address 029h.

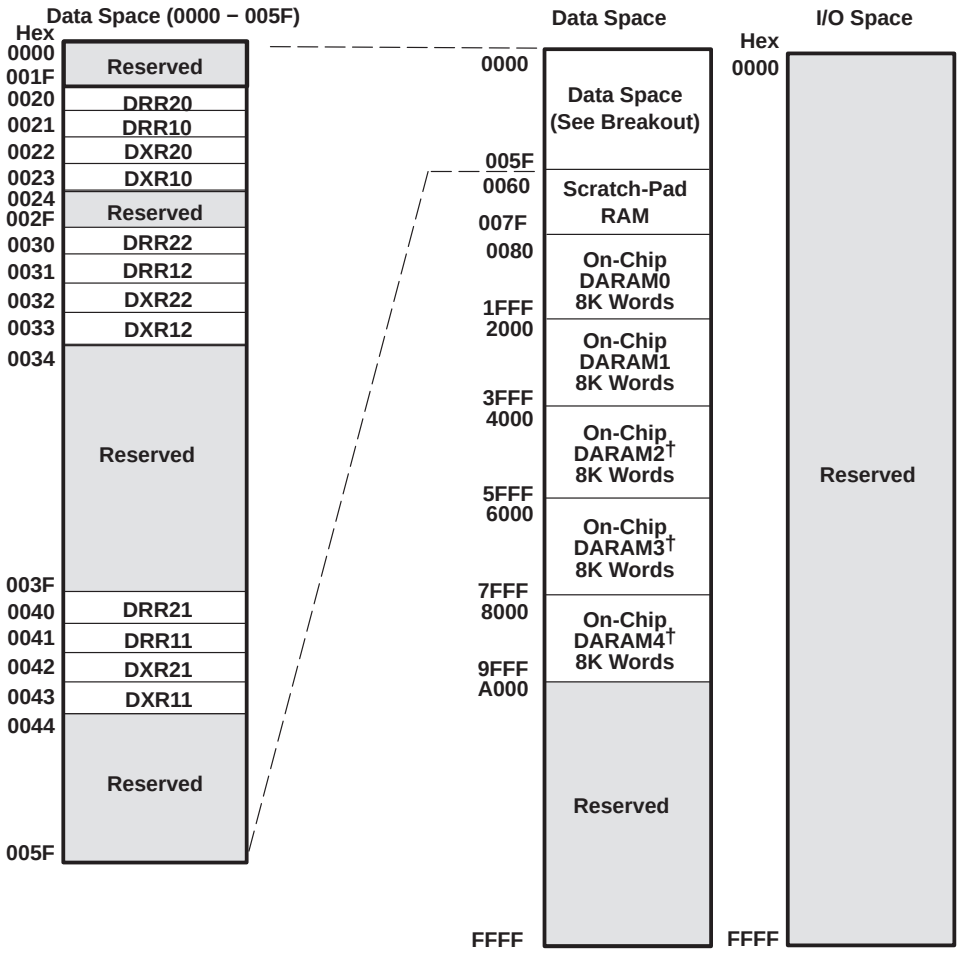
3.12.3 DMA Memory Map

The DMA memory map, shown in Figure 3−19, allows the DMA transfer to be unaffected by the status of the MP/$\overline{\text{MC}}$, DROM, and OVLY bits.



† Reserved on the 5404

Figure 3−19. On-Chip DMA Memory Map for Program Space (DLAXS = 0 and SLAXS = 0)



† Reserved on the 5404

Figure 3−20. On-Chip DMA Memory Map for Data and IO Space (DLAXS = 0 and SLAXS = 0)

3.12.4 DMA Priority Level

Each DMA channel can be independently assigned high- or low-priority relative to each other. Multiple DMA channels that are assigned to the same priority level are handled in a round-robin manner.

3.12.5 DMA Source/Destination Address Modification

The DMA provides flexible address-indexing modes for easy implementation of data management schemes such as autobuffering and circular buffers. Source and destination addresses can be indexed separately and can be post-incremented, post-decremented, or post-incremented with a specified index offset.

3.12.6 DMA in Autoinitialization Mode

The DMA can automatically reinitialize itself after completion of a block transfer. Some of the DMA registers can be preloaded for the next block transfer through the DMA reload registers (DMGSA, DMGDA, DMGCR, and DMGFR). Autoinitialization allows:

- Continuous operation: Normally, the CPU would have to reinitialize the DMA immediately after the completion of the current block transfers, but with the reload registers, it can reinitialize these values for the next block transfer any time after the current block transfer begins.
- Repetitive operation: The CPU does not preload the reload register with new values for each block transfer but only loads them on the first block transfer.

The 5407/5404 DMA has been enhanced to expand the DMA reload register sets. Each DMA channel now has its own DMA reload register set. For example, the DMA reload register set for channel 0 has DMGSA0, DMGDA0, DMGCR0, and DMGFR0 while DMA channel 1 has DMGSA1, DMGDA1, DMGCR1, and DMGFR1, etc.

To utilize the additional DMA reload registers, the AUTOIX bit is added to the DMPREC register as shown in Figure 3−21.

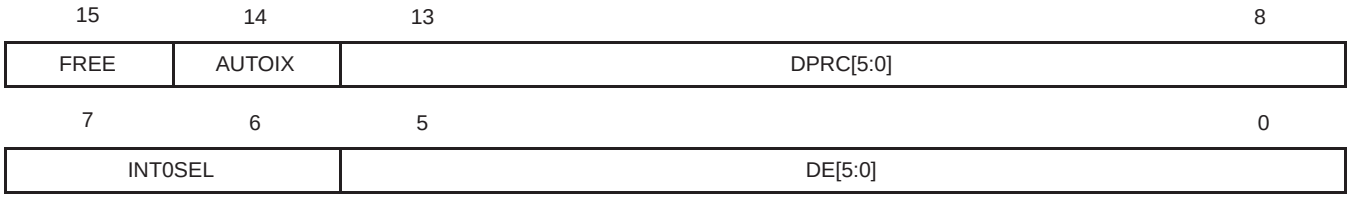


Figure 3−21. DMPREC Register

Table 3−10. DMA Reload Register Selection

AUTOIX	DMA RELOAD REGISTER USAGE IN AUTO INIT MODE
0 (default)	All DMA channels use DMGSA0, DMGDA0, DMGCR0 and DMGFR0
1	Each DMA channel uses its own set of reload registers

3.12.7 DMA Transfer Counting

The DMA channel element count register (DMCTRx) and the frame count register (DMFRCx) contain bit fields that represent the number of frames and the number of elements per frame to be transferred.

- Frame count. This 8-bit value defines the total number of frames in the block transfer. The maximum number of frames per block transfer is 128 (FRAME COUNT= 0FFh). The counter is decremented upon the last read transfer in a frame transfer. Once the last frame is transferred, the selected 8-bit counter is reloaded with the DMA global frame reload register (DMGFR) if the AUTOINIT bit is set to 1. A frame count of 0 (default value) means the block transfer contains a single frame.
- Element count. This 16-bit value defines the number of elements per frame. This counter is decremented after the read transfer of each element. The maximum number of elements per frame is 65536 (DMCTRn = 0FFFFh). In autoinitialization mode, once the last frame is transferred, the counter is reloaded with the DMA global count reload register (DMGCR).

3.12.8 DMA Transfer in Doubleword Mode

Doubleword mode allows the DMA to transfer 32-bit words in any index mode. In doubleword mode, two consecutive 16-bit transfers are initiated and the source and destination addresses are automatically updated following each transfer. In this mode, each 32-bit word is considered to be one element.

3.12.9 DMA Channel Index Registers

The particular DMA channel index register is selected by way of the SIND and DIND fields in the DMA transfer mode control register (DMMCRn). Unlike basic address adjustment, in conjunction with the frame index DMFRI0 and DMFRI1, the DMA allows different adjustment amounts depending on whether or not the element transfer is the last in the current frame. The normal adjustment value (element index) is contained in the element index registers DMIDX0 and DMIDX1. The adjustment value (frame index) for the end of the frame, is determined by the selected DMA frame index register, either DMFRI0 or DMFRI1.

The element index and the frame index affect address adjustment as follows:

- Element index: For all except the last transfer in the frame, the element index determines the amount to be added to the DMA channel for the source/destination address register (DMSRCx/DMDSTx) as selected by the SIND/DIND bits.

- Frame index: If the transfer is the last in a frame, frame index is used for address adjustment as selected by the SIND/DIND bits. This occurs in both single-frame and multi-frame transfers.

3.12.10 DMA Interrupts

The ability of the DMA to interrupt the CPU based on the status of the data transfer is configurable and is determined by the IMOD and DINM bits in the DMA transfer mode control register (DMMCRn). The available modes are shown in Table 3−11.

Table 3−11. DMA Interrupts

MODE	DINM	IMOD	INTERRUPT
ABU (non-decrement)	1	0	At full buffer only
ABU (non-decrement)	1	1	At half buffer and full buffer
Multi frame	1	0	At block transfer complete (DMCTRn = DMSEFCn[7:0] = 0)
Multi frame	1	1	At end of frame and end of block (DMCTRn = 0)
Either	0	X	No interrupt generated
Either	0	X	No interrupt generated

3.12.11 DMA Controller Synchronization Events

The transfers associated with each DMA channel can be synchronized to one of several events. The DSYN bit field of the DMSEFCn register selects the synchronization event for a channel. The list of possible events and the DSYN values are shown in Table 3−12.

Table 3−12. DMA Synchronization Events

DSYN VALUE	DMA SYNCHRONIZATION EVENT
0000b	No synchronization used
0001b	McBSP0 receive event
0010b	McBSP0 transmit event
0011b	McBSP2 receive event
0100b	McBSP2 transmit event
0101b	McBSP1 receive event
0110b	McBSP1 transmit event
0111b	UART†
1000b	Reserved
1001b	Reserved
1010b	Reserved
1011b	Reserved
1100b	Reserved
1101b	Timer 0 interrupt event
1110b	External interrupt 3
1111b	Timer 1 interrupt event

† Note that the UART DMA synchronization event is usable as a synchronization event only, and is not usable for transferring data to or from the UART. The DMA cannot be used to transfer data to or from the UART.

The DMA controller can generate a CPU interrupt for each of the six channels. However, due to a limit on the number of internal CPU interrupt inputs, channels 0, 1, 2, and 3 are multiplexed with other interrupt sources. DMA channels 0, 1, 2, and 3 share an interrupt line with the receive and transmit portions of the McBSP. When the 5407/5404 is reset, the interrupts from these three DMA channels are deselected. The INT0SEL bit field in the DMPREC register can be used to select these interrupts, as shown in Table 3−13.

Table 3−13. DMA/CPU Channel Interrupt Selection

INT0SEL VALUE	IMR/IFR[6]	IMR/IFR[7]	IMR/IFR[10]	IMR/IFR[11]
00b (reset)	BRINT2	BXINT2	BRINT1	BXINT1
01b	BRINT2	BXINT2	DMAC2	DMAC3
10b	DMAC0	DMAC1	DMAC2	DMAC3
11b	Reserved			

3.13 Universal Asynchronous Receiver/Transmitter (UART)

The UART peripheral is based on the industry-standard TL16C550B asynchronous communications element, which in turn is a functional upgrade of the TL16C450. Functionally similar to the TL16C450 on power up (character or TL16C450 mode), the UART can be placed in an alternate FIFO (TL16C550) mode. This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status per byte for the receiver FIFO.

The UART performs serial-to-parallel conversions on data received from a peripheral device or modem and parallel-to-serial conversion on data received from the CPU. The CPU can read the UART status at any time. The UART includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The UART includes a programmable baud rate generator capable of dividing the CPU clock by divisors from 1 to 65535 and producing a 16× reference clock for the internal transmitter and receiver logic. See Section 5.15 for detailed timing specifications for the UART.

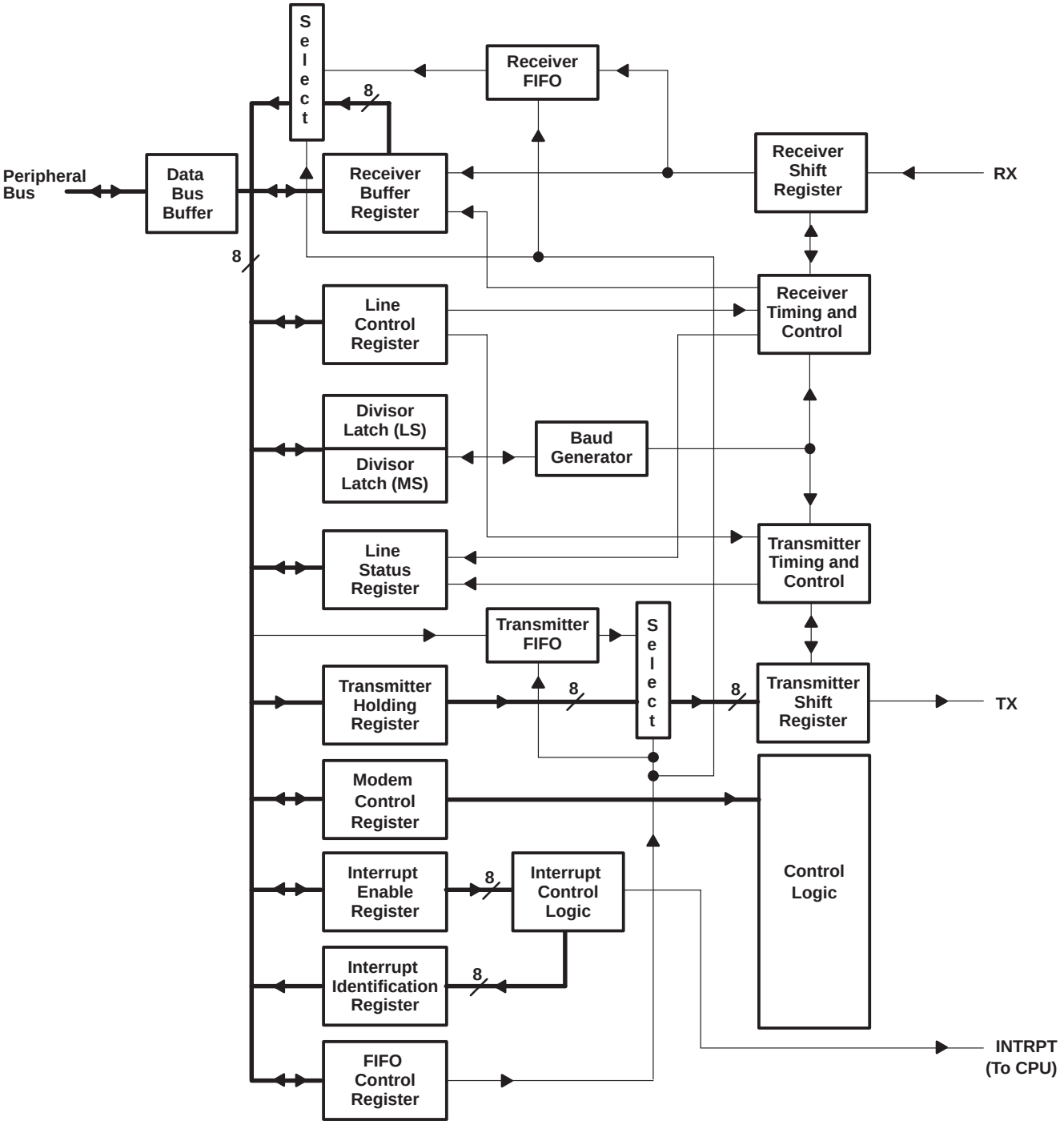


Figure 3−22. UART Functional Block Diagram

Table 3−14. UART Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt enable register	Master reset	All bits cleared (0−3 forced and 4−7 permanent)
Interrupt identification register	Master reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 are cleared, and bits 4−5 are permanently cleared
FIFO control register	Master reset	All bits cleared
Line control register	Master reset	All bits cleared
Modem control register	Master reset	All bits cleared (6−7 permanent)
Line status register	Master reset	Bits 5 and 6 are set; all other bits are cleared
Reserved register	Master reset	Indeterminate
SOUT	Master reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/write THR/MR	Low
Scratch register	Master reset	No effect
Divisor latch (LSB and MSB) registers	Master reset	No effect
Receiver buffer register	Master reset	No effect
Transmitter holding register	Master reset	No effect
RCVR FIFO	MR/FCR1−FCR0/ΔFCR0	All bits cleared
XMIT FIFO	MR/FCR2−FCR0/ΔFCR0	All bits cleared

3.13.1 UART Accessible Registers

The system programmer has access to and control over any of the UART registers that are summarized in Table 3−14. These registers control UART operations, receive data, and transmit data. Descriptions of these registers follow Table 3−15. See Table 3−24 for more information on peripheral memory mapped registers.

Table 3−15. Summary of Accessible Registers

BIT NO.	UART SUBBANK ADDRESS											
	0 (DLAB = 0)	0 (DLAB = 0)	0 (DLAB = 1) OR 8	1 (DLAB = 0)	1 (DLAB = 1) OR 9	2	2	3	4	5	6	7
	RECEIVER BUFFER REGISTER (READ ONLY)	TRANSMITTER HOLDING REGISTER (WRITE ONLY)	DIVISOR LATCH (LSB)	INTERRUPT ENABLE REGISTER	DIVISOR LATCH (MSB)	INTERRUPT IDENT. REGISTER (READ ONLY)	FIFO CONTROL REGISTER (WRITE ONLY)	LINE CONTROL REGISTER	MODEM CONTROL REGISTER	LINE STATUS REGISTER	RESERVED REGISTER	SCRATCH REGISTER
	RBR	THR	DLL	IER	DLM	IIR	FCR	LCR	MCR	LSR	RSV	SCR
0	Data Bit 0†	Data Bit 0	Bit 0	Enable Received Data Available Interrupt (ERBI)	Bit 8	0 if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	X	Data Ready (DR)	X	Bit 0
1	Data Bit 1	Data Bit 1	Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Bit 9	Interrupt ID Bit 1	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	X	Overrun Error (OE)	X	Bit 1
2	Data Bit 2	Data Bit 2	Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Bit 10	Interrupt ID Bit 2	Transmitter FIFO Reset	Number of Stop Bits (STB)	X	Parity Error (PE)	X	Bit 2
3	Data Bit 3	Data Bit 3	Bit 3	0‡	Bit 11	Interrupt ID Bit 3§	0‡	Parity Enable (PEN)	X	Framing Error (FE)	X	Bit 3
4	Data Bit 4	Data Bit 4	Bit 4	0	Bit 12	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	X	Bit 4
5	Data Bit 5	Data Bit 5	Bit 5	0	Bit 13	0	Reserved	Stick Parity	0‡	Transmitter Holding Register (THRE)	X	Bit 5
6	Data Bit 6	Data Bit 6	Bit 6	0	Bit 14	FIFOs Enabled§	Receiver Trigger (LSB)	Break Control	0	Transmitter Empty (TEMT)	X	Bit 6
7	Data Bit 7	Data Bit 7	Bit 7	0	Bit 15	FIFOs Enabled§	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO§	X	Bit 7
8 − 15	0	0	0	0	0	0	0	0	0	0	0	0

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
‡ Must always be written as zero.
§ These bits are always 0 in the TL16C450 mode.
NOTE: X = Don't care for write, indeterminate on read.

3.13.2 FIFO Control Register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables and clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signalling.

- Bit 0: This bit, when set, enables the transmitter and receiver FIFOs. Bit 0 must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: This bit, when set, clears all bytes in the receiver FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 2: This bit, when set, clears all bytes in the transmit FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bits 3, 4, and 5: These three bits are reserved for future use.
- Bits 6 and 7: These two bits set the trigger level for the receiver FIFO interrupt (see Table 3−16).

Table 3−16. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

3.13.3 FIFO Interrupt Mode Operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1, IER2 = 1), a receiver interrupt occurs as follows:

1. The received data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06) has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set when a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled:

1. FIFO time-out interrupt occurs if the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO has occurred more than four continuous character times before. This causes a maximum character received command to interrupt an issued delay of 160 ms at a 300 baud rate with a 12-bit character.
2. Character times are calculated by using the RCLK input for a clock signal (makes the delay proportional to the baud rate).

3. When a time-out interrupt has occurred, it is cleared and the timer is cleared when the microprocessor reads one character from the receiver FIFO.
4. When a time-out interrupt has not occurred, the time-out timer is cleared after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmitter FIFO and THRE interrupt are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The transmitter holding register empty interrupt [IIR (3−0) = 2] occurs when the transmit FIFO is empty. It is cleared [IIR (3−0) = 1] when the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmitter holding register empty interrupt is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmitter FIFO at the same time since the last time that the FIFO was empty. The first transmitter interrupt after changing FCR0 is immediate if it is enabled.

3.13.4 FIFO Polled Mode Operation

With FCR0 = 1 (transmitter and receiver FIFOs enabled), clearing IER0, IER1, IER2, IER3, or all four to 0 puts the UART in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks receiver and transmitter status using the LSR. As stated previously:

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 − LSR4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode; the IIR is not affected since IER2 = 0.
- LSR5 indicates when the THR is empty.
- LSR6 indicates that both the THR and TSR are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or time-out condition indicated in the FIFO polled mode. However, the receiver and transmitter FIFOs are still fully capable of holding characters.

3.13.5 Interrupt Enable Register (IER)

The IER enables each of the five types of interrupts (refer to Table 3−17) and enables INTRPT in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 3−15 and are described in the following bullets.

- Bit 0: When set, this bit enables the received data available interrupt.
- Bit 1: When set, this bit enables the THRE interrupt.
- Bit 2: When set, this bit enables the receiver line status interrupt.
- Bits 3 through 7: These bits are not used

3.13.6 Interrupt Identification Register (IIR)

The UART has an on-chip interrupt generation and prioritization capability that permits flexible communication with the CPU.

The UART provides three prioritized levels of interrupts:

- Priority 1 − Receiver line status (highest priority)
- Priority 2 − Receiver data ready or receiver character time-out
- Priority 3 − Transmitter holding register empty

When an interrupt is generated, the IIR indicates that an interrupt is pending and encodes the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3−15 and described in Table 3−17. Detail on each bit is as follows:

- Bit 0: This bit is used either in a hardwire prioritized or polled interrupt system. When bit 0 is cleared, an interrupt is pending If bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 3−15
- Bit 3: This bit is always cleared in TL16C450 mode. In FIFO mode, bit 3 is set with bit 2 to indicate that a time-out interrupt is pending.
- Bits 4 and 5: These two bits are not used (always cleared).
- Bits 6 and 7: These bits are always cleared in TL16C450 mode. They are set when bit 0 of the FIFO control register is set.

Table 3−17. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error, or break interrupt	Read the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode	Read the receiver buffer register
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time	Read the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Read the interrupt identification register (if source of interrupt) or writing into the transmitter holding register

3.13.7 Line Control Register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3−15 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 3−18.

Table 3−18. Serial Character Word Length

BIT 1	BIT 0	WORD LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit regardless of the number of stop bits selected. The number of stop bits generated in relation to word length and bit 2 are shown in Table 3−19.

Table 3−19. Number of Stop Bits Generated

BIT 2	WORD LENGTH SELECTED BY BITS 1 AND 2	NUMBER OF STOP BITS GENERATED
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set even parity (an even number of logic 1s in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This bit is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. If bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition; i.e., a condition where SOUT is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic; it only effects SOUT.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

3.13.8 Line Status Register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3−15 and described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. DR is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. DR is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1‡: This bit is the overrun error (OE) indicator. When OE is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. OE is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.
- Bit 2‡: This bit is the parity error (PE) indicator. When PE is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). PE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.
- Bit 3‡: This bit is the framing error (FE) indicator. When FE is set, it indicates that the received character did not have a valid (set) stop bit. FE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The UART samples this start bit twice and then accepts the input data.

† The line status register is intended for read operations only; writing to this register is not recommended.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

- Bit 4‡: This bit is the break interrupt (BI) indicator. When BI is set, it indicates that the received data input was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state for at least two RCLK samples and then receives the next valid start bit.
- Bit 5: This bit is the THRE indicator. THRE is set when the THR is empty, indicating that the UART is ready to accept a new character. If the THRE interrupt is enabled when THRE is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. THRE is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, THRE is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. TEMT bit is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, TEMT is cleared. In the FIFO mode, TEMT is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C550C mode, this bit is always cleared. In the TL16C450 mode, this bit is always cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

3.13.9 Modem Control Register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device. On the UART peripheral, only one bit is active in this register

- Bit 4: This bit (LOOP) provides a local loop back feature for diagnostic testing of the UART. When LOOP is set, the following occurs:
  - The transmitter SOUT is set high.
  - The receiver SIN is disconnected.
  - The output of the TSR is looped back into the receiver shift register input.

3.13.10 Programmable Baud Generator

The UART contains a programmable baud generator that takes a clock input in the range between DC and 16 MHz and divides it by a divisor in the range between 1 and ($2^{16}-1$). The output frequency of the baud generator is sixteen times (16×) the baud rate. The formula for the divisor is:

divisor = XIN frequency input ÷ (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the UART in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Table 3−20 and Table 3−21 illustrate the use of the baud generator with clock frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38.4 kbits/s and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected clock frequency.

‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

NOTE: The clock rates in Table 3−20 and Table 3−21 are shown, for example only, to illustrate the relationship of clock rate and divisor value, to baud rate and baud rate error. Typically, higher clock rates will normally be used, and error values will differ accordingly.

Table 3−20. Baud Rates Using a 1.8432-MHz Clock

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

Table 3−21. Baud Rates Using a 3.072-MHz Clock

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

3.13.10.1 Receiver Buffer Register (RBR)

The UART receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is supplied by the 16× receiver clock. Receiver section control is a function of the UART line control register.

The UART RSR receives serial data from SIN. The RSR then concatenates the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled (IER0 = 1), an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

3.13.10.2 Scratch Register

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other UART operation.

3.13.10.3 Transmitter Holding Register (THR)

The UART transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Transmitter section control is a function of the UART line control register.

The UART THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at SOUT. In the TL16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled (IER1 = 1), an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

3.14 General-Purpose I/O Pins

In addition to the standard $\overline{\text{BIO}}$ and XF pins, the 5407/5404 has pins that can be configured for general-purpose I/O. These pins are:

- 16 McBSP pins — BCLKX0/1, BCLKR0/1, BDR0/1/2, BFSX0/1, BFSR0/1, BDX0/1/2, BCLKRX2, BFSRX2
- 8 HPI data pins — HD0−HD7

The general-purpose I/O function of these pins is only available when the primary pin function is not required.

3.14.1 McBSP Pins as General-Purpose I/O

When the receive or transmit portion of a McBSP is in reset, its pins can be configured as general-purpose inputs or outputs. For more details on this feature, see Section 3.8.

3.14.2 HPI Data Pins as General-Purpose I/O

The 8-bit bidirectional data bus of the HPI can be used as general-purpose input/output (GPIO) pins when the HPI is disabled (HPIENA = 0) or when the HPI is used in HPI16 mode (HPI16 = 1). Two memory-mapped registers are used to control the GPIO function of the HPI data pins — the general-purpose I/O control register (GPIOCR) and the general-purpose I/O status register (GPIOSR). The GPIOCR is shown in Figure 3−23.

15	14						8
TOUT1	Reserved						
R/W-0	0						

7			4	3			0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read, W = Write, *n* = *value after reset*

Figure 3−23. General-Purpose I/O Control Register (GPIOCR) [MMR Address 003Ch]

The direction bits (DIRx) are used to configure HD0−HD7 as inputs or outputs (0 = input, 1 = output).

Bit 15 of the GPIOCR is also used as the Timer1 output enable bit, TOUT1. The TOUT1 bit enables or disables the Timer1 output on the $\overline{\text{HINT}}$/TOUT1 pin. If TOUT1 = 0, the Timer1 output is not available externally; if TOUT1 = 1, the Timer1 output is driven on the $\overline{\text{HINT}}$/TOUT1 pin. Note also that the Timer1 output is only available when the HPI is disabled (HPIENA input pin = 0).

The status of the GPIO pins can be monitored using the bits of the GPIOSR. The GPIOSR is shown in Figure 3−24. When read, these bits reflect the state of the input pins, and when written, determine the state of outputs.

15							8
Reserved							
0							

7			4	3			0
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read, W = Write, *n* = *value after reset*

Figure 3−24. General-Purpose I/O Status Register (GPIOSR) [MMR Address 003Dh]

3.15 Device ID Register

A read-only memory-mapped register has been added to the 5407/5404 to allow user application software to identify on which device the program is being executed.

15							8
Chip ID							
R							

7			4	3			0
Chip Revision				SUBSYSID			
R				R			

LEGEND: R = Read, W = Write

Figure 3−25. Device ID Register (CSIDR) [MMR Address 003Eh]

Table 3−22. Device ID Register (CSIDR) Field Descriptions

BIT	FIELD	DESCRIPTION
15−8	Chip ID	Chip identification (hex code of 06 for 5407 and 03 for 5404)
7−4	Chip Revision	Chip revision identification
3−0	SUBSYSID	Subsystem identification (0000b for single core devices)

3.16 Memory-Mapped Registers

The 5407/5404 has 27 memory-mapped CPU registers, which are mapped in data memory space address 0h to 1Fh. Each 5407/5404 device also has a set of memory-mapped registers associated with peripherals. Table 3−23 gives a list of CPU memory-mapped registers (MMRs) available on 5407/5404. Table 3−24 shows additional peripheral MMRs associated with the 5407/5404.

Table 3−23. CPU Memory-Mapped Registers

NAME	ADDRESS		DESCRIPTION
	DEC	HEX	
IMR	0	0	Interrupt mask register
IFR	1	1	Interrupt flag register
—	2−5	2−5	Reserved for testing
ST0	6	6	Status register 0
ST1	7	7	Status register 1
AL	8	8	Accumulator A low word (15−0)
AH	9	9	Accumulator A high word (31−16)
AG	10	A	Accumulator A guard bits (39−32)
BL	11	B	Accumulator B low word (15−0)
BH	12	C	Accumulator B high word (31−16)
BG	13	D	Accumulator B guard bits (39−32)
TREG	14	E	Temporary register
TRN	15	F	Transition register
AR0	16	10	Auxiliary register 0
AR1	17	11	Auxiliary register 1
AR2	18	12	Auxiliary register 2
AR3	19	13	Auxiliary register 3
AR4	20	14	Auxiliary register 4
AR5	21	15	Auxiliary register 5
AR6	22	16	Auxiliary register 6
AR7	23	17	Auxiliary register 7
SP	24	18	Stack pointer register
BK	25	19	Circular buffer size register
BRC	26	1A	Block repeat counter
RSA	27	1B	Block repeat start address
REA	28	1C	Block repeat end address
PMST	29	1D	Processor mode status (PMST) register
XPC	30	1E	Extended program page register
—	31	1F	Reserved

Table 3−24. Peripheral Memory-Mapped Registers for Each DSP Subsystem

NAME	ADDRESS DEC	ADDRESS HEX	DESCRIPTION
DRR20	32	20	McBSP 0 Data Receive Register 2
DRR10	33	21	McBSP 0 Data Receive Register 1
DXR20	34	22	McBSP 0 Data Transmit Register 2
DXR10	35	23	McBSP 0 Data Transmit Register 1
TIM	36	24	Timer 0 Register
PRD	37	25	Timer 0 Period Register
TCR	38	26	Timer 0 Control Register
—	39	27	Reserved
SWWSR	40	28	Software Wait-State Register
BSCR	41	29	Bank-Switching Control Register
—	42	2A	Reserved
SWCR	43	2B	Software Wait-State Control Register
HPIC	44	2C	HPI Control Register (HMODE = 0 only)
—	45−47	2D−2F	Reserved
DRR22	48	30	McBSP 2 Data Receive Register 2
DRR12	49	31	McBSP 2 Data Receive Register 1
DXR22	50	32	McBSP 2 Data Transmit Register 2
DXR12	51	33	McBSP 2 Data Transmit Register 1
SPSA2	52	34	McBSP 2 Subbank Address Register†
SPSD2	53	35	McBSP 2 Subbank Data Register†
—	54−55	36−37	Reserved
SPSA0	56	38	McBSP 0 Subbank Address Register†
SPSD0	57	39	McBSP 0 Subbank Data Register†
—	58−59	3A−3B	Reserved
GPIOCR	60	3C	General-Purpose I/O Control Register
GPIOSR	61	3D	General-Purpose I/O Status Register
CSIDR	62	3E	Device ID Register
—	63	3F	Reserved
DRR21	64	40	McBSP 1 Data Receive Register 2
DRR11	65	41	McBSP 1 Data Receive Register 1
DXR21	66	42	McBSP 1 Data Transmit Register 2
DXR11	67	43	McBSP 1 Data Transmit Register 1
USAR	68	44	UART Subbank Address Register
USDR	69	45	UART Subbank Data Register
—	70−71	46−47	Reserved
SPSA1	72	48	McBSP 1 Subbank Address Register†
SPSD1	73	49	McBSP 1 Subbank Data Register†
—	74−75	4A−4B	Reserved
TIM1	76	4C	Timer 1 Register
PRD1	77	4D	Timer 1 Period Register
TCR1	78	4E	Timer 1 Control Register

† See Table 3−25 for a detailed description of the McBSP control registers and their subaddresses.
‡ See Table 3−26 for a detailed description of the DMA subbank addressed registers.

Table 3−24. Peripheral Memory-Mapped Registers for Each DSP Subsystem (Continued)

NAME	ADDRESS DEC	ADDRESS HEX	DESCRIPTION
—	79−83	4F−53	Reserved
DMPREC	84	54	DMA Priority and Enable Control Register
DMSA	85	55	DMA Subbank Address Register‡
DMSDI	86	56	DMA Subbank Data Register with Autoincrement‡
DMSDN	87	57	DMA Subbank Data Register‡
CLKMD	88	58	Clock Mode Register (CLKMD)
—	89−95	59−5F	Reserved

† See Table 3−25 for a detailed description of the McBSP control registers and their subaddresses.
‡ See Table 3−26 for a detailed description of the DMA subbank addressed registers.

3.17 McBSP Control Registers and Subaddresses

The control registers for the multichannel buffered serial port (McBSP) are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The McBSP subbank address register (SPSA) is used as a pointer to select a particular register within the subbank. The McBSP data register (SPSDx) is used to access (read or write) the selected register. Table 3−25 shows the McBSP control registers and their corresponding subaddresses.

Table 3−25. McBSP Control Registers and Subaddresses

MCBSP0		MCBSP1		MCBSP2		SUB-ADDRESS	DESCRIPTION
NAME	ADDRESS	NAME	ADDRESS	NAME	ADDRESS		
SPCR10	39h	SPCR11	49h	SPCR12	35h	00h	Serial port control register 1
SPCR20	39h	SPCR21	49h	SPCR22	35h	01h	Serial port control register 2
RCR10	39h	RCR11	49h	RCR12	35h	02h	Receive control register 1
RCR20	39h	RCR21	49h	RCR22	35h	03h	Receive control register 2
XCR10	39h	XCR11	49h	XCR12	35h	04h	Transmit control register 1
XCR20	39h	XCR21	49h	XCR22	35h	05h	Transmit control register 2
SRGR10	39h	SRGR11	49h	SRGR12	35h	06h	Sample rate generator register 1
SRGR20	39h	SRGR21	49h	SRGR22	35h	07h	Sample rate generator register 2
MCR10	39h	MCR11	49h	MCR12	35h	08h	Multichannel register 1
MCR20	39h	MCR21	49h	MCR22	35h	09h	Multichannel register 2
RCERA0	39h	RCERA1	49h	RCERA2	35h	0Ah	Receive channel enable register partition A
RCERB0	39h	RCERB1	49h	RCERA2	35h	0Bh	Receive channel enable register partition B
XCERA0	39h	XCERA1	49h	XCERA2	35h	0Ch	Transmit channel enable register partition A
XCERB0	39h	XCERB1	49h	XCERA2	35h	0Dh	Transmit channel enable register partition B
PCR0	39h	PCR1	49h	PCR2	35h	0Eh	Pin control register
RCERC0	39h	RCERC1	49h	RCERC2	35h	010h	Additional channel enable register for 128-channel selection
RCERD0	39h	RCERD1	49h	RCERD2	35h	011h	Additional channel enable register for 128-channel selection
XCERC0	39h	XCERC1	49h	XCERC2	35h	012h	Additional channel enable register for 128-channel selection
XCERD0	39h	XCERD1	49h	XCERD2	35h	013h	Additional channel enable register for 128-channel selection
RCERE0	39h	RCERE1	49h	RCERE2	35h	014h	Additional channel enable register for 128-channel selection

Table 3−25. McBSP Control Registers and Subaddresses

NAME	ADDRESS	NAME	ADDRESS	NAME	ADDRESS	SUB-ADDRESS	DESCRIPTION
RCERF0	39h	RCERF1	49h	RCERF2	35h	015h	Additional channel enable register for 128-channel selection
XCERE0	39h	XCERE1	49h	XCERE2	35h	016h	Additional channel enable register for 128-channel selection
XCERF0	39h	XCERF1	49h	XCERF2	35h	017h	Additional channel enable register for 128-channel selection
RCERG0	39h	RCERG1	49h	RCERG2	35h	018h	Additional channel enable register for 128-channel selection
RCERH0	39h	RCERH1	49h	RCERH2	35h	019h	Additional channel enable register for 128-channel selection
XCERG0	39h	XCERG1	49h	XCERG2	35h	01Ah	Additional channel enable register for 128-channel selection
XCERH0	39h	XCERH1	49h	XCERH2	35h	01Bh	Additional channel enable register for 128-channel selection

3.18 DMA Subbank Addressed Registers

The direct memory access (DMA) controller has several control registers associated with it. The main control register (DMPREC) is a standard memory-mapped register. However, the other registers are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The DMA subbank address (DMSA) register is used as a pointer to select a particular register within the subbank, while the DMA subbank data (DMSD) register or the DMA subbank data register with autoincrement (DMSDI) is used to access (read or write) the selected register.

When the DMSDI register is used to access the subbank, the subbank address is automatically postincremented so that a subsequent access affects the next register within the subbank. This autoincrement feature is intended for efficient, successive accesses to several control registers. If the autoincrement feature is not required, the DMSDN register should be used to access the subbank. Table 3−26 shows the DMA controller subbank addressed registers and their corresponding subaddresses.

Table 3−26. DMA Subbank Addressed Registers

NAME	ADDRESS	SUB-ADDRESS	DESCRIPTION
DMSRC0	56h/57h	00h	DMA channel 0 source address register
DMDST0	56h/57h	01h	DMA channel 0 destination address register
DMCTR0	56h/57h	02h	DMA channel 0 element count register
DMSFC0	56h/57h	03h	DMA channel 0 sync select and frame count register
DMMCR0	56h/57h	04h	DMA channel 0 transfer mode control register
DMSRC1	56h/57h	05h	DMA channel 1 source address register
DMDST1	56h/57h	06h	DMA channel 1 destination address register
DMCTR1	56h/57h	07h	DMA channel 1 element count register
DMSFC1	56h/57h	08h	DMA channel 1 sync select and frame count register
DMMCR1	56h/57h	09h	DMA channel 1 transfer mode control register
DMSRC2	56h/57h	0Ah	DMA channel 2 source address register
DMDST2	56h/57h	0Bh	DMA channel 2 destination address register
DMCTR2	56h/57h	0Ch	DMA channel 2 element count register
DMSFC2	56h/57h	0Dh	DMA channel 2 sync select and frame count register

Table 3−26. DMA Subbank Addressed Registers (Continued)

NAME	ADDRESS	SUB-ADDRESS	DESCRIPTION
DMMCR2	56h/57h	0Eh	DMA channel 2 transfer mode control register
DMSRC3	56h/57h	0Fh	DMA channel 3 source address register
DMDST3	56h/57h	10h	DMA channel 3 destination address register
DMCTR3	56h/57h	11h	DMA channel 3 element count register
DMSFC3	56h/57h	12h	DMA channel 3 sync select and frame count register
DMMCR3	56h/57h	13h	DMA channel 3 transfer mode control register
DMSRC4	56h/57h	14h	DMA channel 4 source address register
DMDST4	56h/57h	15h	DMA channel 4 destination address register
DMCTR4	56h/57h	16h	DMA channel 4 element count register
DMSFC4	56h/57h	17h	DMA channel 4 sync select and frame count register
DMMCR4	56h/57h	18h	DMA channel 4 transfer mode control register
DMSRC5	56h/57h	19h	DMA channel 5 source address register
DMDST5	56h/57h	1Ah	DMA channel 5 destination address register
DMCTR5	56h/57h	1Bh	DMA channel 5 element count register
DMSFC5	56h/57h	1Ch	DMA channel 5 sync select and frame count register
DMMCR5	56h/57h	1Dh	DMA channel 5 transfer mode control register
DMSRCP	56h/57h	1Eh	DMA source program page address (common channel)
DMDSTP	56h/57h	1Fh	DMA destination program page address (common channel)
DMIDX0	56h/57h	20h	DMA element index address register 0
DMIDX1	56h/57h	21h	DMA element index address register 1
DMFRI0	56h/57h	22h	DMA frame index register 0
DMFRI1	56h/57h	23h	DMA frame index register 1
DMGSA0	56h/57h	24h	DMA global source address reload register, channel 0
DMGDA0	56h/57h	25h	DMA global destination address reload register, channel 0
DMGCR0	56h/57h	26h	DMA global count reload register, channel 0
DMGFR0	56h/57h	27h	DMA global frame count reload register, channel 0
XSRCDP	56h/57h	28h	DMA extended source data page
XDSTDP	56h/57h	29h	DMA extended destination data page
DMGSA1	56h/57h	2Ah	DMA global source address reload register, channel 1
DMGDA1	56h/57h	2Bh	DMA global destination address reload register, channel 1
DMGCR1	56h/57h	2Ch	DMA global count reload register, channel 1
DMGFR1	56h/57h	2Dh	DMA global frame count reload register, channel 1
DMGSA2	56h/57h	2Eh	DMA global source address reload register, channel 2
DMGDA2	56h/57h	2Fh	DMA global destination address reload register, channel 2
DMGCR2	56h/57h	30h	DMA global count reload register, channel 2
DMGFR2	56h/57h	31h	DMA global frame count reload register, channel 2
DMGSA3	56h/57h	32h	DMA global source address reload register, channel 3
DMGDA3	56h/57h	33h	DMA global destination address reload register, channel 3
DMGCR3	56h/57h	34h	DMA global count reload register, channel 3
DMGFR3	56h/57h	35h	DMA global frame count reload register, channel 3
DMGSA4	56h/57h	36h	DMA global source address reload register, channel 4
DMGDA4	56h/57h	37h	DMA global destination address reload register, channel 4

Table 3−26. DMA Subbank Addressed Registers (Continued)

NAME	ADDRESS	SUB-ADDRESS	DESCRIPTION
DMGCR4	56h/57h	38h	DMA global count reload register, channel 4
DMGFR4	56h/57h	39h	DMA global frame count reload register, channel 4
DMGSA5	56h/57h	3Ah	DMA global source address reload register, channel 5
DMGDA5	56h/57h	3Bh	DMA global destination address reload register, channel 5
DMGCR5	56h/57h	3Ch	DMA global count reload register, channel 5
DMGFR5	56h/57h	3Dh	DMA global frame count reload register, channel 5

3.19 Interrupts

Vector-relative locations and priorities for all internal and external interrupts are shown in Table 3−27.

Table 3−27. Interrupt Locations and Priorities

NAME	LOCATION DECIMAL	LOCATION HEX	PRIORITY	FUNCTION
$\overline{\text{RS}}$, SINTR	0	00	1	Reset (hardware and software reset)
$\overline{\text{NMI}}$, SINT16	4	04	2	Nonmaskable interrupt
SINT17	8	08	—	Software interrupt #17
SINT18	12	0C	—	Software interrupt #18
SINT19	16	10	—	Software interrupt #19
SINT20	20	14	—	Software interrupt #20
SINT21	24	18	—	Software interrupt #21
SINT22	28	1C	—	Software interrupt #22
SINT23	32	20	—	Software interrupt #23
SINT24	36	24	—	Software interrupt #24
SINT25	40	28	—	Software interrupt #25
SINT26	44	2C	—	Software interrupt #26
SINT27	48	30	—	Software interrupt #27
SINT28	52	34	—	Software interrupt #28
SINT29	56	38	—	Software interrupt #29
SINT30	60	3C	—	Software interrupt #30
$\overline{\text{INT0}}$, SINT0	64	40	3	External user interrupt #0
$\overline{\text{INT1}}$, SINT1	68	44	4	External user interrupt #1
$\overline{\text{INT2}}$, SINT2	72	48	5	External user interrupt #2
TINT0, SINT3	76	4C	6	Timer 0 interrupt
BRINT0, SINT4	80	50	7	McBSP #0 receive interrupt
BXINT0, SINT5	84	54	8	McBSP #0 transmit interrupt
BRINT2, SINT6	88	58	9	McBSP #2 receive interrupt (default)†
BXINT2, SINT7	92	5C	10	McBSP #2 transmit interrupt (default)†
$\overline{\text{INT3}}$, TINT1, SINT8	96	60	11	External user interrupt #3/Timer 1 interrupt‡
$\overline{\text{HINT}}$, SINT9	100	64	12	HPI interrupt
BRINT1, SINT10	104	68	13	McBSP #1 receive interrupt (default)†
BXINT1, SINT11	108	6C	14	McBSP #1 transmit interrupt (default)†
DMAC4,SINT12	112	70	15	DMA channel 4
DMAC5,SINT13	116	74	16	DMA channel 5
UART, SINT14	120	78	—	UART interrupt
Reserved	124−127	7C−7F	—	Reserved

† See Table 3−13 for other interrupt selections.
‡ The $\overline{\text{INT3}}$ and TINT1 interrupts are ORed together. To distinguish one from the other, one of these two interrupt sources must be inhibited.

3.19.1 IFR and IMR Registers

The bit layout of the interrupt flag register (IFR) and the interrupt mask register (IMR) is shown in Figure 3−26.

15	14	13	12	11	10	9	8
Reserved	UART	DMAC5	DMAC4	BXINT1	BRINT1	$\overline{\text{HINT}}$	$\overline{\text{INT3}}$†
7	6	5	4	3	2	1	0
BXINT2	BRINT2	BXINT0	BRINT0	TINT0	$\overline{\text{INT2}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$

† Bit 8 reflects the status of either $\overline{\text{INT3}}$ or TINT1: these two interrupts are ORed together. To distinguish one from the other, one of these two interrupt sources must be inhibited.

Figure 3−26. IFR and IMR

4 Documentation Support

Extensive documentation supports all TMS320™ DSP family of devices from product announcement through applications development. The following types of documentation are available to support the design and use of the C5000™ platform of DSPs:

- *TMS320C54x™ DSP Functional Overview* (literature number SPRU307)
- Device-specific data sheets
- Complete user's guides
- Development support tools
- Hardware and software application reports

The five-volume *TMS320C54x DSP Reference Set* (literature number SPRU210) consists of:

- *Volume 1: CPU and Peripherals* (literature number SPRU131)
- *Volume 2: Mnemonic Instruction Set* (literature number SPRU172)
- *Volume 3: Algebraic Instruction Set* (literature number SPRU179)
- *Volume 4: Applications Guide* (literature number SPRU173)
- *Volume 5: Enhanced Peripherals* (literature number SPRU302)

The reference set describes in detail the TMS320C54x™ DSP products currently available and the hardware and software applications, including algorithms, for fixed-point TMS320™ DSP family of devices.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320™ DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320™ DSP customers on product information.

Information regarding TI DSP products is also available on the Worldwide Web at *http://www.ti.com* uniform resource locator (URL).

TMS320 and C5000 are trademarks of Texas Instruments.

4.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., TMS320VC5407/TMS320VC5404). Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TMS320 is a trademark of Texas Instruments.

5 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320VC5407/TMS320VC5404 DSP.

5.1 Absolute Maximum Ratings

The list of absolute maximum ratings are specified over operating case temperature. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to DV_{SS}. Figure 5−1 provides the test load circuit values for a 3.3-V device.

Supply voltage I/O range, DV_{DD} . . . . . −0.3 V to 4.0 V
Supply voltage core range, CV_{DD} . . . . . −0.3 V to 2.0 V
Input voltage range . . . . . −0.3 V to 4.5 V
Output voltage range . . . . . −0.3 V to 4.5 V
Operating case temperature range, T_C . . . . . 0°C to 100°C
Storage temperature range, T_{stg} . . . . . −55°C to 150°C

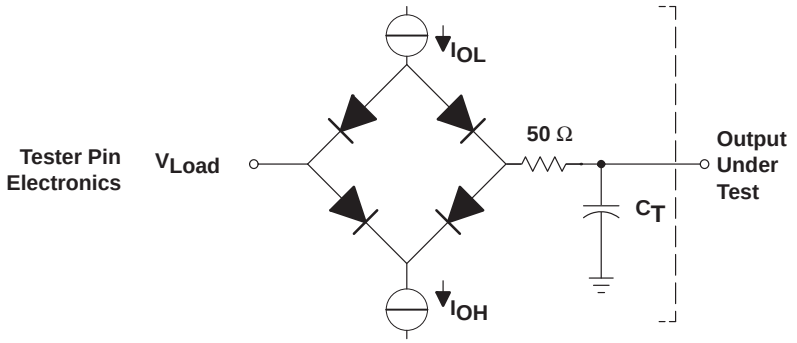
5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
DV_{DD}	Device supply voltage, I/O		2.7	3.3	3.6	V
CV_{DD}	Device supply voltage, core		1.42	1.5	1.65	V
DV_{SS}, CV_{SS}	Supply voltage, GND			0		V
V_{IH}	High-level input voltage, I/O	$\overline{RS}$, $\overline{INTn}$, $\overline{NMI}$, X2/CLKIN, $\overline{BIO}$, $\overline{TRST}$, Dn, An, HDn, $\overline{CLKMDn}$, $\overline{BCLKRn}$, $\overline{BCLKXn}$, $\overline{HCS}$, $\overline{HDS1}$, $\overline{HDS2}$, $\overline{HAS}$, RX, TCK	2.4		DV_{DD} + 0.3	V
		All other inputs	2		DV_{DD} + 0.3	
V_{IL}	Low-level input voltage		−0.3		0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature		0		100	°C

5.3 Electrical Characteristics Over Recommended Operating Case Temperature Range (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage‡		DV_{DD} = 3 V to 3.6 V, I_{OH} = MAX	2.4			V
			DV_{DD} = 2.7 V to 3 V, I_{OH} = MAX	2.2			
V_{OL}	Low-level output voltage‡		I_{OL} = MAX			0.4	V
I_{IZ}	Input current in high impedance	A[22:0]	DV_{DD} = MAX, V_O = DV_{SS} to DV_{DD}	−275		275	µA
I_I	Input current (V_I = DV_{SS} to DV_{DD})	X2/CLKIN		−40		40	µA
		$\overline{TRST}$	With internal pulldown	−10		800	µA
		HPIENA	With internal pulldown, $\overline{RS}$ = 0	−10		400	
		TMS, TCK, TDI, HPI§	With internal pullups	−400		10	
		D[15:0], HD[7:0]	Bus holders enabled, DV_{DD} = MAX☆	−275		275	
		All other input-only pins		−5		5	
I_{DDC}	Supply current, core CPU		CV_{DD} = 1.5 V, f_X = 120 MHz,¶ T_C = 25°C		42#		mA
I_{DDP}	Supply current, pins		DV_{DD} = 3.0 V, f_X = 120 MHz,¶ T_C = 25°C		20‖		mA
I_{DD}	Supply current, standby	IDLE2	PLL × 1 mode, 20 MHz input		2		mA
		IDLE3	Divide-by-two mode, CLKIN stopped		1□		mA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All values are typical unless otherwise specified.
‡ All input and output voltage levels except $\overline{RS}$, $\overline{INT0}$–$\overline{INT3}$, $\overline{NMI}$, X2/CLKIN, CLKMD1–CLKMD3 are LVTTL-compatible.
§ HPI input signals except for HPIENA.
¶ Clock mode: PLL × 1 with external source
# This value was obtained with 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with program being executed.
‖ This value was obtained with single-cycle external writes, CLKOFF = 0 and load = 15 pF. For more details on how this calculation is performed, refer to the *Calculation of TMS320LC54x Power Dissipation* application report (literature number SPRA164).
☆ $V_{IL(MIN)} \le V_I \le V_{IL(MAX)}$ or $V_{IH(MIN)} \le V_I \le V_{IH(MAX)}$
□ Material with high I_{DD} has been observed with an I_{DD} as high as 7 mA during high temperature testing.



Where: I_{OL} = 1.5 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{Load} = 1.5 V
C_T = 20-pF typical load circuit capacitance

Figure 5−1. 3.3-V Test Load Circuit

5.4 Timing Parameter Symbology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:

a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)
X	Unknown, changing, or don't care level

Letters and symbols and their meanings:

H	High
L	Low
V	Valid
Z	High impedance

5.5 Internal Oscillator With External Crystal

The internal oscillator is enabled by selecting the appropriate clock mode at reset (this is device-dependent; see Section 3.10) and connecting a crystal or ceramic resonator across X1 and X2/CLKIN. The CPU clock frequency is one-half, one-fourth, or a multiple of the oscillator frequency. The multiply ratio is determined by the bit settings in the CLKMD register.

The crystal should be in fundamental-mode operation, and parallel resonant, with an effective series resistance of 30 Ω maximum and power dissipation of 1 mW. The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in Figure 5−2. The load capacitors, C_1 and C_2, should be chosen such that the equation below is satisfied. C_L (recommended value of 10 pF) in the equation is the load specified for the crystal.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 5−1. Input Clock Frequency Characteristics

		MIN	MAX	UNIT
f_X	Input clock frequency	10†	20‡	MHz

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz

‡ It is recommended that the PLL multiply by N clocking option be used for maximum frequency operation.

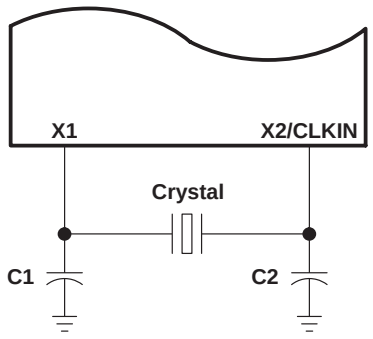


Figure 5−2. Internal Divide-by-Two Clock Option With External Crystal

5.6 Clock Options

The frequency of the reference clock provided at the CLKIN pin can be divided by a factor of two or four or multiplied by one of several values to generate the internal machine cycle.

5.6.1 Divide-By-Two and Divide-By-Four Clock Options

The frequency of the reference clock provided at the X2/CLKIN pin can be divided by a factor of two or four to generate the internal machine cycle. The selection of the clock mode is described in Section 3.10.

When an external clock source is used, the frequency injected must conform to specifications listed in Table 5−3.

An external frequency source can be used by applying an input clock to X2/CLKIN with X1 left unconnected.

Table 5−2 shows the configuration options for the CLKMD pins that generate the external divide-by-2 or divide-by-4 clock option.

Table 5−2. Clock Mode Pin Settings for the Divide-By-2 and By Divide-by-4 Clock Options

CLKMD1	CLKMD2	CLKMD3	CLOCK MODE
0	0	0	1/2, PLL and oscillator disabled
1	0	1	1/4, PLL and oscillator disabled
1	1	1	1/2, PLL and oscillator disabled

Table 5−3 and Table 5−4 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−3).

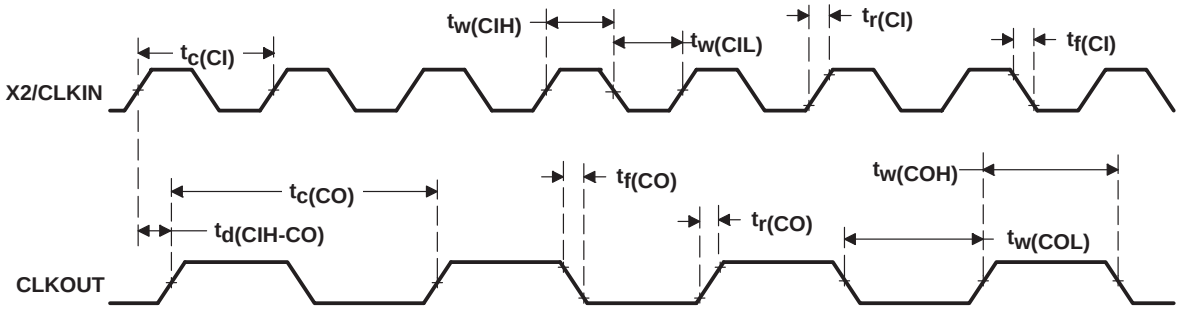
Table 5−3. Divide-By-2 and Divide-by-4 Clock Options Timing Requirements

		MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, X2/CLKIN	20		ns
$t_{f(CI)}$	Fall time, X2/CLKIN		4	ns
$t_{r(CI)}$	Rise time, X2/CLKIN		4	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low	4		ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high	4		ns

Table 5−4. Divide-By-2 and Divide-by-4 Clock Options Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	8.33†		‡	ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN high to CLKOUT high/low	4	7	11	ns
$t_{f(CO)}$	Fall time, CLKOUT		1		ns
$t_{r(CO)}$	Rise time, CLKOUT		1		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low	H − 3	H	H + 3	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high	H − 3	H	H + 3	ns

† It is recommended that the PLL clocking option be used for maximum frequency operation.
‡ This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz.



NOTE A: The CLKOUT timing in this diagram assumes the CLKOUT divide factor (DIVFCT field in the BSCR) is configured as 00 (CLKOUT not divided). DIVFCT is configured as CLKOUT divided-by-4 mode following reset.

Figure 5−3. External Divide-by-Two Clock Timing

5.6.2 Multiply-By-N Clock Option (PLL Enabled)

The frequency of the reference clock provided at the X2/CLKIN pin can be multiplied by a factor of N to generate the internal machine cycle. The selection of the clock mode and the value of N is described in Section 3.10. Following reset, the software PLL can be programmed for the desired multiplication factor. Refer to the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (literature number SPRU131) for detailed information on programming the PLL.

When an external clock source is used, the external frequency injected must conform to specifications listed in Table 5−5.

Table 5−5 and Table 5−6 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−4).

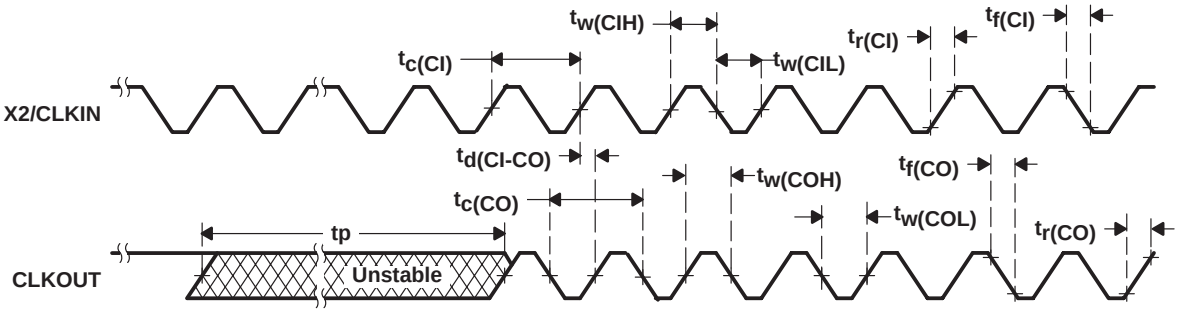
Table 5−5. Multiply-By-N Clock Option Timing Requirements

			MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, X2/CLKIN	Integer PLL multiplier N (N = 1−15)†	20	200	ns
		PLL multiplier N = x.5†	20	100	
		PLL multiplier N = x.25, x.75†	20	50	
$t_{f(CI)}$	Fall time, X2/CLKIN			4	ns
$t_{r(CI)}$	Rise time, X2/CLKIN			4	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low		4		ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high		4		ns

† N is the multiplication factor.

Table 5−6. Multiply-By-N Clock Option Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	8.33			ns
$t_{d(CI-CO)}$	Delay time, X2/CLKIN high/low to CLKOUT high/low	4	7	11	ns
$t_{f(CO)}$	Fall time, CLKOUT		2		ns
$t_{r(CO)}$	Rise time, CLKOUT		2		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low		H		ns
$t_{w(COH)}$	Pulse duration, CLKOUT high		H		ns
t_p	Transitory phase, PLL lock-up time			30	µs



NOTE A: The CLKOUT timing in this diagram assumes the CLKOUT divide factor (DIVFCT field in the BSCR) is configured as 00 (CLKOUT not divided). DIVFCT is configured as CLKOUT divided-by-4 mode following reset.

Figure 5−4. Multiply-by-One Clock Timing

5.7 Memory and Parallel I/O Interface Timing

5.7.1 Memory Read

External memory reads can be performed in consecutive or nonconsecutive mode under control of the CONSEC bit in the BSCR. Table 5−7 and Table 5−8 assume testing over recommended operating conditions with $\overline{\text{MSTRB}}$ = 0 and H = 0.5$t_{c(CO)}$ (see Figure 5−5 and Figure 5−6).

Table 5−7. Memory Read Timing Requirements

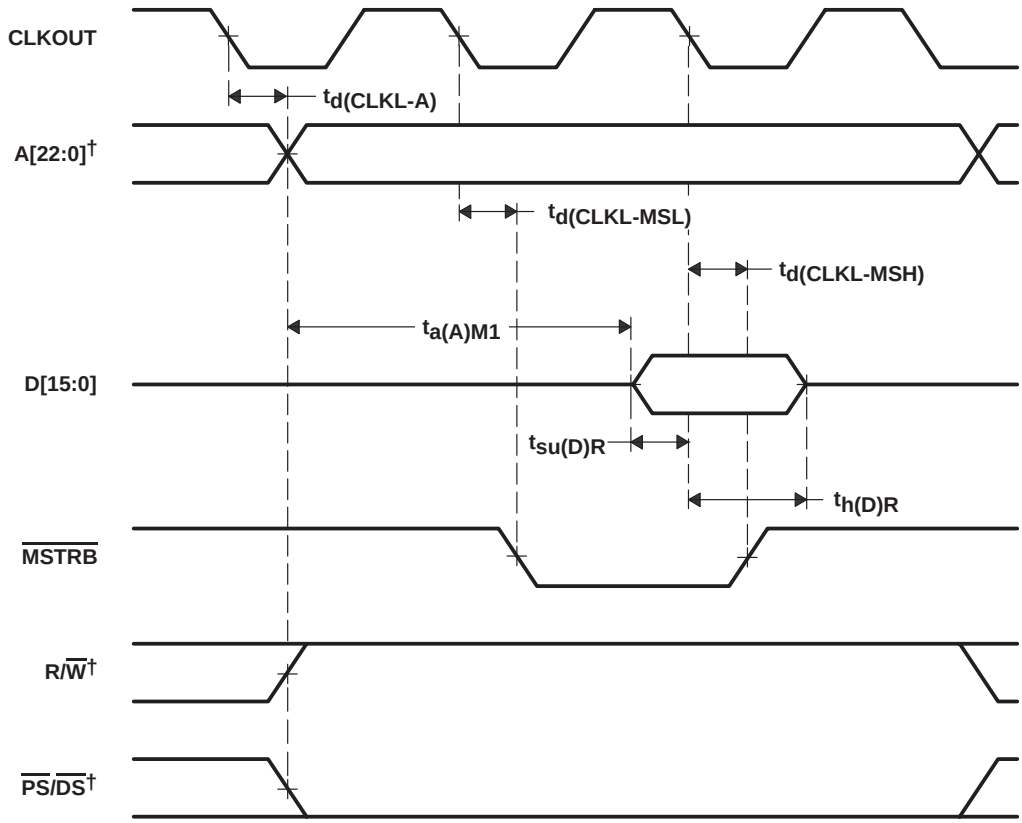
			MIN	MAX	UNIT
$t_{a(A)M1}$	Access time, read data access from address valid, first read access†	For accesses not immediately following a HOLD operation		4H−9	ns
		For read accesses immediately following a HOLD operation		4H−11	ns
$t_{a(A)M2}$	Access time, read data access from address valid, consecutive read accesses†			2H−9	ns
$t_{su(D)R}$	Setup time, read data valid before CLKOUT low		7		ns
$t_{h(D)R}$	Hold time, read data valid after CLKOUT low		0		ns

† Address,R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.

Table 5−8. Memory Read Switching Characteristics

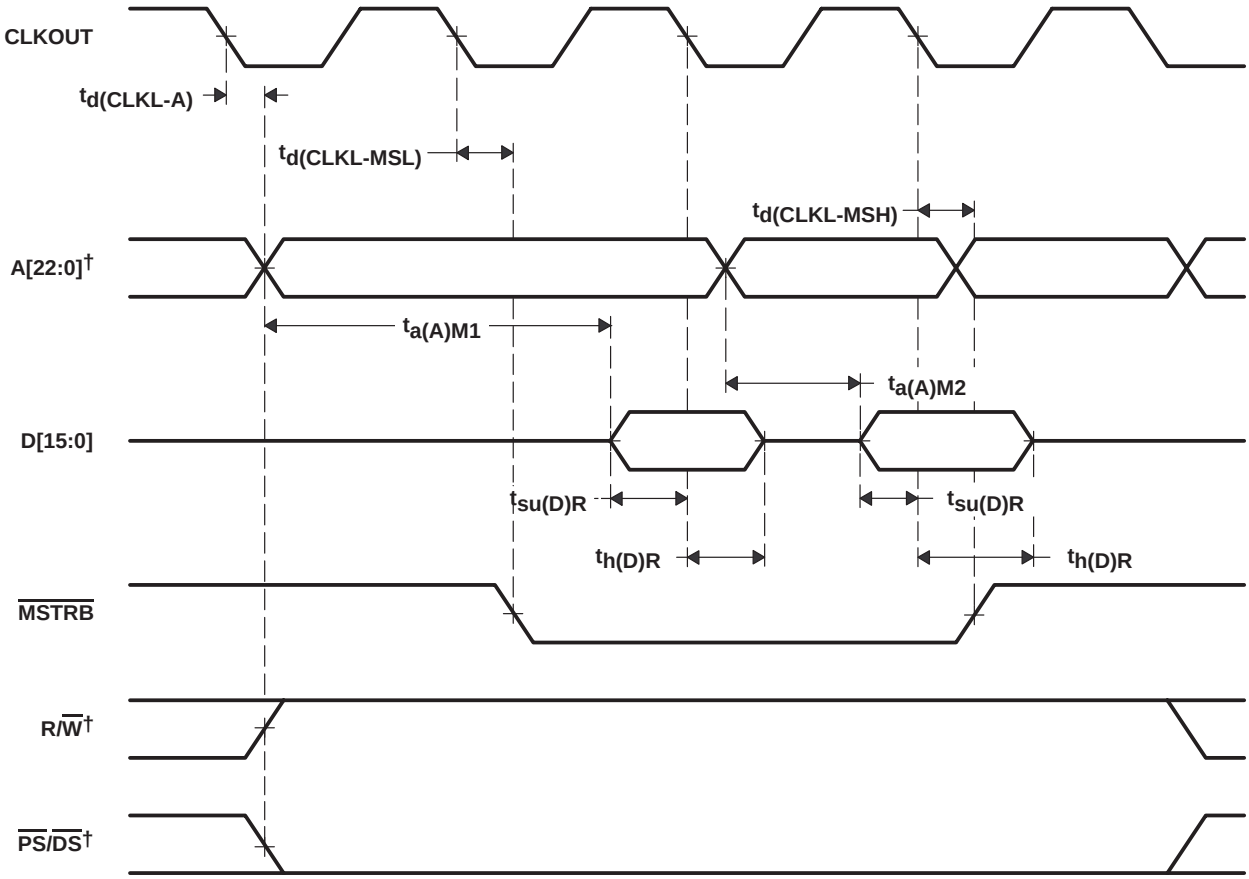
PARAMETER			MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid†	For accesses not immediately following a HOLD operation	−1	4	ns
		For read accesses immediately following a HOLD operation	−1	6	ns
$t_{d(CLKL-MSL)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low		−1	4	ns
$t_{d(CLKL-MSH)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high		0	4	ns

† Address,R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.



† Address,R/W, PS, DS, and IS timings are all included in timings referenced as address.

Figure 5−5. Nonconsecutive Mode Memory Reads



† Address,R/W, PS, DS, and IS timings are all included in timings referenced as address.

Figure 5−6. Consecutive Mode Memory Reads

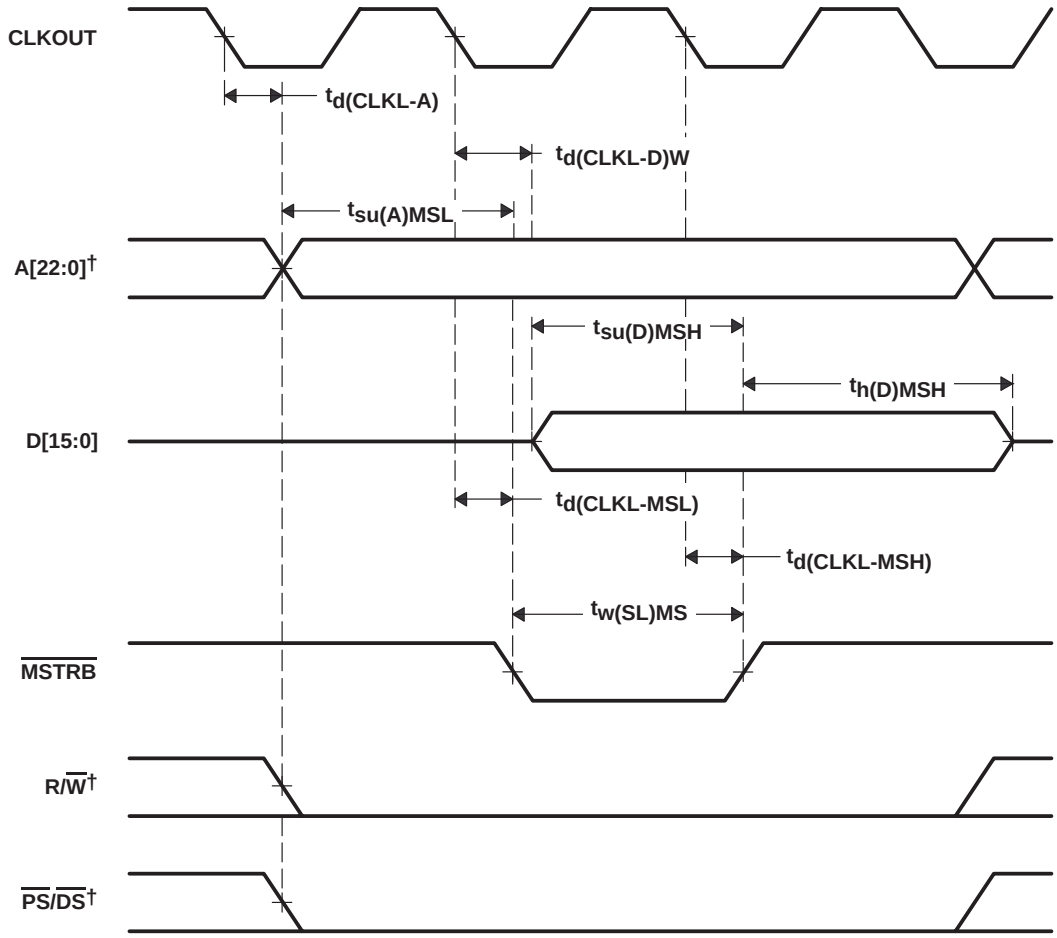
5.7.2 Memory Write

Table 5−9 assumes testing over recommended operating conditions with $\overline{\text{MSTRB}}$ = 0 and H = 0.5$t_{c(CO)}$ (see Figure 5−7).

Table 5−9. Memory Write Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid†	For accesses not immediately following a HOLD operation	− 1	4	ns
		For read accesses immediately following a HOLD operation	− 1	6	ns
$t_{su(A)MSL}$	Setup time, address valid before $\overline{\text{MSTRB}}$ low†	For accesses not immediately following a HOLD operation	2H − 3		ns
		For read accesses immediately following a HOLD operation	2H − 5		ns
$t_{d(CLKL-D)W}$	Delay time, CLKOUT low to data valid		− 1	5	ns
$t_{su(D)MSH}$	Setup time, data valid before $\overline{\text{MSTRB}}$ high		2H − 5	2H + 6	ns
$t_{h(D)MSH}$	Hold time, data valid after $\overline{\text{MSTRB}}$ high		2H − 5	2H + 6	ns
$t_{d(CLKL-MSL)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low		− 1	4	ns
$t_{w(SL)MS}$	Pulse duration, $\overline{\text{MSTRB}}$ low		2H − 2		ns
$t_{d(CLKL-MSH)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high		0	4	ns

† Address, R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.



† Address, R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.

Figure 5−7. Memory Write ($\overline{MSTRB}$ = 0)

5.7.3 I/O Read

Table 5−10 and Table 5−11 assume testing over recommended operating conditions, $\overline{\text{IOSTRB}}$ = 0, and H = 0.5$t_{c(CO)}$ (see Figure 5−8).

Table 5−10. I/O Read Timing Requirements

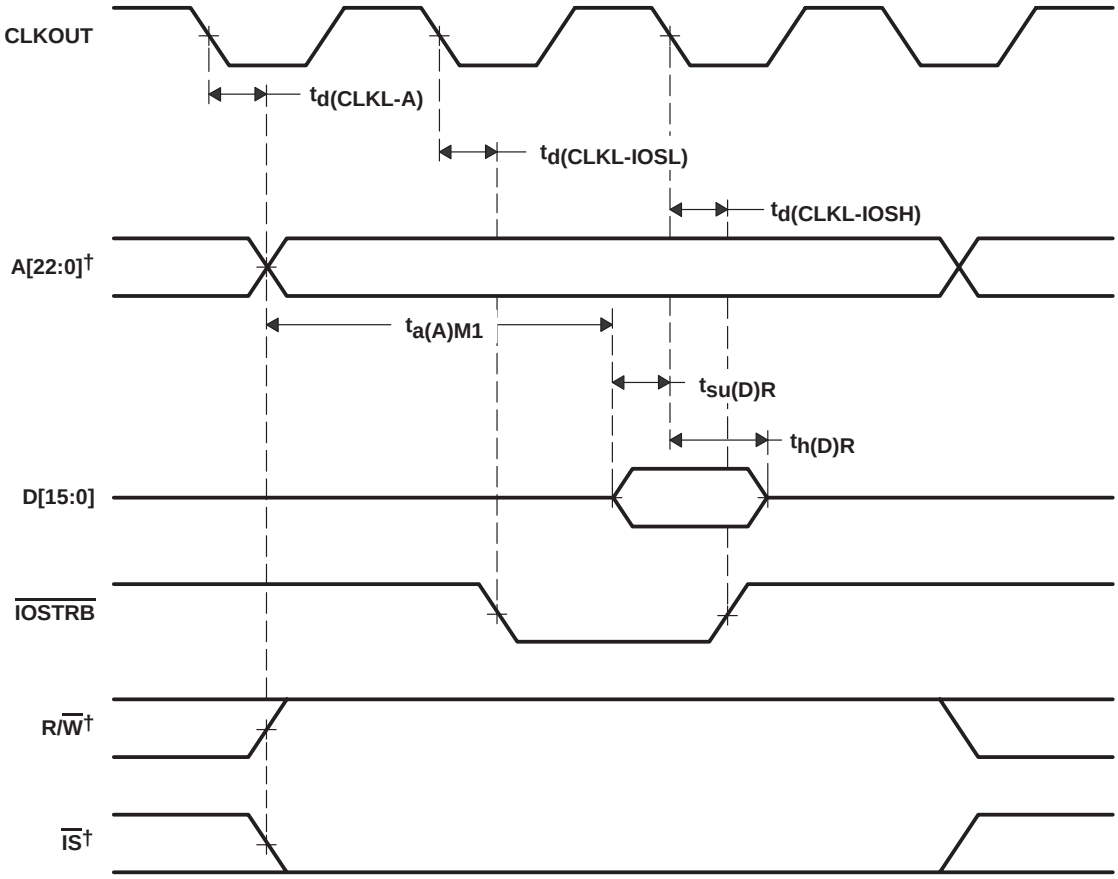
			MIN	MAX	UNIT
$t_{a(A)M1}$	Access time, read data access from address valid, first read access†	For accesses not immediately following a HOLD operation		4H − 9	ns
		For read accesses immediately following a HOLD operation		4H − 11	ns
$t_{su(D)R}$	Setup time, read data valid before CLKOUT low		7		ns
$t_{h(D)R}$	Hold time, read data valid after CLKOUT low		0		ns

† Address R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are included in timings referenced as address.

Table 5−11. I/O Read Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid†	For accesses not immediately following a HOLD operation	− 1	4	ns
		For read accesses immediately following a HOLD operation	− 1	6	ns
$t_{d(CLKL-IOSL)}$	Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ low		− 1	4	ns
$t_{d(CLKL-IOSH)}$	Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ high		0	4	ns

† Address R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are included in timings referenced as address.



† Address, R/W, PS, DS, and IS timings are all included in timings referenced as address.

Figure 5−8. Parallel I/O Port Read (IOSTRB = 0)

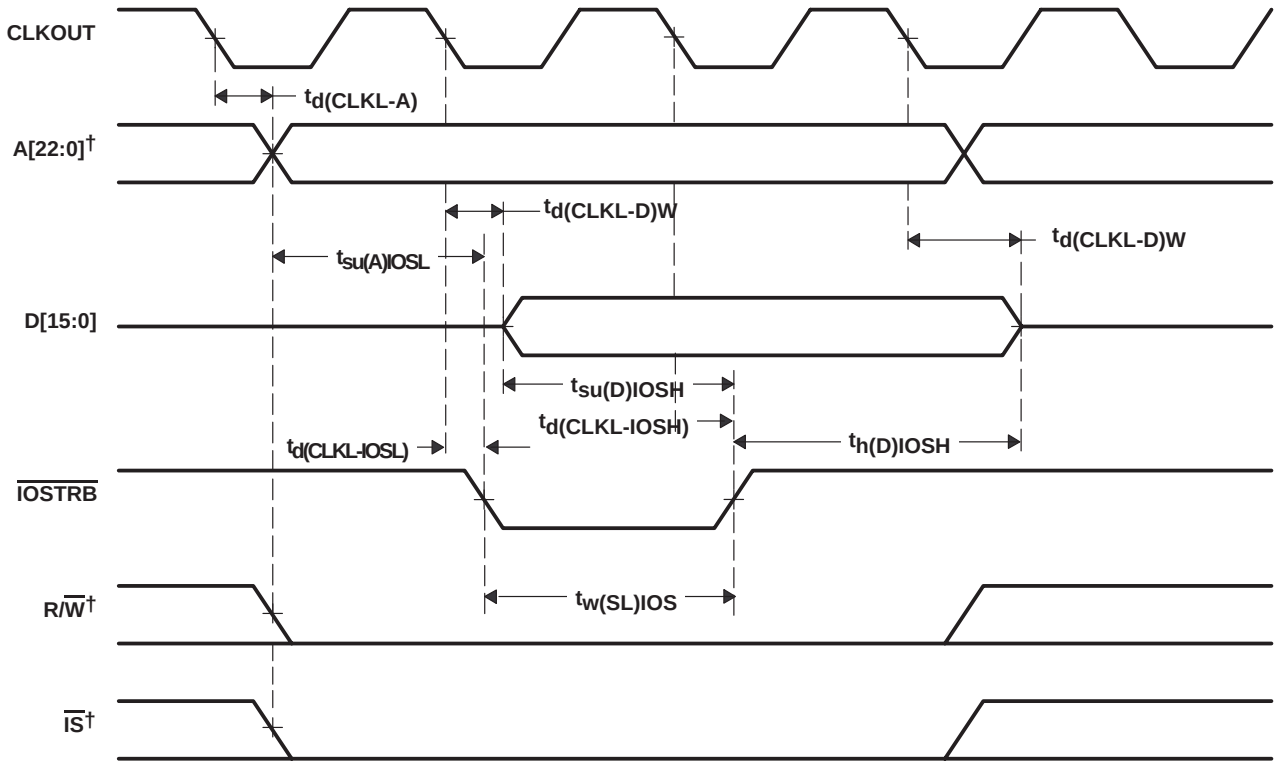
5.7.4 I/O Write

Table 5−12 assumes testing over recommended operating conditions, $\overline{\text{IOSTRB}}$ = 0, and H = 0.5$t_{c(CO)}$ (see Figure 5−9).

Table 5−12. I/O Write Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid†	For accesses not immediately following a HOLD operation	− 1	4	ns
		For read accesses immediately following a HOLD operation	− 1	6	ns
$t_{su(A)IOSL}$	Setup time, address valid before $\overline{\text{IOSTRB}}$ low†	For accesses not immediately following a HOLD operation	2H − 3		ns
		For read accesses immediately following a HOLD operation	2H − 5		ns
$t_{d(CLKL-D)W}$	Delay time, CLKOUT low to write data valid		− 1	4	ns
$t_{su(D)IOSH}$	Setup time, data valid before $\overline{\text{IOSTRB}}$ high		2H − 5	2H + 6	ns
$t_{h(D)IOSH}$	Hold time, data valid after $\overline{\text{IOSTRB}}$ high		2H − 5	2H + 6	ns
$t_{d(CLKL-IOSL)}$	Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ low		− 1	4	ns
$t_{w(SL)IOS}$	Pulse duration, $\overline{\text{IOSTRB}}$ low		2H − 2		ns
$t_{d(CLKL-IOSH)}$	Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ high		0	4	ns

† Address R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are included in timings referenced as address.



† Address, R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.

Figure 5−9. Parallel I/O Port Write ($\overline{\text{IOSTRB}}$ = 0)

5.8 Ready Timing for Externally Generated Wait States

Table 5−13 and Table 5−14 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−10, Figure 5−11, Figure 5−12, and Figure 5−13).

Table 5−13. Ready Timing Requirements for Externally Generated Wait States†

		MIN	MAX	UNIT
$t_{su(RDY)}$	Setup time, READY before CLKOUT low	7		ns
$t_{h(RDY)}$	Hold time, READY after CLKOUT low	0		ns
$t_{v(RDY)MSTRB}$	Valid time, READY after $\overline{MSTRB}$ low‡		4H − 4	ns
$t_{h(RDY)MSTRB}$	Hold time, READY after $\overline{MSTRB}$ low‡	4H		ns
$t_{v(RDY)IOSTRB}$	Valid time, READY after $\overline{IOSTRB}$ low‡		4H − 4	ns
$t_{h(RDY)IOSTRB}$	Hold time, READY after $\overline{IOSTRB}$ low‡	4H		ns

† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.
‡ These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT.

Table 5−14. Ready Switching Characteristics for Externally Generated Wait States†

PARAMETER		MIN	MAX	UNIT
$t_{d(MSCL)}$	Delay time, $\overline{MSC}$ low to CLKOUT low	− 1	4	ns
$t_{d(MSCH)}$	Delay time, CLKOUT low to $\overline{MSC}$ high	− 1	4	ns

† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.

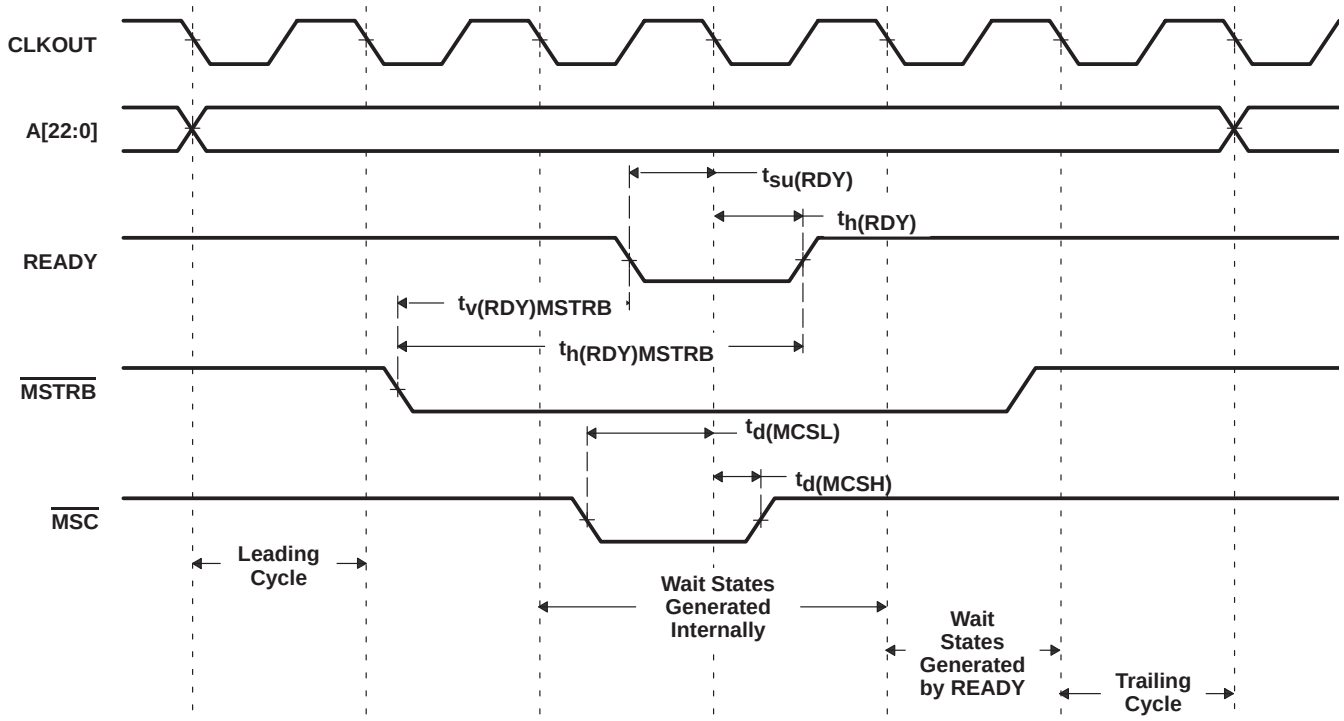


Figure 5−10. Memory Read With Externally Generated Wait States

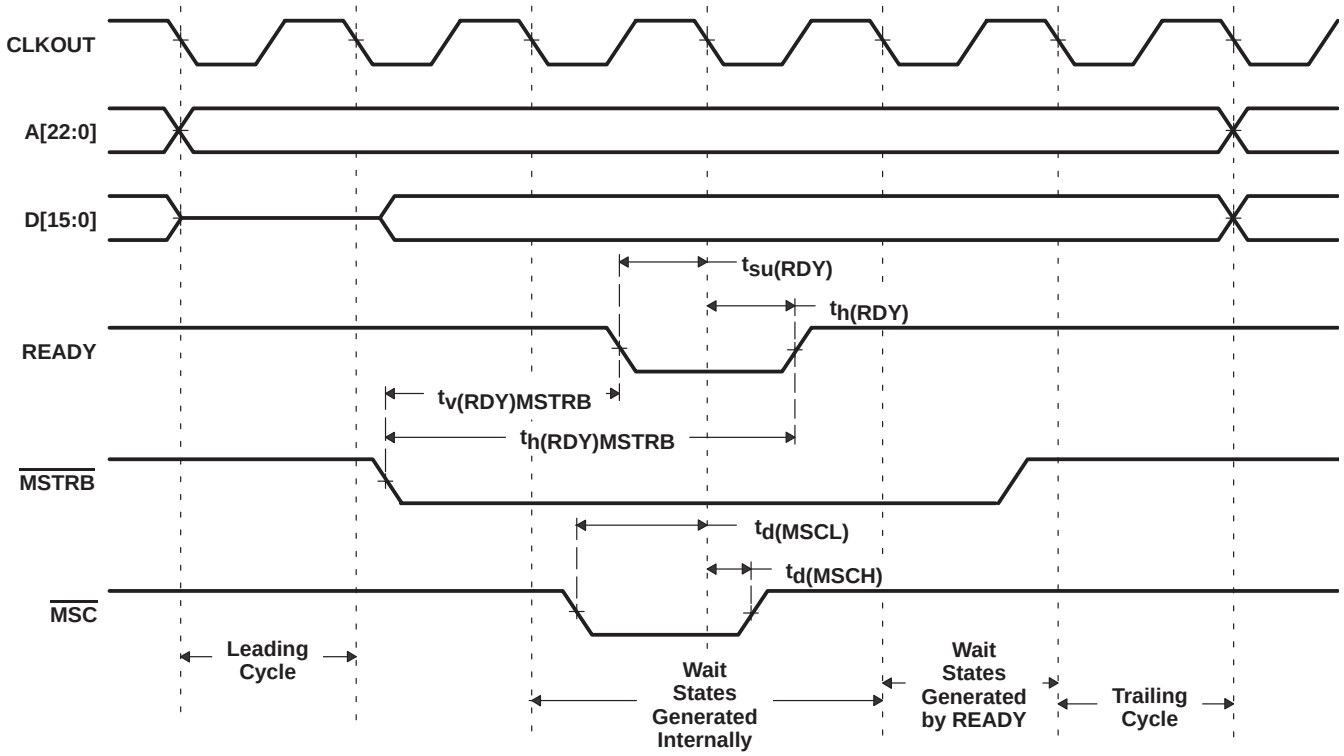


Figure 5−11. Memory Write With Externally Generated Wait States

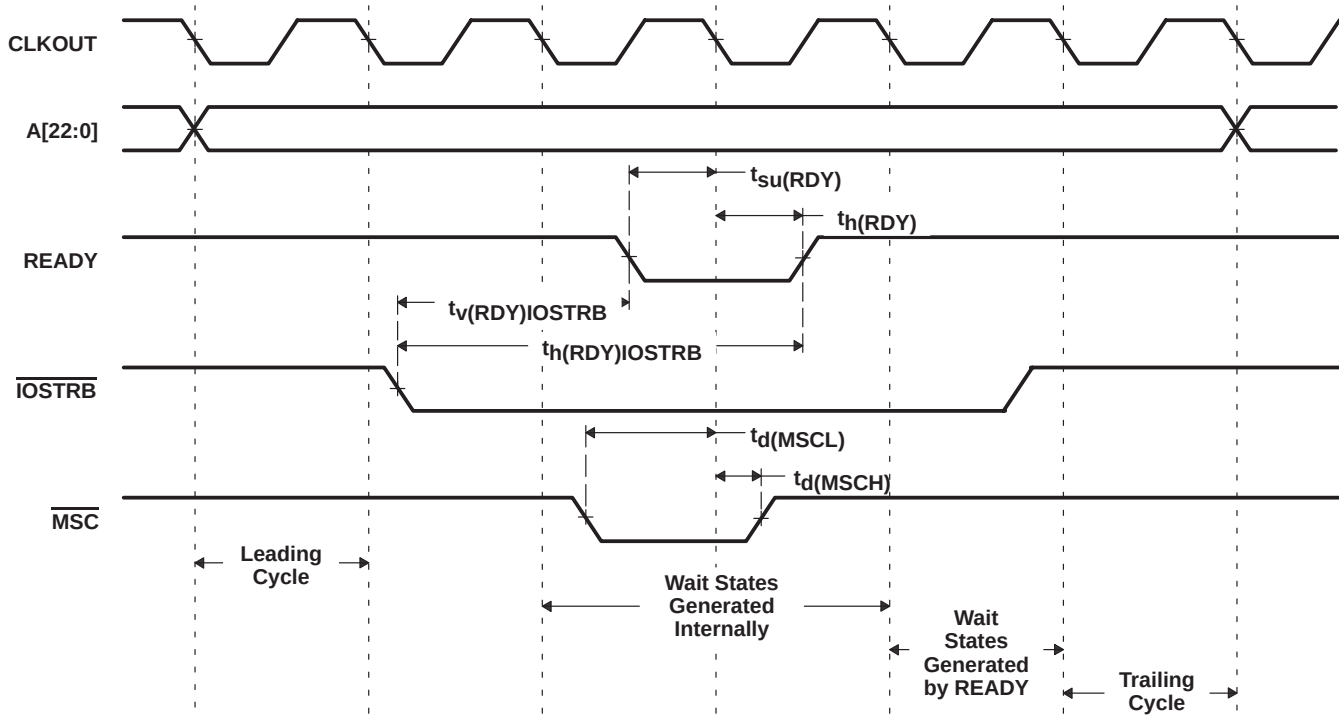


Figure 5−12. I/O Read With Externally Generated Wait States

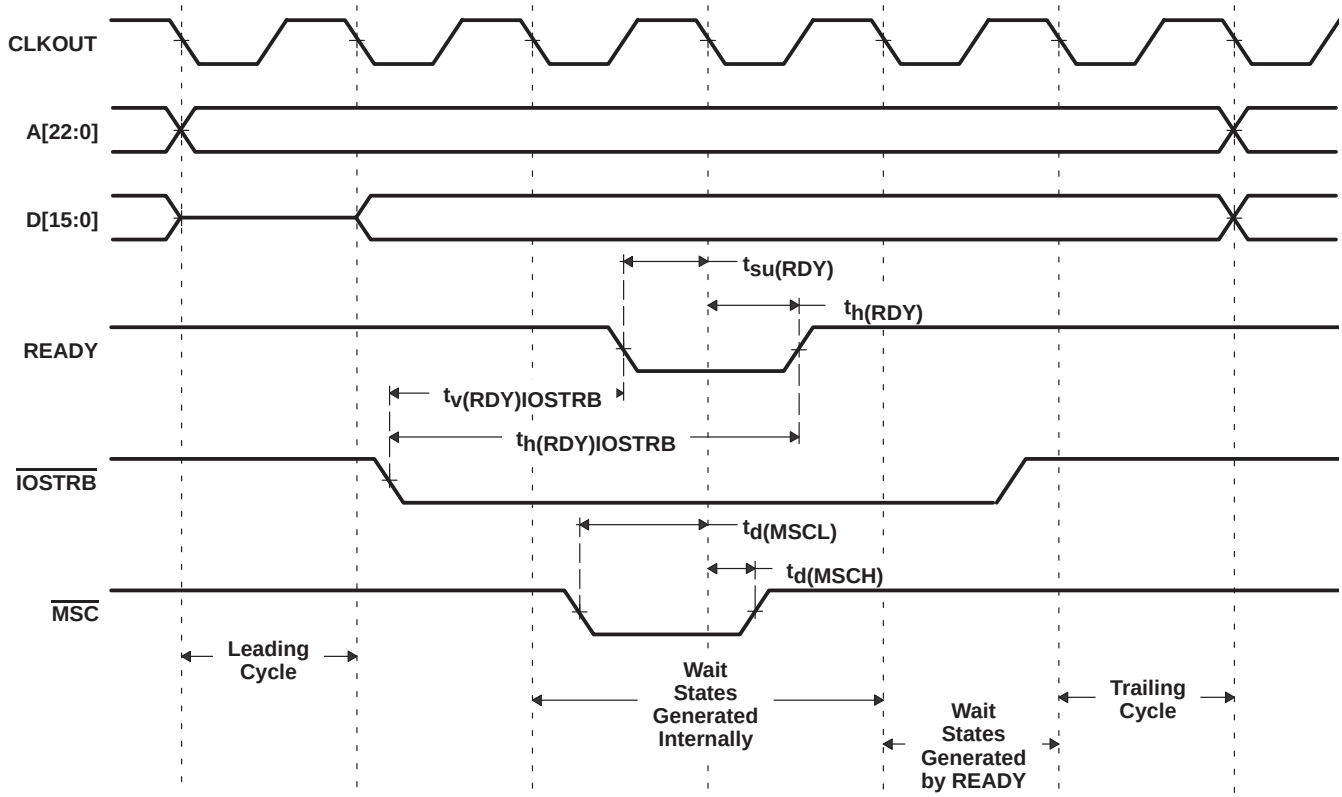


Figure 5−13. I/O Write With Externally Generated Wait States

5.9 $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timings

Table 5−15 and Table 5−16 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−14).

Table 5−15. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timing Requirements

		MIN	MAX	UNIT
$t_{w(HOLD)}$	Pulse duration, $\overline{\text{HOLD}}$ low duration	4H+8		ns
$t_{su(HOLD)}$	Setup time, $\overline{\text{HOLD}}$ before CLKOUT low	7		ns

Table 5−16. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{dis(CLKL-A)}$	Disable time, Address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$ high impedance from CLKOUT low		3	ns
$t_{dis(CLKL-RW)}$	Disable time, R/$\overline{\text{W}}$ high impedance from CLKOUT low		3	ns
$t_{dis(CLKL-S)}$	Disable time, $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ high impedance from CLKOUT low		3	ns
$t_{en(CLKL-A)}$	Enable time, Address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$ valid from CLKOUT low		2H+4	ns
$t_{en(CLKL-RW)}$	Enable time, R/$\overline{\text{W}}$ enabled from CLKOUT low		2H+3	ns
$t_{en(CLKL-S)}$	Enable time, $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ enabled from CLKOUT low	2	2H+3	ns
$t_{v(HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ low after CLKOUT low	− 1	4	ns
	Valid time, $\overline{\text{HOLDA}}$ high after CLKOUT low	− 1	4	ns
$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low duration	2H−3		ns

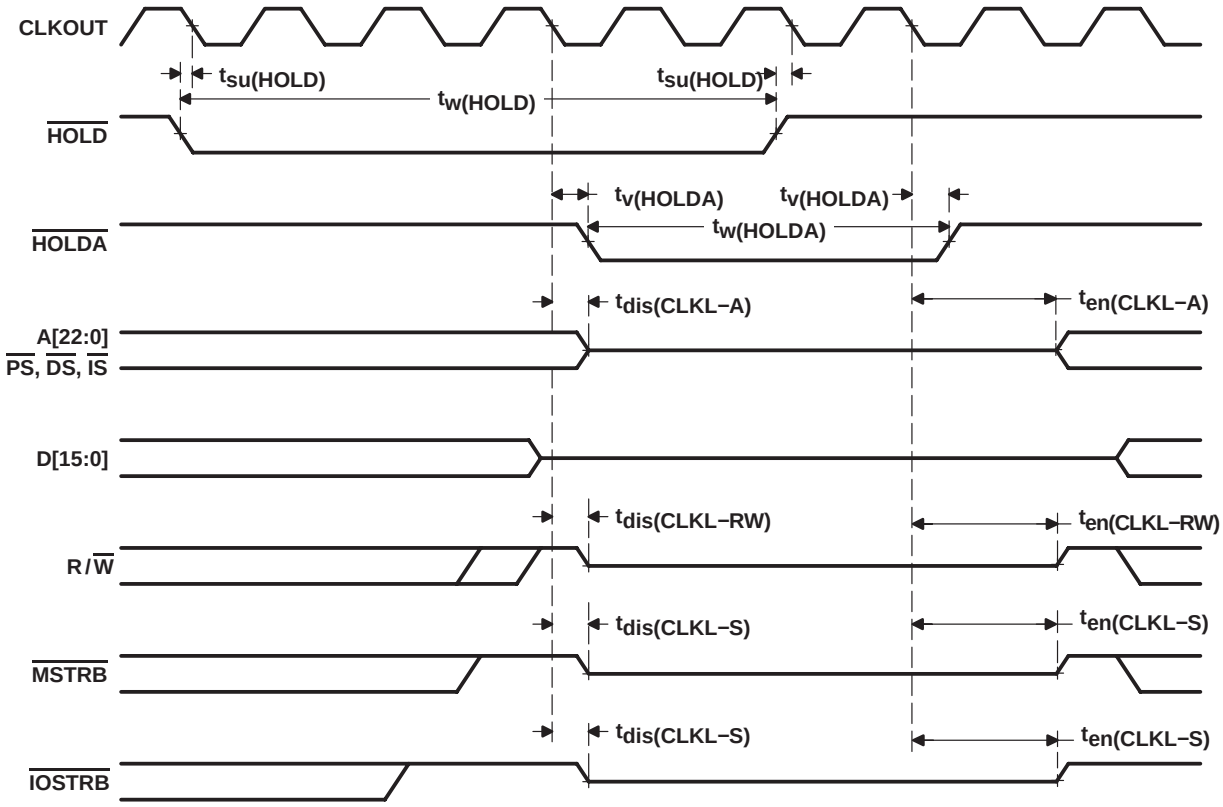


Figure 5−14. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timings (HM = 1)

5.10 Reset, $\overline{\text{BIO}}$, Interrupt, and MP/$\overline{\text{MC}}$ Timings

Table 5−17 assumes testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−15, Figure 5−16, and Figure 5−17).

Table 5−17. Reset, $\overline{\text{BIO}}$, Interrupt, and MP/$\overline{\text{MC}}$ Timing Requirements

		MIN	MAX	UNIT
$t_{h(RS)}$	Hold time, $\overline{\text{RS}}$ after CLKOUT low	3		ns
$t_{h(BIO)}$	Hold time, $\overline{\text{BIO}}$ after CLKOUT low	4		ns
$t_{h(INT)}$	Hold time, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$, after CLKOUT low†	1		ns
$t_{h(MPMC)}$	Hold time, MP/$\overline{\text{MC}}$ after CLKOUT low	4		ns
$t_{w(RSL)}$	Pulse duration, $\overline{\text{RS}}$ low‡§	4H+3		ns
$t_{w(BIO)S}$	Pulse duration, $\overline{\text{BIO}}$ low, synchronous	2H+3		ns
$t_{w(BIO)A}$	Pulse duration, $\overline{\text{BIO}}$ low, asynchronous	4H		ns
$t_{w(INTH)S}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ high (synchronous)	2H+2		ns
$t_{w(INTH)A}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ high (asynchronous)	4H		ns
$t_{w(INTL)S}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low (synchronous)	2H+2		ns
$t_{w(INTL)A}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low (asynchronous)	4H		ns
$t_{w(INTL)WKP}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low for IDLE2/IDLE3 wakeup	8		ns
$t_{su(RS)}$	Setup time, $\overline{\text{RS}}$ before X2/CLKIN low¶	3		ns
$t_{su(BIO)}$	Setup time, $\overline{\text{BIO}}$ before CLKOUT low	7		ns
$t_{su(INT)}$	Setup time, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$, $\overline{\text{RS}}$ before CLKOUT low	7		ns
$t_{su(MPMC)}$	Setup time, MP/$\overline{\text{MC}}$ before CLKOUT low	5		ns

† The external interrupts ($\overline{\text{INT0}}$−$\overline{\text{INT3}}$, $\overline{\text{NMI}}$) are synchronized to the core CPU by way of a two-flip-flop synchronizer that samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1−0−0 sequence at the timing that is corresponding to three CLKOUTs sampling sequence.

‡ If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, $\overline{\text{RS}}$ must be held low for at least 50 µs to ensure synchronization and lock-in of the PLL.

§ Note that $\overline{\text{RS}}$ may cause a change in clock frequency, therefore changing the value of H.

¶ The diagram assumes clock mode is divide-by-2 and the CLKOUT divide factor is set to no-divide mode (DIVFCT=00 field in the BSCR).

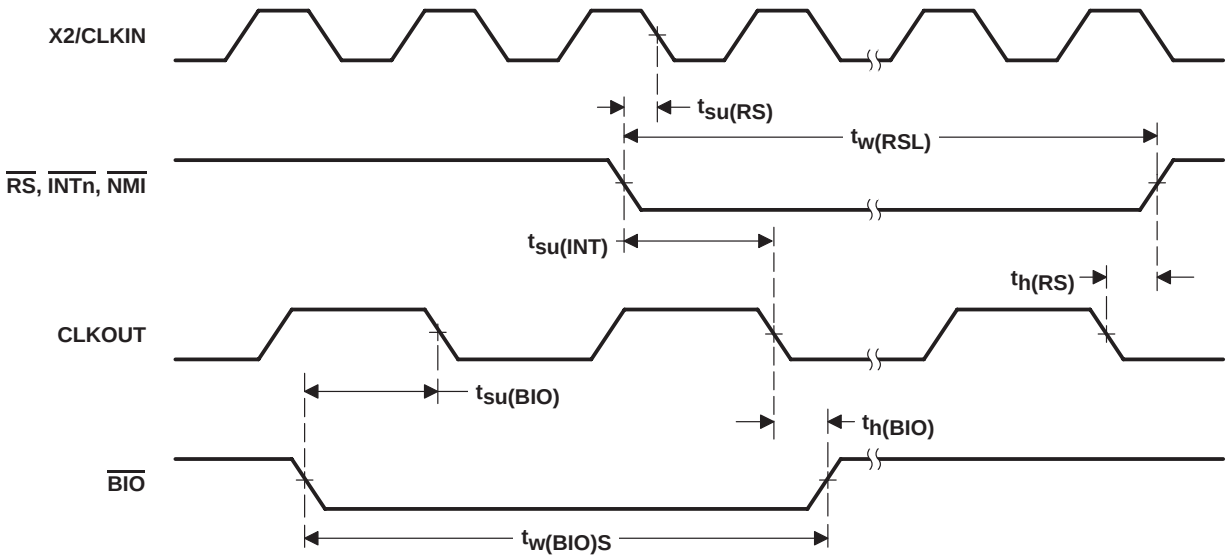


Figure 5−15. Reset and $\overline{\text{BIO}}$ Timings

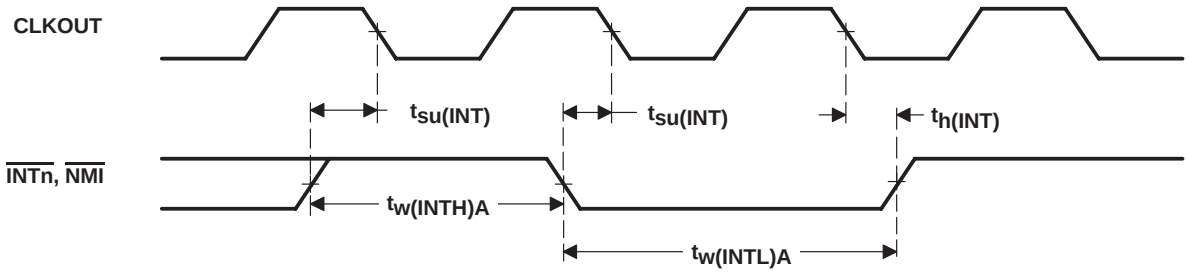


Figure 5−16. Interrupt Timing

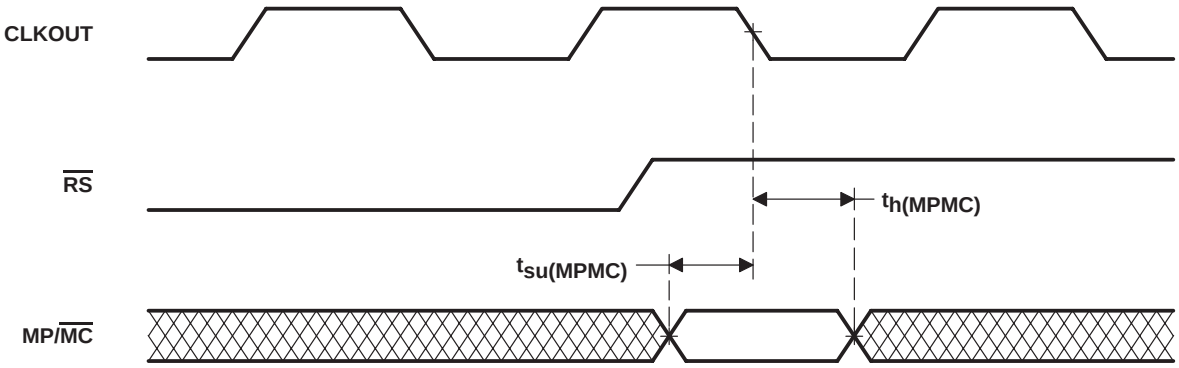


Figure 5−17. MP/$\overline{MC}$ Timing

5.11 Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Timings

Table 5−18 assumes testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−18).

Table 5−18. Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(CLKL-IAQL)}$	Delay time, CLKOUT low to $\overline{IAQ}$ low	− 1	4	ns
$t_{d(CLKL-IAQH)}$	Delay time, CLKOUT low to $\overline{IAQ}$ high	− 1	4	ns
$t_{d(A)IAQ}$	Delay time, $\overline{IAQ}$ low to address valid		2	ns
$t_{d(CLKL-IACKL)}$	Delay time, CLKOUT low to $\overline{IACK}$ low	− 1	4	ns
$t_{d(CLKL-IACKH)}$	Delay time, CLKOUT low to $\overline{IACK}$ high	− 1	4	ns
$t_{d(A)IACK}$	Delay time, $\overline{IACK}$ low to address valid		2	ns
$t_{h(A)IAQ}$	Hold time, address valid after $\overline{IAQ}$ high	− 2		ns
$t_{h(A)IACK}$	Hold time, address valid after $\overline{IACK}$ high	− 2		ns
$t_{w(IAQL)}$	Pulse duration, $\overline{IAQ}$ low	2H − 2		ns
$t_{w(IACKL)}$	Pulse duration, $\overline{IACK}$ low	2H − 2		ns

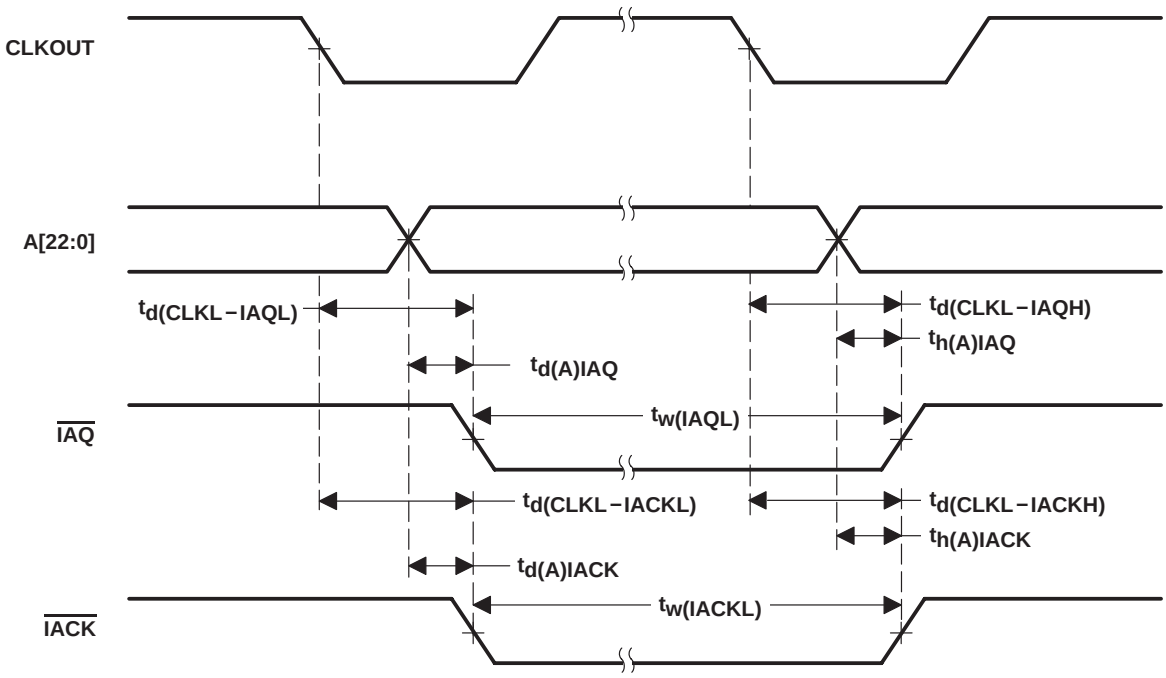


Figure 5−18. Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Timings

5.12 External Flag (XF) and TOUT Timings

Table 5−19 assumes testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−19 and Figure 5−20).

Table 5−19. External Flag (XF) and TOUT Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(XF)}$	Delay time, CLKOUT low to XF high	− 1	4	ns
	Delay time, CLKOUT low to XF low	− 1	4	
$t_{d(TOUTH)}$	Delay time, CLKOUT low to TOUT high	− 1	4	ns
$t_{d(TOUTL)}$	Delay time, CLKOUT low to TOUT low	− 1	4	ns
$t_{w(TOUT)}$	Pulse duration, TOUT	2H − 4		ns

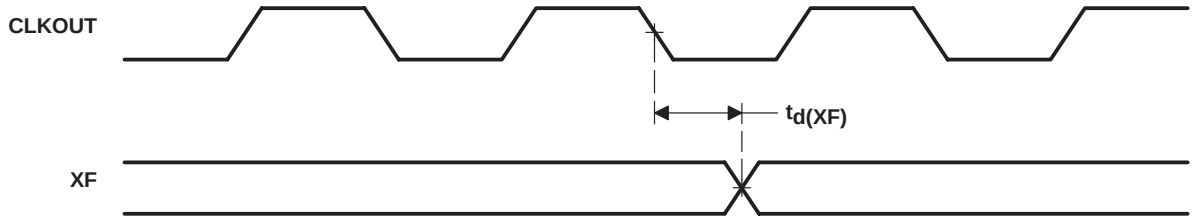


Figure 5−19. External Flag (XF) Timing

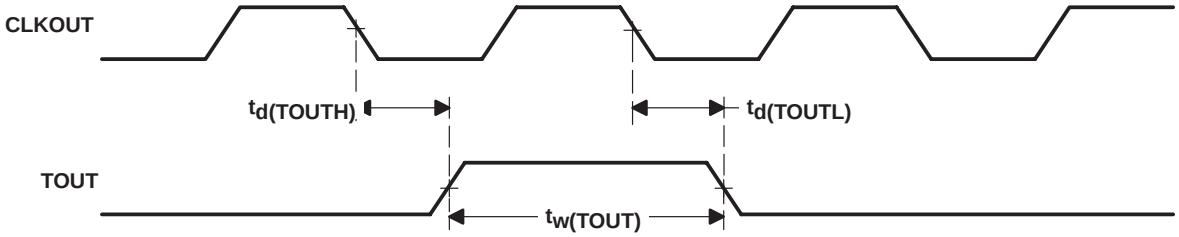


Figure 5−20. TOUT Timing

5.13 Multichannel Buffered Serial Port (McBSP) Timing

5.13.1 McBSP Transmit and Receive Timings

Table 5−20 and Table 5−21 assume testing over recommended operating conditions (see Figure 5−21 and Figure 5−22).

Table 5−20. McBSP Transmit and Receive Timing Requirements†

			MIN	MAX	UNIT
$t_{c(BCKRX)}$	Cycle time, BCLKR/X	BCLKR/X ext	4P‡		ns
$t_{w(BCKRX)}$	Pulse duration, BCLKR/X high or BCLKR/X low	BCLKR/X ext	2P−1‡		ns
$t_{su(BFRH-BCKRL)}$	Setup time, external BFSR high before BCLKR low	BCLKR int	8		ns
		BCLKR ext	1		
$t_{h(BCKRL-BFRH)}$	Hold time, external BFSR high after BCLKR low	BCLKR int	1		ns
		BCLKR ext	2		
$t_{su(BDRV-BCKRL)}$	Setup time, BDR valid before BCLKR low	BCLKR int	7		ns
		BCLKR ext	1		
$t_{h(BCKRL-BDRV)}$	Hold time, BDR valid after BCLKR low	BCLKR int	2		ns
		BCLKR ext	3		
$t_{su(BFXH-BCKXL)}$	Setup time, external BFSX high before BCLKX low	BCLKX int	10		ns
		BCLKX ext	1		
$t_{h(BCKXL-BFXH)}$	Hold time, external BFSX high after BCLKX low	BCLKX int	0		ns
		BCLKX ext	2		
$t_{r(BCKRX)}$	Rise time, BCKR/X	BCLKR/X ext		6	ns
$t_{f(BCKRX)}$	Fall time, BCKR/X	BCLKR/X ext		6	ns

† CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
‡ P = 0.5 * processor clock

Table 5−21. McBSP Transmit and Receive Switching Characteristics†

PARAMETER				MIN	MAX	UNIT
$t_{c(BCKRX)}$	Cycle time, BCLKR/X		BCLKR/X int	4P‡		ns
$t_{w(BCKRXH)}$	Pulse duration, BCLKR/X high		BCLKR/X int	D − 1§	D + 1§	ns
$t_{w(BCKRXL)}$	Pulse duration, BCLKR/X low		BCLKR/X int	C − 1§	C + 1§	ns
$t_{d(BCKRH-BFRV)}$	Delay time, BCLKR high to internal BFSR valid		BCLKR int	− 3	3	ns
			BCLKR ext	0	12	ns
$t_{d(BCKXH-BFXV)}$	Delay time, BCLKX high to internal BFSX valid		BCLKX int	− 1	5	ns
			BCLKX ext	2	10	
$t_{dis(BCKXH-BDXHZ)}$	Disable time, BCLKX high to BDX high impedance following last data bit of transfer		BCLKX int		6	ns
			BCLKX ext		10	
$t_{d(BCKXH-BDXV)}$	Delay time, BCLKX high to BDX valid	DXENA = 0#	BCLKX int	− 1¶	10	ns
			BCLKX ext	2	20	
$t_{d(BFXH-BDXV)}$	Delay time, BFSX high to BDX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode		BFSX int	−1¶	7	ns
			BFSX ext	2	11	

† CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
‡ P = 0.5 * processor clock
§ T = BCLKRX period = (1 + CLKGDV) * 2P
C = BCLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
D = BCLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
¶ Minimum delay times also represent minimum output hold times.
# The transmit delay enable (DXENA) feature of the McBSP is not implemented on the TMS320VC5407/TMS320VC5404.

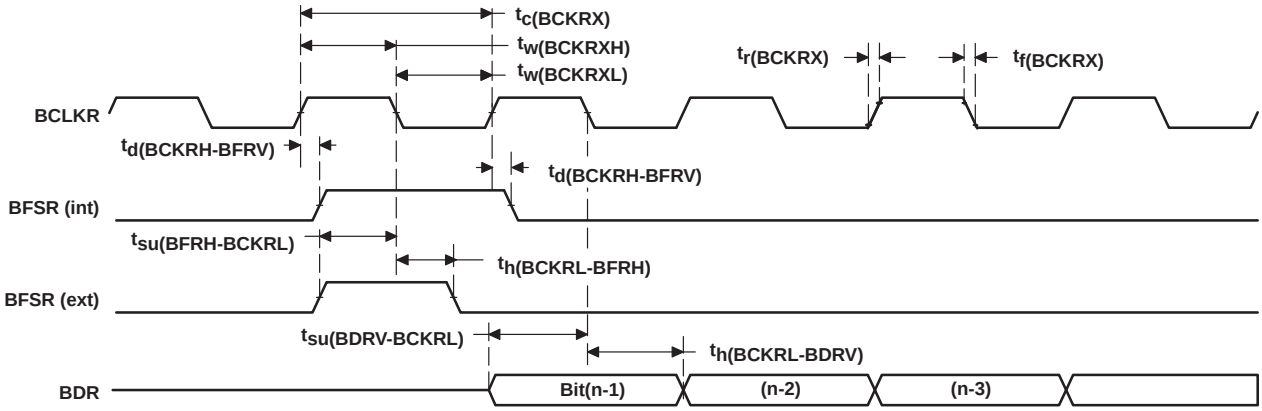


Figure 5−21. McBSP Receive Timings

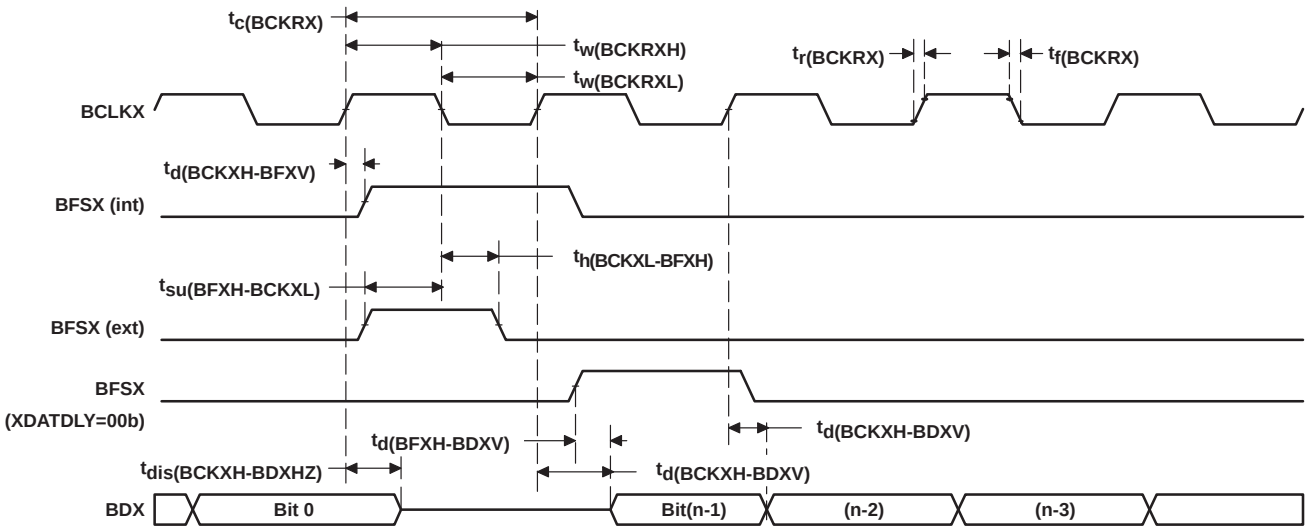


Figure 5−22. McBSP Transmit Timings

5.13.2 McBSP General-Purpose I/O Timing

Table 5−22 and Table 5−23 assume testing over recommended operating conditions (see Figure 5−23).

Table 5−22. McBSP General-Purpose I/O Timing Requirements

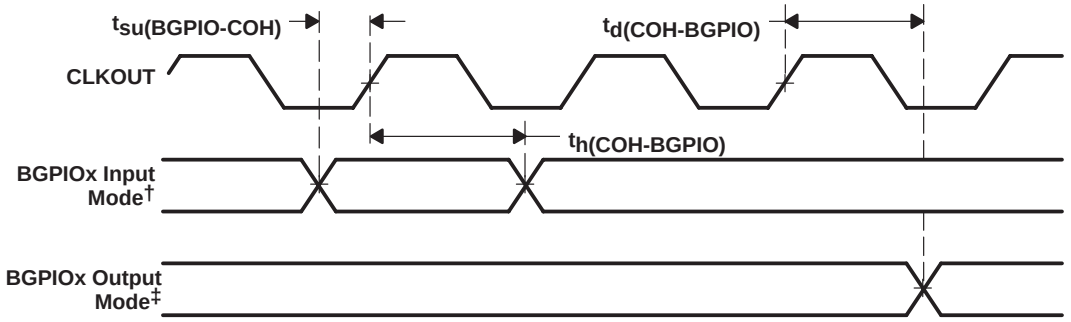
		MIN	MAX	UNIT
$t_{su(BGPIO-COH)}$	Setup time, BGPIOx input mode before CLKOUT high†	7		ns
$t_{h(COH-BGPIO)}$	Hold time, BGPIOx input mode after CLKOUT high†	0		ns

† BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.

Table 5−23. McBSP General-Purpose I/O Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(COH-BGPIO)}$	Delay time, CLKOUT high to BGPIOx output mode‡	− 2	4	ns

‡ BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general-purpose output.



† BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.
‡ BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general-purpose output.

Figure 5−23. McBSP General-Purpose I/O Timings

5.13.3 McBSP as SPI Master or Slave Timing

Table 5−24 to Table 5−31 assume testing over recommended operating conditions (see Figure 5−24, Figure 5−25, Figure 5−26, and Figure 5−27).

Table 5−24. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXL)}$	Setup time, BDR valid before BCLKX low	12		2 − 6P‡		ns
$t_{h(BCKXL-BDRV)}$	Hold time, BDR valid after BCLKX low	4		5 + 12P‡		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock

Table 5−25. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)†

PARAMETER		MASTER§		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXL-BFXL)}$	Hold time, BFSX low after BCLKX low¶	T − 3	T + 4			ns
$t_{d(BFXL-BCKXH)}$	Delay time, BFSX low to BCLKX high#	C − 4	C + 3			ns
$t_{d(BCKXH-BDXV)}$	Delay time, BCLKX high to BDX valid	− 4	5	6P + 2‡	10P + 17‡	ns
$t_{dis(BCKXL-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX low	C − 2	C + 3			ns
$t_{dis(BFXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BFSX high			2P− 4‡	6P + 17‡	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid			4P+ 2‡	8P + 17‡	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock
§ T = BCLKX period = (1 + CLKGDV) * 2P
C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

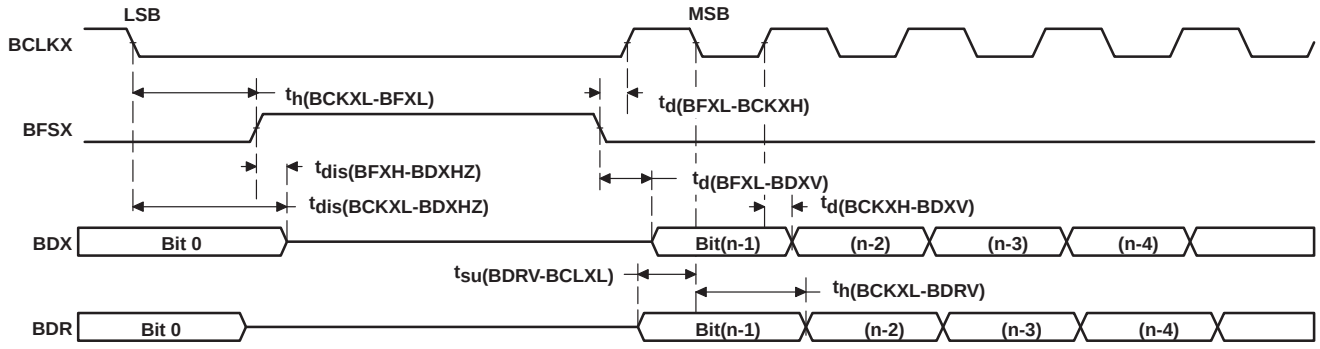


Figure 5−24. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

Table 5−26. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXL)}$	Setup time, BDR valid before BCLKX low	12		2 − 6P‡		ns
$t_{h(BCKXH-BDRV)}$	Hold time, BDR valid after BCLKX high	4		5 + 12P‡		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock

Table 5−27. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)†

PARAMETER		MASTER§		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXL-BFXL)}$	Hold time, BFSX low after BCLKX low¶	C −3	C + 4			ns
$t_{d(BFXL-BCKXH)}$	Delay time, BFSX low to BCLKX high#	T − 4	T + 3			ns
$t_{d(BCKXL-BDXV)}$	Delay time, BCLKX low to BDX valid	− 4	5	6P + 2‡	10P + 17‡	ns
$t_{dis(BCKXL-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX low	− 2	4	6P − 4‡	10P + 17‡	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid	D − 2	D + 4	4P + 2‡	8P + 17‡	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock
§ T = BCLKX period = (1 + CLKGDV) * 2P
C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

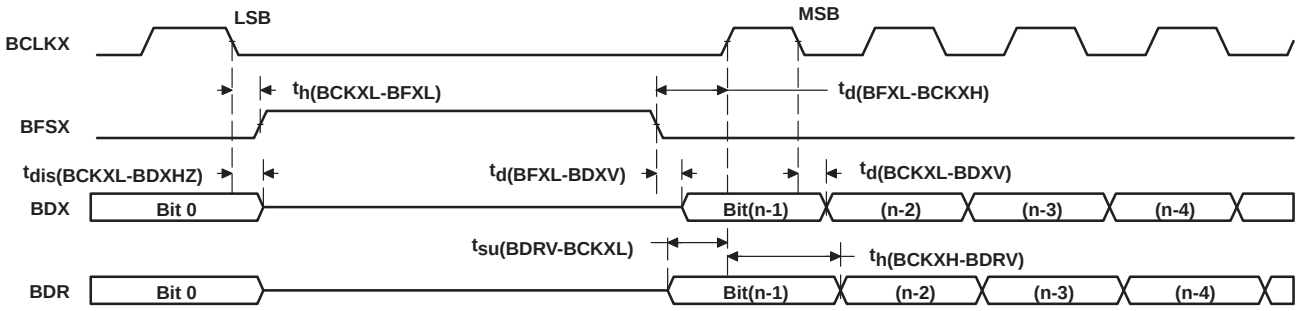


Figure 5−25. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

Table 5−28. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXH)}$	Setup time, BDR valid before BCLKX high	12		2 − 6P‡		ns
$t_{h(BCKXH-BDRV)}$	Hold time, BDR valid after BCLKX high	4		5 + 12P‡		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock

Table 5−29. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)†

PARAMETER		MASTER§		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXH-BFXL)}$	Hold time, BFSX low after BCLKX high¶	T − 3	T + 4			ns
$t_{d(BFXL-BCKXL)}$	Delay time, BFSX low to BCLKX low#	D − 4	D + 3			ns
$t_{d(BCKXL-BDXV)}$	Delay time, BCLKX low to BDX valid	− 4	5	6P + 2‡	10P + 17‡	ns
$t_{dis(BCKXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX high	D − 2	D + 3			ns
$t_{dis(BFXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BFSX high			2P − 4‡	6P + 17‡	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid			4P + 2‡	8P + 17‡	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock
§ T = BCLKX period = (1 + CLKGDV) * 2P
D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

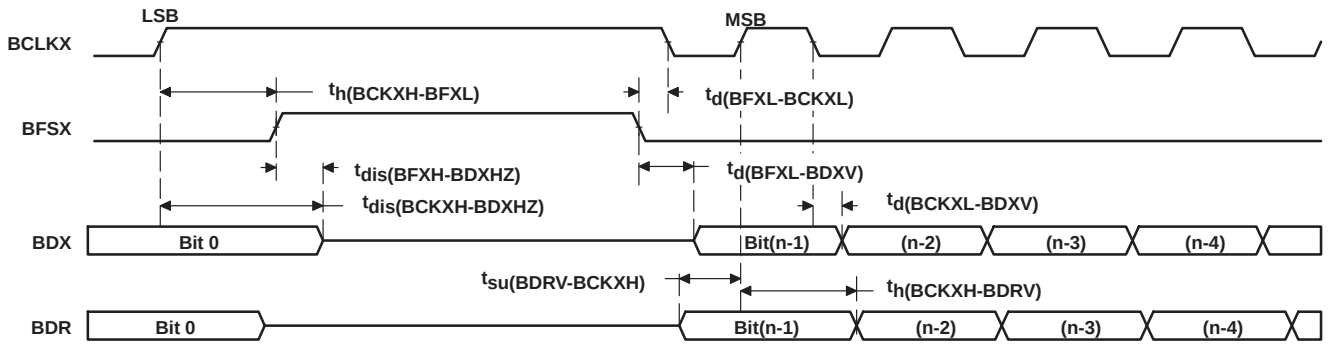


Figure 5−26. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

Table 5−30. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXL)}$	Setup time, BDR valid before BCLKX low	12		2 − 6P‡		ns
$t_{h(BCKXL-BDRV)}$	Hold time, BDR valid after BCLKX low	4		5 + 12P‡		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock

Table 5−31. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)†

PARAMETER		MASTER§		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXH-BFXL)}$	Hold time, BFSX low after BCLKX high¶	D − 3	D + 4			ns
$t_{d(BFXL-BCKXL)}$	Delay time, BFSX low to BCLKX low#	T − 4	T + 3			ns
$t_{d(BCKXH-BDXV)}$	Delay time, BCLKX high to BDX valid	− 4	5	6P + 2‡	10P + 17‡	ns
$t_{dis(BCKXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX high	− 2	4	6P − 4‡	10P + 17‡	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid	C − 2	C + 4	4P + 2‡	8P + 17‡	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock
§ T = BCLKX period = (1 + CLKGDV) * 2P
C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

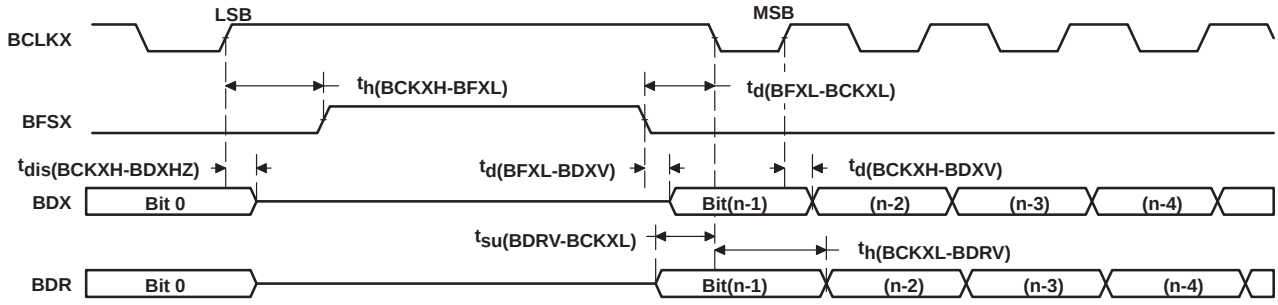


Figure 5−27. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

5.14 Host-Port Interface Timing

5.14.1 HPI8 Mode

Table 5−32 and Table 5−33 assume testing over recommended operating conditions and P = 0.5 * processor clock (see Figure 5−28 through Figure 5−31). In the following tables, DS refers to the logical OR of $\overline{HCS}$, $\overline{HDS1}$, and $\overline{HDS2}$. HD refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.). HAD stands for HCNTL0, HCNTL1, and HR/$\overline{W}$.

Table 5−32. HPI8 Mode Timing Requirements

		MIN	MAX	UNIT
$t_{su(HBV-DSL)}$	Setup time, HBIL valid before DS low (when $\overline{HAS}$ is not used), or HBIL valid before $\overline{HAS}$ low	6		ns
$t_{h(DSL-HBV)}$	Hold time, HBIL valid after DS low (when $\overline{HAS}$ is not used), or HBIL valid after $\overline{HAS}$ low	3		ns
$t_{su(HSL-DSL)}$	Setup time, $\overline{HAS}$ low before DS low	8		ns
$t_{w(DSL)}$	Pulse duration, DS low	13		ns
$t_{w(DSH)}$	Pulse duration, DS high	7		ns
$t_{su(HDV-DSH)}$	Setup time, HD valid before DS high, HPI write	3		ns
$t_{h(DSH-HDV)W}$	Hold time, HD valid after DS high, HPI write	2		ns
$t_{su(GPIO-COH)}$	Setup time, HDx input valid before CLKOUT high, HDx configured as general-purpose input	3		ns
$t_{h(GPIO-COH)}$	Hold time, HDx input valid before CLKOUT high, HDx configured as general-purpose input	0		ns

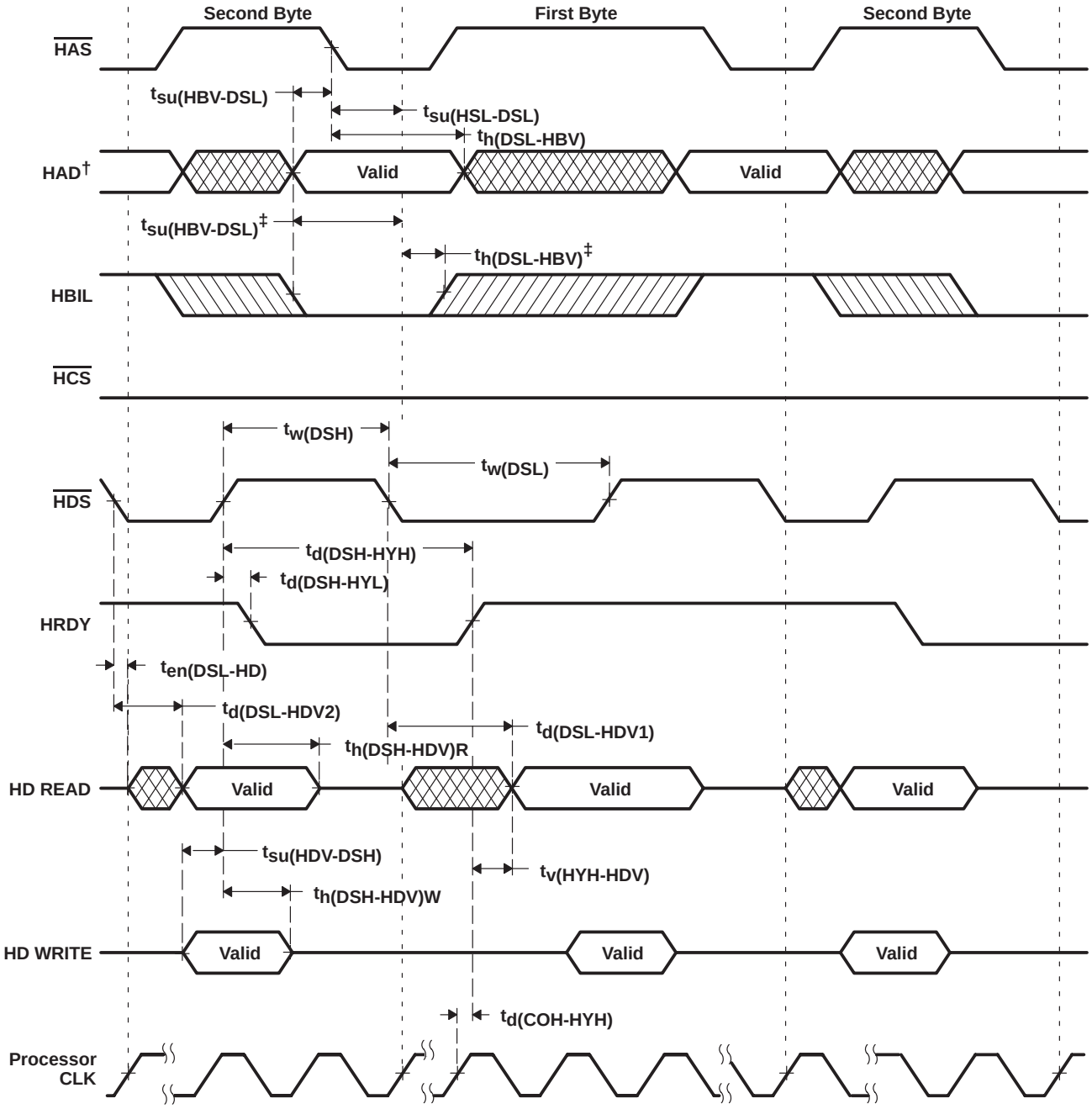
Table 5−33. HPI8 Mode Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{en(DSL-HD)}$	Enable time, HD driven from DS low		0	10	ns
$t_{d(DSL-HDV1)}$	Delay time, DS low to HD valid for first byte of an HPI read	Case 1a: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)} < I8H$†		18P+10−$t_{w(DSH)}$	ns
		Case 1b: Memory accesses when DMAC is active in 32-bit mode and $t_{w(DSH)} \geq I8H$†		36P+10−$t_{w(DSH)}$	
		Case 1c: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)} \geq I8H$†		10	
		Case 1d: Memory accesses when DMAC is active in 32-bit mode and $t_{w(DSH)} \geq I8H$†		10	
		Case 2a: Memory accesses when DMAC is inactive and $t_{w(DSH)} < 10H$†		10P+15−$t_{w(DSH)}$	
		Case 2b: Memory accesses when DMAC is inactive and $t_{w(DSH)} \geq 10H$†		10	
		Case 3: Register accesses		10	
$t_{d(DSL-HDV2)}$	Delay time, DS low to HD valid for second byte of an HPI read			10	ns
$t_{h(DSH-HDV)R}$	Hold time, HD valid after DS high, for a HPI read		2		ns
$t_{v(HYH-HDV)}$	Valid time, HD valid after HRDY high			2	ns
$t_{d(DSH-HYL)}$	Delay time, DS high to HRDY low‡			8	ns
$t_{d(DSH-HYH)}$	Delay time, DS high to HRDY high‡	Case 1a: Memory accesses when DMAC is active in 16-bit mode†		18P+6	ns
		Case 1b: Memory accesses when DMAC is active in 32-bit mode†		36P+6	
		Case 2: Memory accesses when DMAC is inactive†		10P+6	
		Case 3: Write accesses to HPIC register§		6P+6	
$t_{d(HCS-HRDY)}$	Delay time, $\overline{HCS}$ low/high to HRDY low/high			6	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT high to HRDY high			9	ns
$t_{d(COH-HTX)}$	Delay time, CLKOUT high to $\overline{HINT}$ change			6	ns
$t_{d(COH-GPIO)}$	Delay time, CLKOUT high to HDx output change. HDx is configured as a general-purpose output			5	ns

† DMAC stands for direct memory access controller (DMAC). The HPI8 shares the internal DMA bus with the DMAC, thus HPI8 access times are affected by DMAC activity.

‡ The HRDY output is always high when the $\overline{HCS}$ input is high, regardless of DS timings.

§ This timing applies when writing a one to the DSPINT bit or $\overline{HINT}$ bit of the HPIC register. All other writes to the HPIC occur asynchronously, and do not cause HRDY to be deasserted.



† HAD refers to HCNTL0, HCNTL1, and HR/$\overline{W}$.
‡ When $\overline{HAS}$ is not used ($\overline{HAS}$ always high)

Figure 5−28. Using $\overline{HDS}$ to Control Accesses ($\overline{HCS}$ Always Low)

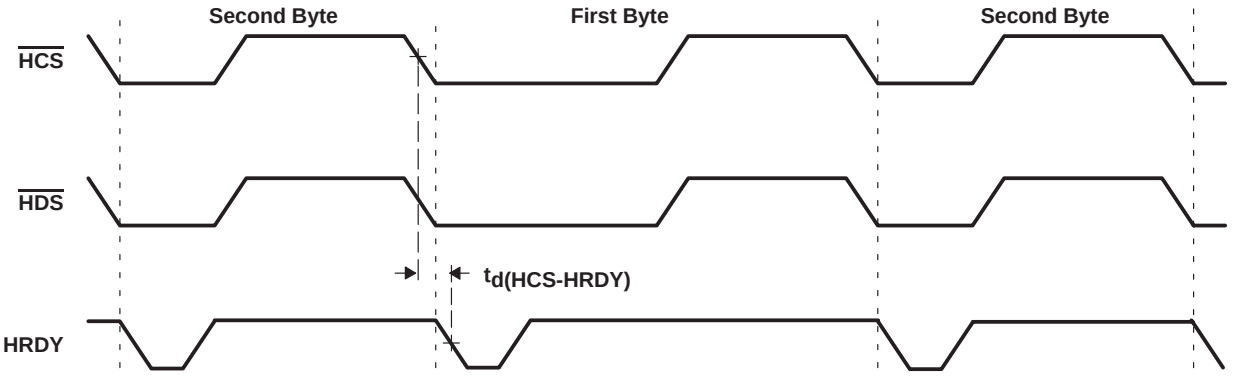


Figure 5−29. Using $\overline{\text{HCS}}$ to Control Accesses

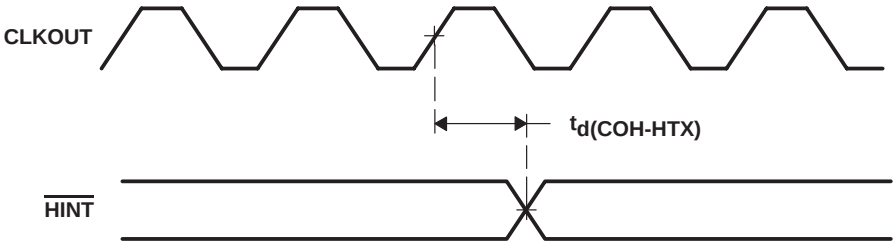
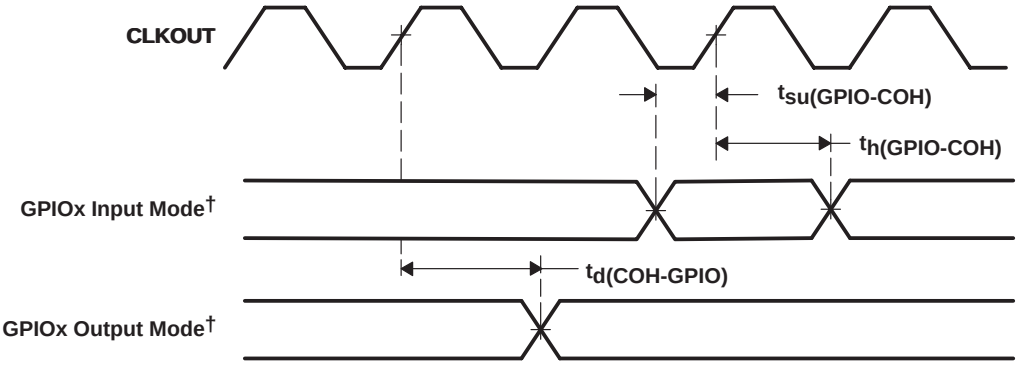


Figure 5−30. $\overline{\text{HINT}}$ Timing



† GPIOx refers to HD0, HD1, HD2, ...HD7, when the HD bus is configured for general-purpose input/output (I/O).

Figure 5−31. GPIOx† Timings

5.14.2 HPI16 Mode

Table 5−34 and Table 5−35 assume testing over recommended operating conditions and P = 0.5 * processor clock (see Figure 5−32 through Figure 5−34). In the following tables, DS refers to the logical OR of $\overline{HCS}$, $\overline{HDS1}$, and $\overline{HDS2}$, and HD refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.). These timings are shown assuming that $\overline{HDS}$ is the signal controlling the transfer. See the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for additional information.

Table 5−34. HPI16 Mode Timing Requirements

				MIN	MAX	UNIT
$t_{su(HBV-DSL)}$	Setup time, HR/$\overline{W}$ valid before DS falling edge			6		ns
$t_{h(DSL-HBV)}$	Hold time, HR/$\overline{W}$ valid after DS falling edge			5		ns
$t_{su(HAV-DSH)}$	Setup time, address valid before DS rising edge (write)			5		ns
$t_{su(HAV-DSL)}$	Setup time, address valid before DS falling edge (read)			−(4P − 6)		ns
$t_{h(DSH-HAV)}$	Hold time, address valid after DS rising edge			1		ns
tw(DSL)	Pulse duration, DS low			30		ns
$t_{w(DSH)}$	Pulse duration, DS high			10		ns
$t_{c(DSH-DSH)}$	Cycle time, DS rising edge to next DS rising edge	Memory accesses with no DMA activity.	Reads	10P + 30		ns
			Writes	10P + 10		
		Memory accesses with 16-bit DMA activity.	Reads	16P + 30		
			Writes	16P + 10		
		Memory accesses with 32-bit DMA activity.	Reads	24P + 30		
			Writes	24P + 10		
$t_{su(HDV-DSH)W}$	Setup time, HD valid before DS rising edge			8		ns
$t_{h(DSH-HDV)W}$	Hold time, HD valid after DS rising edge, write			2		ns

Table 5−35. HPI16 Mode Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(DSL-HDD)}$	Delay time, DS low to HD driven		0	10	ns
$t_{d(DSL-HDV1)}$	Delay time, DS low to HD valid for first word of an HPI read	Case 1a: Memory accesses initiated immediately following a write when DMAC is active in 16-bit mode and $t_{w(DSH)}$ was < 18H		32P + 20 − $t_{w(DSH)}$	ns
		Case 1b: Memory accesses not immediately following a write when DMAC is active in 16-bit mode		16P + 20	
		Case 1c: Memory accesses initiated immediately following a write when DMAC is active in 32-bit mode and $t_{w(DSH)}$ was < 26H		48P + 20 − $t_{w(DSH)}$	
		Case 1d: Memory access not immediately following a write when DMAC is active in 32-bit mode		24P + 20	
		Case 2a: Memory accesses initiated immediately following a write when DMAC is inactive and $t_{w(DSH)}$ was < 10H		20P + 20 − $t_{w(DSH)}$	
		Case 2b: Memory accesses not immediately following a write when DMAC is inactive		10P + 20	
$t_{d(DSH-HYH)}$	Delay time, DS high to HRDY high	Memory writes when no DMA is active		10P + 5	ns
		Memory writes with one or more 16-bit DMA channels active		16P + 5	
		Memory writes with one or more 32-bit DMA channels active		24P + 5	
$t_{v(HYH-HDV)}$	Valid time, HD valid after HRDY high			7	ns
$t_{h(DSH-HDV)R}$	Hold time, HD valid after DS rising edge, read		1	6	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT rising edge to HRDY high			5	ns
$t_{d(DSL-HYL)}$	Delay time, DS low to HRDY low			12	ns
$t_{d(DSH-HYL)}$	Delay time, DS high to HRDY low			12	ns

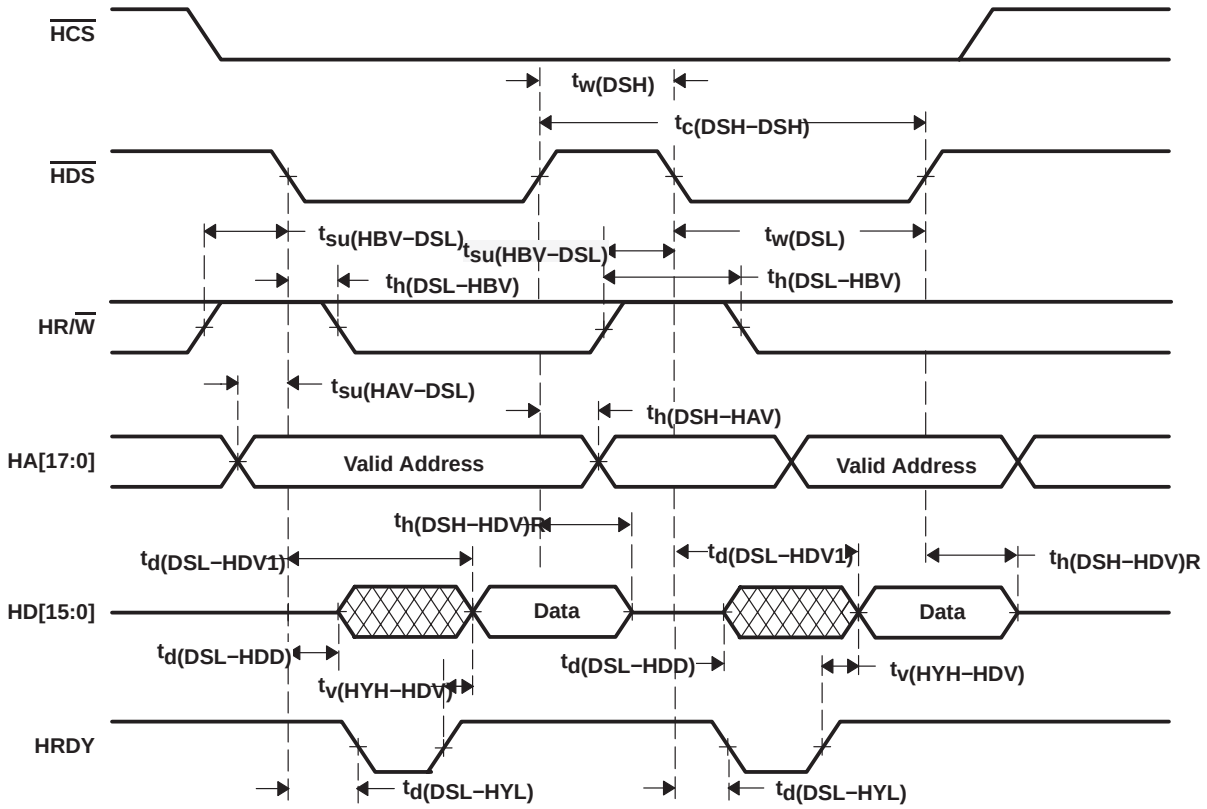


Figure 5−32. Nonmultiplexed Read Timings

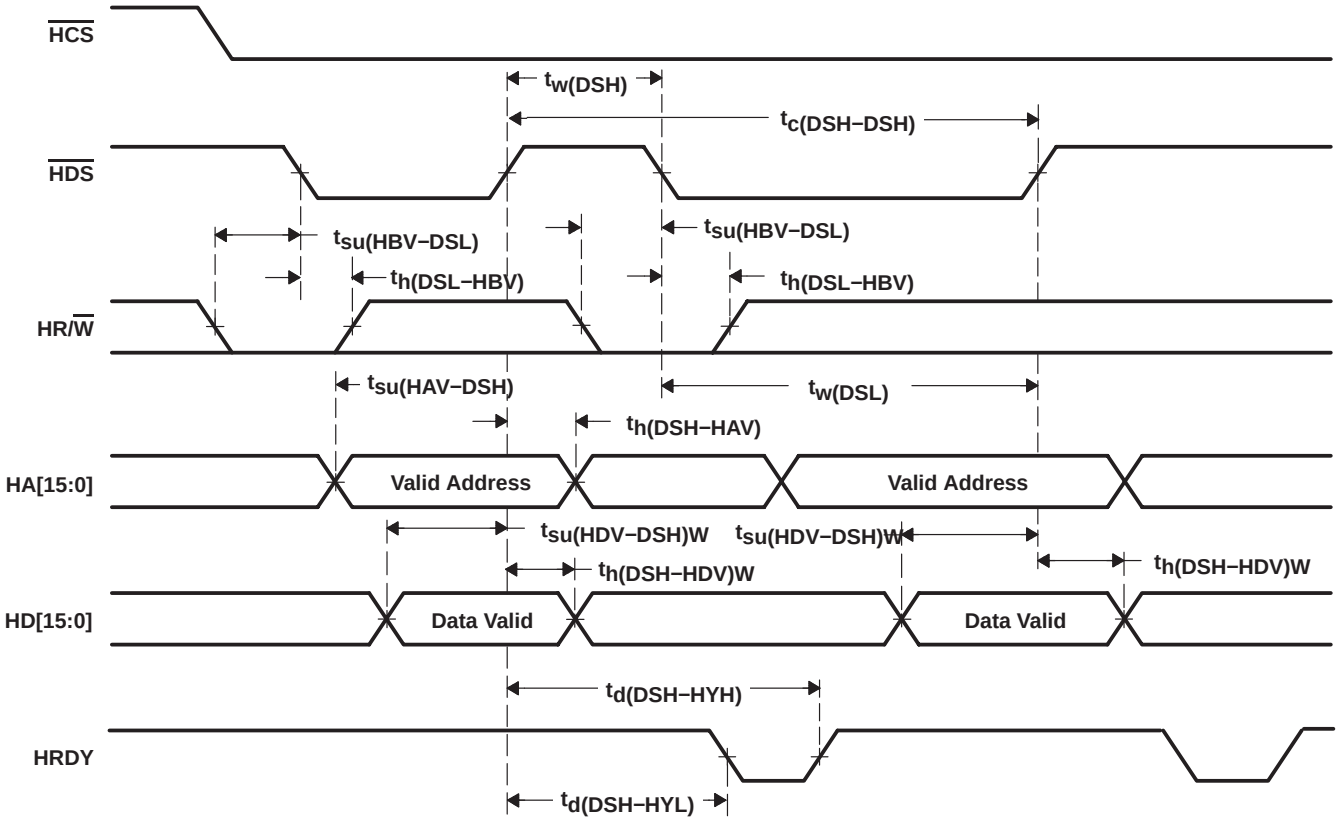


Figure 5−33. Nonmultiplexed Write Timings

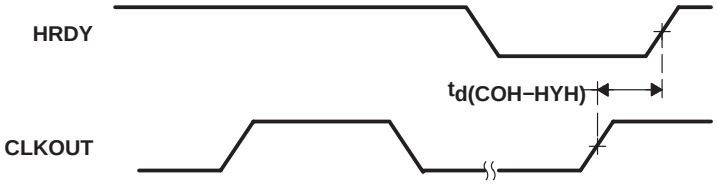


Figure 5−34. HRDY Relative to CLKOUT

5.15 UART Timing

Table 5−36 to Table 5−37 assume testing over recommended operating conditions (see Figure 5−35).

Table 5−36. UART Timing Requirements

		MIN	MAX	UNIT
$t_{w(UDB)R}$	Pulse width, receive data bit	0.99U†	1.01U†	ns
$t_{w(USB)R}$	Pulse width, receive start bit	0.99U†	1.01U†	ns

† U = UART baud time = 1/programmed baud rate

Table 5−37. UART Switching Characteristics

PARAMETER		MIN	MAX	UNIT
f_{baud}	Maximum programmable baud rate		5	MHz
$t_{w(UDB)X}$	Pulse width, transmit data bit	U − 2†	U + 2†	ns
$t_{w(USB)X}$	Pulse width, transmit start bit	U − 2†	U + 2†	ns

† U = UART baud time = 1/programmed baud rate

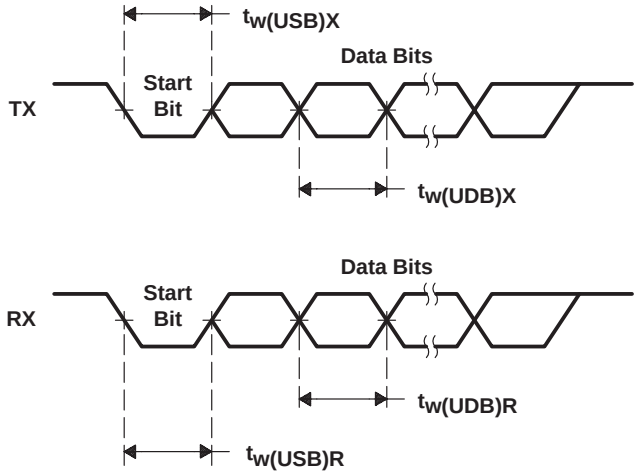


Figure 5−35. UART Timings

6 Mechanical Data

6.1 Package Thermal Resistance Characteristics

Table 6−1 provides the estimated thermal resistance characteristics for the recommended package types used on the TMS320VC5407/TMS320VC5404 DSP.

Table 6−1. Thermal Resistance Characteristics

PARAMETER	GGU PACKAGE	PGE PACKAGE	UNIT
$R_{\Theta JA}$	38	56	°C/W
$R_{\Theta JC}$	5	5	°C/W

6.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMS320VC5404PGE	Active	Production	LQFP (PGE) | 144	60 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 0	320VC5404 PGE TMS
TMS320VC5404PGE.A	Active	Production	LQFP (PGE) | 144	60 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 110	320VC5404 PGE TMS
TMS320VC5407PGE	Active	Production	LQFP (PGE) | 144	60 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 0	320VC5407 PGE TMS
TMS320VC5407PGE.A	Active	Production	LQFP (PGE) | 144	60 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 100	320VC5407 PGE TMS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

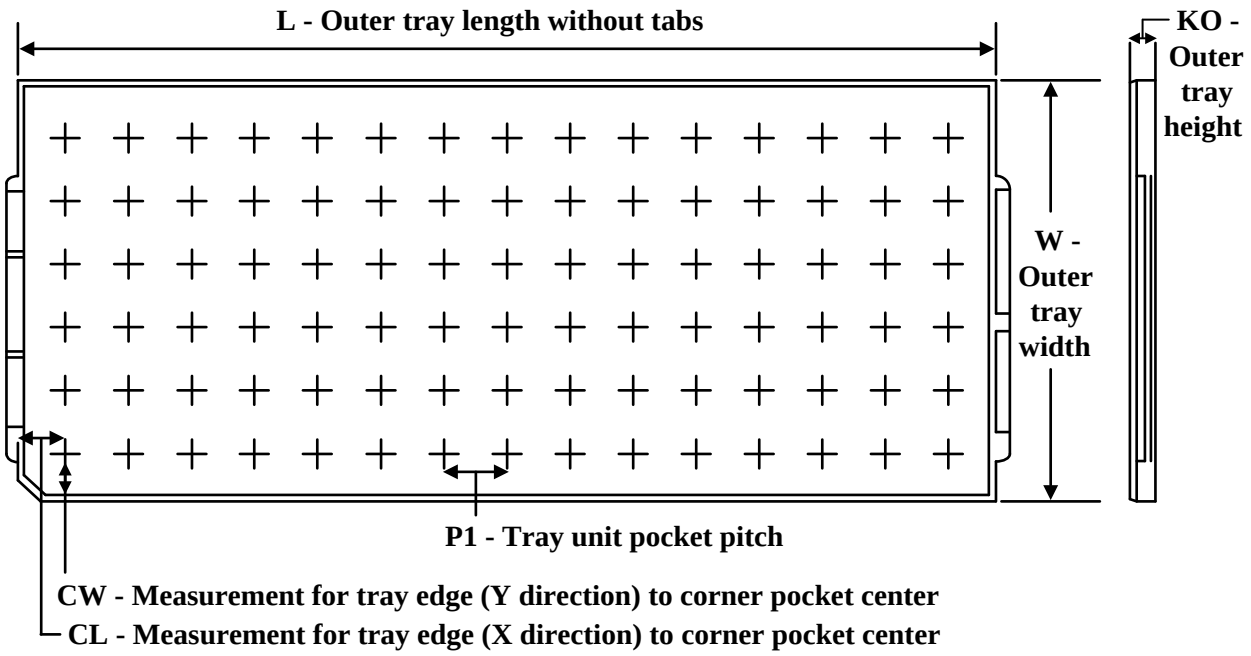
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



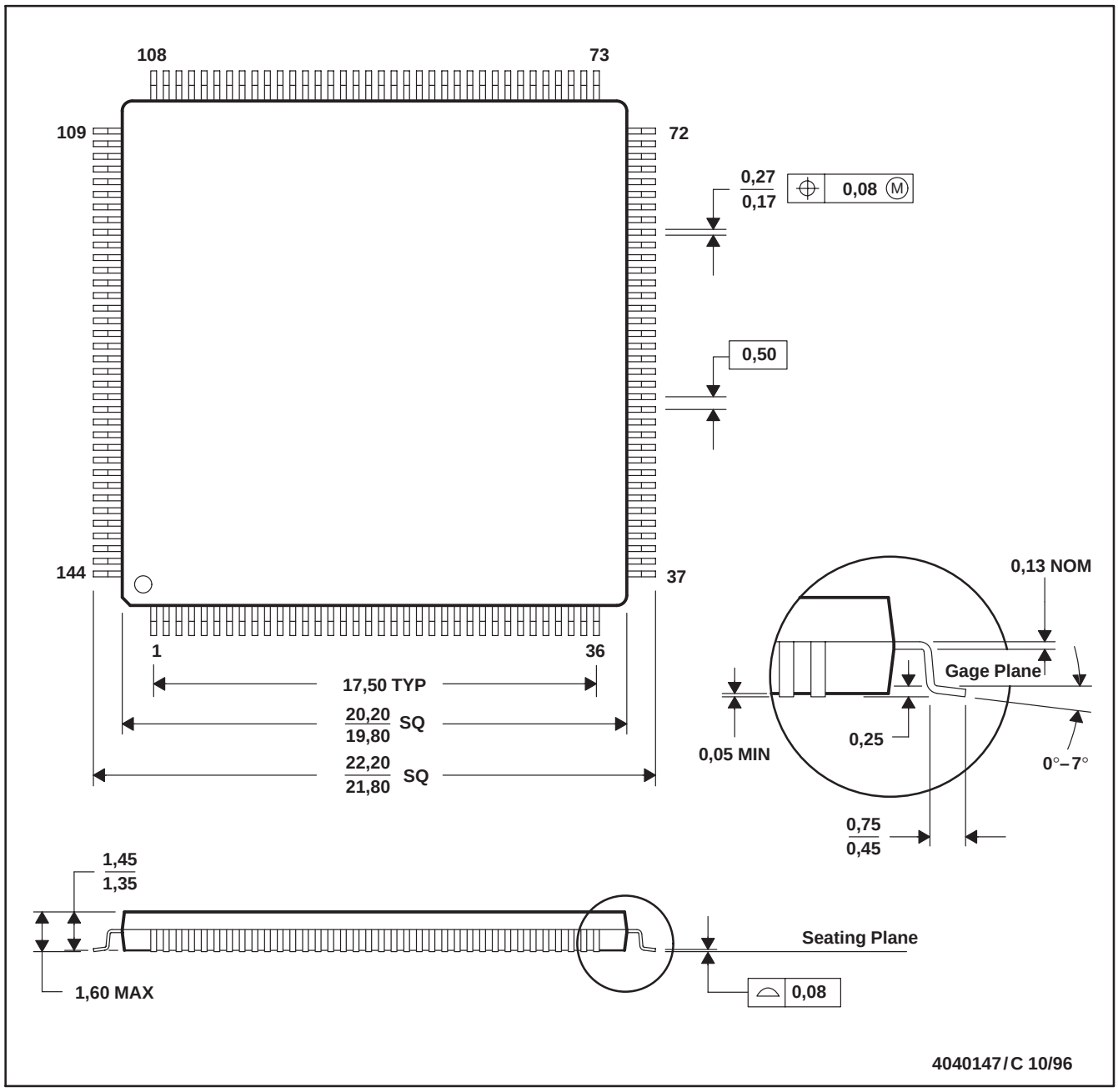
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TMS320VC5404PGE	PGE	LQFP	144	60	5X12	150	315	135.9	7620	25.4	17.8	17.55
TMS320VC5404PGE.A	PGE	LQFP	144	60	5X12	150	315	135.9	7620	25.4	17.8	17.55
TMS320VC5407PGE	PGE	LQFP	144	60	5X12	150	315	135.9	7620	25.4	17.8	17.55
TMS320VC5407PGE.A	PGE	LQFP	144	60	5X12	150	315	135.9	7620	25.4	17.8	17.55

MTQF017A – OCTOBER 1994 – REVISED DECEMBER 1996

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



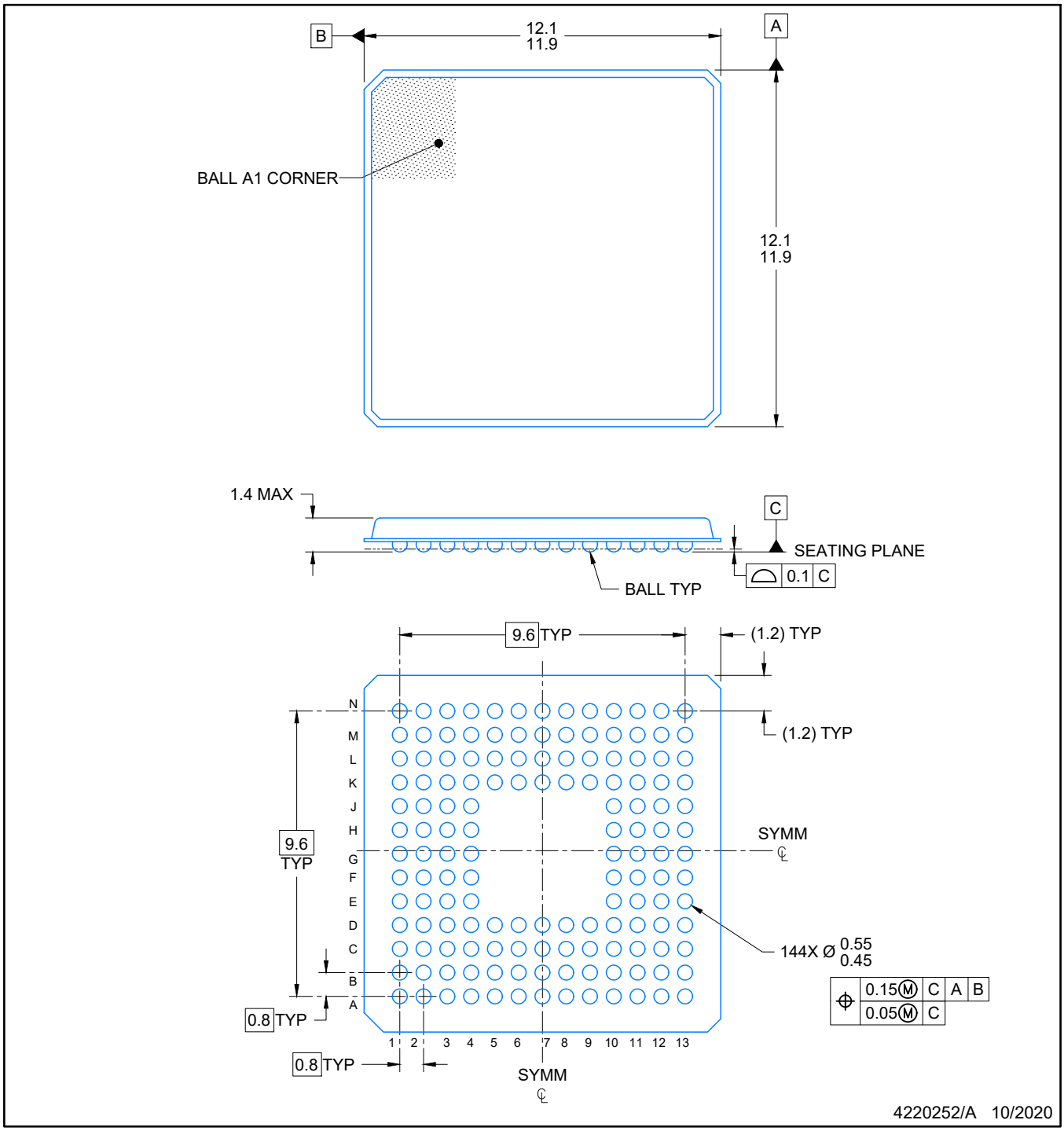
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PACKAGE OUTLINE

ZGU0144A

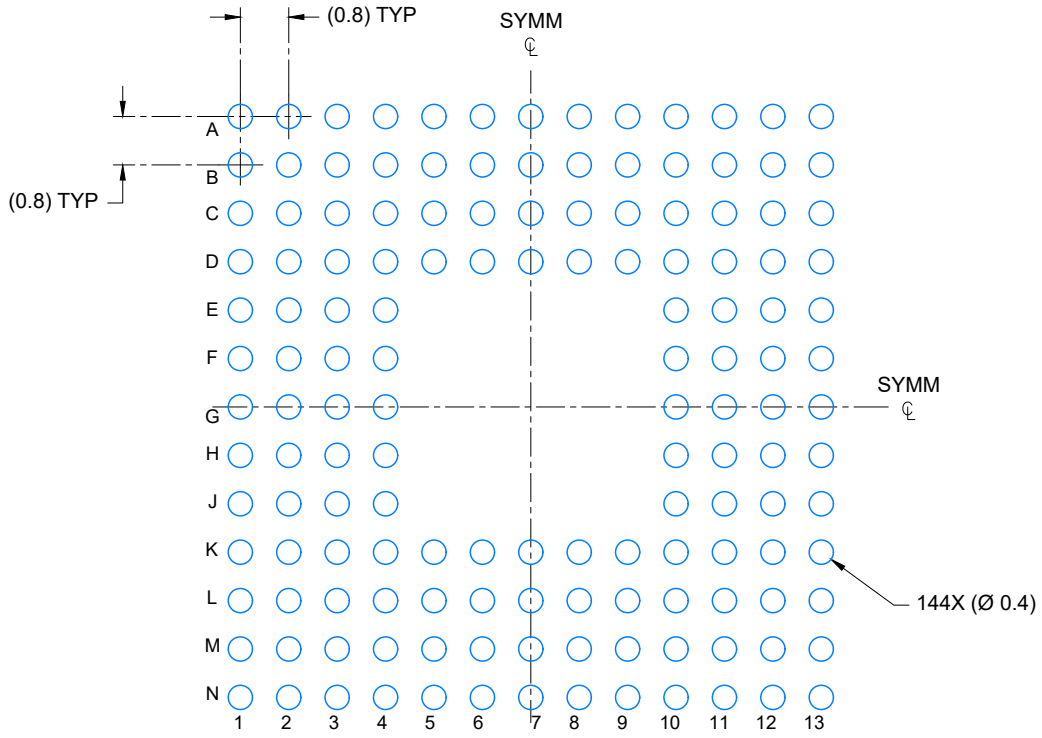
UBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY

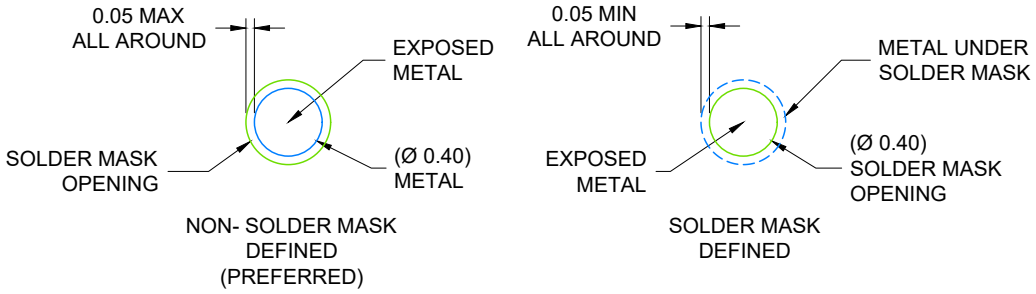


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-Free ball design.



LAND PATTERN EXAMPLE
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

4220252/A 10/2020

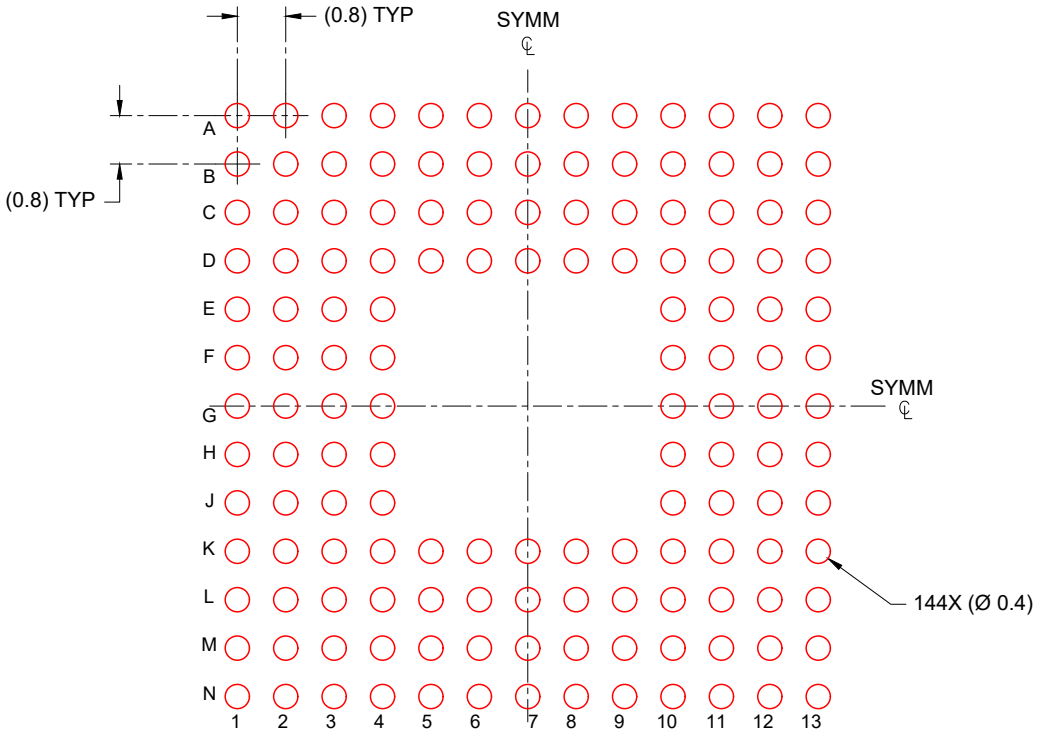
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.

EXAMPLE STENCIL DESIGN

UBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

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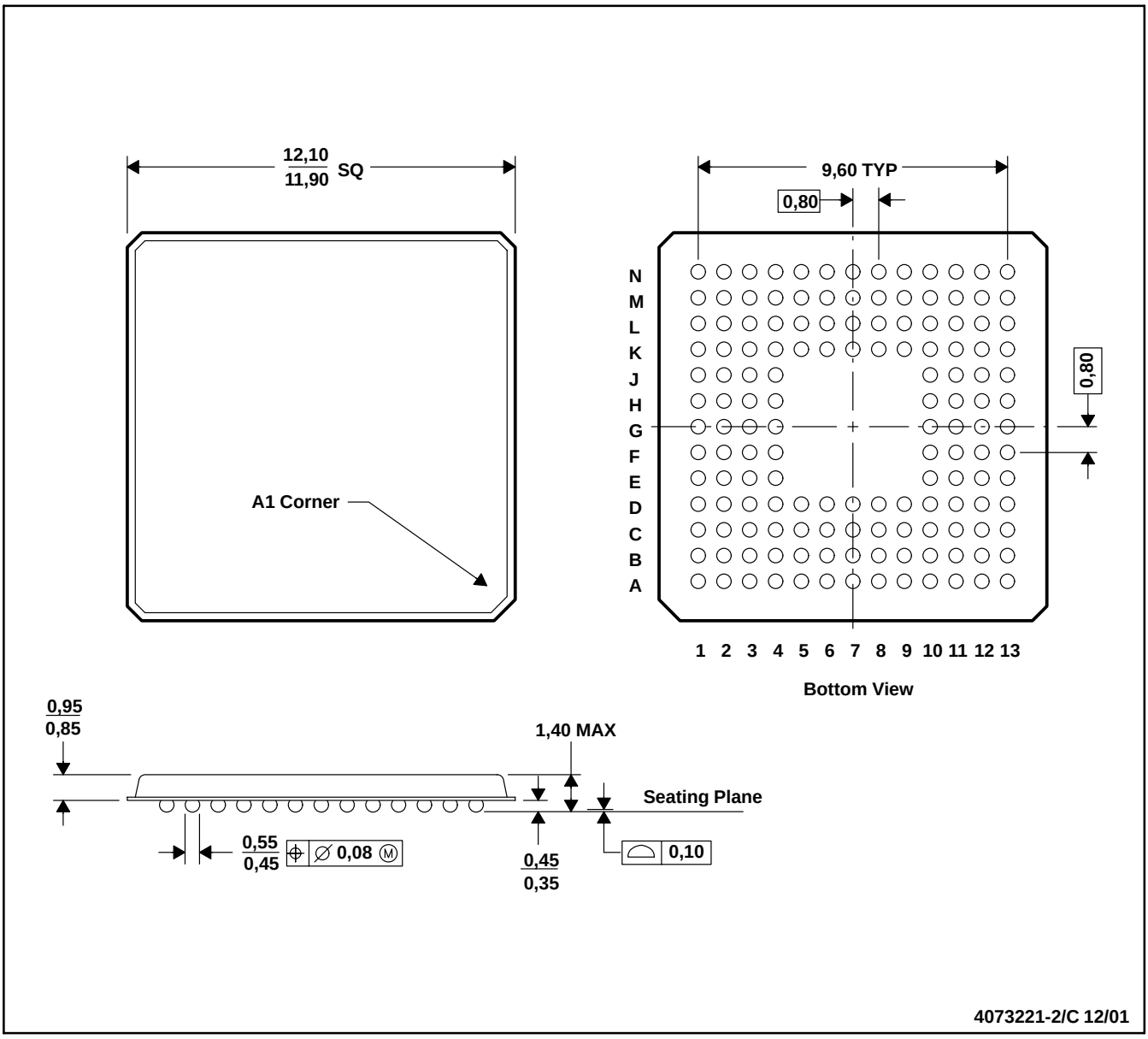
NOTES: (continued)

5. For alternate stencil design recommendations see IPC-7525 or board assembly site preference.

MPBG021C – DECEMBER 1996 – REVISED MAY 2002

GGU (S–PBGA–N144) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice
C. MicroStar BGA™ configuration

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