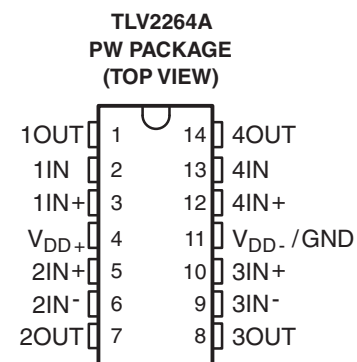
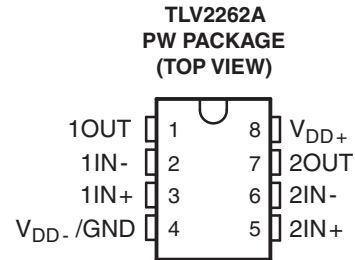


## Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

### FEATURES

- Qualified for Automotive Applications
- Output Swing Includes Both Supply Rails
- Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Low Power . . . 500 μA Max
- Common-Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Voltage . . . 950 μV Max at T<sub>A</sub> = 25°C
- Wide Supply Voltage Range . . . 2.7 V to 8 V
- Macromodel Included



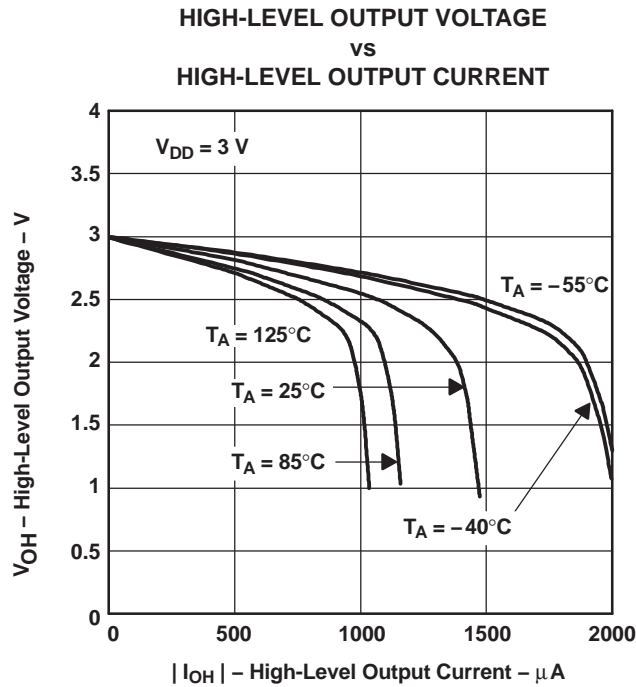
### DESCRIPTION

The TLV2262 and TLV2264 are dual and quad low voltage operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single or split supply applications. The TLV226x family offers a compromise between the micropower TLV225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. This family is fully characterized at 3 V and 5 V and is optimized for low-voltage applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 μA (typ) of supply current per amplifier.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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The TLV226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV226xA family is available and has a maximum input offset voltage of 950  $\mu$ V.

The TLV2262/4 also makes great upgrades to the TLV2332/4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high density, battery-powered equipment.

**ORDERING INFORMATION<sup>(1)</sup>**

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	TSSOP – PW (8 pin)	Reel of 2000	TLV2262AQPWRQ1	TQ262A
	TSSOP – PW (14 pin)	Reel of 2000	TLV2264AQPWRQ1	P2264AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)

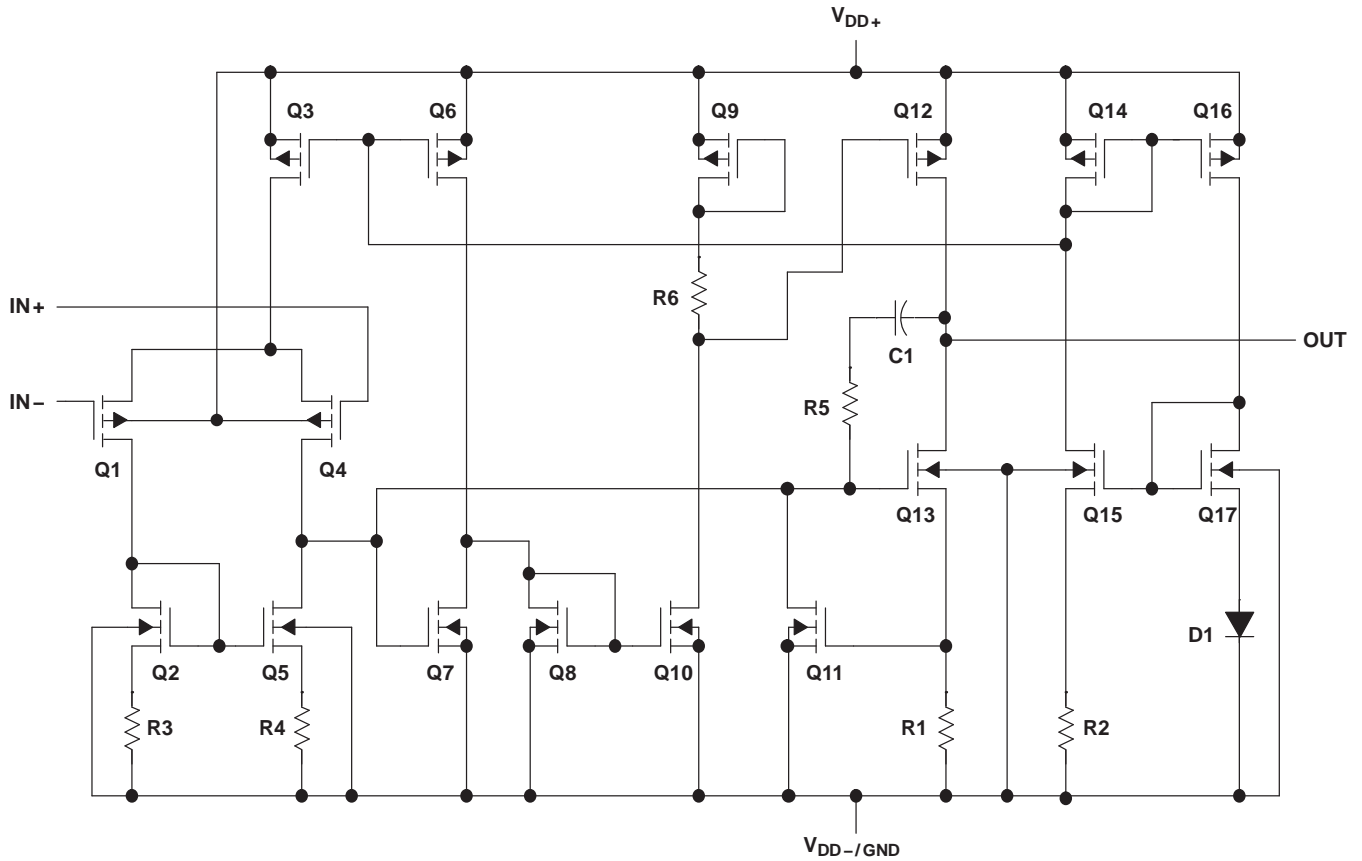


Table 1. Actual Device Component Count

COMPONENT	TLV2262	TLV2264
Transistors	38	76
Resistors	28	54
Diodes	9	18
Capacitors	3	6

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

V <sub>DD</sub>	Supply voltage <sup>(2)</sup>	–0.3 V to 16 V
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>	±V <sub>DD</sub>
V <sub>I</sub>	Input voltage range	(V <sub>DD–</sub> – 0.3 V) to V <sub>DD+</sub>
I <sub>I</sub>	Input current, any input	±5 mA
I <sub>O</sub>	Output current	±50 mA
	Total current into V <sub>DD+</sub>	±50 mA
	Total current out of V <sub>DD–</sub>	±50 mA
	Duration of short-circuit current (at or below) 25°C <sup>(4)</sup>	Unlimited
P <sub>D</sub>	Continuous total power dissipation	See Dissipation Rating Table
T <sub>A</sub>	Operating free-air temperature range	–40°C to 125°C
T <sub>stg</sub>	Storage temperature range	–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to V<sub>DD–</sub>.
- (3) Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below V<sub>DD–</sub> – 0.3 V.
- (4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

### DISSIPATION RATINGS

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
PW-8	525 mW	4.2 mW/°C	273 mW	105 mW
PW-14	700 mW	5.6 mW/°C	364 mW	140 mW

### RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
V <sub>DD±</sub> Supply voltage <sup>(1)</sup>	2.7	8	V
V <sub>I</sub> Input voltage	V <sub>DD–</sub>	V <sub>DD+</sub> – 1.3	V
V <sub>IC</sub> Common-mode input voltage	V <sub>DD–</sub>	V <sub>DD+</sub> – 1.3	V
T <sub>A</sub> Operating free-air temperature	–40	125	°C

- (1) All voltage values, except differential voltages, are with respect to V<sub>DD–</sub>.

**TLV2262A ELECTRICAL CHARACTERISTICS**
 $V_{DD} = 3\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{DD\pm} = \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		300	950	mV
				Full range			1500	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_{DD\pm} = \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C to 125°C		2		$\mu\text{V}/^\circ\text{C}$
	Input offset voltage long-term drift <sup>(1)</sup>	$V_{DD\pm} = \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		0.003		$\mu\text{V}/\text{mo}$
$I_{IO}$	Input offset current	$V_{DD\pm} = \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		0.5	60	pA
				125°C			800	
$I_{IB}$	Input bias current	$V_{DD\pm} = \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		1	60	pA
				125°C			800	
$V_{ICR}$	Common-mode input voltage range	$R_S = 50\ \Omega$ , $ V_{IO}  \leq 5\text{ mV}$		25°C	0 to 2	-0.3 to 2.2		V
				Full range	0 to 1.7			
$V_{OH}$	High-level output voltage			25°C		2.99		V
				25°C		2.85		
				Full range		2.82		
				25°C		2.7		
$V_{OL}$	Low-level output voltage	$V_{IC} = 1.5\text{ V}$		25°C		10		mV
				25°C		100	150	
				Full range			165	
				25°C		200	300	
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}$ , $V_O = 1\text{ V to }2\text{ V}$		25°C		60	100	V/mV
				Full range		25		
				25°C		100		
				Full range			300	
$r_{i(d)}$	Differential input resistance			25°C		$10^{12}$		$\Omega$
$r_{i(c)}$	Common-mode input resistance			25°C		$10^{12}$		$\Omega$
$C_{i(c)}$	Common-mode input capacitance	$f = 10\text{ kHz}$		25°C		8		pF
$Z_o$	Closed-loop output impedance	$f = 100\text{ kHz}$ , $A_V = 10$		25°C		270		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}$ , $V_O = 1.5\text{ V}$ , $R_S = 50\ \Omega$		25°C		65	77	dB
				Full range		60		
$k_{SVR}$	Supply voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 2.7\text{ V to }8\text{ V}$ , $V_{IC} = V_{DD}/2$ , No load		25°C		80	100	dB
				Full range		80		
$I_{DD}$	Supply current	$V_O = 1.5\text{ V}$ , No load		25°C		400	500	$\mu\text{A}$
				Full range			500	

(1) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

(2) Referenced to 1.5 V

**TLV2262A OPERATING CHARACTERISTICS**

V<sub>DD</sub> = 3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V <sub>O</sub> = 0.5 V to 1.7 V, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	0.35	0.55		V/μs
			Full range	0.25			
V <sub>n</sub>	Equivalent input noise voltage	f = 10 Hz	25°C	43			nV/√Hz
		f = 1 kHz	25°C	12			
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C	0.6			μV
		f = 0.1 Hz to 10 Hz	25°C	1			
I <sub>n</sub>	Equivalent input noise current		25°C	0.6			fA/√Hz
THD+N	Total harmonic distortion plus noise	V <sub>O</sub> = 0.5 V to 2.5 V, f = 20 kHz, R <sub>L</sub> = 50 kΩ <sup>(1)</sup>	A <sub>V</sub> = 1	25°C	0.03		%
			A <sub>V</sub> = 10	25°C	0.05		
	Gain-bandwidth product	f = 1 kHz, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	0.67			MHz
B <sub>OM</sub>	Maximum output-swing bandwidth	V <sub>O(PP)</sub> = 1 V, A <sub>V</sub> = 1, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	395			kHz
t <sub>s</sub>	Settling time	A <sub>V</sub> = -1, Step = 1 V to 2 V, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	To 0.1%	25°C	5.6		μs
			To 0.01%	25°C	12.5		
φ <sub>m</sub>	Phase margin at unity gain	R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	55			°
G <sub>m</sub>	Gain margin	R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	11			dB

(1) Referenced to 1.5 V

**TLV2262A ELECTRICAL CHARACTERISTICS**
 $V_{DD} = 5\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		300	950	mV
				Full range			1500	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C to 125°C		2		$\mu\text{V}/^\circ\text{C}$
	Input offset voltage long-term drift <sup>(1)</sup>	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		0.003		$\mu\text{V}/\text{mo}$
$I_{IO}$	Input offset current	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		0.5	60	pA
				125°C			800	
$I_{IB}$	Input bias current	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		1	60	pA
				125°C			800	
$V_{ICR}$	Common-mode input voltage range	$R_S = 50\ \Omega$ , $ V_{IO}  \leq 5\text{ mV}$		25°C	0 to 4	-0.3 to 4.2		V
				Full range	0 to 3.5			
$V_{OH}$	High-level output voltage			25°C		4.99		V
				25°C	$I_{OH} = -100\ \mu\text{A}$	4.85	4.94	
				Full range		4.82		
				25°C	$I_{OH} = -400\ \mu\text{A}$	4.7	4.85	
$V_{OL}$	Low-level output voltage	$V_{IC} = 2.5\text{ V}$		25°C	$I_{OL} = 50\ \mu\text{A}$	0.01		V
				25°C	$I_{OL} = 500\ \mu\text{A}$	0.09	0.15	
				Full range			0.15	
				25°C	$I_{OL} = 1\text{ mA}$	0.2	0.3	
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$ , $V_O = 1\text{ V to }4\text{ V}$		25°C	$R_L = 50\text{ k}\Omega^{(2)}$	80	170	V/mV
				Full range		50		
				25°C	$R_L = 1\text{ M}\Omega^{(2)}$		550	
$r_{i(d)}$	Differential input resistance			25°C		$10^{12}$		$\Omega$
$r_{i(c)}$	Common-mode input resistance			25°C		$10^{12}$		$\Omega$
$C_{i(c)}$	Common-mode input capacitance	$f = 10\text{ kHz}$		25°C		8		pF
$Z_o$	Closed-loop output impedance	$f = 100\text{ kHz}$ , $A_V = 10$		25°C		240		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$ , $V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$		25°C		70	83	dB
				Full range		70		
$k_{SVR}$	Supply voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }8\text{ V}$ , $V_{IC} = V_{DD}/2$ , No load		25°C		80	95	dB
				Full range		80		
$I_{DD}$	Supply current	$V_O = 2.5\text{ V}$ , No load		25°C		400	500	$\mu\text{A}$
				Full range			500	

(1) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

(2) Referenced to 2.5 V

### TLV2262A OPERATING CHARACTERISTICS

V<sub>DD</sub> = 5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V <sub>O</sub> = 0.5 V to 3.5 V, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	0.35	0.55		V/μs
			Full range	0.25			
V <sub>n</sub>	Equivalent input noise voltage	f = 10 Hz	25°C	40			nV/√Hz
		f = 1 kHz	25°C	12			
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C	0.7			μV
		f = 0.1 Hz to 10 Hz	25°C	1.3			
I <sub>n</sub>	Equivalent input noise current		25°C	0.6			fA/√Hz
THD+N	Total harmonic distortion plus noise	V <sub>O</sub> = 0.5 V to 2.5 V, f = 20 kHz, R <sub>L</sub> = 50 kΩ <sup>(1)</sup>	A <sub>V</sub> = 1	25°C	0.017		%
			A <sub>V</sub> = 10	25°C	0.03		
	Gain-bandwidth product	f = 50 kHz, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	0.71			MHz
B <sub>OM</sub>	Maximum output-swing bandwidth	V <sub>O(PP)</sub> = 2 V, A <sub>V</sub> = 1, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	185			kHz
t <sub>s</sub>	Settling time	A <sub>V</sub> = -1, Step = 0.5 V to 2.5 V, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	To 0.1%	25°C	6.4		μs
			To 0.01%	25°C	14.1		
φ <sub>m</sub>	Phase margin at unity gain	R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	56			°
G <sub>m</sub>	Gain margin	R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	11			dB

(1) Referenced to 2.5 V



**TLV2264A ELECTRICAL CHARACTERISTICS**
 $V_{DD} = 3\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{DD\pm} = \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		300	950	mV
				Full range			1500	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_{DD\pm} = \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C to 125°C		2		$\mu\text{V}/^\circ\text{C}$
	Input offset voltage long-term drift <sup>(1)</sup>	$V_{DD\pm} = \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		0.003		$\mu\text{V}/\text{mo}$
$I_{IO}$	Input offset current	$V_{DD\pm} = \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		0.5	60	pA
				125°C			800	
$I_{IB}$	Input bias current	$V_{DD\pm} = \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		1	60	pA
				125°C			800	
$V_{ICR}$	Common-mode input voltage range	$R_S = 50\ \Omega$ , $ V_{IO}  \leq 5\text{ mV}$		25°C	0 to 2	-0.3 to 2.2		V
				Full range	0 to 1.7			
$V_{OH}$	High-level output voltage			25°C		2.99		V
				25°C		2.85		
				Full range		2.82		
				25°C		2.7		
$V_{OL}$	Low-level output voltage	$V_{IC} = 1.5\text{ V}$		25°C		10		mV
				25°C		100	150	
				Full range			150	
				25°C		200	300	
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}$ , $V_O = 1\text{ V to }2\text{ V}$		25°C		60	100	V/mV
				Full range		25		
				25°C		100		
				Full range			300	
$r_{i(d)}$	Differential input resistance			25°C		$10^{12}$		$\Omega$
$r_{i(c)}$	Common-mode input resistance			25°C		$10^{12}$		$\Omega$
$C_{i(c)}$	Common-mode input capacitance	$f = 10\text{ kHz}$		25°C		8		pF
$Z_o$	Closed-loop output impedance	$f = 100\text{ kHz}$ , $A_V = 10$		25°C		270		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}$ , $V_O = 1.5\text{ V}$ , $R_S = 50\ \Omega$		25°C		65	77	dB
				Full range		60		
$k_{SVR}$	Supply voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 2.7\text{ V to }8\text{ V}$ , $V_{IC} = V_{DD}/2$ , No load		25°C		80	100	dB
				Full range		80		
$I_{DD}$	Supply current	$V_O = 1.5\text{ V}$ , No load		25°C		0.8	1	mA
				Full range			1	

(1) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

(2) Referenced to 1.5 V

### TLV2264A OPERATING CHARACTERISTICS

V<sub>DD</sub> = 3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V <sub>O</sub> = 0.5 V to 1.7 V, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	0.35	0.55		V/μs
			Full range	0.25			
V <sub>n</sub>	Equivalent input noise voltage	f = 10 Hz	25°C		43		nV/√Hz
		f = 1 kHz	25°C		12		
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.6		μV
		f = 0.1 Hz to 10 Hz	25°C		1		
I <sub>n</sub>	Equivalent input noise current		25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	V <sub>O</sub> = 0.5 V to 2.5 V, f = 20 kHz, R <sub>L</sub> = 50 kΩ <sup>(1)</sup>	A <sub>V</sub> = 1	25°C		0.03	%
			A <sub>V</sub> = 10	25°C		0.05	
	Gain-bandwidth product	f = 1 kHz, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C		0.67		MHz
B <sub>OM</sub>	Maximum output-swing bandwidth	V <sub>O(PP)</sub> = 1 V, A <sub>V</sub> = 1, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C		395		kHz
t <sub>s</sub>	Settling time	A <sub>V</sub> = -1, Step = 1 V to 2 V, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	To 0.1%	25°C		5.6	μs
			To 0.01%	25°C		12.5	
φ <sub>m</sub>	Phase margin at unity gain	R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C		55		°
G <sub>m</sub>	Gain margin	R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C		11		dB

(1) Referenced to 1.5 V

**TLV2264A ELECTRICAL CHARACTERISTICS**
 $V_{DD} = 5\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		300	950	mV
				Full range			1500	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C to 125°C		2		$\mu\text{V}/^\circ\text{C}$
	Input offset voltage long-term drift <sup>(1)</sup>	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		0.003		$\mu\text{V}/\text{mo}$
$I_{IO}$	Input offset current	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		0.5	60	pA
				125°C			800	
$I_{IB}$	Input bias current	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		25°C		1	60	pA
				125°C			800	
$V_{ICR}$	Common-mode input voltage range	$R_S = 50\ \Omega$ , $ V_{IO}  \leq 5\text{ mV}$		25°C	0 to 4	-0.3 to 4.2		V
				Full range	0 to 3.5			
$V_{OH}$	High-level output voltage			25°C		4.99		V
				25°C	$I_{OH} = -100\ \mu\text{A}$	4.85	4.94	
				Full range		4.82		
				25°C	$I_{OH} = -400\ \mu\text{A}$	4.7	4.85	
$V_{OL}$	Low-level output voltage	$V_{IC} = 2.5\text{ V}$		25°C	$I_{OL} = 50\ \mu\text{A}$	0.01		V
				25°C	$I_{OL} = 500\ \mu\text{A}$	0.09	0.15	
				Full range			0.15	
				25°C	$I_{OL} = 1\text{ mA}$	0.2	0.3	
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$ , $V_O = 1\text{ V to }4\text{ V}$		25°C	$R_L = 50\text{ k}\Omega^{(2)}$	80	170	V/mV
				Full range		50		
				25°C	$R_L = 1\text{ M}\Omega^{(2)}$		550	
$r_{i(d)}$	Differential input resistance			25°C		$10^{12}$		$\Omega$
$r_{i(c)}$	Common-mode input resistance			25°C		$10^{12}$		$\Omega$
$C_{i(c)}$	Common-mode input capacitance	$f = 10\text{ kHz}$		25°C		8		pF
$Z_o$	Closed-loop output impedance	$f = 100\text{ kHz}$ , $A_V = 10$		25°C		240		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$ , $V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$		25°C		70	83	dB
				Full range		70		
$k_{SVR}$	Supply voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }8\text{ V}$ , $V_{IC} = V_{DD}/2$ , No load		25°C		80	95	dB
				Full range		80		
$I_{DD}$	Supply current	$V_O = 2.5\text{ V}$ , No load		25°C		0.8	1	mA
				Full range			1	

(1) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

(2) Referenced to 2.5 V

### TLV2264A OPERATING CHARACTERISTICS

V<sub>DD</sub> = 5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V <sub>O</sub> = 0.5 V to 3.5 V, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	0.35	0.55		V/μs
			Full range	0.25			
V <sub>n</sub>	Equivalent input noise voltage	f = 10 Hz	25°C	40			nV/√Hz
		f = 1 kHz	25°C	12			
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C	0.7			μV
		f = 0.1 Hz to 10 Hz	25°C	1.3			
I <sub>n</sub>	Equivalent input noise current		25°C	0.6			fA/√Hz
THD+N	Total harmonic distortion plus noise	V <sub>O</sub> = 0.5 V to 2.5 V, f = 20 kHz, R <sub>L</sub> = 50 kΩ <sup>(1)</sup>	A <sub>V</sub> = 1	25°C	0.017		%
			A <sub>V</sub> = 10	25°C	0.03		
	Gain-bandwidth product	f = 50 kHz, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	0.71			MHz
B <sub>OM</sub>	Maximum output-swing bandwidth	V <sub>O(PP)</sub> = 2 V, A <sub>V</sub> = 1, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	185			kHz
t <sub>s</sub>	Settling time	A <sub>V</sub> = -1, Step = 0.5 V to 2.5 V, R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	To 0.1%	25°C	6.4		μs
			To 0.01%	25°C	14.1		
φ <sub>m</sub>	Phase margin at unity gain	R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	56			°
G <sub>m</sub>	Gain margin	R <sub>L</sub> = 50 kΩ <sup>(1)</sup> , C <sub>L</sub> = 100 pF <sup>(1)</sup>	25°C	11			dB

(1) Referenced to 2.5 V

## TYPICAL CHARACTERISTICS

For all curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3\text{ V}$ , all loads are referenced to 1.5 V. Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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**DISTRIBUTION OF TLV2262  
INPUT OFFSET VOLTAGE**

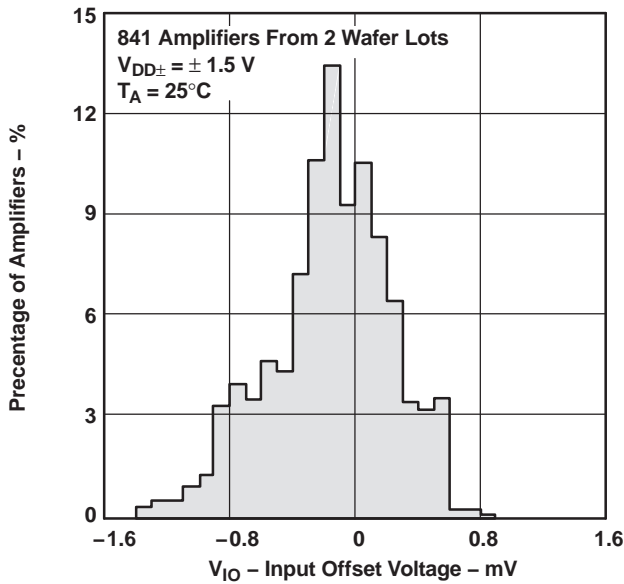


Figure 2.

**DISTRIBUTION OF TLV2262  
INPUT OFFSET VOLTAGE**

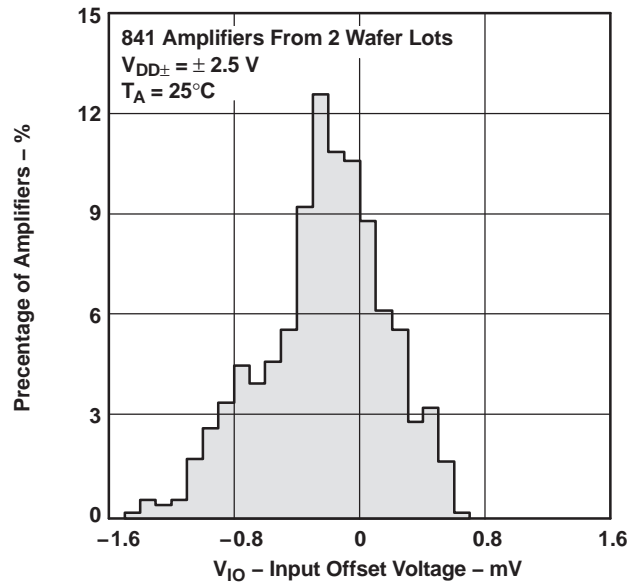


Figure 3.

**DISTRIBUTION OF TLV2264  
INPUT OFFSET VOLTAGE**

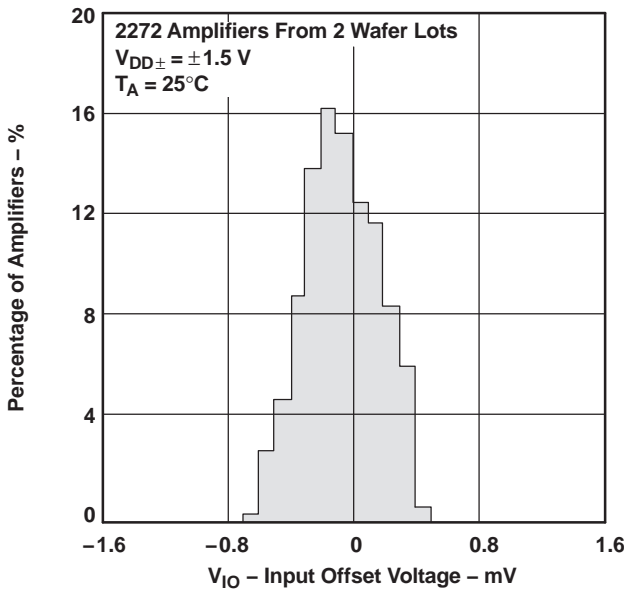


Figure 4.

**DISTRIBUTION OF TLV2264  
INPUT OFFSET VOLTAGE**

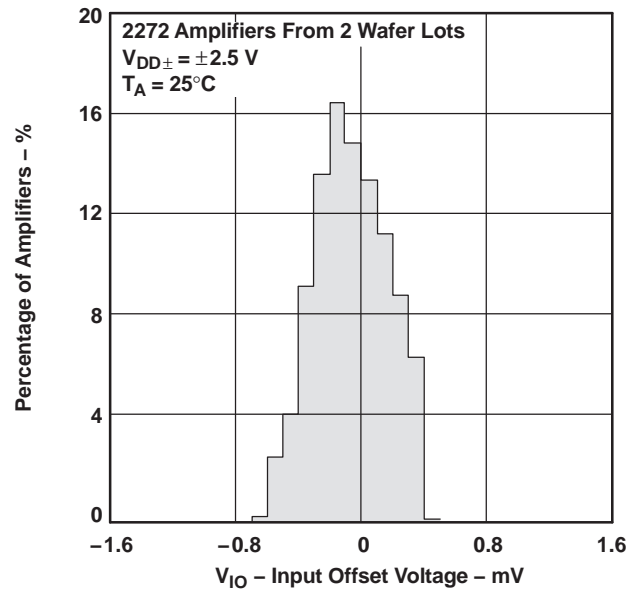


Figure 5.

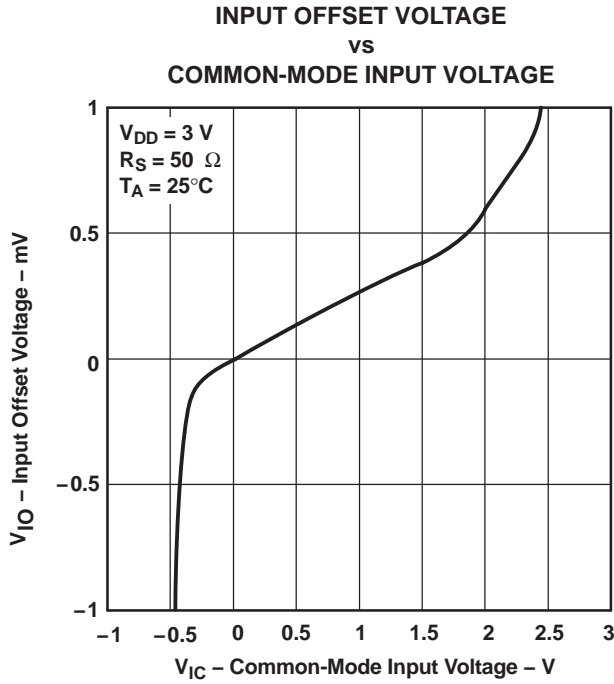


Figure 6.

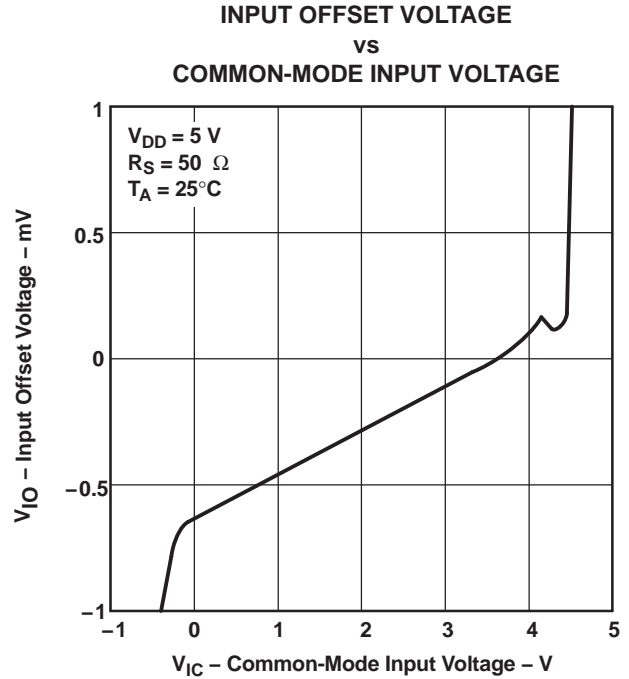


Figure 7.

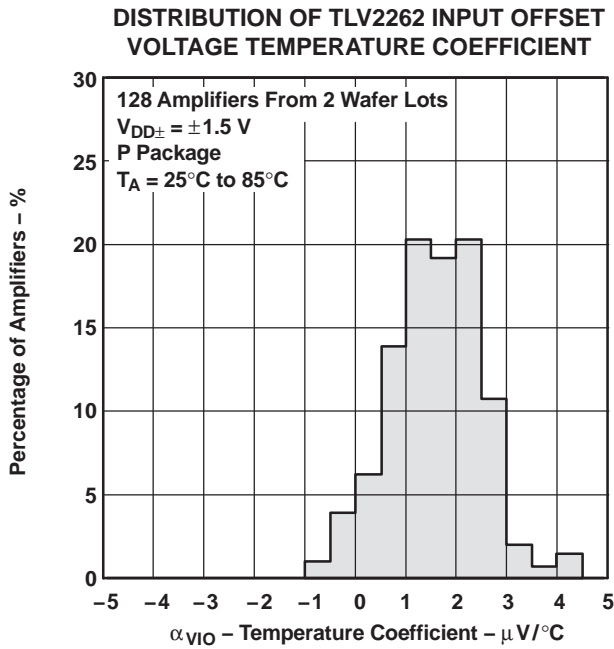


Figure 8.

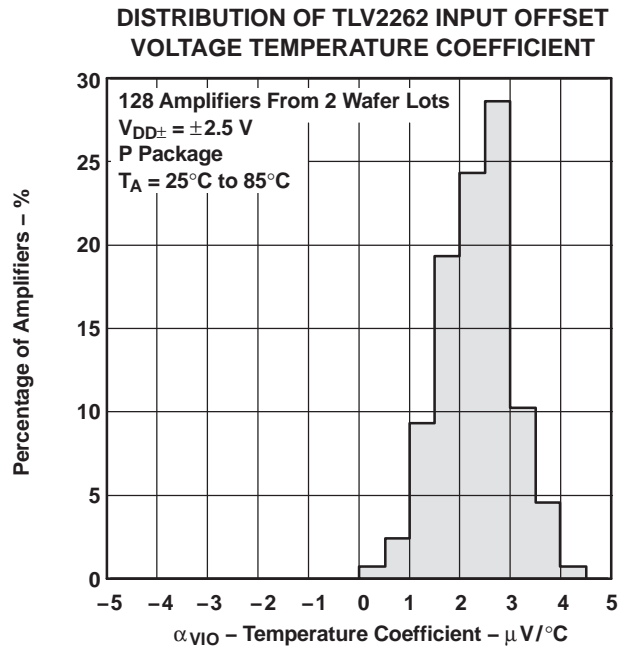


Figure 9.

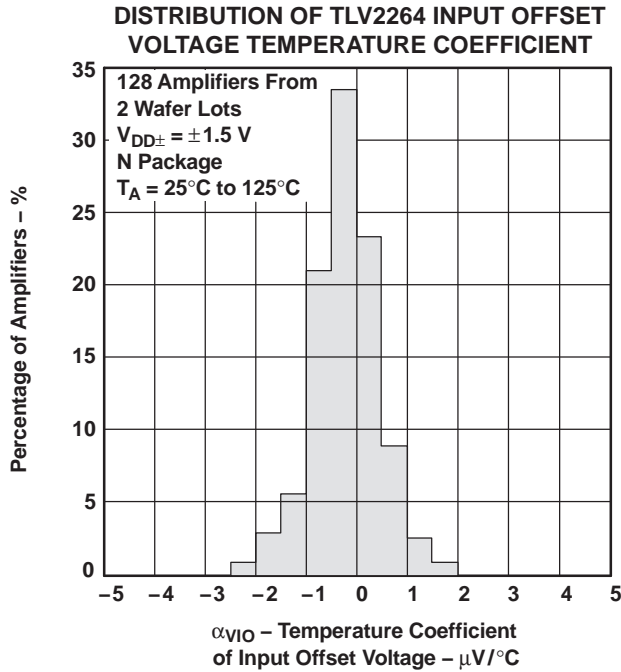


Figure 10.

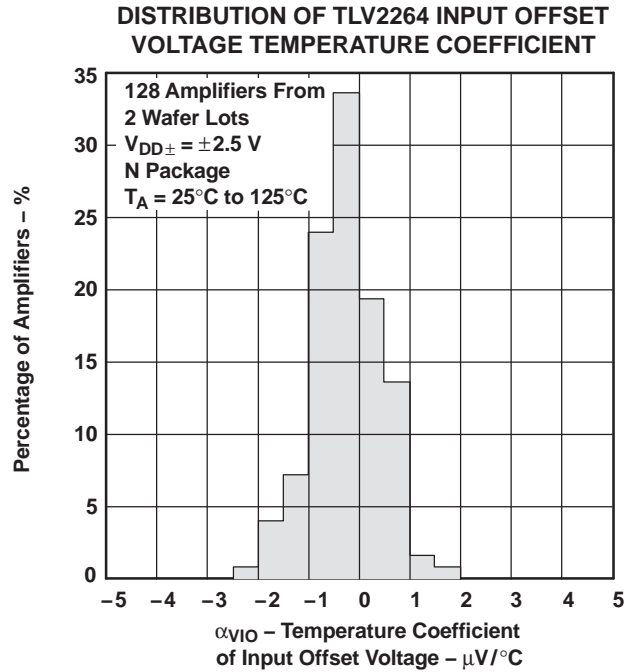


Figure 11.

**INPUT BIAS AND INPUT OFFSET CURRENTS  
vs  
FREE-AIR TEMPERATURE**

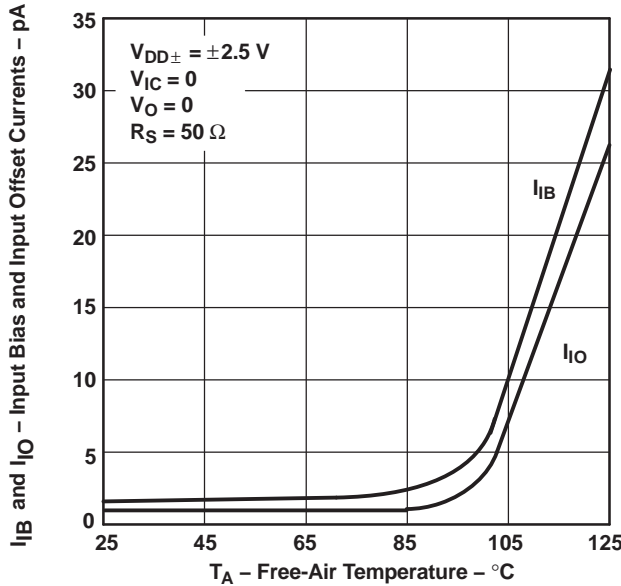


Figure 12.

**INPUT VOLTAGE  
vs  
SUPPLY VOLTAGE**

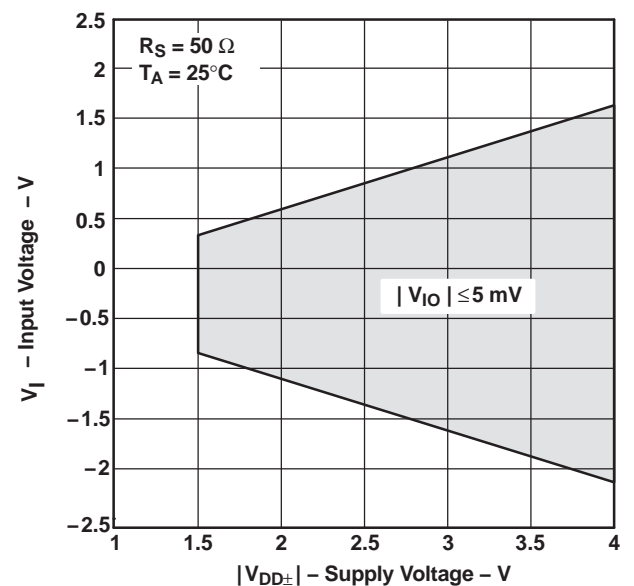
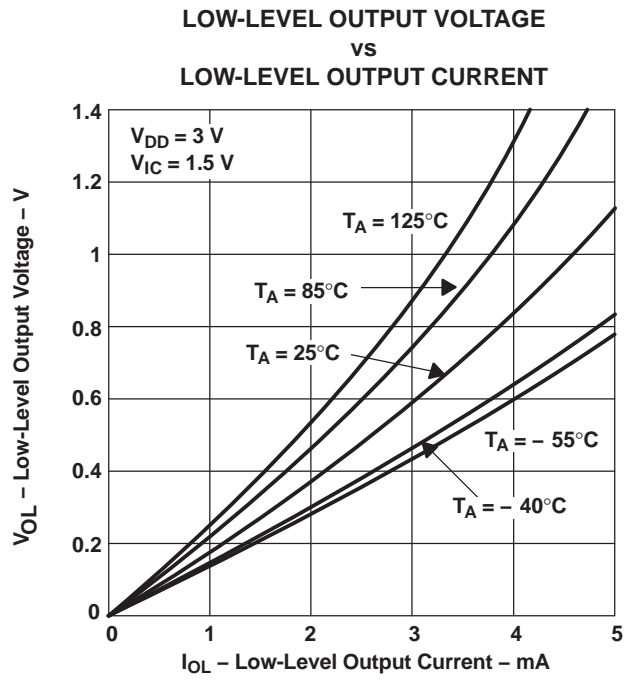
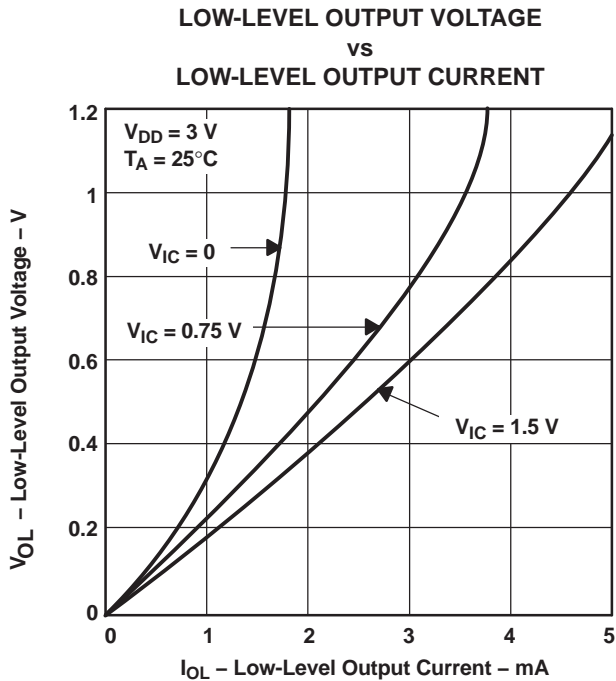
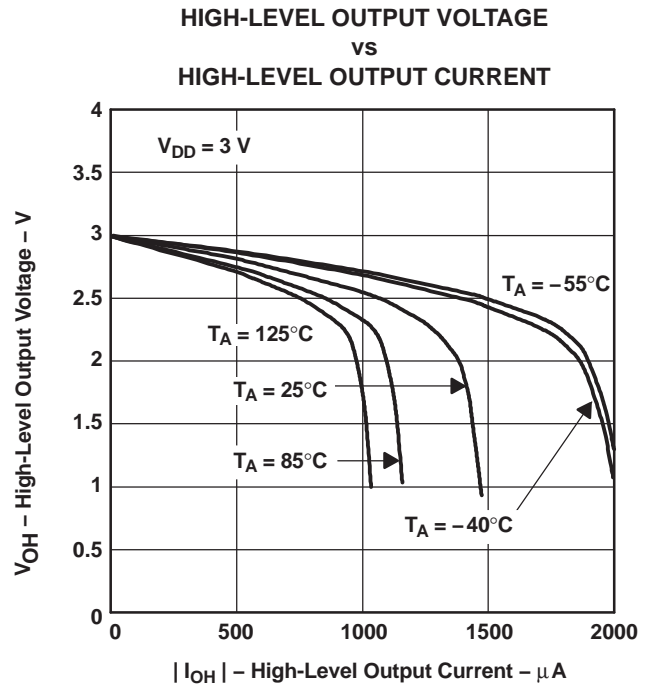
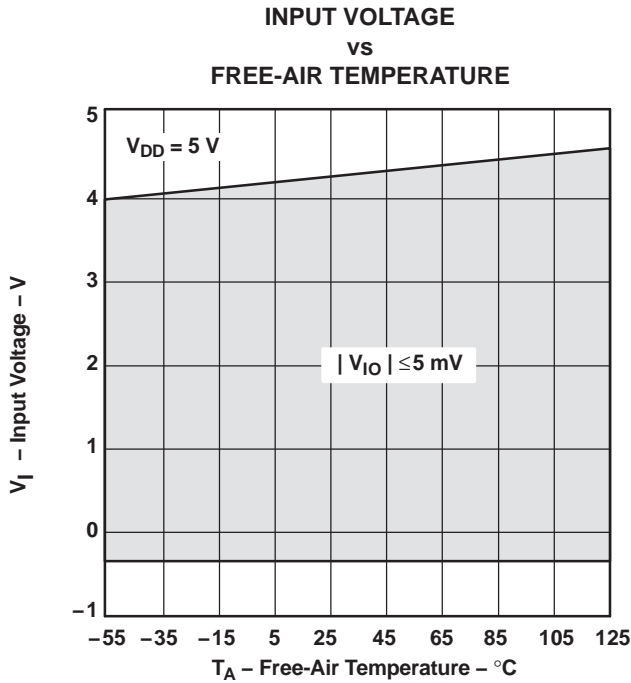
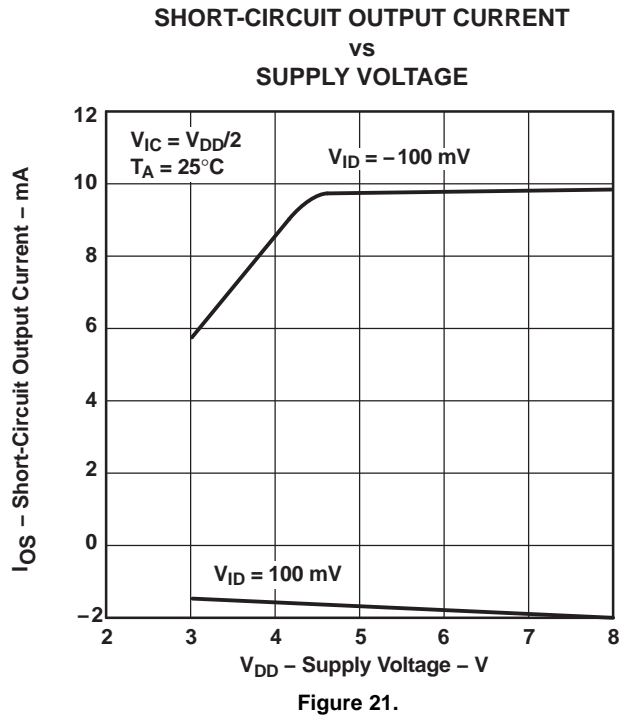
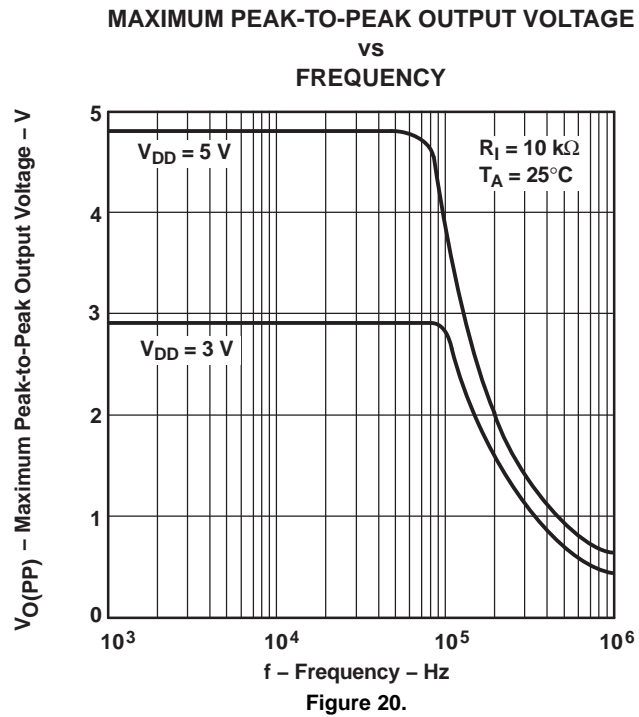
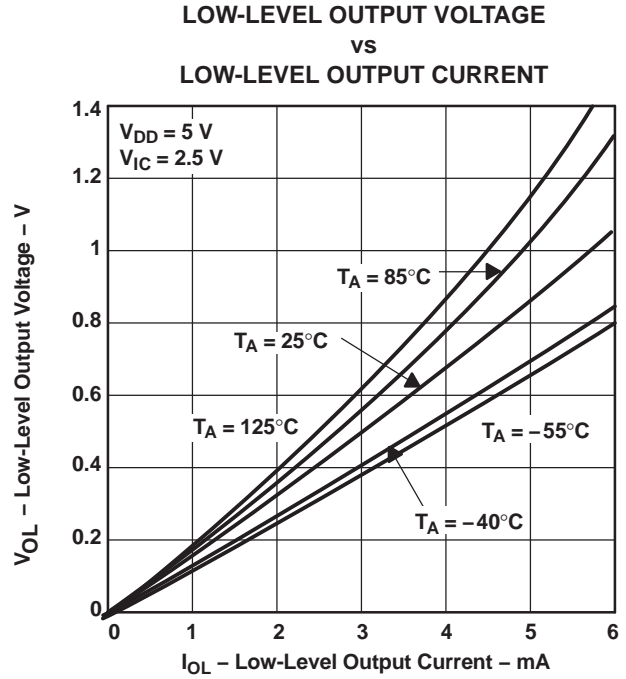
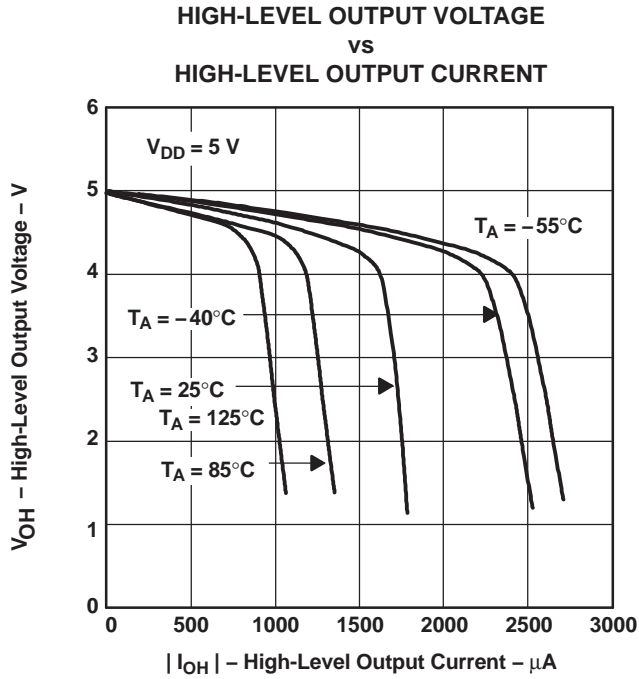


Figure 13.







SHORT-CIRCUIT OUTPUT CURRENT  
vs  
FREE-AIR TEMPERATURE

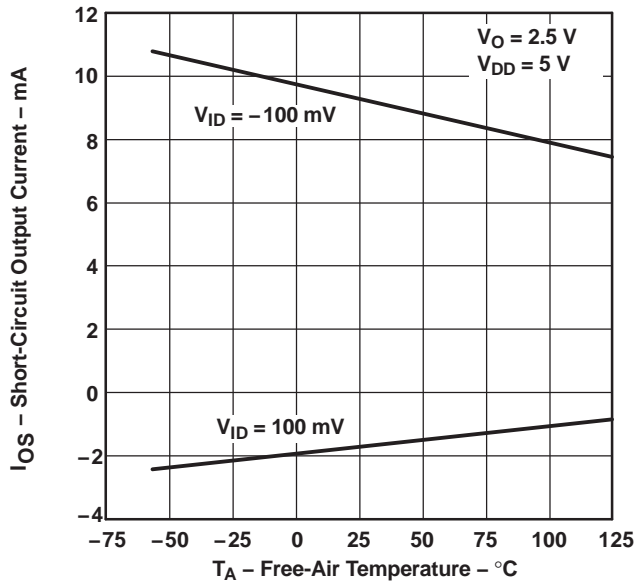


Figure 22.

DIFFERENTIAL INPUT VOLTAGE  
vs  
OUTPUT VOLTAGE

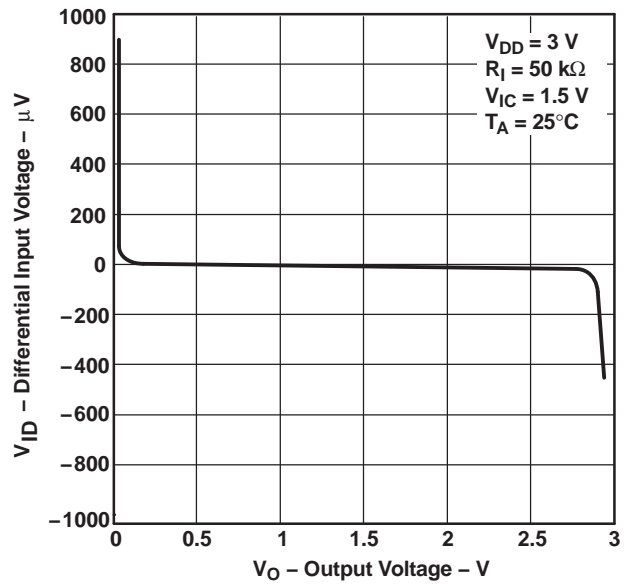


Figure 23.

DIFFERENTIAL INPUT VOLTAGE  
vs  
OUTPUT VOLTAGE

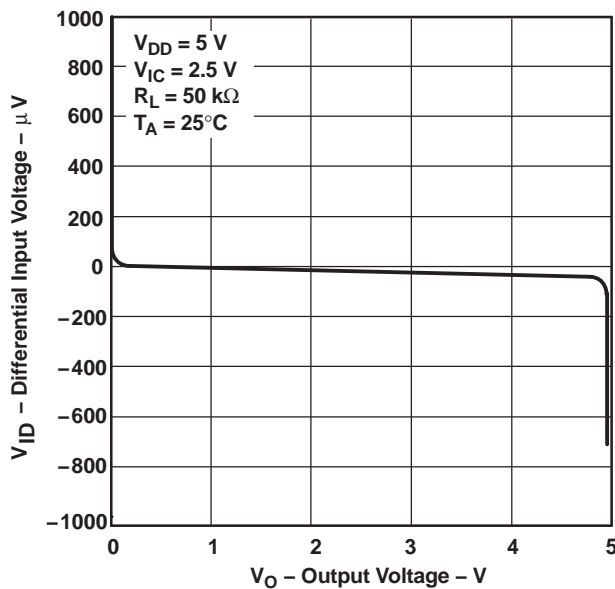


Figure 24.

DIFFERENTIAL VOLTAGE AMPLIFICATION  
vs  
LOAD RESISTANCE

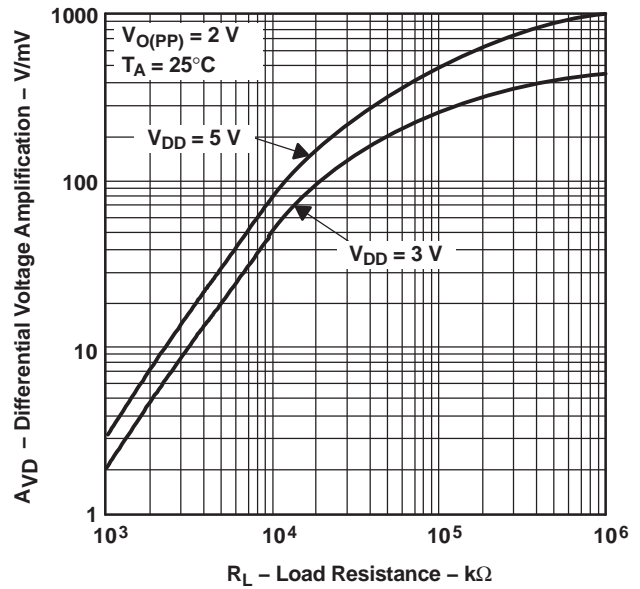


Figure 25.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN VS FREQUENCY

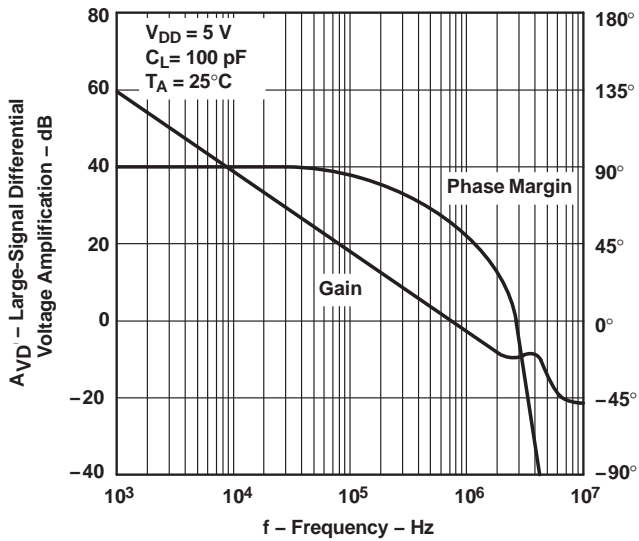


Figure 26.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN VS FREQUENCY

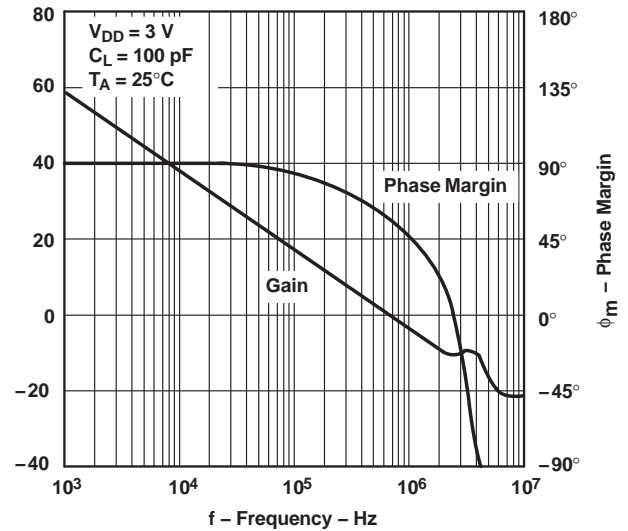


Figure 27.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VS FREE-AIR TEMPERATURE

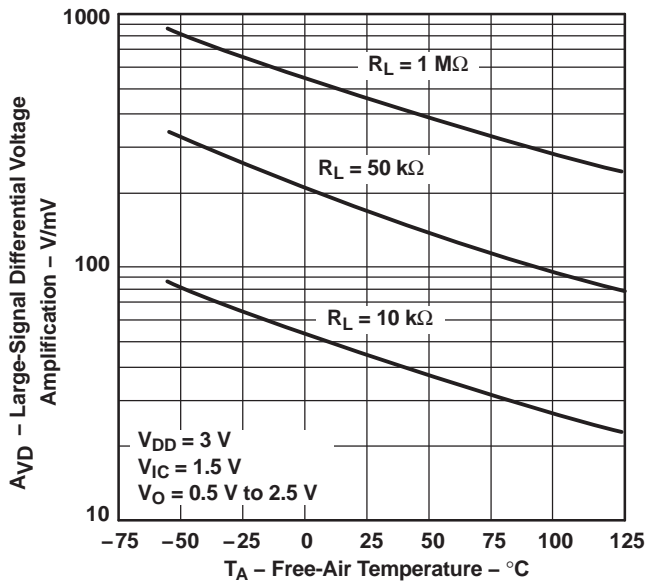


Figure 28.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VS FREE-AIR TEMPERATURE

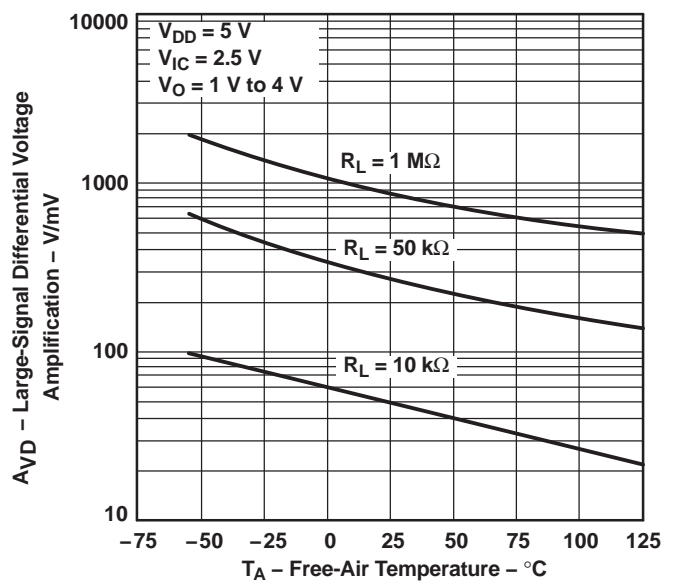


Figure 29.

OUTPUT IMPEDANCE  
VS  
FREQUENCY

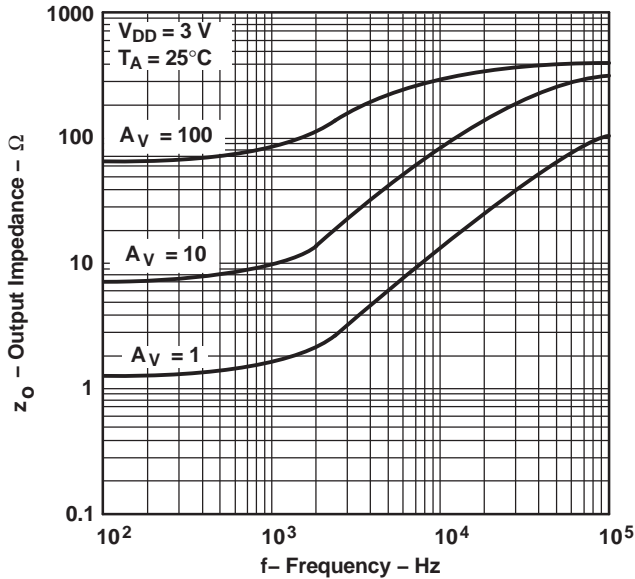


Figure 30.

OUTPUT IMPEDANCE  
VS  
FREQUENCY

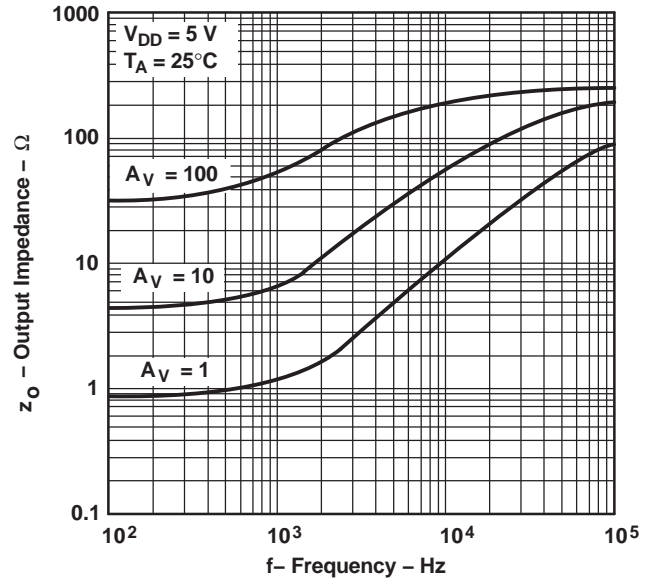


Figure 31.

COMMON-MODE REJECTION RATIO  
VS  
FREQUENCY

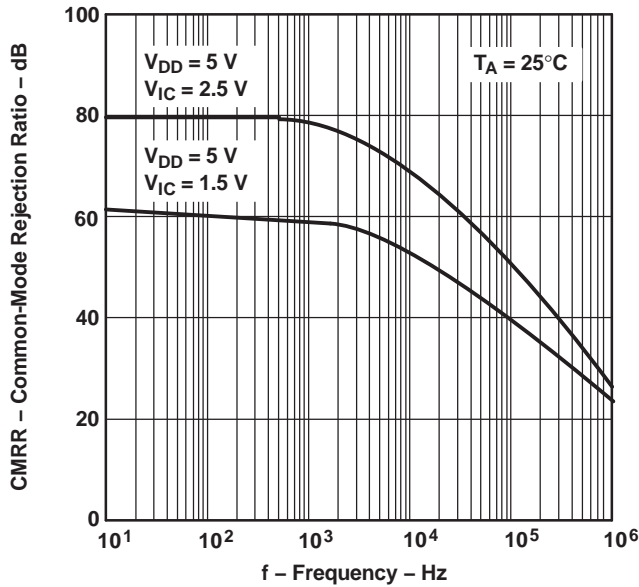


Figure 32.

COMMON-MODE REJECTION RATIO  
VS  
FREE-AIR TEMPERATURE

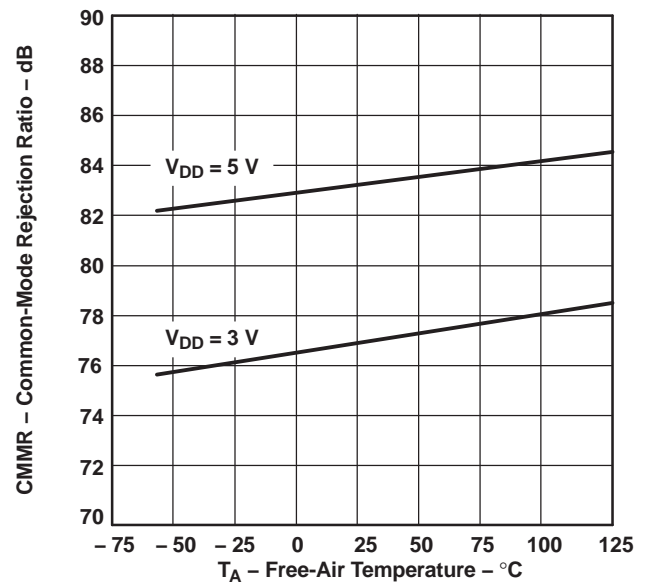


Figure 33.

**SUPPLY-VOLTAGE REJECTION RATIO  
VS  
FREQUENCY**

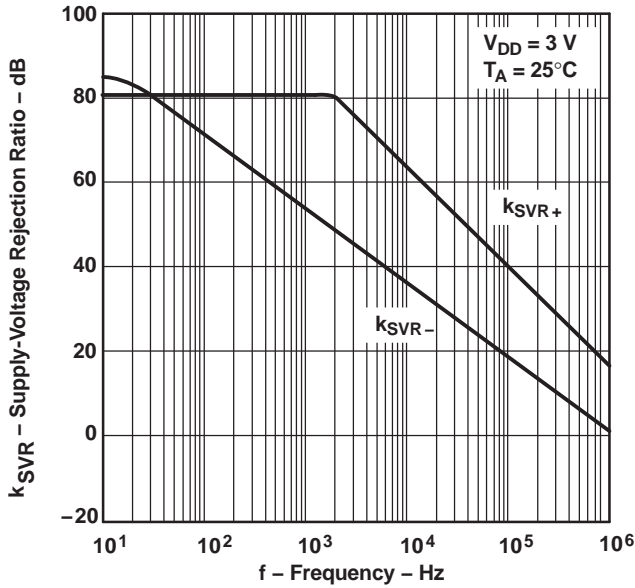


Figure 34.

TLV2262

**SUPPLY-VOLTAGE REJECTION RATIO  
VS  
FREE-AIR TEMPERATURE**

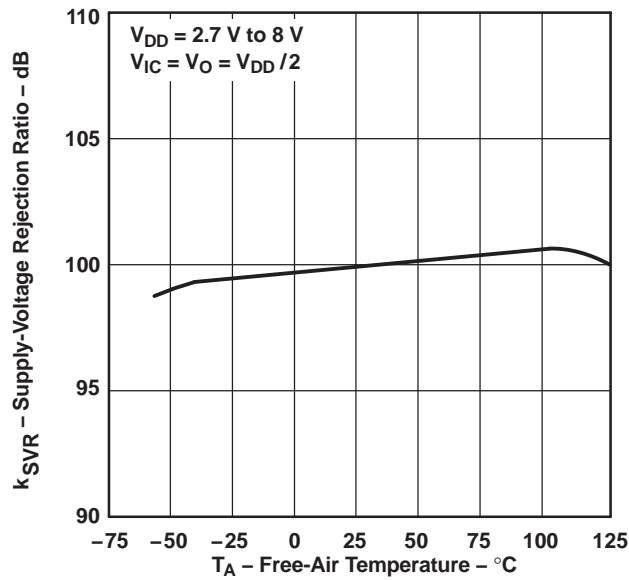


Figure 36.

**SUPPLY-VOLTAGE REJECTION RATIO  
VS  
FREQUENCY**

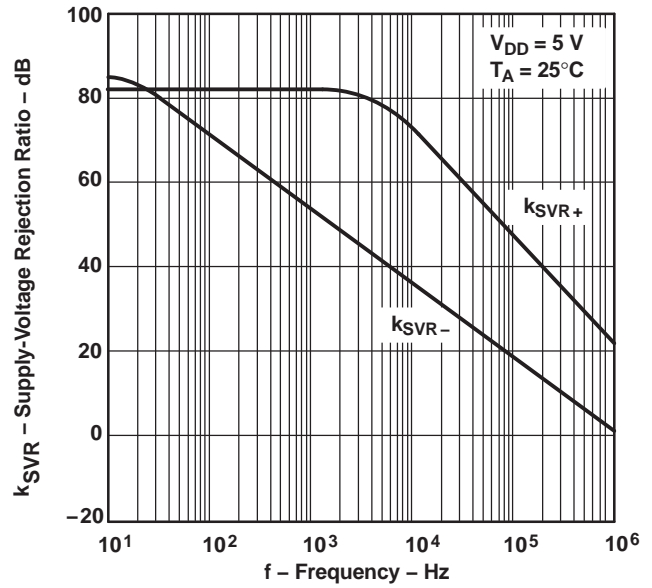


Figure 35.

TLV2264

**SUPPLY-VOLTAGE REJECTION RATIO  
VS  
FREE-AIR TEMPERATURE**

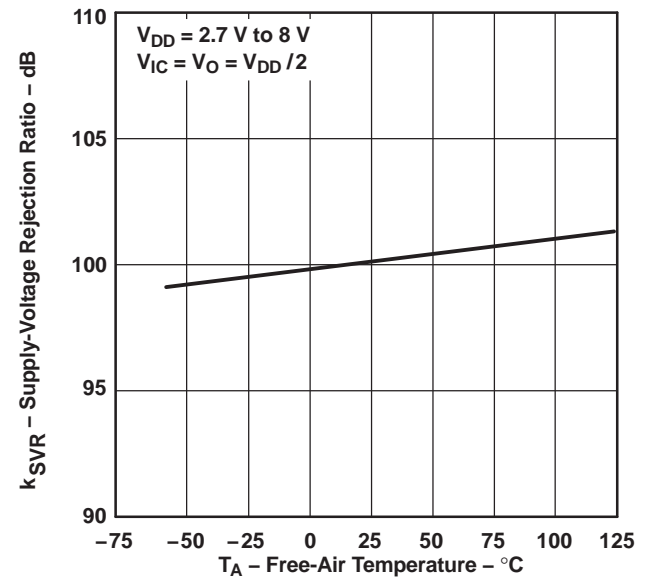


Figure 37.

TLV2262  
SUPPLY CURRENT  
vs  
FREE-AIR TEMPERATURE

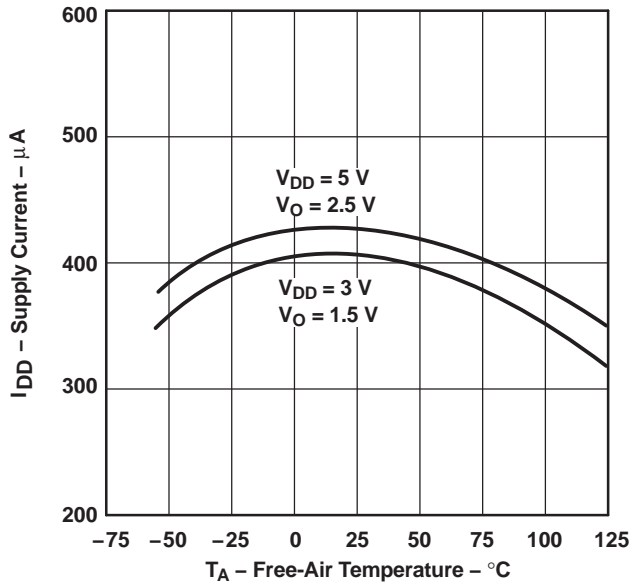


Figure 38.

TLV2264  
SUPPLY CURRENT  
vs  
FREE-AIR TEMPERATURE

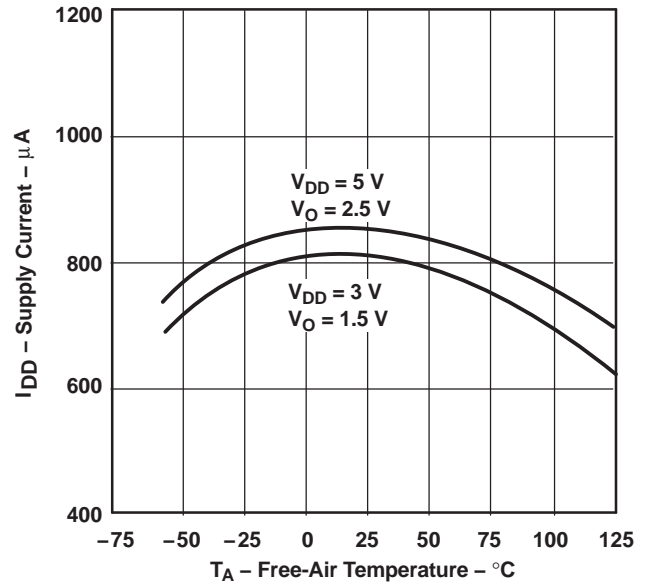


Figure 39.

SLEW RATE  
vs  
LOAD CAPACITANCE

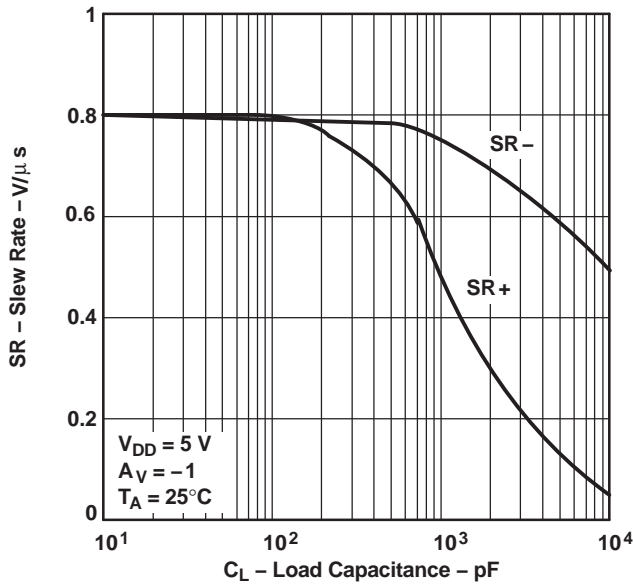


Figure 40.

SLEW RATE  
vs  
FREE-AIR TEMPERATURE

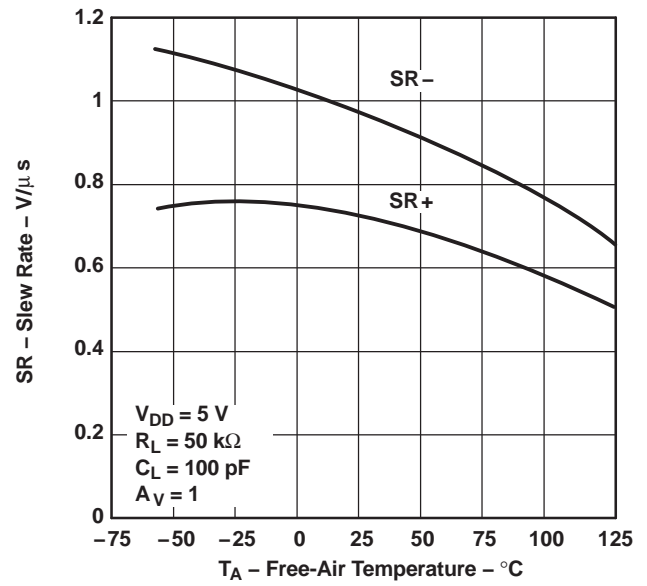


Figure 41.

**INVERTING LARGE-SIGNAL PULSE RESPONSE**

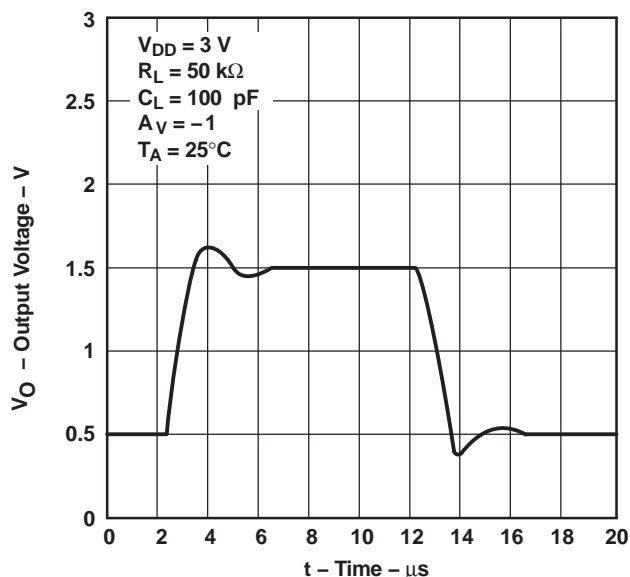


Figure 42.

**INVERTING LARGE-SIGNAL PULSE RESPONSE**

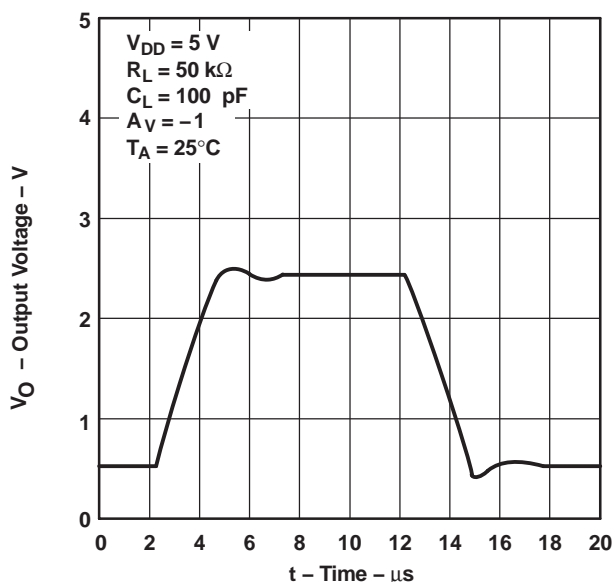


Figure 43.

**VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE**

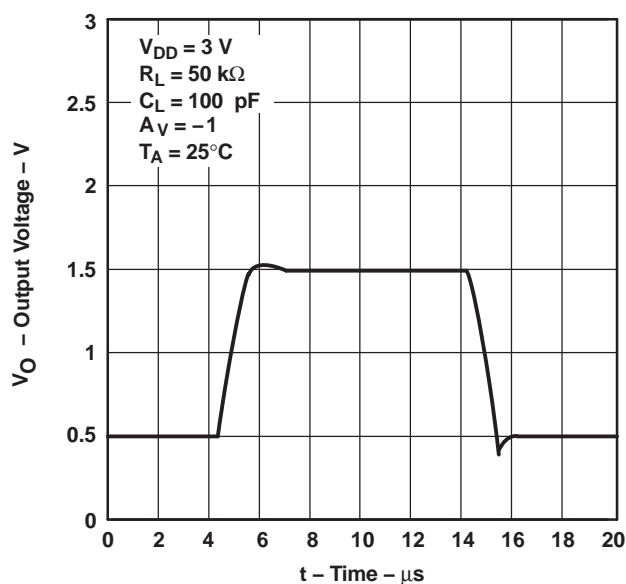


Figure 44.

**VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE**

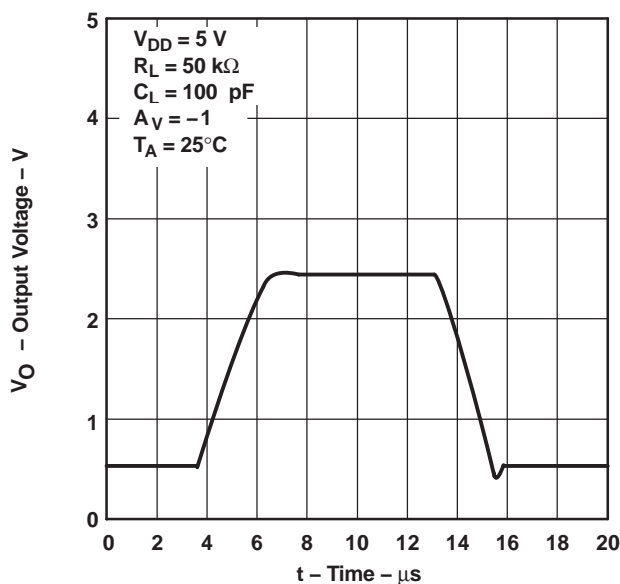


Figure 45.



INVERTING SMALL-SIGNAL PULSE RESPONSE

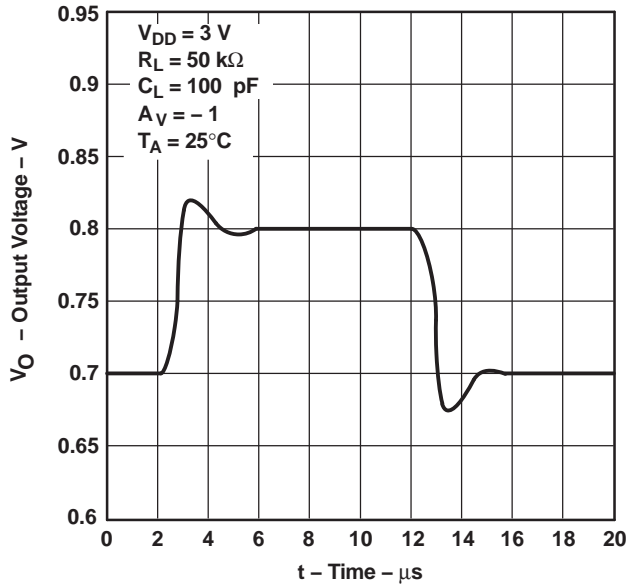


Figure 46.

INVERTING SMALL-SIGNAL PULSE RESPONSE

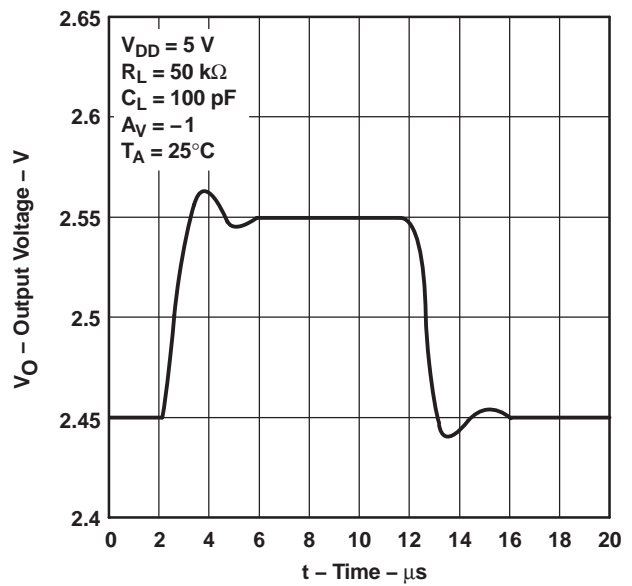


Figure 47.

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

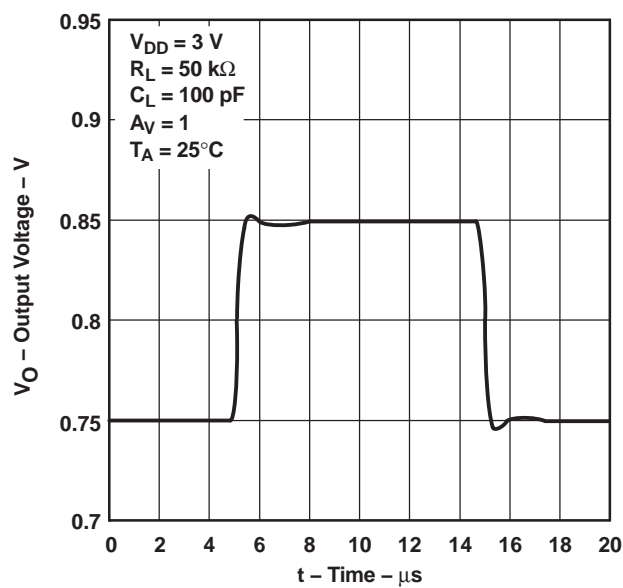


Figure 48.

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

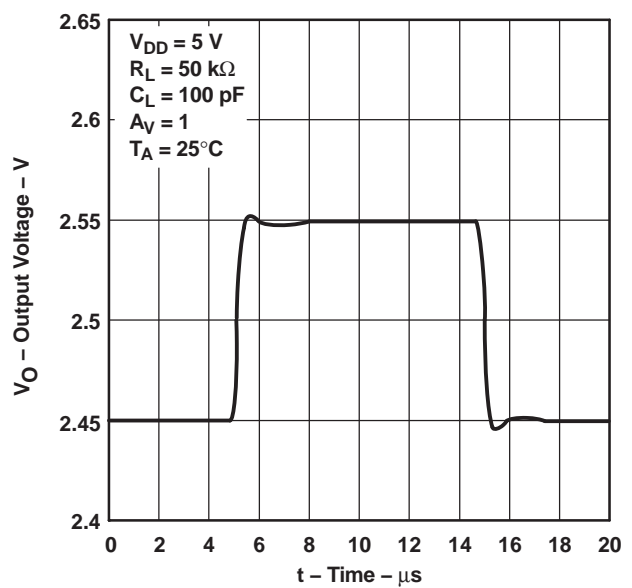


Figure 49.

**EQUIVALENT INPUT NOISE VOLTAGE  
VS  
FREQUENCY**

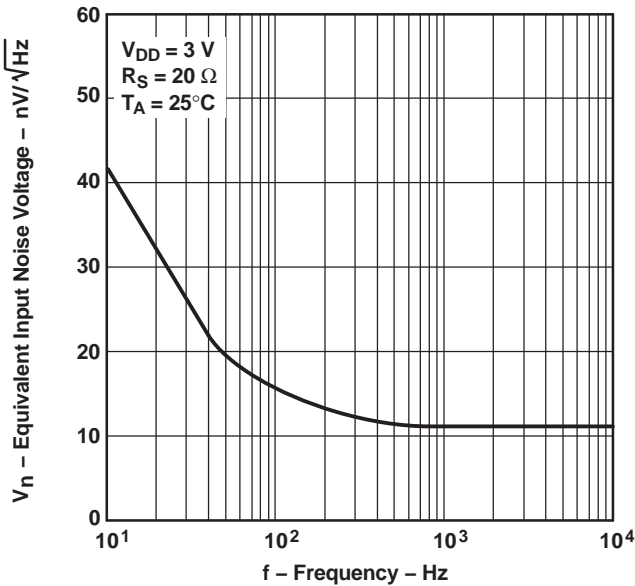


Figure 50.

**EQUIVALENT INPUT NOISE VOLTAGE  
VS  
FREQUENCY**

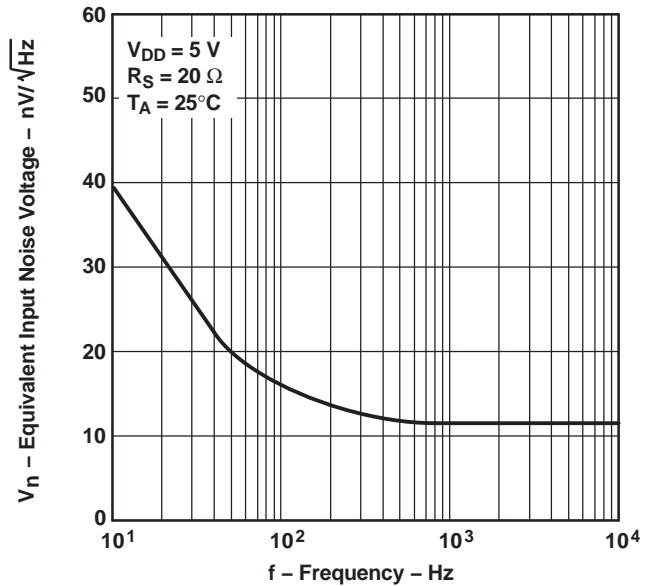


Figure 51.

**INPUT NOISE VOLTAGE OVER  
A 10-SECOND PERIOD**

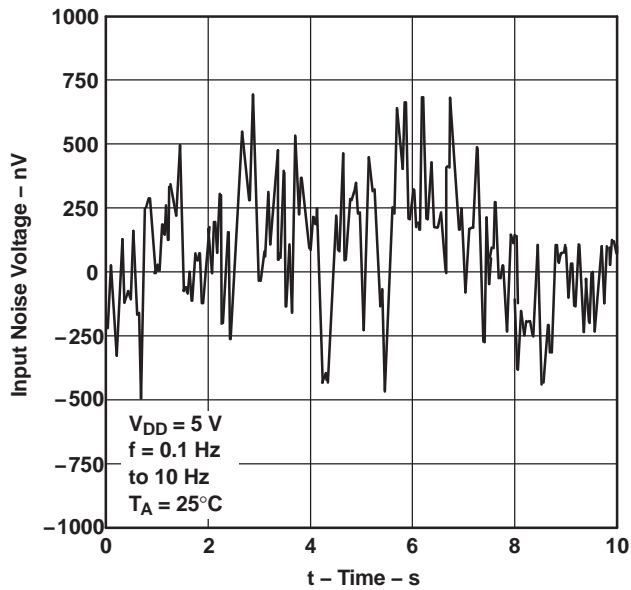


Figure 52.

**INTEGRATED NOISE VOLTAGE  
VS  
FREQUENCY**

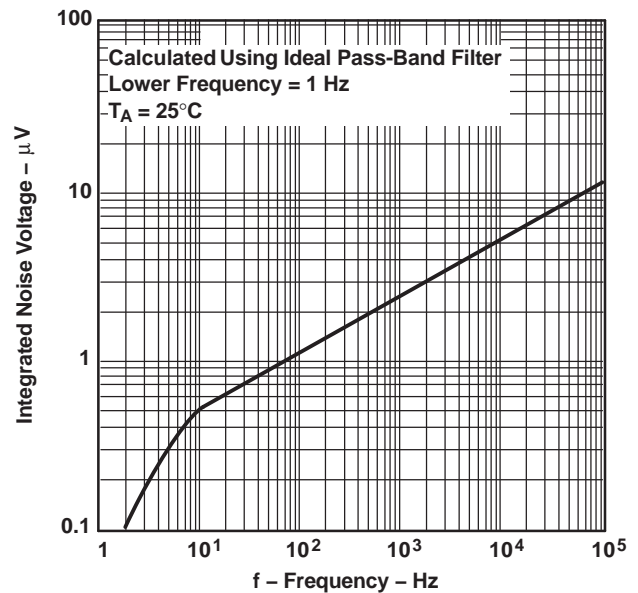


Figure 53.

TOTAL HARMONIC DISTORTION PLUS NOISE  
VS  
FREQUENCY

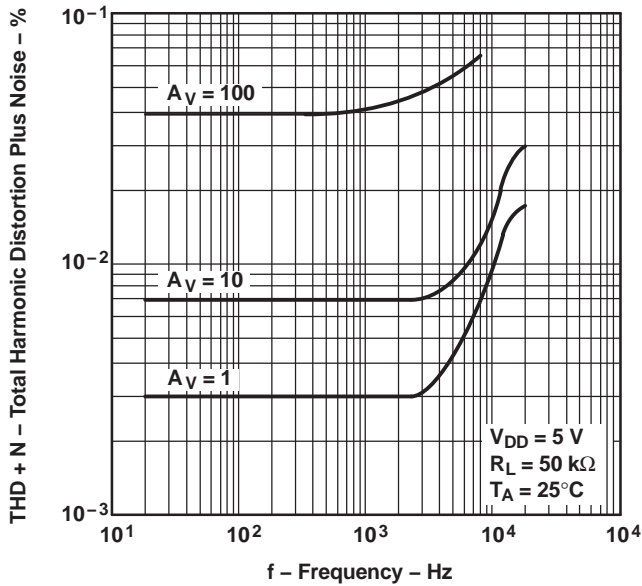


Figure 54.  
GAIN-BANDWIDTH PRODUCT  
VS  
FREE-AIR TEMPERATURE

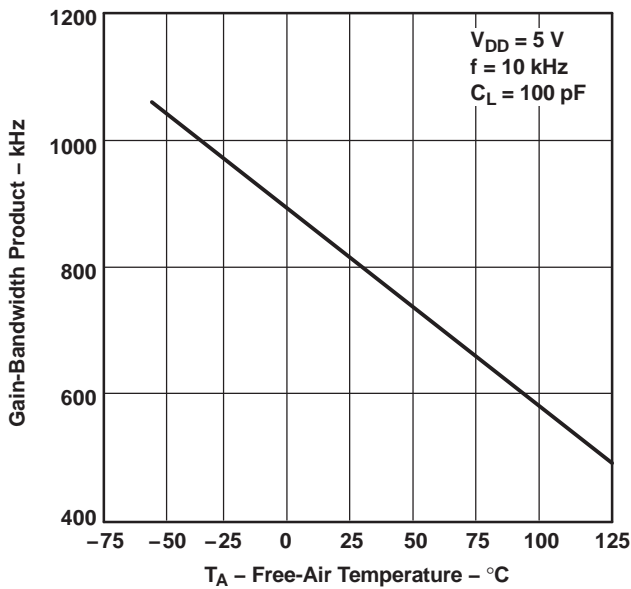


Figure 56.

GAIN-BANDWIDTH PRODUCT  
VS  
SUPPLY VOLTAGE

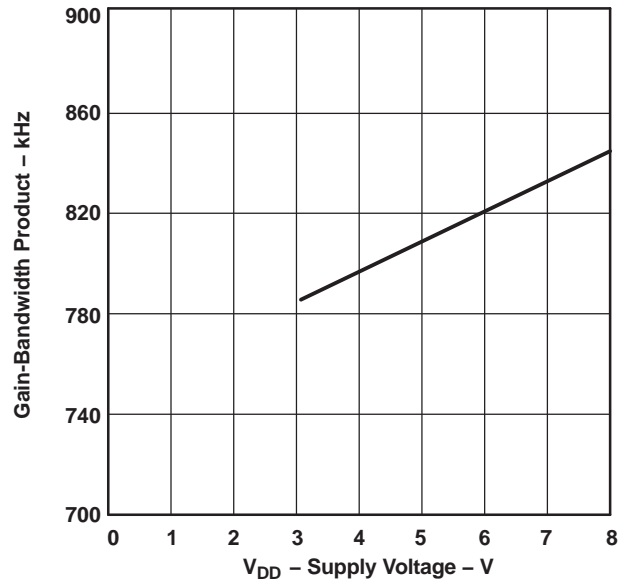


Figure 55.  
PHASE MARGIN  
VS  
LOAD CAPACITANCE

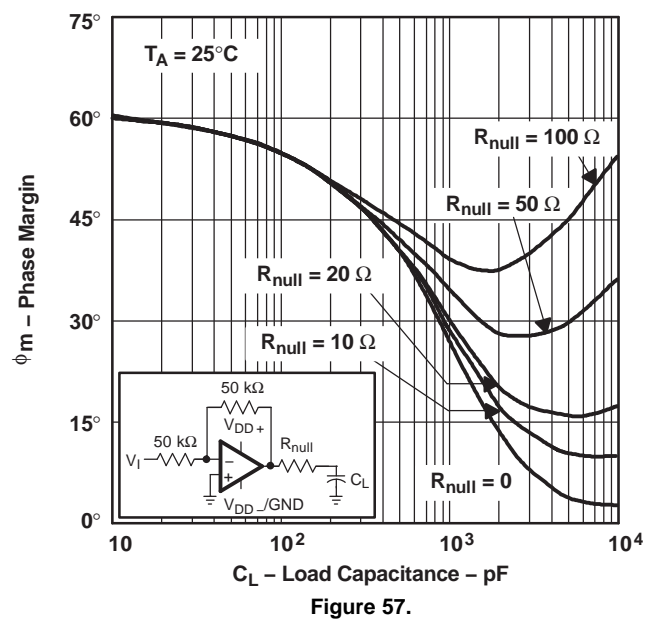


Figure 57.

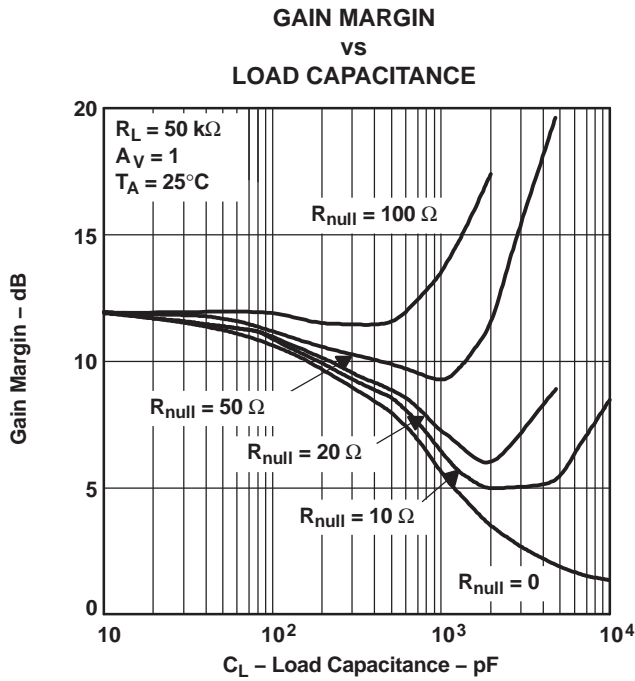


Figure 58.

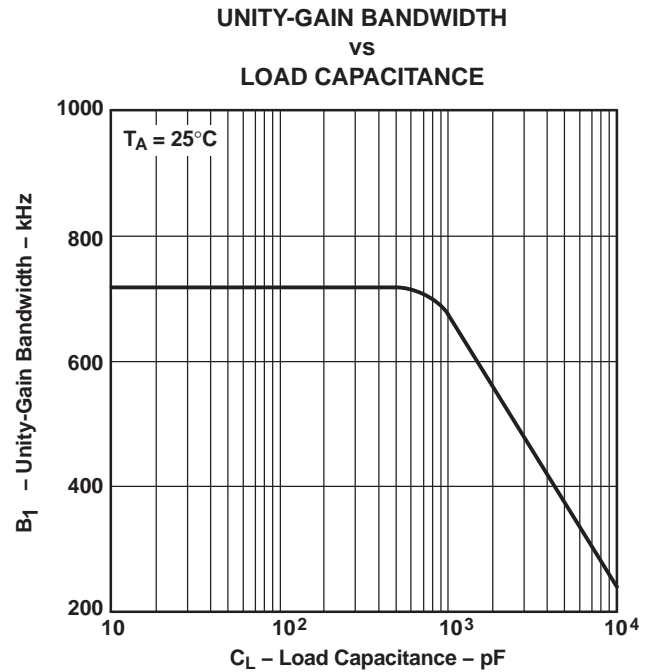
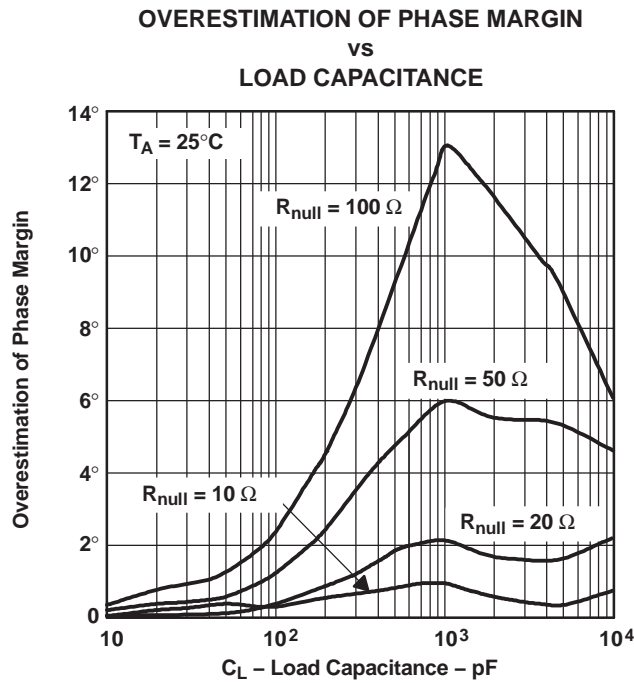


Figure 59.



NOTE: See application information.  
Figure 60.

## APPLICATION INFORMATION

### Driving Large Capacitive Loads

The TLV226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins ( $R_{null} = 0$ ).

A smaller series resistor ( $R_{null}$ ) at the output of the device (see Figure 61) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10  $\Omega$ , 20  $\Omega$ , 50  $\Omega$ , and 100  $\Omega$ . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, Equation 1 can be used.

$$\Delta\theta_{m1} = \tan^{-1} \left( 2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right)$$

Where :

$\Delta\theta_{m1}$  = improvement in phase margin

UGBW = unity-gain bandwidth frequency

$R_{null}$  = output series resistance

$C_L$  = load capacitance

(1)

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use Equation 1, UGBW must be approximated from Figure 53.

Using Equation 1 alone overestimates the improvement in phase margin as illustrated in Figure 60. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in Equation 2.

$$F = \frac{1}{1 + g_m \times R_{null}}$$

Where :

F = factor reducing frequency of pole

$g_m$  = small-signal output transconductance (typically  $4.83 \times 10^{-3}$  mhos)

$R_{null}$  = output series resistance

(2)

For the TLV226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with  $C_L$ : at  $C_L = 10$  pF, use 70 MHz, at  $C_L = 1000$  pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (see Equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the Equation 1 to better approximate the improvement in phase margin.

$$\Delta\theta_{m2} = \tan^{-1} \left[ \frac{\text{UGBW}}{(F \times P_2)} \right] - \tan^{-1} \left( \frac{\text{UGBW}}{P_2} \right)$$

Where :

$\Delta\theta_{m2}$  = reduction in phase margin

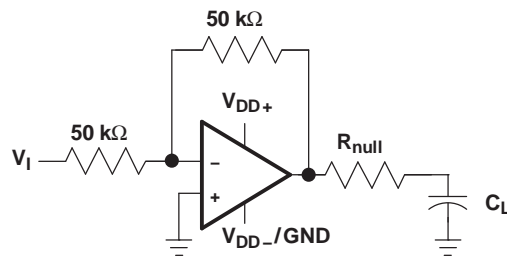
UGBW = unity-gain bandwidth frequency

F = factor from equation (2)

$P_2$  = unadjusted pole (70 MHz @ 10 pF, 7 MHz @ 100 pF, etc.)

(3)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.



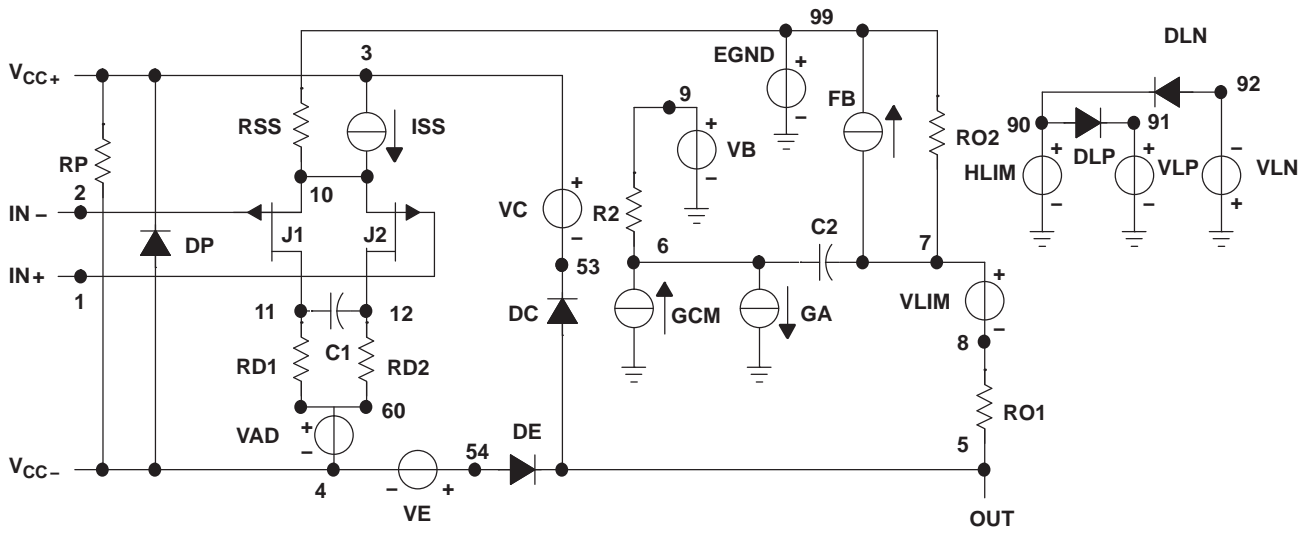
**Figure 61. Series-Resistance Circuit**

### Macromodel Information

Macromodel information provided was derived using Microsim Parts™, the model generation software used with Microsim PSpice™. The Boyle macromodel<sup>(1)</sup> and subcircuit in Figure 62 are generated using the TLV226x typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



```

.SUBCKT TLV226x 1 2 3 4 5
C1      11  12  5.5E-12
C2      6   7   20.00E-12
DC      5   53  DX
DE      54  5   DX
DLP     90  91  DX
DLN     92  90  DX
DP      4   3   DX
EGND    99  0   POLY (2) (3,0) (4,0) 0 .5 .5
FB      7   99  POLY (5) VB VC VE VLP
+ VLN 0 8.84E6 -10E6 10E6 10E6 -10E6
GA      6   0   11   12 62.83E-6
GCM     0   6   10   99 12.34E-9
ISS     3   10  DC 11.05E-6
HLIM    90  0   VLIM 1K
J1      11  2   10 JX
J2      12  1   10 JX
R2      6   9   100.0E3
RD1     60  11  15.92E3
RD2     60  12  15.92E3
R01     8   5   135
R02     7   99  135
RP      3   4   15.87E3
RSS     10  99  18.18E6
VAD     60  4   -.5
VB      9   0   DC 0
VC      3   53  DC .615
VE      54  4   DC .615
VLIM    7   8   DC 0
VLP     91  0   DC 1
VLN     0   92  DC 5.1
.MODEL DX D (IS=800.0E-18)
.MODEL JX PJF (IS=500.0E-15 BETA=325E-6
+ VTO=-.08)
.ENDS

```

Figure 62. Boyle Macromodel and Subcircuit

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV2262AQPWRQ1</a>	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TQ262A
TLV2262AQPWRQ1.A	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TQ262A
<a href="#">TLV2264AQPWRQ1</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264AQ
TLV2264AQPWRQ1.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264AQ
TLV2264AQPWRQ1.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264AQ

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TLV2262A-Q1, TLV2264A-Q1 :**

- Catalog : [TLV2262A](#), [TLV2264A](#)
- Military : [TLV2262AM](#), [TLV2264AM](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2262AQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2264AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2262AQPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0
TLV2264AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

PW0014A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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