TL082-Q1 FET-Input Operational Amplifier

1 Features

- Qualified for automotive applications
- Low power consumption
- Wide common-mode and differential voltage ranges
- Low input bias and offset currents
- Low total harmonic distortion: 0.003% typical
- High input impedance: FET-input stage
- Latchup-free operation
- High slew rate: 21V/µs typical
- Common-mode input voltage range includes V_{CC+}

2 Applications

- TFT-LCD flat panel V_{COM} driver
- A/D converter buffer
- High side or low side sensing
- Headphone amplifier

3 Description

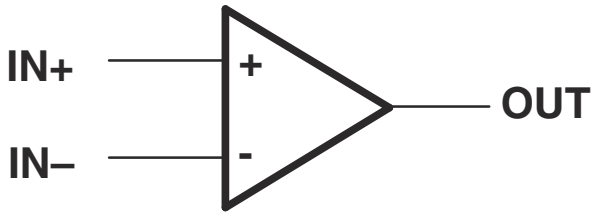
The TL082 FET-input operational amplifier incorporates well-matched, high-voltage FET, and bipolar transistors in a monolithic integrated circuit. The device features high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient.

The I-suffix device is characterized for operation from –40°C to 85°C. The Q-suffix device is characterized for operation from –40°C to 125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TL082-Q1	SOIC (8)	4.9mm × 6mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (Each Amplifier)

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4 Pin Configuration and Functions

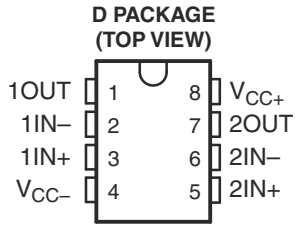

Table 4-1. Pin Functions TL082x

PIN		TYPE	DESCRIPTION
NAME	NO.		
1OUT	1	Output	Output Channel 1
1IN–	2	Input	Inverting input, channel 1
1IN+	3	Input	Non-inverting input, channel 1
VCC–	4	—	Power supply negative
2IN+	5	Input	Non-inverting input, channel 2
2IN–	6	Input	Inverting input, channel 2
2OUT	7	Output	Output Channel 2
VCC+	8	—	Power supply positive

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			VALUE
V_{CC+}	Supply voltage, positive(2)		18V
$V_{CC–}$	Supply voltage, negative(2)		–18V
V_{ID}	Differential input voltage(3)		±30V
V_I	Input voltage(2) (4)		±15V
	Duration of output short circuit(5)		Unlimited
	Continuous total power dissipation		(6)
T_A	Operating free-air temperature range	TL082I	–40°C to 85°C
		TL082Q	–40°C to 125°C
θ_{JA}	Package thermal impedance, junction to free air(7)		97°C/W
T_J	Operating virtual junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN–.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15V, whichever is less.
(5) The output can short to ground or to either supply. Limit temperature and supply voltages to verify that the dissipation rating is not exceeded.
(6) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is

$$PD = \frac{\left[T_J(max) - T_A\right]}{\theta_{JA}} \quad (1)$$

Operating at the absolute maximum T_J of 150°C can affect reliability.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 ESD Ratings

		VALUE	UNIT
ESD rating(1)	Human-Body Model	1.5kV (H1C)	V
	Charged-Device Model	1.5kV (C5)	V
	Machine Model	200V (M3)	V

(1) ESD protection level per JEDEC classifications JESD22A114 (HBM), JESD22A115 (MM), and JESD22-C101 (CDM).

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5.3 Electrical Characteristics

$V_{CC±}$ = ±15V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	T_A (2)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50Ω	25°C		±0.125	6	mV
			Full range			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50Ω	Full range		±0.3		µV/°C
I_{IO}	Input offset current(3)	V_O = 0	25°C		±10	100	pA
			Full range			20	nA
I_{IB}	Input bias current(3)	V_O = 0	25°C		±10	200	pA
			Full range			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10kΩ	25°C	±12	±14.950		V
A_{VD}	Large-signal differential voltage amplification	V_O = ±10V, R_L ≥ 2kΩ	25°C	94	130		dB
			Full range	83.5			
B1	Unity-gain bandwidth		25°C		4.5		MHz
r_i	Input resistance		25°C		10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min), V_O = 0, R_S = 50Ω	25°C	75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±15V to ± 9V, V_O = 0, R_S = 50Ω	25°C	80	130		dB
I_{CC}	Supply current (per amplifier)	V_O = 0, No load	25°C		0.560	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range for T_A is from –40°C to 85°C for I-suffix devices and from –40°C to 125°C for Q-suffix devices.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 5-20. Use pulse techniques that maintain the junction temperature as close to the ambient temperature as possible.

5.4 Operating Characteristics

$V_{CC±}$ = ±15V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain(1)	R_L = 2kΩ, C_L = 100pF	V_{ID} = 1V		21		V/µs
			V_{ID} = 100mV		0.5		
V_n	Equivalent input noise voltage	R_S = 20Ω	f = 1kHz		10.8		nV/√Hz
			f = 0.1Hz to 10Hz		1.8		μV_{PP}
I_n	Equivalent input noise current	R_S = 20Ω, f = 1kHz			2		fA/√Hz
THD	Total harmonic distortion	V_{Irms} = 6V, f = 1kHz, AVD = 1, R_S ≤ 1kΩ, R_L ≥ 2kΩ			0.003		%
		New Die, V_S = 40V, V_O = $3V_{RMS}$, G = 1, f = 1kHz			0.00021		%

(1) The new die has a slew boost architecture. For more details, see Full Power Bandwidth and Op Amp Distortion

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5.5 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

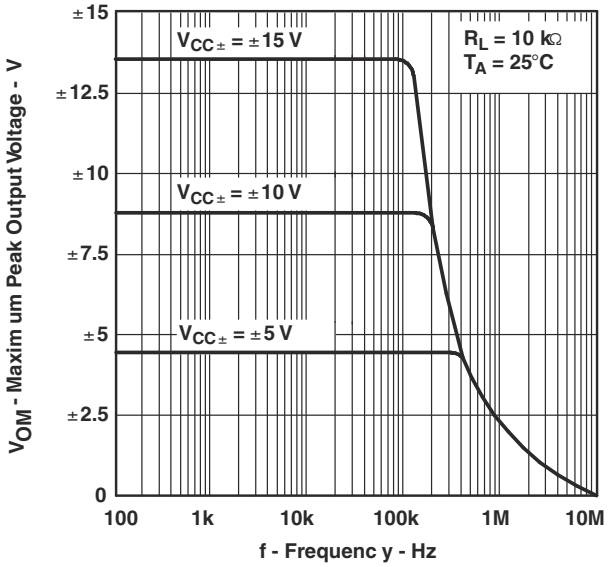

Figure 5-1. Maximum Peak Output Voltage vs Frequency, Old Die

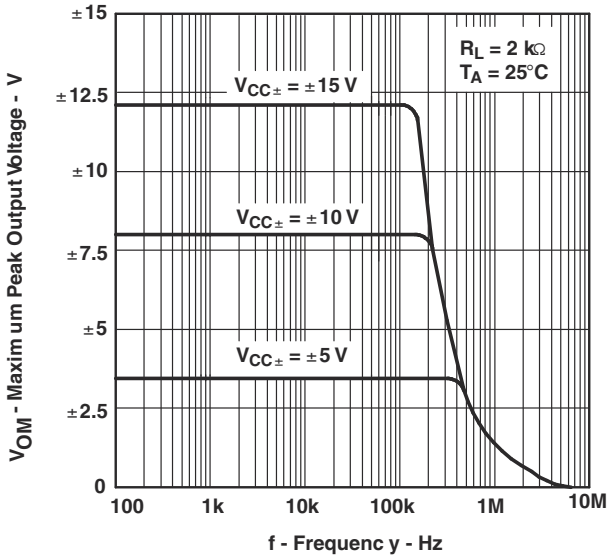

Figure 5-2. Maximum Peak Output Voltage vs Frequency, Old Die

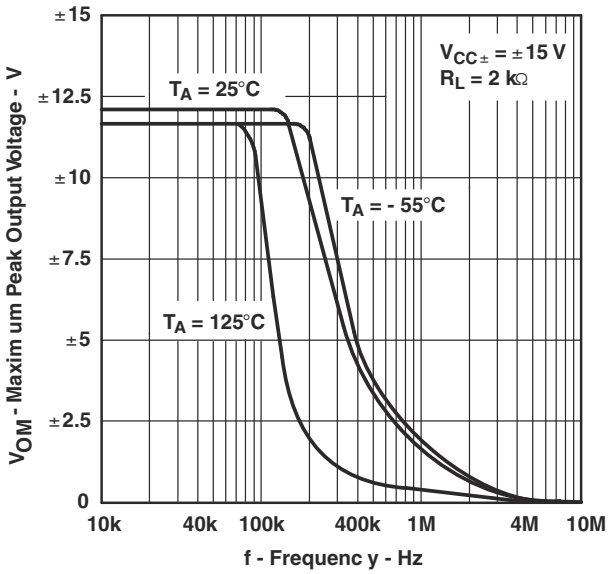

Figure 5-3. Maximum Peak Output Voltage vs Frequency, Old Die

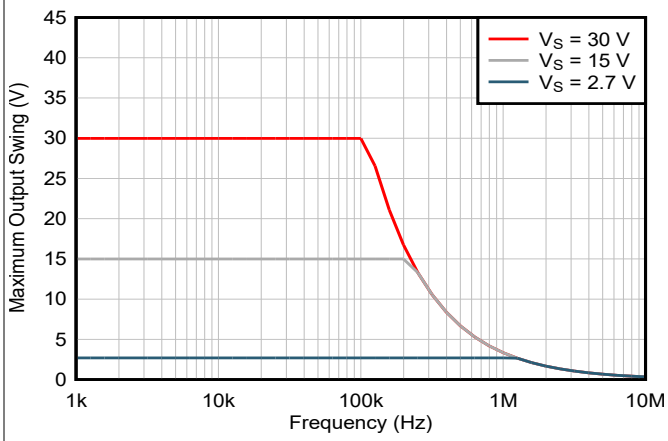

Figure 5-4. Maximum Output Voltage vs Frequency, New Die

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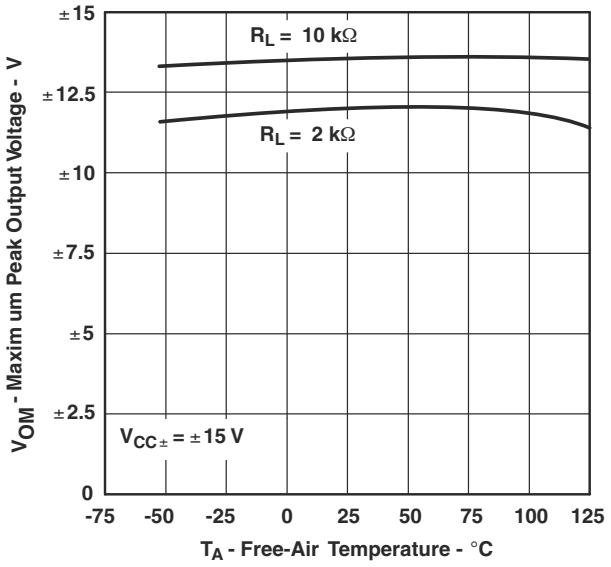


See Figure 6-1

Figure 5-5. Maximum Peak Output Voltage vs Free-Air Temperature, Old Die

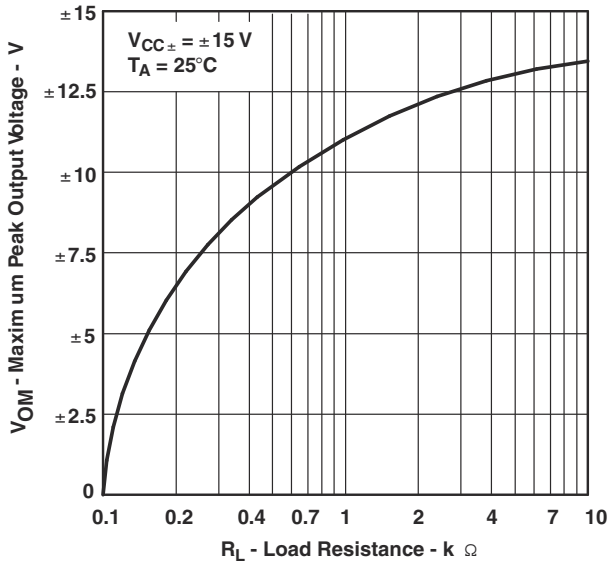


Figure 5-6. Maximum Peak Output Voltage vs Load Resistance, Old Die

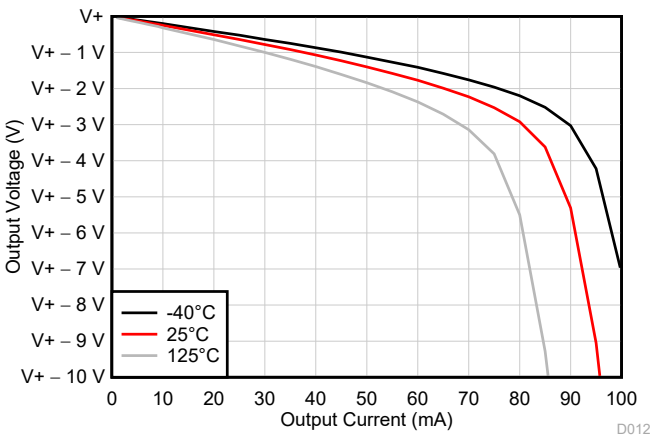


Figure 5-7. Output Voltage Swing vs Output Current (Sourcing), New Die

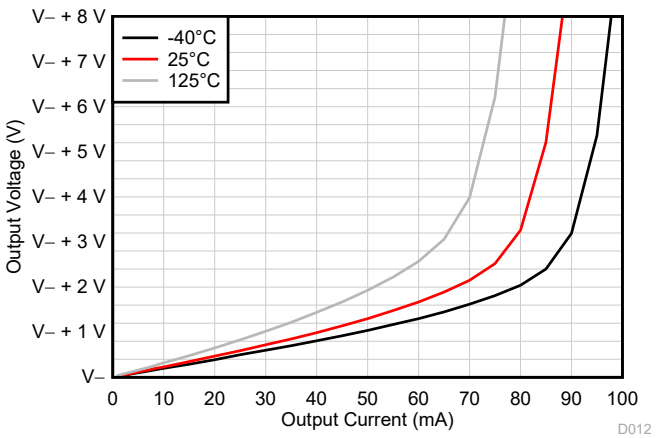


Figure 5-8. Output Voltage Swing vs Output Current (Sinking), New Die

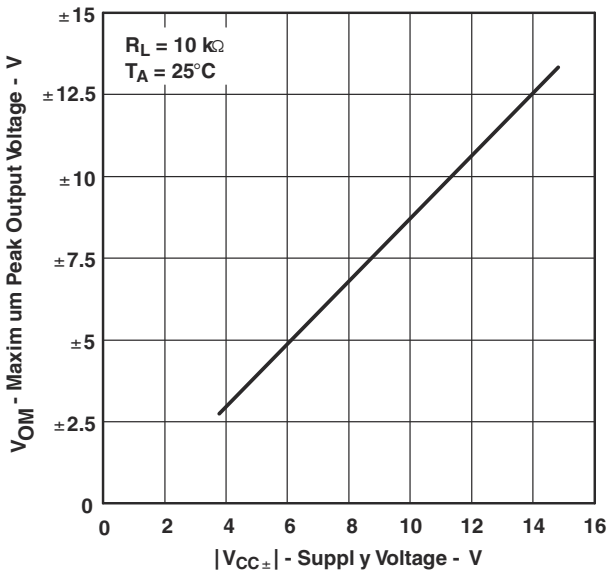


Figure 5-9. Maximum Peak Output Voltage vs Supply Voltage, Old Die

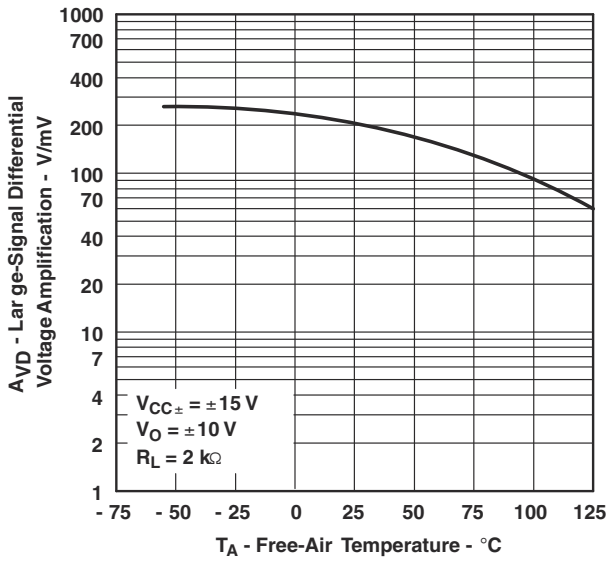


Figure 5-10. Large-signal Differential Voltage Amplification vs Free-air Temperature, Old Die

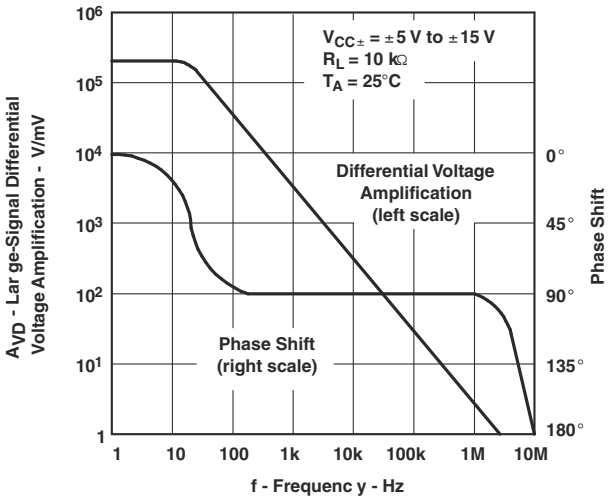
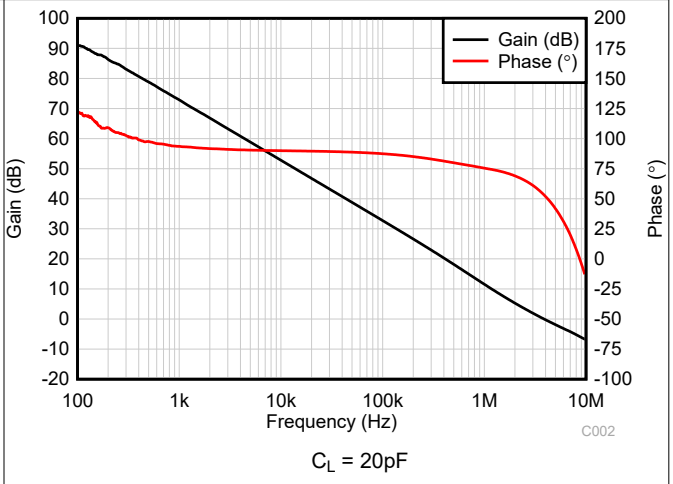


Figure 5-11. Large-signal Differential Voltage Amplification vs Frequency, Old Die



C_L = 20pF

Figure 5-12. Open-Loop Gain and Phase vs Frequency, New Die

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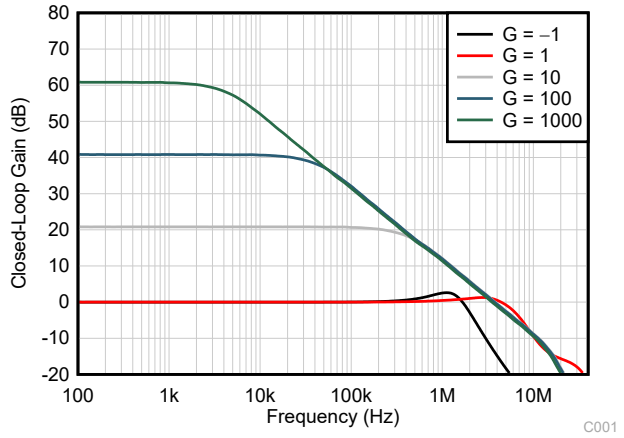

Figure 5-13. Closed-Loop Gain vs Frequency, New Die

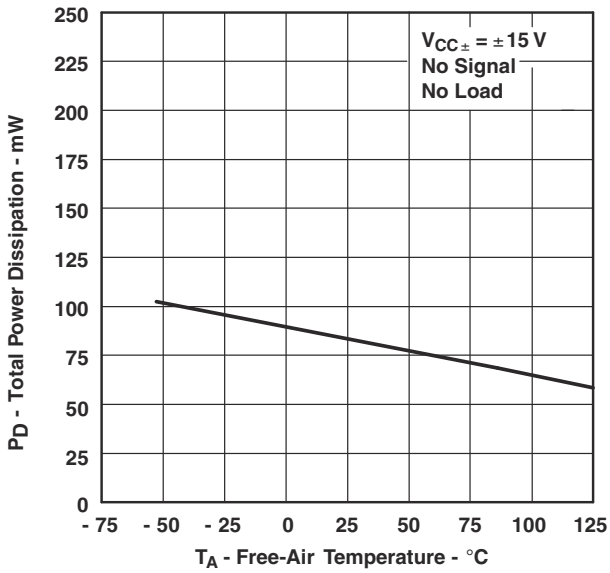

Figure 5-14. Power Dissipation vs Free-air Temperature, Old Die

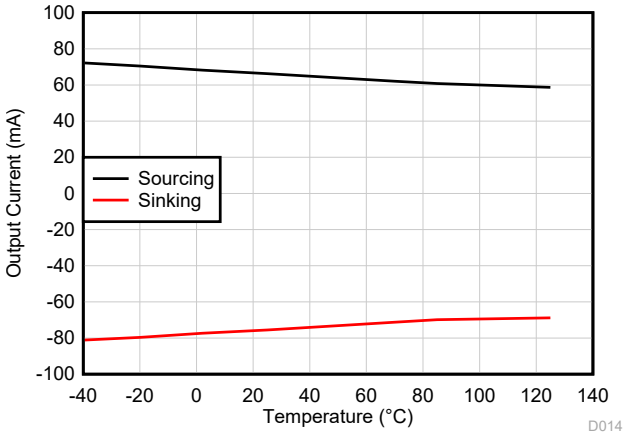

Figure 5-15. Short-Circuit Current vs Temperature, New Die

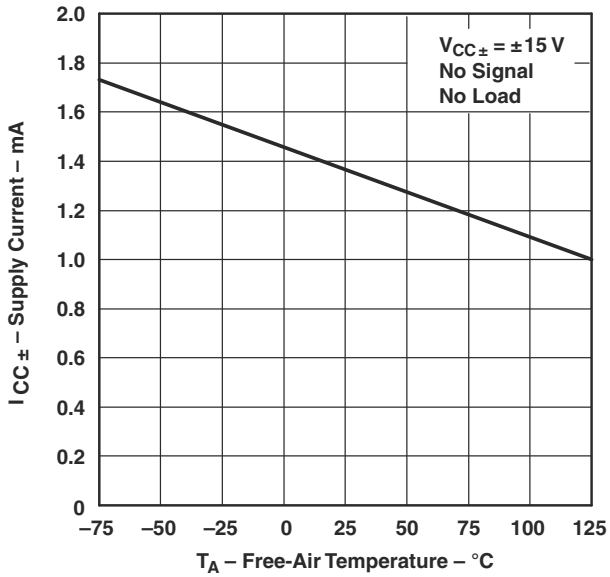

Figure 5-16. Supply Current vs Free-air Temperature, Old Die

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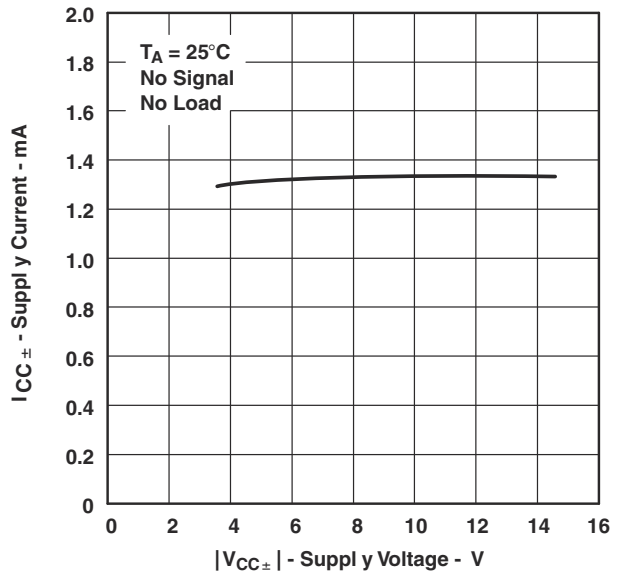

Figure 5-17. Supply Current vs Supply Voltage, Old Die

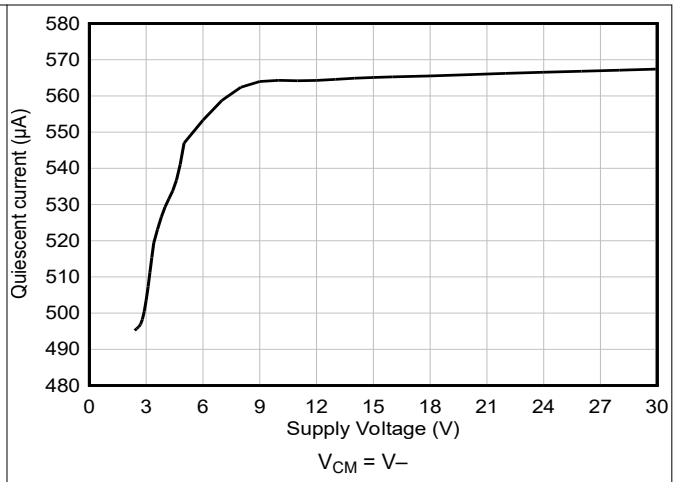

Figure 5-18. Quiescent Current vs Supply Voltage, New Die

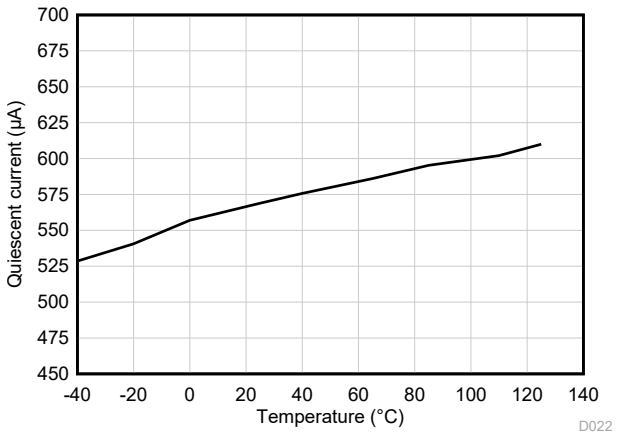

Figure 5-19. Quiescent Current vs Temperature, New Die

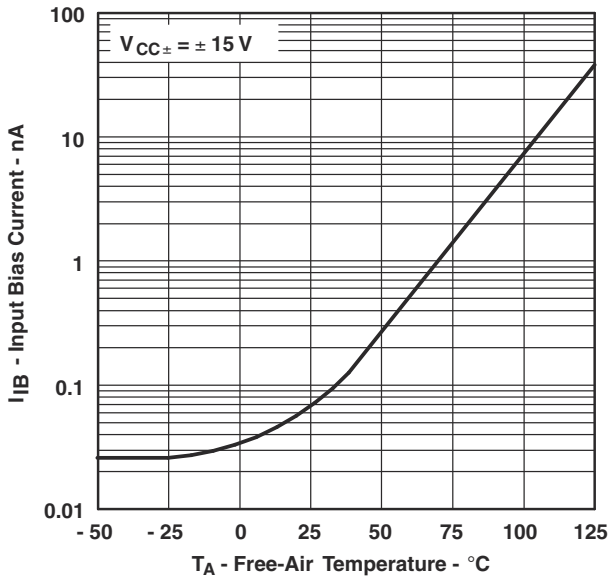

Figure 5-20. Input Bias Current vs Free-Air Temperature, Old Die

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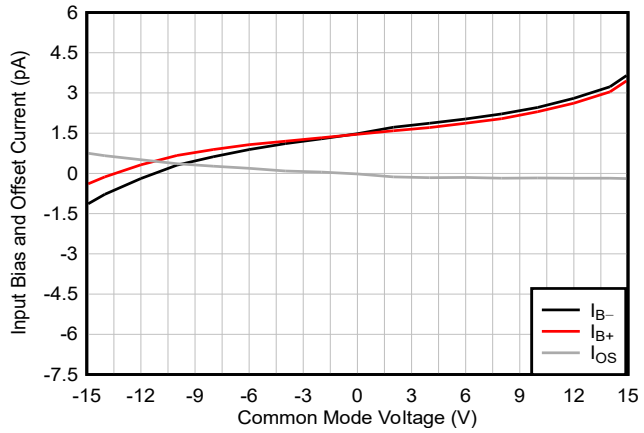


Figure 5-21. Input Bias Current vs Common-Mode Voltage, New Die

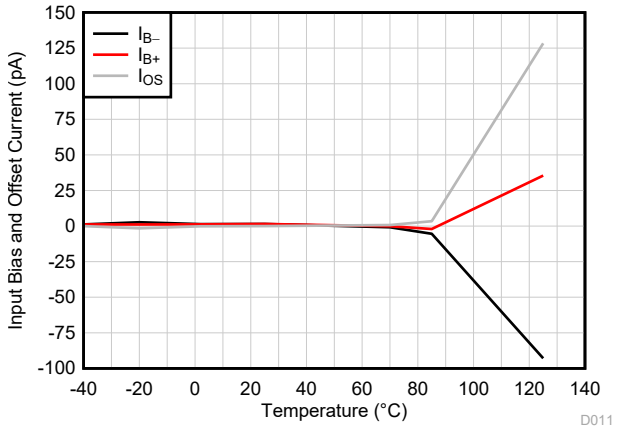


Figure 5-22. Input Bias Current vs Temperature, New Die

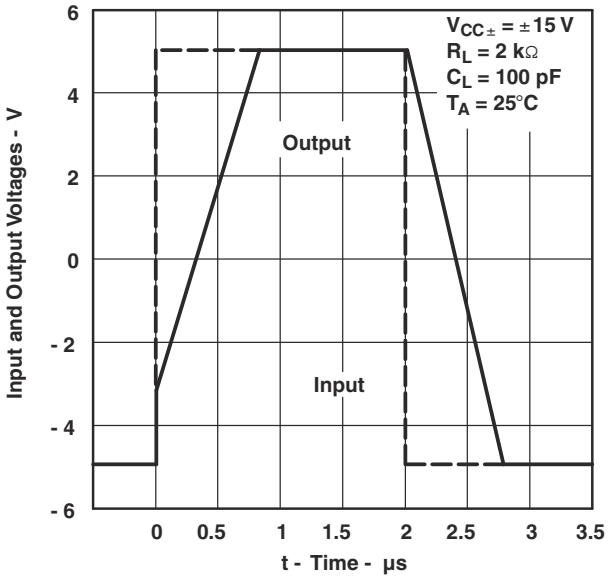
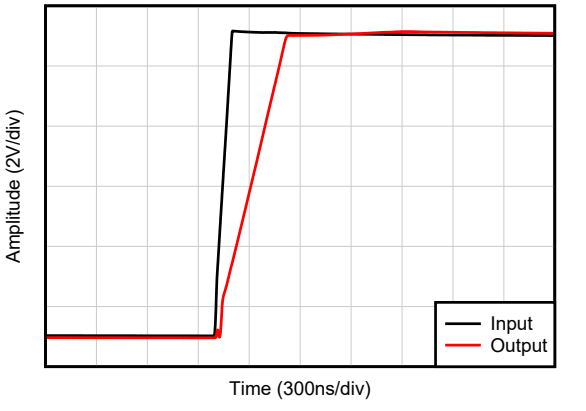
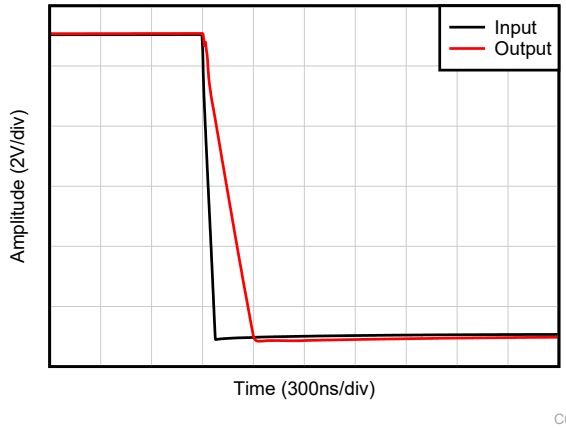


Figure 5-23. Voltage-Follower Large-Signal Pulse Response, Old Die



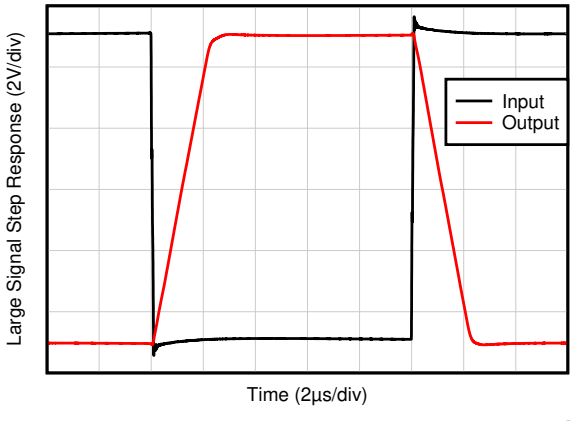
C_L = 20pF, G = 1

Figure 5-24. Large-Signal Step Response (Rising), New Die



C_L = 20pF, G = 1

Figure 5-25. Large-Signal Step Response (Falling), New Die



C_L = 20pF, G = –1

Figure 5-26. Large-Signal Step Response, New Die

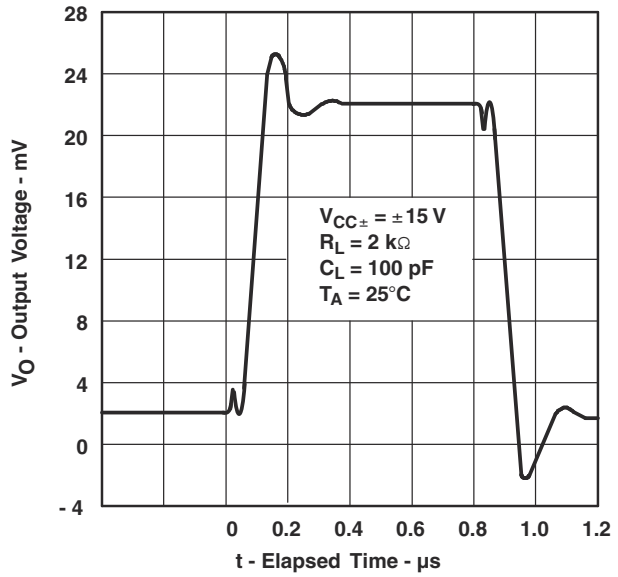


Figure 5-27. Output Voltage vs Elapsed Time, Old Die

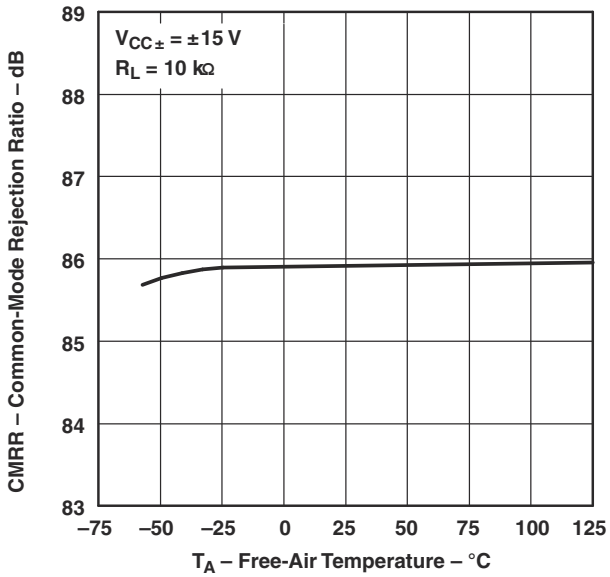


Figure 5-28. Common-Mode Rejection Ratio vs Free-Air Temperature, Old Die

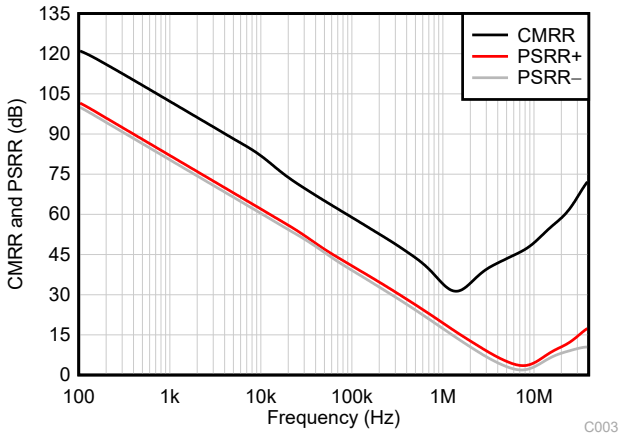


Figure 5-29. CMRR and PSRR vs Frequency, New Die

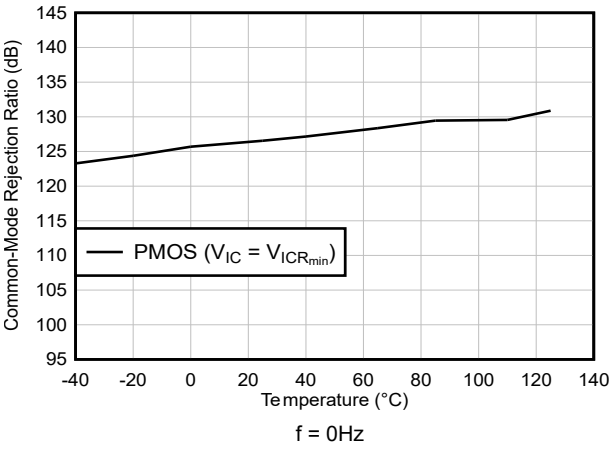


Figure 5-30. CMRR vs Temperature (dB), New Die

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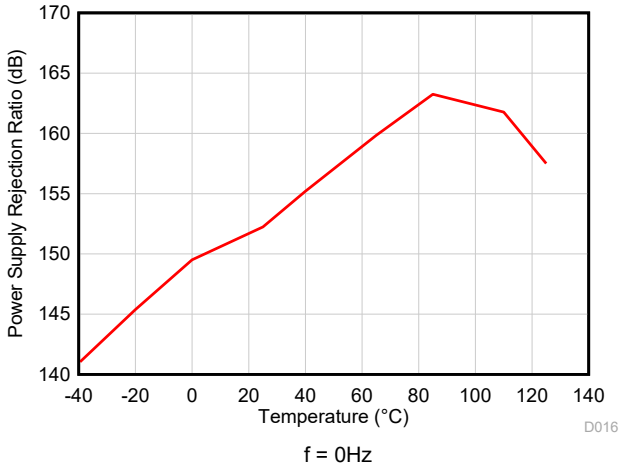


Figure 5-31. PSRR vs Temperature (dB), New Die

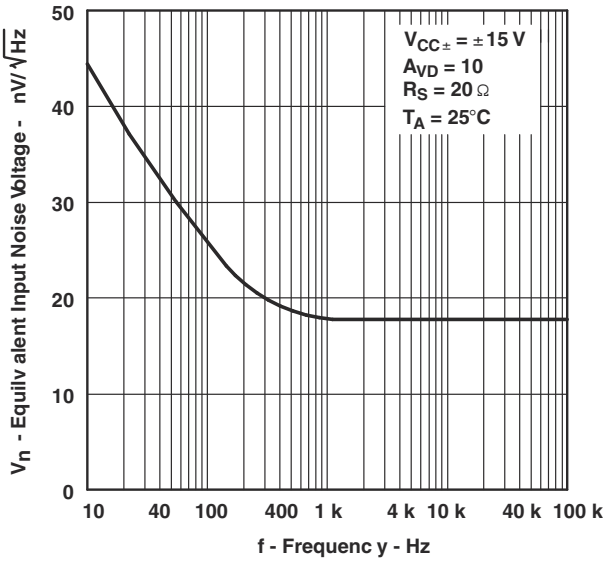


Figure 5-32. Equivalent Input Noise Voltage vs Frequency, Old Die

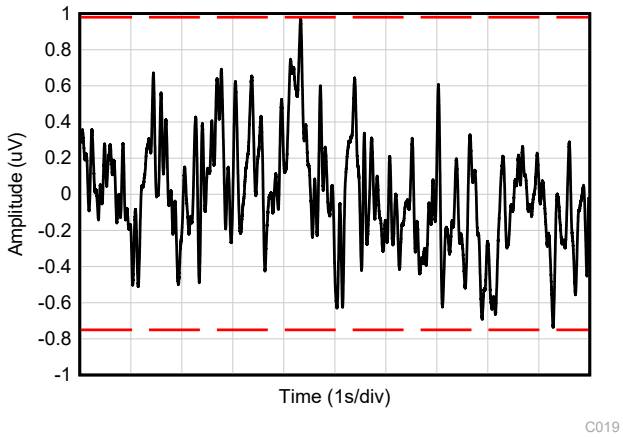


Figure 5-33. 0.1Hz to 10Hz Noise, New Die

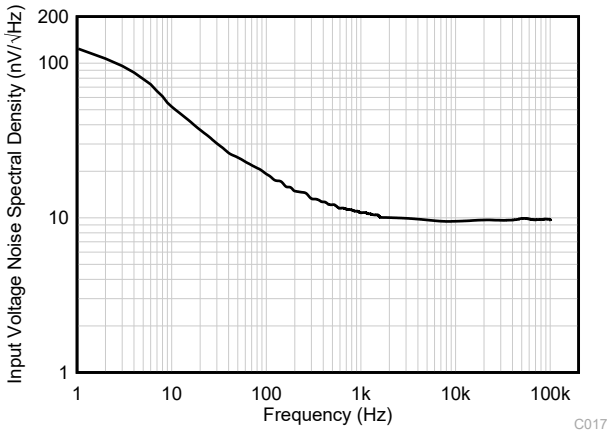


Figure 5-34. Input Voltage Noise Spectral Density vs Frequency, New Die

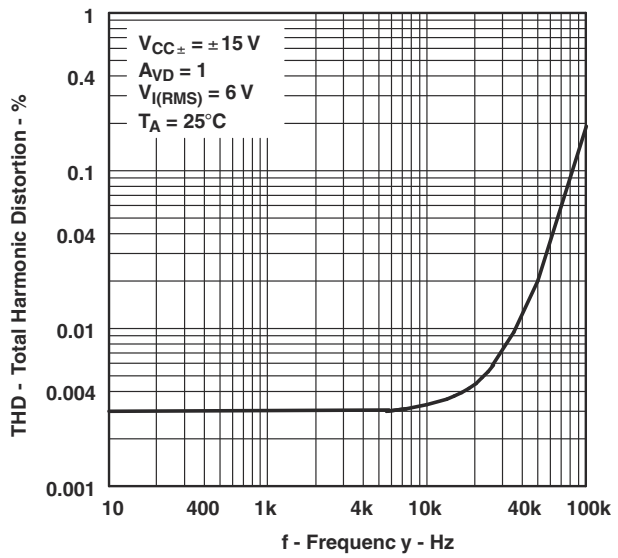
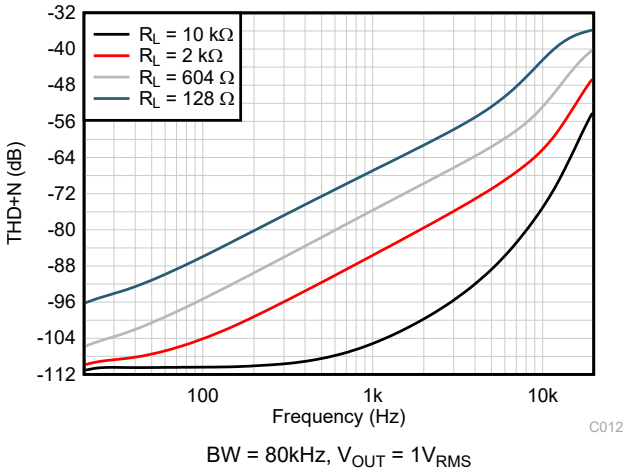
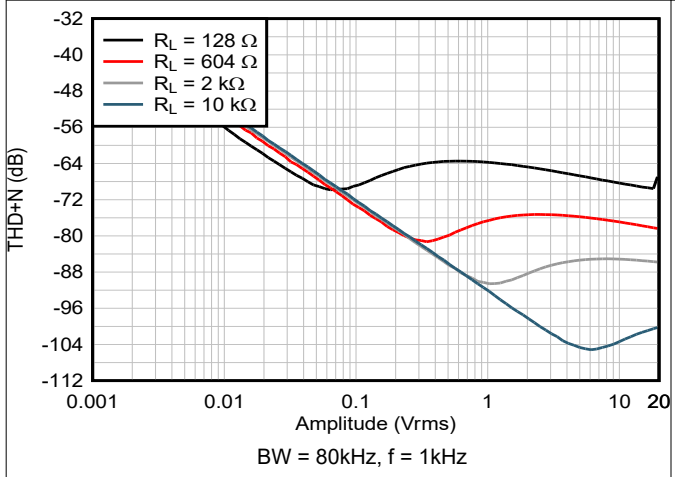


Figure 5-35. Total Harmonic Distortion vs Frequency, Old Die



BW = 80kHz, V_{OUT} = 1V_{RMS}

Figure 5-36. THD+N Ratio vs Frequency, New Die



BW = 80kHz, f = 1kHz

Figure 5-37. THD+N vs Output Amplitude, New Die

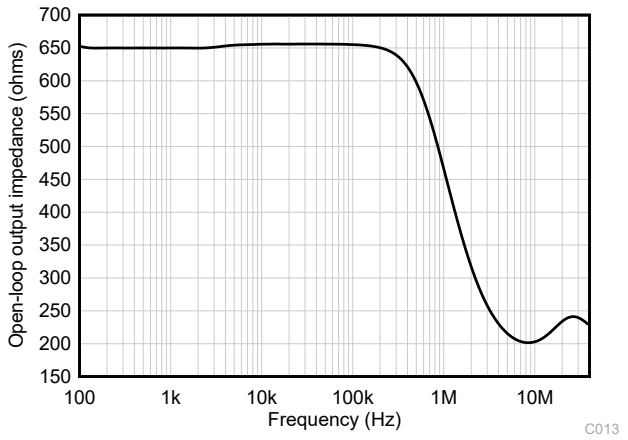


Figure 5-38. Open-Loop Output Impedance vs Frequency, New Die

5.6 Old Versus New Die Comparison

As of the publication of revision A of this datasheet, Texas Instruments has moved manufacturing of the die for TL082-Q1 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die. The die origin can separate from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “SHE”, for the new die the CSO is “RFB”. The old die information is in the shipping information. The old die information is maintained in this datasheet for comparison purposes, but all new manufacturing has moved to the new die.

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6 Parameter Measurement Information

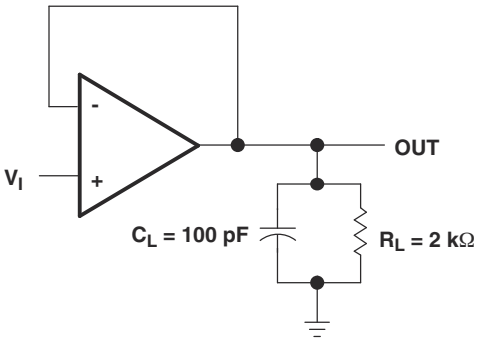

Figure 6-1. Test Figure 1

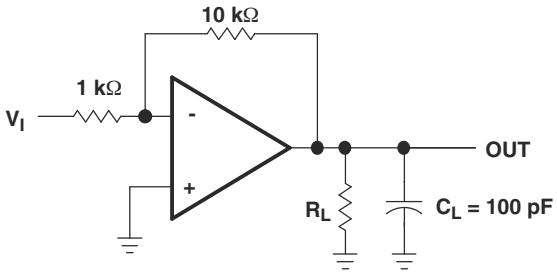

Figure 6-2. Test Figure 2

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7 Application Information

7.1 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.2 Application Information

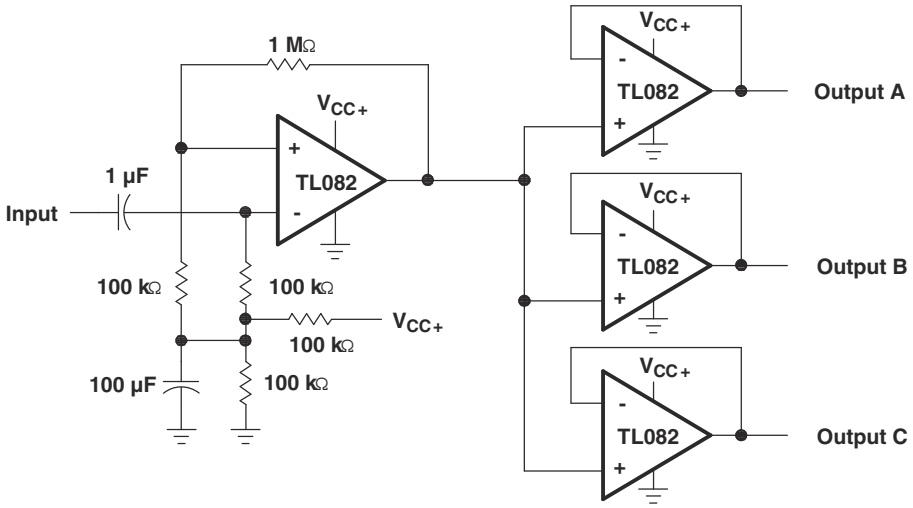

Figure 7-1. Audio-Distribution Amplifier

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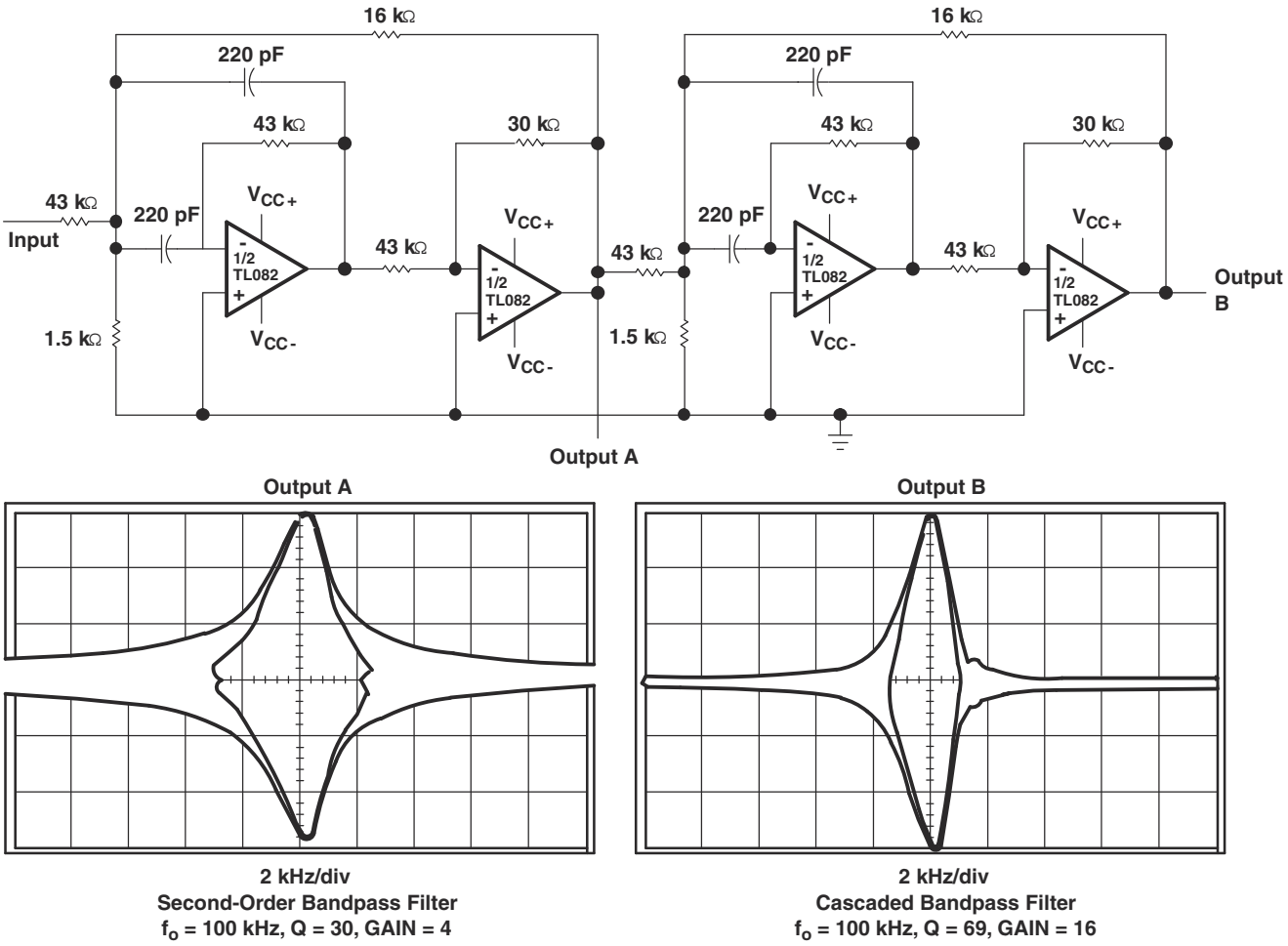

Figure 7-2. Positive-Feedback Bandpass Filter

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2007) to Revision A (June 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated High Slew rate from 13V/µs to 21V/µs	1
• Added *Applications* section	1
• Updated the description as per new die	1
• Added package information table	1
• Deleted ordering information table	1
• Added Pin Functions table	3
• Removed ESD ratings parameter	4
• Added *ESD Ratings* section	4
• Updated Input Offset Voltage typical value from 3mV to ± 0.125mV	5
• Updated Temperature Coefficient of Input Offset Voltage typical value from 18µV/°C to ± 0.3µV/°C	5
• Updated Input Offset Current typical value from 5pA to ± 10pA	5
• Updated Input Bias Current typical value from 30pA to ± 10pA	5
• Updated Maximum peak output voltage swing typical value from 13.5V to 14.950V	5
• Removed Maximum peak output voltage swing Full range values	5
• Updated Large-signal differential voltage amplification at 25°C minimum value from 50V/mV to 94dB and typical value from 200V/mV to 130dB and Full range minimum value from 15V/mV to 83.5dB	5
• Updated Unity-gain bandwidth from 3MHz to 4.5MHz	5
• Updated Common-mode rejection ratio typical value from 86dB to 100dB	5

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- Updated Supply Voltage rejection ratio typical value from 86dB to 130dB....5
- Updated Supply current typical from 1.4mA to 0.560mA....5
- Removed Slew rate at unity gain minimum value....5
- Updated Slew rate at unity gain typical value from 13V/µs to 21V/µs for V_{ID} = 1V....5
- Added Slew rate at unity gain typical value at V_{ID} = 100mV to reflect new die performance....5
- Removed Rise time and Overshoot factor spec....5
- Updated Equivalent input noise voltage at 1kHz typical value from 18nV/√Hz to 10.8nV/√Hz....5
- Updated Equivalent input noise voltage from 0.1Hz to 10Hz typical value from 4µV_{PP} to 1.8µV_{PP}....5
- Updated Equivalent input noise current typical value from 0.01pA/√ Hz to 2fA/√ Hz....5
- Added New Die specifications for Total Harmonic Distortion....5
- Updated plots as per New Die Characteristics....6
- Added *Old Versus New Die Comparison*....14
- Removed 100kHz Quadrature Oscillator from *Application Information* section....16

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL082IDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I
TL082IDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I
TL082QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL082Q
TL082QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL082Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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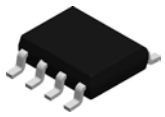
OTHER QUALIFIED VERSIONS OF TL082-Q1 :

- Catalog : TL082
- Military : TL082M

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

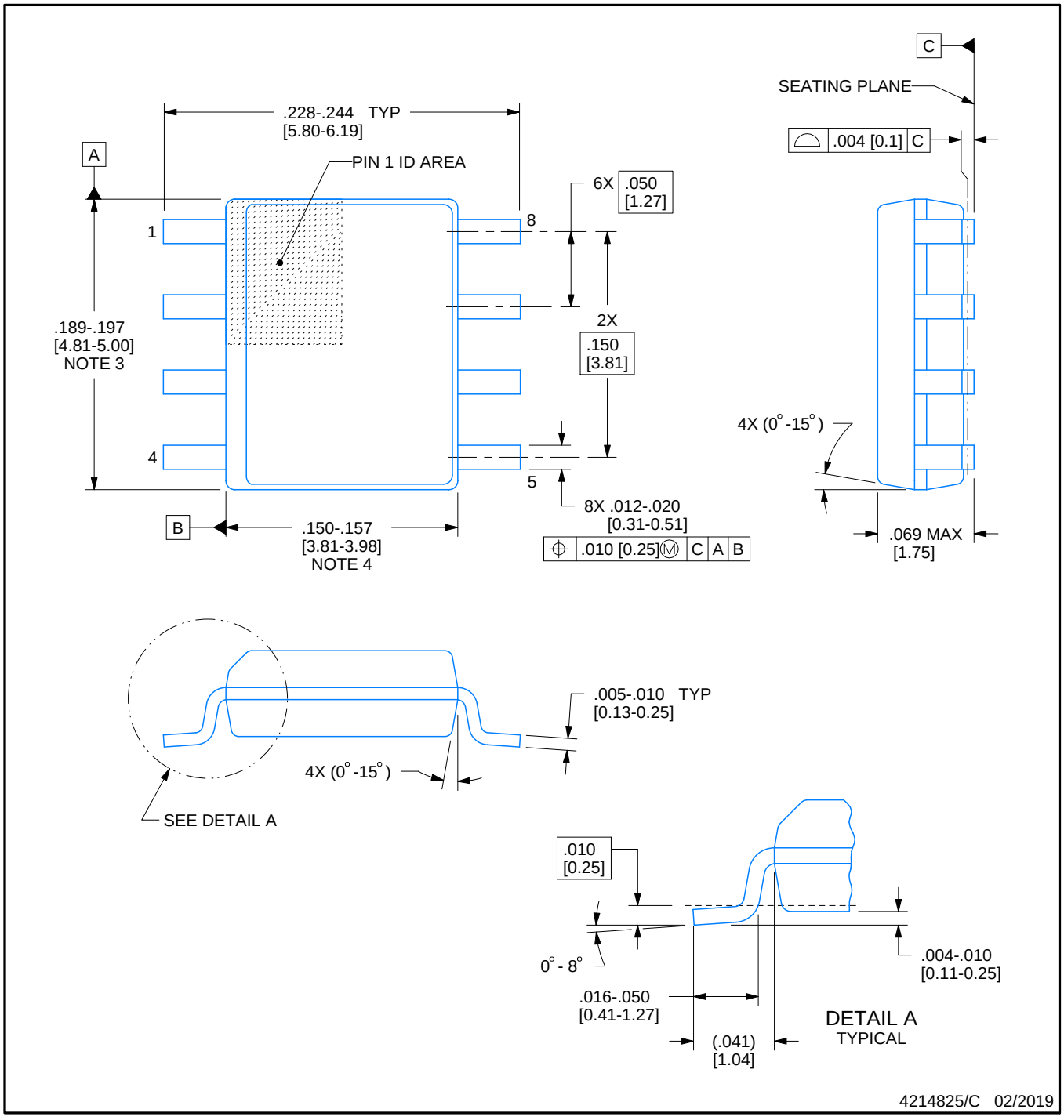


PACKAGE OUTLINE

D0008A

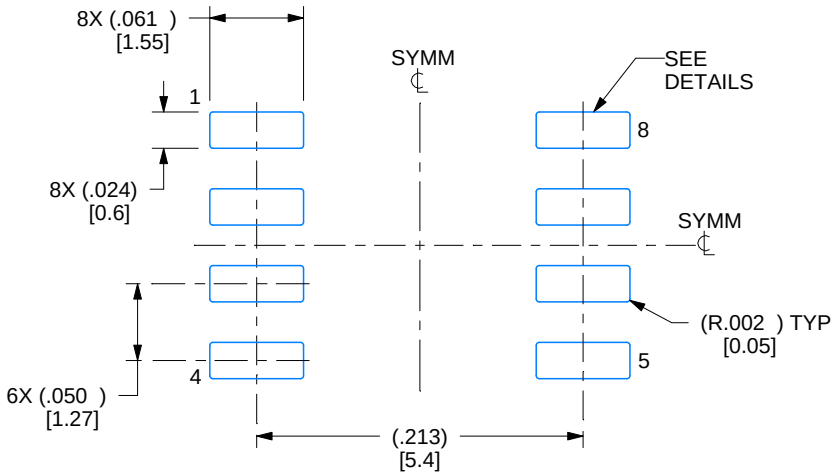
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

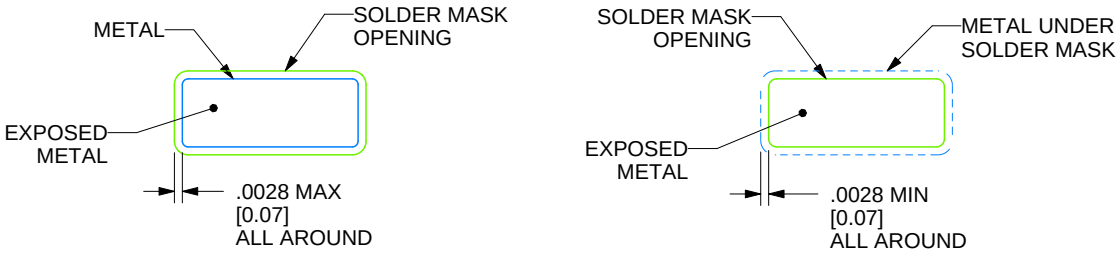


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

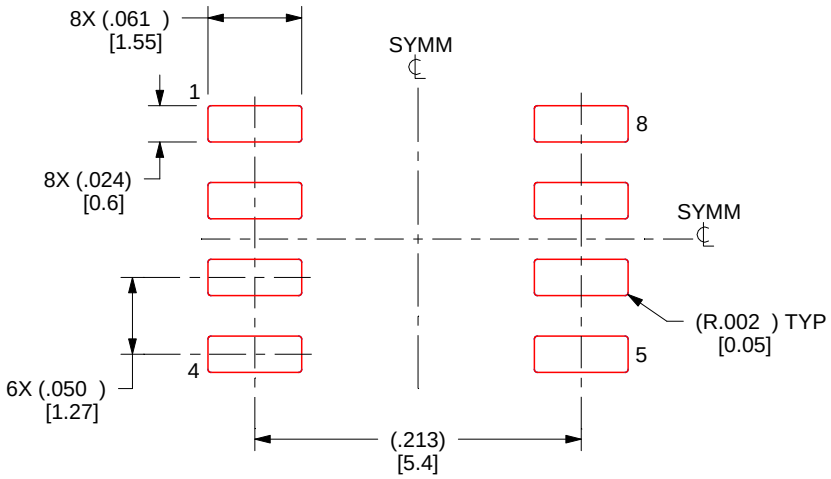
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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