Enhanced FET Low-Offset Operational Amplifiers

1 Features

- Direct upgrades to TL07x and TL08x FET operational amplifiers
- On-chip offset-voltage trimming for improved DC performance

2 Description

The TL05x series of FET-Input operational amplifiers offers improved dc and ac characteristics over the TL07x and TL08x families of FET operational amplifiers. Texas Instruments improved FET process and optimized designs also yield improved bandwidth and slew rate without increased power consumption. The TL05x devices are pin-compatible with the TL07x and TL08x and can be used to upgrade existing circuits or for excellent performance in new designs.

FET operational amplifiers offer the inherently higher input impedance of the FET-Input transistors, without sacrificing the output drive associated with bipolar amplifiers. This makes them better designed for interfacing with high-impedance sensors or very low-level ac signals.

The TL05x family are designed to offer higher precision and better ac response than the TL08x, with the low noise floor of the TL07x. Designers requiring significantly faster ac response can consider the Excalibur TLE208x and TLE207x families of FET operational amplifiers.

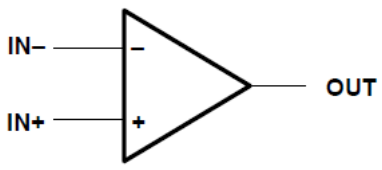
Because FET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required, and loads terminated to a virtual-ground node at mid-supply. Texas Instruments TLE2426 integrated virtual ground generator is useful when operating FET amplifiers from single supplies.

The TL05x are fully specified at ±15V and ±5V. For operation in low-voltage and/or single-supply systems, Texas Instruments LinCMOS families of operational amplifiers (TLC-prefix) are recommended. When moving from FET to CMOS amplifiers, particular attention to be paid to the slew rate and bandwidth requirements, and also the output loading.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TL051, TL052	D (SOIC, 8)	4.90mm × 3.90mm
TL051, TL052	P (PDIP, 8)	9.81mm × 6.30mm
TL052	PS (SOP, 8)	6.20mm × 5.30mm
TL054	D (SOIC, 14)	4.90mm × 3.90mm
	DB (SSOP, 14)	6.20mm × 5.30mm
	N (PDIP, 14)	19.30mm × 6.30mm
	NS (SOP, 14)	10.30mm × 5.30mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.



Symbol (Each Amplifier)

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3 Pin Configuration and Functions

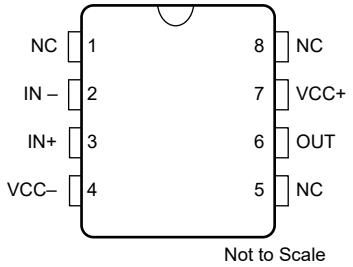


Figure 3-1. TL051 D or P Package, 8-Pin SOIC or PDIP (Top View)

Table 3-1. Pin Functions TL051x

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
NC	1	—	Do not connect
IN–	2	Input	Inverting Input
IN+	3	Input	Non Inverting Input
VCC–	4	—	Power supply negative
NC	5	—	Do not connect
OUT	6	Output	Output
VCC+	7	—	Power supply positive
NC	8	—	Do not connect

(1) I = input, O = output.

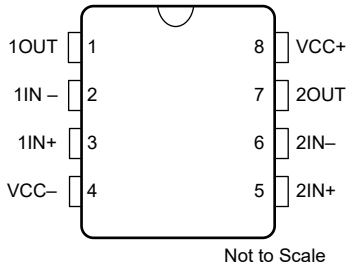


Figure 3-2. TL052 D, P, or PS Package, 8-Pin SOIC, PDIP, or SOP (Top View)

Table 3-2. Pin Functions TL052x

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1OUT	1	Output	Output Channel 1
1IN–	2	Input	Inverting input, channel 1
1IN+	3	Input	Non-inverting input, channel 1
VCC–	4	—	Power supply negative
2IN+	5	Input	Non-inverting input, channel 2
2IN–	6	Input	Inverting input, channel 2
2OUT	7	Output	Output Channel 2
VCC+	8	—	Power supply positive

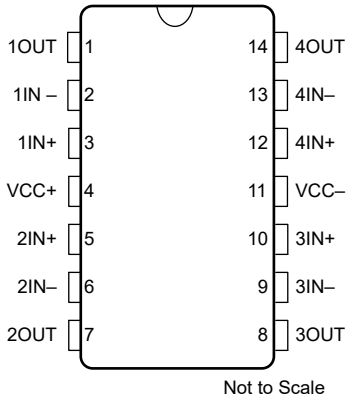


Figure 3-3. TL054 D, DB, N, or NS Package, 14-Pin SOIC, SSOP, PDIP, or SOP (Top View)

Table 3-3. Pin Functions TL054x

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1OUT	1	Output	Output channel 1
1IN–	2	Input	Inverting input, channel 1
1IN+	3	Input	Non-inverting input, channel 1
VCC+	4	—	Power supply positive
2IN+	5	Input	Non-inverting input, channel 2
2IN–	6	Input	Inverting input, channel 2
2OUT	7	Output	Output channel 2
3OUT	8	Output	Output channel 3
3IN–	9	Input	Inverting input, channel 3
3IN+	10	Input	Non-inverting input, channel 3
VCC–	11	—	Power supply negative
4IN+	12	Input	Non-inverting input, channel 4
4IN–	13	Input	Inverting input, channel 4
4OUT	14	Output	Output channel 4

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)			18	V
$V_{CC–}$	Supply voltage(2)			–18	V
	Differential input voltage(3)		–30	30	V
V_I	Input voltage range(2) (4)	Any input	–15	15	V
I_I	Input current	Each input	–1	1	mA
I_O	Output current	Each input	–80	80	mA
	Total current into V_{CC+}			160	mA
	Total current out of $V_{CC–}$			160	mA
	Duration of short-circuit current at (or below) 25°C			Unlimited	
T_J	Operating virtual junction temperature			150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 4.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN–.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 1, whichever is less.

4.2 Thermal Information

THERMAL METRIC(1)		TL051, TL052	TL051, TL052	TL052	TL054				UNIT
		D	P	PS	D	DB	N	NS	
		8	8	8	14	14	14	14	
θ_{JA}	Package thermal impedance	97	85	95	86	96	80	76	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.

4.3 Recommended Operating Conditions

			C SUFFIX		I SUFFIX		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC±}$	Supply voltage		±5	±15	±5	±15	V
V_{IC}	Common-mode input voltage	$V_{CC±}$ = ±5V	–1	4	–1	4	V
		$V_{CC±}$ = ±15V	–11	11	–11	11	
T_A	Operating free-air temperature		0	70	–40	85	°C

4.4 TL05xC and TL05xAC Electrical Characteristics

at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A [1]	TL05xC, TL05xAC						UNIT
					$V_{CC\pm}$ = ±5V			$V_{CC\pm}$ = ±15V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0 V_{IC} = 0 R_S = 50Ω	TL051C,Tl052C	25°C		0.75	3.5		0.65	1.5	mV
			TL054C	25°C			5.5			4	
			TL051C,TL052C	Full range			4.5			2.5	
			TL054C	Full range			7.7			6.2	
			TL051AC,TL052AC	25°C		0.57	2.8		0.5	0.8	
			TL054AC	25°C			3.5			1.5	
			TL051AC,TL052AC	Full range			3.8			1.8	
			TL054AC	Full range			5.7			3.7	
a_{VIO}	Temperature coefficient of input offset voltage		TL05xC	25°C to 70°C		25			23		µV/°C
			TL05xAC	25°C to 70°C		24			23		
	Input offset-voltage long-term drift	V_O = 0 R_S = 50Ω V_{IC} = 0		25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0 V_{IC} = 0		25°C		10	100		10	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	V_O = 0 V_{IC} = 0		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	–1 to 4	–2.3 to 5.1		–11 to 11	–12.3 to 15.1		V
				Full range	–1 to 4			–11 to 11			

4.4 TL05xC and TL05xAC Electrical Characteristics (continued)

at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A [1]	TL05xC, TL05xAC						UNIT
					$V_{CC\pm}$ = ±5V			$V_{CC\pm}$ = ±15V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10kΩ		25°C	–2.5	–3.5		–12	–13.2		V
				Full range	–2.5			–12			
		R_L = 2kΩ		25°C	–2.3	–3.2		–11	–12		
				Full range	–2.3			–11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2kΩ		25°C	104	130		120	145		dB
				0°C		125			142		
				70°C		125			142		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			10		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR\ min}$ V_O = 0 R_S = 50Ω		25°C	65	84		75	92		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_O = 0 R_S = 50Ω		25°C	75	99		75	99		dB
				0°C	75	98		75	98		
				70°C	75	97		75	97		
I_{CC}	Supply current (four amplifiers)	V_O = 0 No load		25°C		8.1	11.2		8.4	12.8	mA
				0°C		8.5	12.8		8.5	12.8	
				70°C		7.9	11.2		8.2	12.8	
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100		25°C		106			106		dB
SR+	Positive slew rate at unity gain	R_L = 2kΩ C_L = 100pF		25°C		15.4			17.8		V/μs
				Full range		16.4			17.5		
SR–	Negative slew rate at unity gain[2]			25°C		13.9			15.9		
				Full range		16			15.5		
V_n	Equivalent input noise voltage[3]	R_S = 20Ω	f = 10Hz	25°C		50			50		nV/√Hz
			f = 1kHz	25°C		10.8			10.8		

4.4 TL05xC and TL05xAC Electrical Characteristics (continued)

at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A (1)	TL05xC, TL05xAC							UNIT
				$V_{CC\pm}$ = ±5V				$V_{CC\pm}$ = ±15V			
				MIN	TYP		MAX	MIN	TYP	MAX	
I_n	Equivalent input noise current	f = 1kHz	25°C		2				2		fA/√Hz
THD	Total harmonic distortion(4)	R_S = 1kΩ f = 1kHz R_L = 2kΩ	25°C		0.00021				0.00021		%
B_1	Unity-gain bandwidth	V_I = 10mV C_L = 25pF, R_L = 2kΩ	25°C		4.5				4.5		MHz
φ_m	Phase margin at unity gain	V_I = 10mV C_L = 25pF R_L = 2kΩ	25°C		60				60		deg

(1) Full range is 0°C to 70°C.
(2) This parameter is tested on a sample basis for the TL05xA. For other test requirements, please contact the factory. This statement has no bearing on testing or non-testing of other parameters.
(3) Typical values are based on the input offset-voltage shift observed through 168 hours of operating life test at T_A = 150°C, extrapolated to T_A = 25°C using the Arrhenius equation, and assuming an activation energy of 0.96 eV.
(4) For $V_{CC\pm}$ = ±5V, V_O = ±2.3V, or for $V_{CC\pm}$ = ±15V, V_O = ±10V.

4.5 TL05xI and TL05xAI Electrical Characteristics

PARAMETER		TEST CONDITIONS		T_A [1]	TL05xI, TL05xAI						UNIT
					$V_{CC±}$ = ±5V			$V_{CC±}$ = ±15V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0 V_{IC} = 0 R_S = 50Ω	TL051C, TI052C	25°C		0.75	3.5		0.65	1.5	mV
			TL054C	25°C			5.5			4	
			TL051C, TI052C	Full range			5.3			3.3	
			TL054C	Full range			8.8			7.3	
			TL051AC, TL052AC	25°C		0.57	2.8		0.5	0.8	
			TL054AC	25°C			3.5			1.5	
			TL051AC, TL052AC	Full range			4.6			2.6	
			TL051C, TI052C	Full range			6.8				
a_{VIO}	Temperature coefficient of input offset voltage[2]		TL051I	25°C to 85°C		25			24		µV/°C
			TL051AI	25°C to 85°C		25			23		
	Input offset-voltage long-term drift[3]			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0	V_{IC} = 0,	25°C		10	100		10		pA
				85°C		0.06	10		0.07		nA
I_{IB}	Input bias current	V_O = 0	V_{IC} = 0,	25°C		20	200		30		pA
				85°C		0.6	20		0.7		nA
V_{ICR}	Common-mode input voltage range			25°C	–1 to 4	–2.3 to 5.1		–11 to 11	–12.3 to 15.1		V
				Full range	–1 to 4			–11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			

4.5 TL05xI and TL05xAI Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS		T_A [1]	TL05xI, TL05xAI						UNIT
					$V_{CC\pm}$ = ±5V			$V_{CC\pm}$ = ±15V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10kΩ		25°C	–2.5	–3.5		–12	–13.2		V
				Full range	–2.5			–12			
		R_L = 2kΩ		25°C	–2.3	–3.2		–11	–12		
				Full range	–2.3			–11			
A_{VD}	Large-signal differential voltage amplification[4]	R_L = 2kΩ		25°C	104	130		120	145		dB
				0°C		125			142		
				85°C		125			142		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			10		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin} VO= 0, R_S = 50Ω		25°C	65	84		75	92		dB
				–40°C	65	83		75	90		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_O = 0, R_S = 50Ω		25°C	75	99		75	99		dB
				–40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current	V_O = 0	No load	25°C		2.6	3.2		2.7		mA
				–40°C		2.4	3.2		2.6		
				85°C		2.5	3.2		2.6		
V_{O1}/V_{O2}	Crosstalk attenuation			25°C		106.0206			106.0206		dB
SR+	Positive slew rate at unity gain	R_L = 2kΩ	C_L = 100pF	25°C		15.4		9	17.8		V/µs
				Full range				8			
SR–	Negative slew rate at unity gain			25°C		13.9		9	15.9		
				Full range				8			
V_n	Equivalent input noise voltage	R_S = 20Ω	f = 10Hz	25°C		50			50		nV/√Hz
			f = 1kHz	25°C		10.8			10.8		
I_n	Equivalent input noise current	f = 1kHz		25°C		2			2		fA/√Hz
THD	Total harmonic distortion	R_S = 1kΩ, f =1kHz	R_L = 2kΩ	25°C		0.00021			0.00021		%
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 25pF,	R_L = 2kΩ	25°C		4.5			4.5		MHz
φ_m	Phase margin at unity gain	V_I = 10mV, C_L = 25pF	R_L = 2kΩ	25°C		60			60		deg

(1) Full range is –40°C to 85°C.

(2) This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or non-testing of other parameters.
(3) Typical values are based on the input offset-voltage shift observed through 168 hours of operating life test at T_A = 150°C, extrapolated to T_A = 25°C using the Arrhenius equation, and assuming an activation energy of 0.96 eV.
(4) For $V_{CC\pm}$ = ±5V, V_O = ±2.3V, or for $V_{CC\pm}$ = ±15V, V_O = ±10V.

4.6 Typical Characteristics

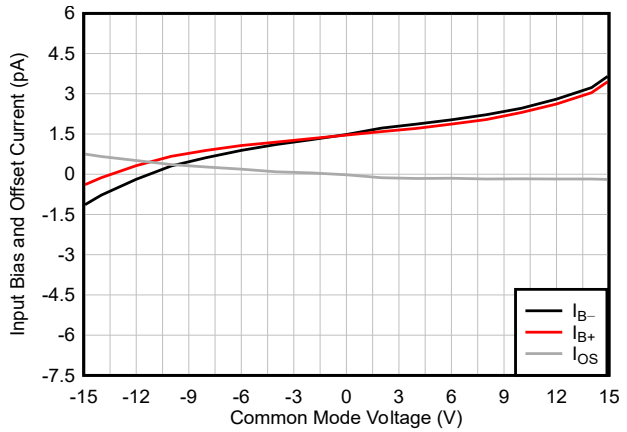
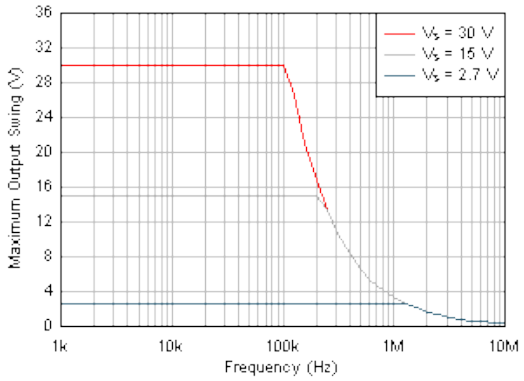


Figure 4-1. Input Bias Current vs Common-Mode Input Voltage



A. Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 4-2. Maximum Peak-to-Peak Output Voltage vs Frequency

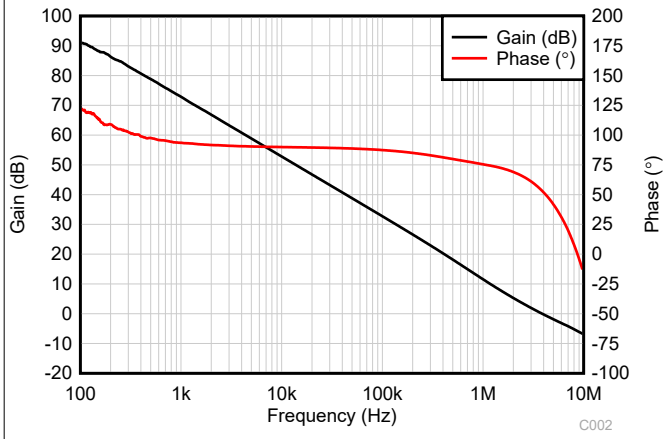


Figure 4-3. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

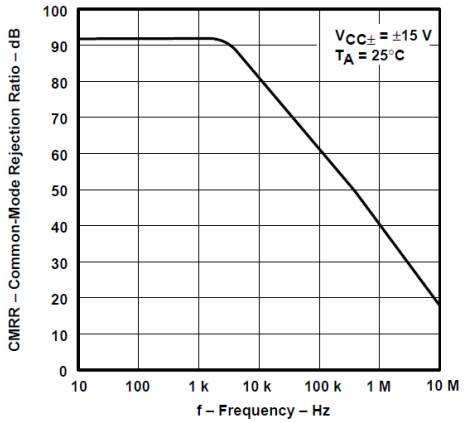
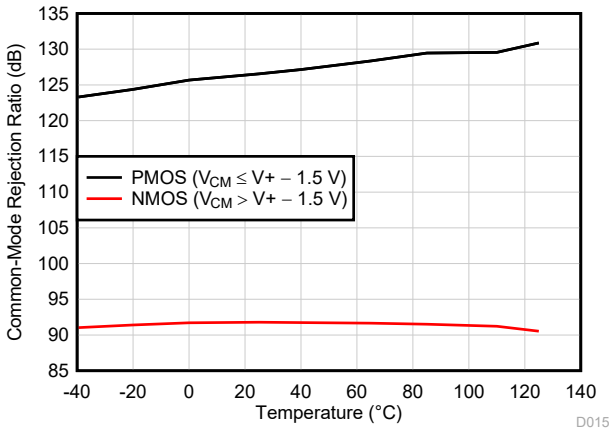


Figure 4-4. Common-Mode Rejection Ratio vs Frequency

4.6 Typical Characteristics (continued)



A. Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 4-5. Common-Mode Rejection Ratio vs Free-Air Temperature

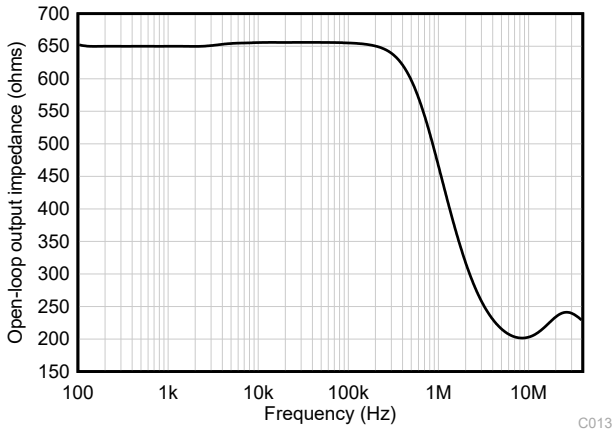
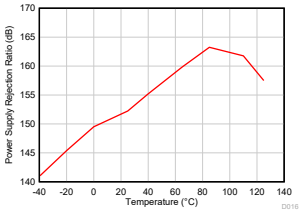
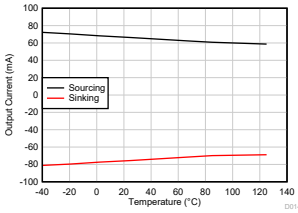


Figure 4-6. Output Loop Output Impedance vs Frequency



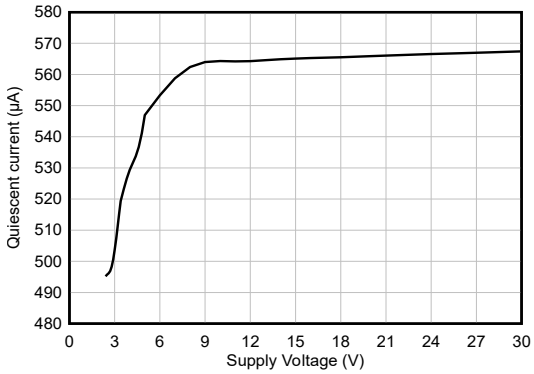
A. Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 4-7. PSSR vs Temperature(dB)



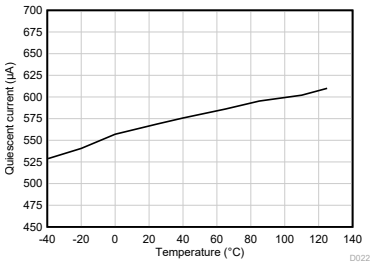
A. Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 4-8. Short-Circuit Output Current vs Temperature



A. Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 4-9. Supply Current vs Supply Voltage



A. Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 4-10. Supply Current vs Free-Air Temperature

4.6 Typical Characteristics (continued)

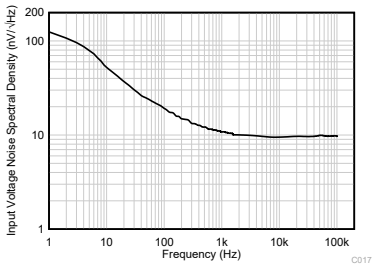
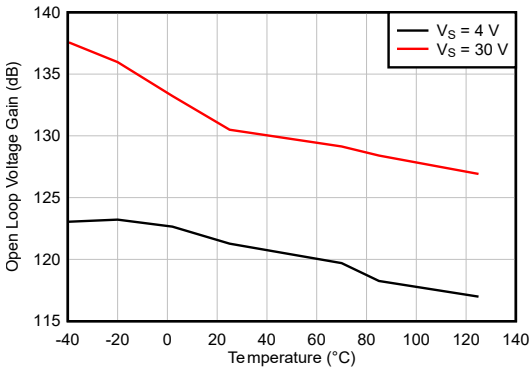
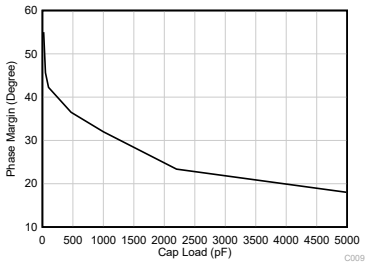


Figure 4-11. Equivalent Input Noise Voltage vs Frequency



A. Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 4-12. Unity-Gain Bandwidth vs Free-Air Temperature



A. Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 4-13. Phase Margin vs Load Capacitance

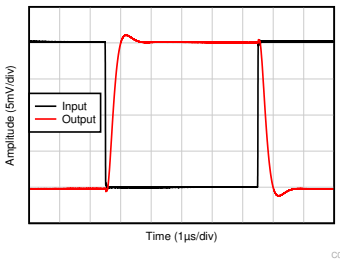


Figure 4-14. Voltage-Follower Small-Signal Pulse Response

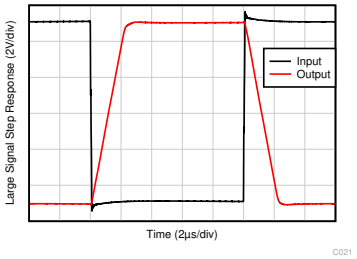


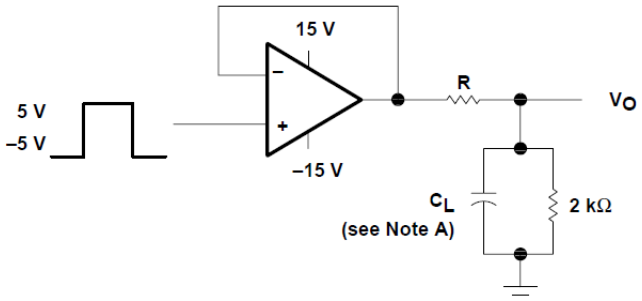
Figure 4-15. Voltage-Follower Large-Signal Pulse Response

5 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

5.1 Application Information



A. C_L includes fixture capacitance.

Figure 5-1. Test Circuit for Output Characteristics

5.1.1 Output Characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 10pF load capacitance. The TL05x and TL05xA drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load can alleviate the problem. Capacitive loads of 1000pF, and larger, can be driven if enough resistance is added in series with the output (see Figure 5-2).

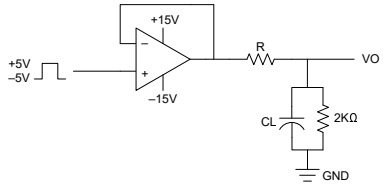


Figure 5-2. Test Circuit for Output Characteristics

Note

CL includes fixture capacitance.

5.1.2 Input Characteristics

The TL05x and TL05xA are specified with a minimum and a maximum input voltage that, if exceeded at either input, can cause the device to malfunction.

Because of the extremely high input impedance and resulting low-bias current requirements, the TL05x and TL05xA are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets easily can exceed bias current requirements and cause degradation in system performance. Good practice is to include guard rings around inputs (see Figure 5-3). These guards can be driven from a low-impedance source at the same voltage level as the common-mode input.

Unused amplifiers can be connected as grounded unity-gain followers to avoid possible oscillation.

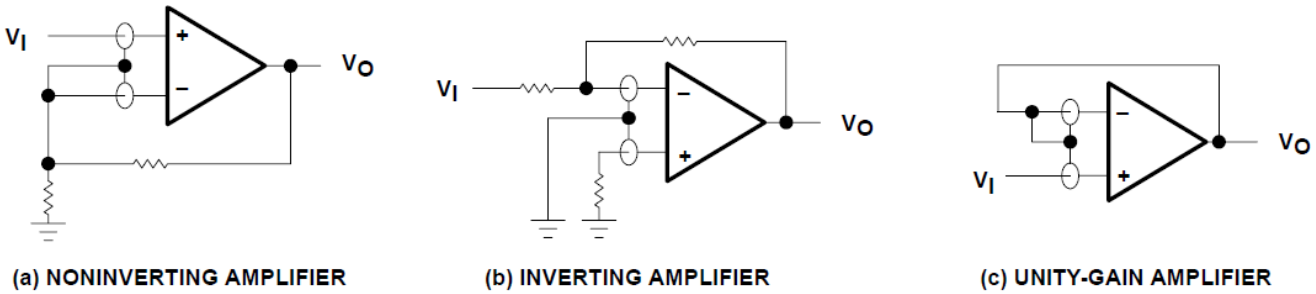


Figure 5-3. Use of Guard Rings

5.1.3 Noise Performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input-bias current requirements of the TL05x and TL05xA result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50kΩ.

5.1.4 Instrumentation Amplifier with Adjustable Gain/Null

The instrumentation amplifier in Figure 5-4 benefits greatly from the high input impedance and stable input offset voltage of the TL05xA. Amplifiers U1A, U1B, and U2A form the actual instrumentation amplifier, while U2B provides offset null. Potentiometer R1 provides gain adjustment. With R1 = 2kΩ, the circuit gain equals 100, while with R1 = 200kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

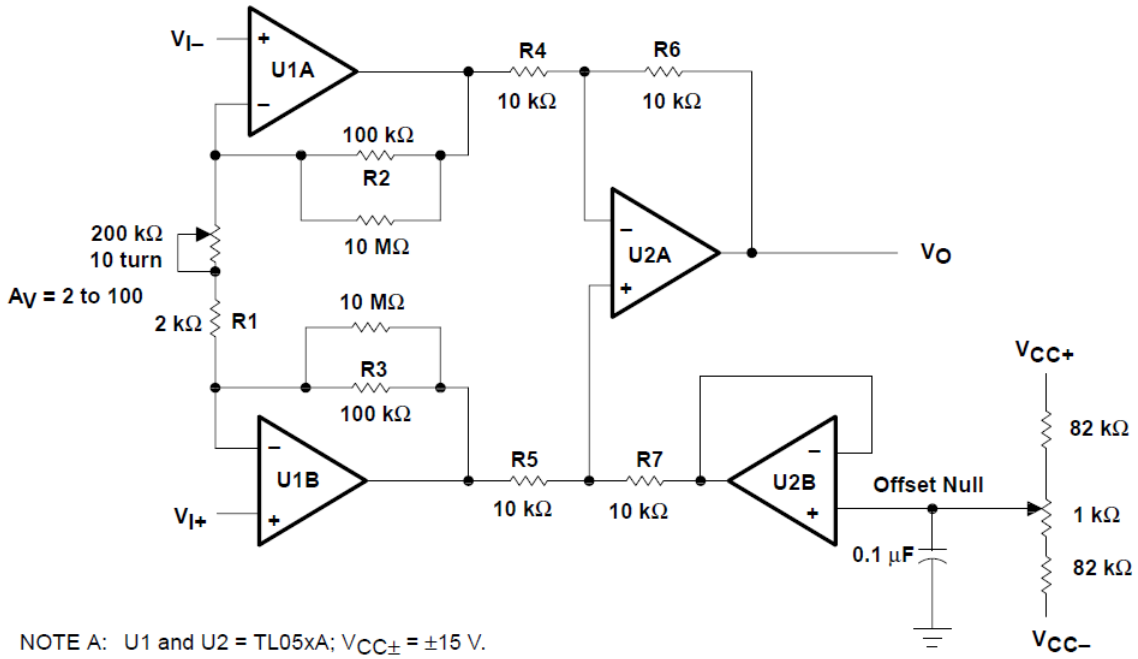
$$A_V = 1 + \left(\frac{R2 + R3}{R1}\right) \quad (1)$$

Readjusting the offset null is necessary when the circuit gain is changed. If U2B is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL05xA minimizes the dc error of the circuit. For best matching, all resistors can be one-percent tolerance. The matching between R4, R5, R6, and R7 controls the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This dc error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature also creates an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets, rather than initial offsets. The improved stability of Texas Instruments enhanced FETs minimizes the error resulting from change in input offset voltage with time. Assuming V_I equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2}\left[\left(1 + \frac{R3}{R1}\right)\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R2}{R1}\left(\frac{R6}{R4}\right)\right] \quad (2)$$

$$-V_{IO1}\left[\frac{R3}{R1}\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R6}{R4}\left(1 + \frac{R2}{R1}\right)\right] + V_{IO3}\left(1 + \frac{R6}{R4}\right) \quad (3)$$



NOTE A: U1 and U2 = TL05xA; $V_{CC\pm}$ = ±15 V.

Figure 5-4. Instrumentation Amplifier

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2003) to Revision B (January 2026)	Page
• Deleted "Precision grades are available (1.5mV, TL051A)"	1
• Changed BIFET to FET	1
• Deleted "Faster slew rate (20V/µs typ) without increased power consumption	1
• Changed JFET to FET	1
• Deleted Trimming function details	1
• Deleted Bipolar and CMOS power consumption comparison	1
• Updated Pin1 and Pin5 from OFFSET1 and OFFSET2 to NC	3
• Combined Single, dual and quad channel electrical characteristics	6
• Changed Input Offset Current value from 4pA to 10pA for 5V and 5pA to 10pA for 15V	6
• Changed Input Noise at 10Hz from 70nV/√Hz to 50nV/√Hz and at 1kHz from 18nV/√Hz to 10.8nV/√Hz	6
• Changed Crosstalk Attenuation value from 120dB to 106dB	6
• Updated Large-signal differential voltage amplification section values	6
• Combined Single, dual and quad channel electrical characteristics	9
• Updated Large-signal differential voltage amplification section values	9

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL051ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	051AC
TL051ACP	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	0 to 70	TL051ACP
TL051CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	TL051C
TL051CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL051C
TL051CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL051C
TL051CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL051CP
TL051CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL051CP
TL051CPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TL052ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	052AC
TL052ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	052AC
TL052ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	052AC
TL052ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL052ACP
TL052ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL052ACP
TL052AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	052AI
TL052AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	052AI
TL052AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	052AI
TL052AIP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL052AIP
TL052AIP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL052AIP
TL052CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	TL052C
TL052CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL052C
TL052CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL052C
TL052CDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL052C
TL052CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL052C
TL052CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL052CP
TL052CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL052CP
TL052CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T052
TL052CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T052
TL052ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	TL052I
TL052IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL052I

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL052IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL052I
TL052IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL052I
TL052IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL052I
TL052IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL052IP
TL052IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL052IP
TL054ACD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL054AC
TL054ACDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL054AC
TL054ACDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL054AC
TL054ACN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL054ACN
TL054ACN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL054ACN
TL054AID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	TL054AI
TL054AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL054AI
TL054AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL054AI
TL054AIDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL054AI
TL054AIDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL054AI
TL054CD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL054C
TL054CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL054C
TL054CDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL054C
TL054CN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL054CN
TL054CN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL054CN
TL054CNSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL054
TL054CNSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL054
TL054ID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	TL054I
TL054IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL054I
TL054IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL054I
TL054IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL054IN
TL054IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL054IN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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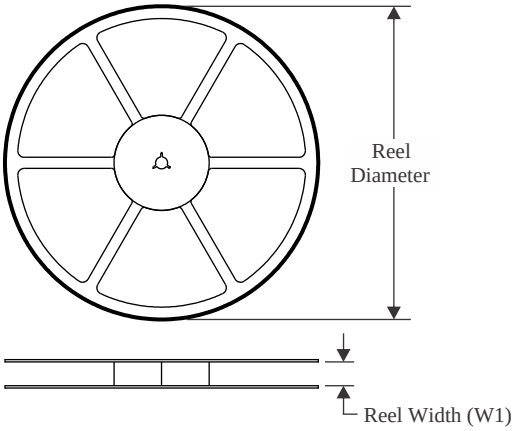
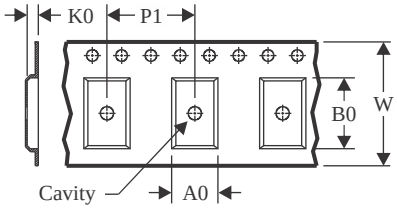
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

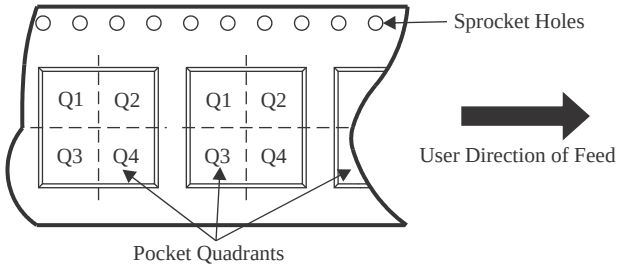


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

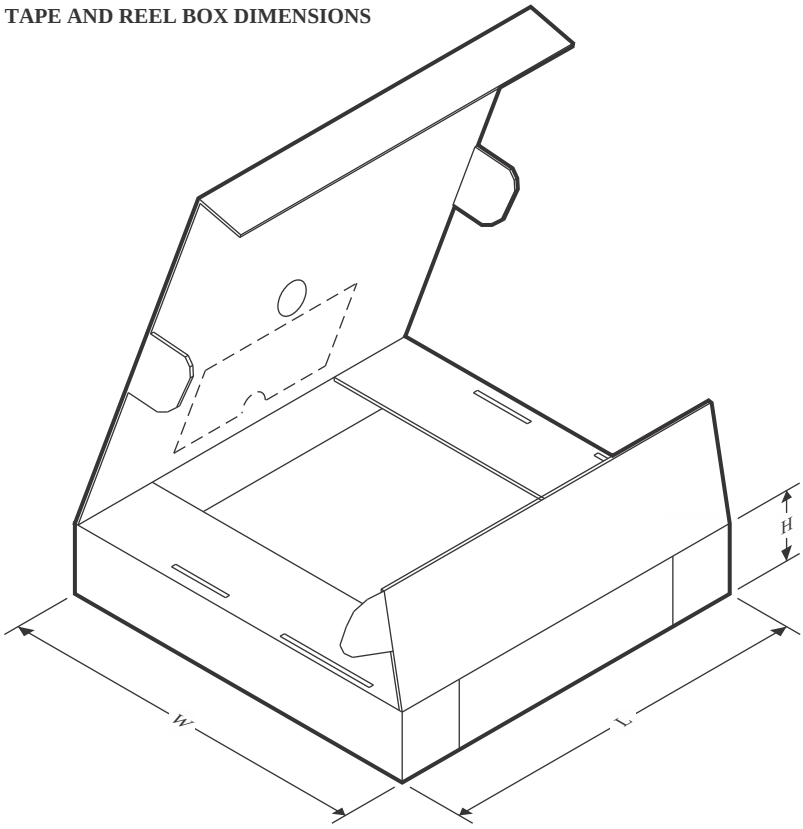
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL051CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL052ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL052AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL052CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL052CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL052IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL052IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL054ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL054AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL054AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL054CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL054CNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
TL054IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

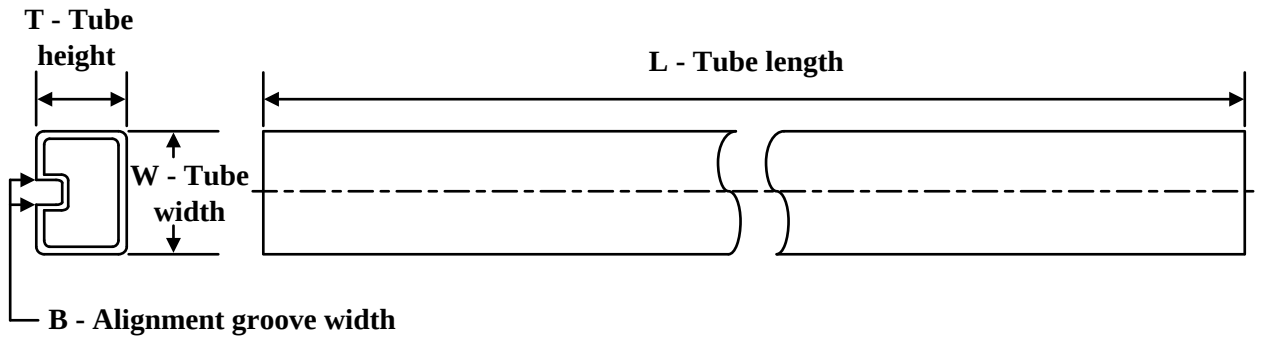
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

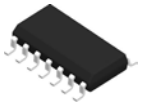
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL051CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL052ACDR	SOIC	D	8	2500	353.0	353.0	32.0
TL052AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TL052CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL052CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL052IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL052IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TL054ACDR	SOIC	D	14	2500	340.5	336.1	32.0
TL054AIDR	SOIC	D	14	2500	340.5	336.1	32.0
TL054AIDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TL054CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL054CNSR	SOP	NS	14	2000	353.0	353.0	32.0
TL054IDR	SOIC	D	14	2500	340.5	336.1	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL051CP	P	PDIP	8	50	506	13.97	11230	4.32
TL051CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL052ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL052ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL052AIP	P	PDIP	8	50	506	13.97	11230	4.32
TL052AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL052CP	P	PDIP	8	50	506	13.97	11230	4.32
TL052CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL052IP	P	PDIP	8	50	506	13.97	11230	4.32
TL052IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL054ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL054ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL054CN	N	PDIP	14	25	506	13.97	11230	4.32
TL054CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL054IN	N	PDIP	14	25	506	13.97	11230	4.32
TL054IN.A	N	PDIP	14	25	506	13.97	11230	4.32

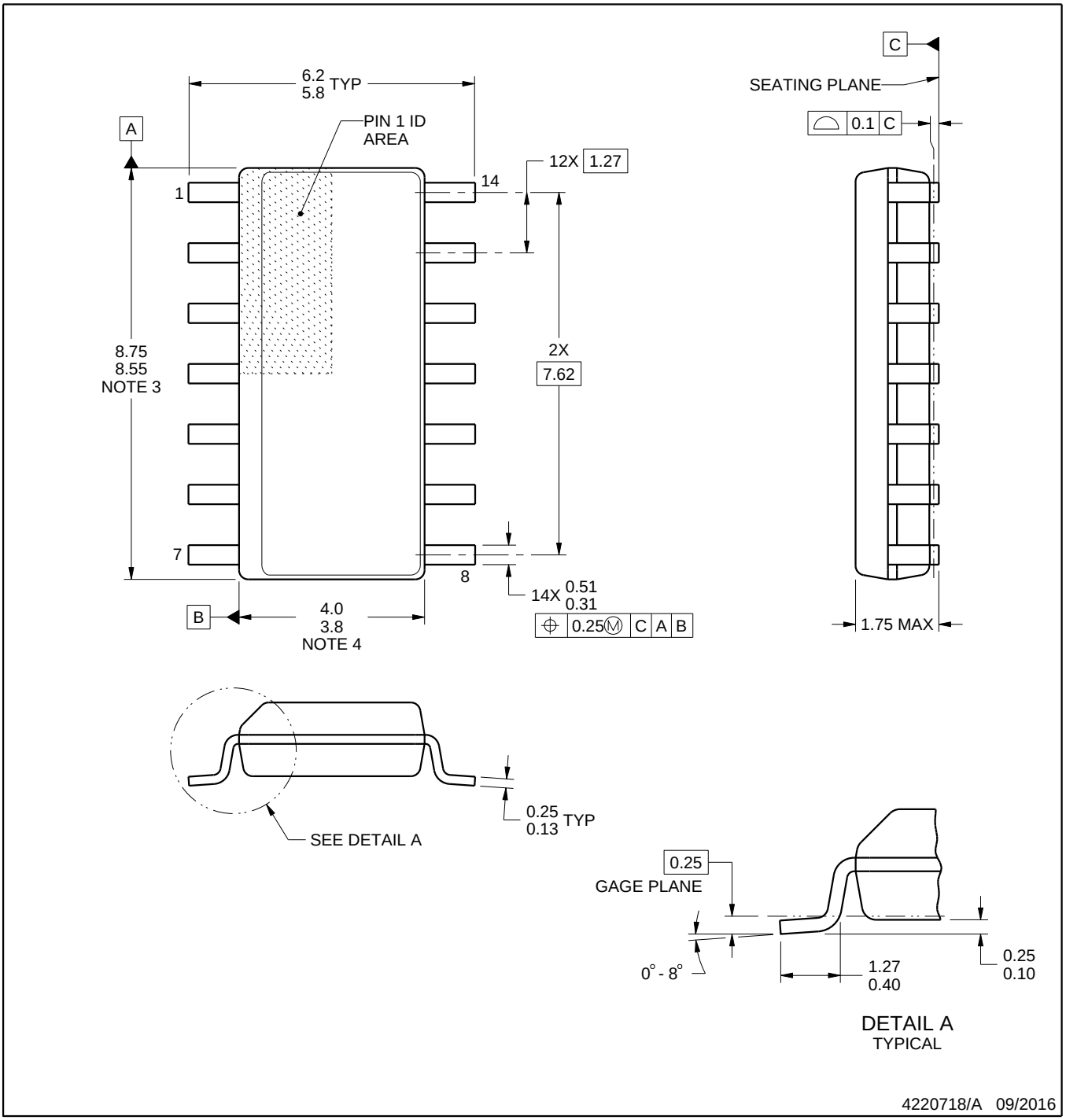


PACKAGE OUTLINE

D0014A

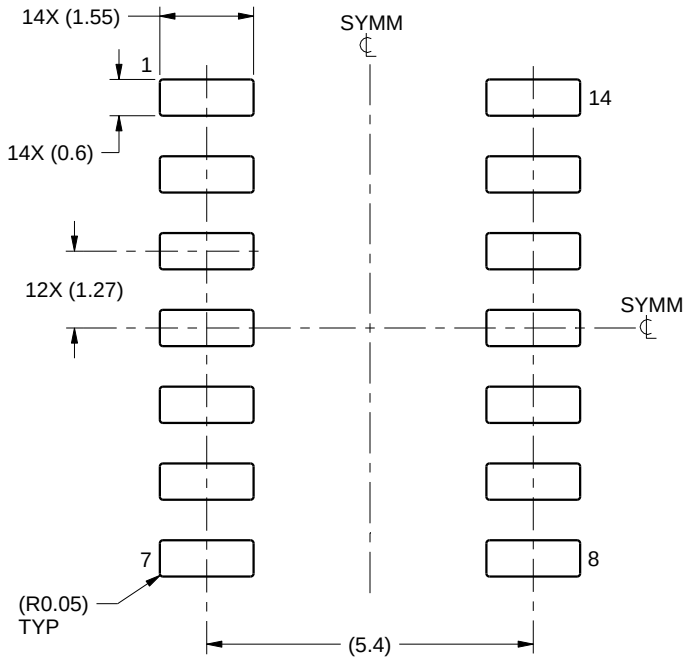
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

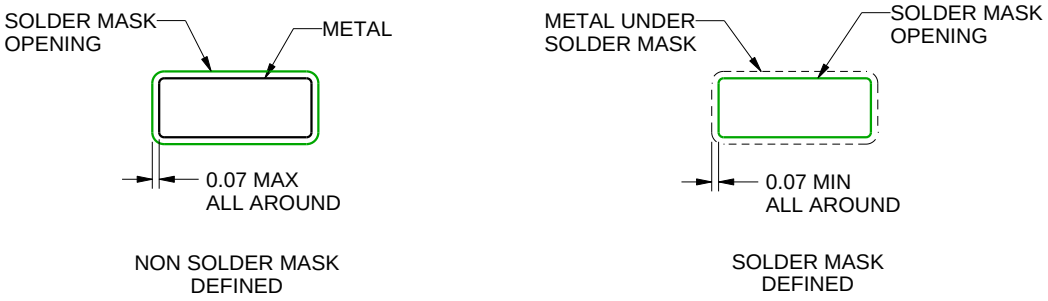


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

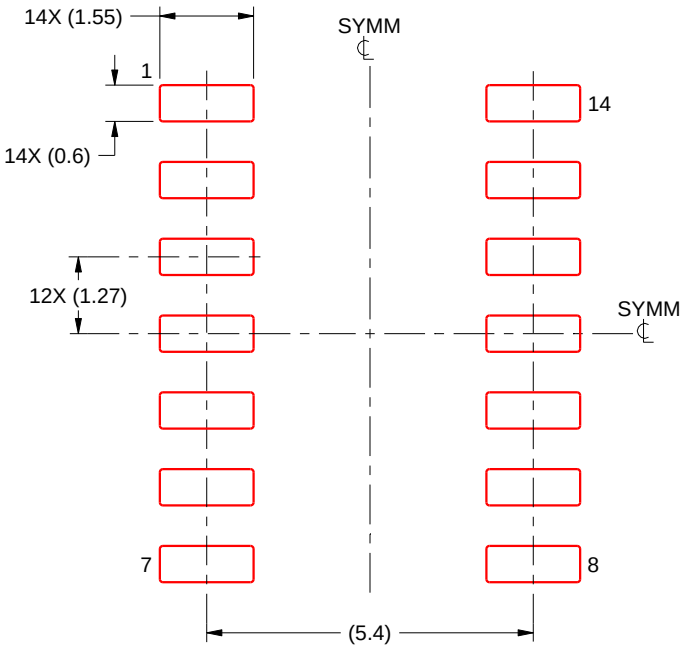
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

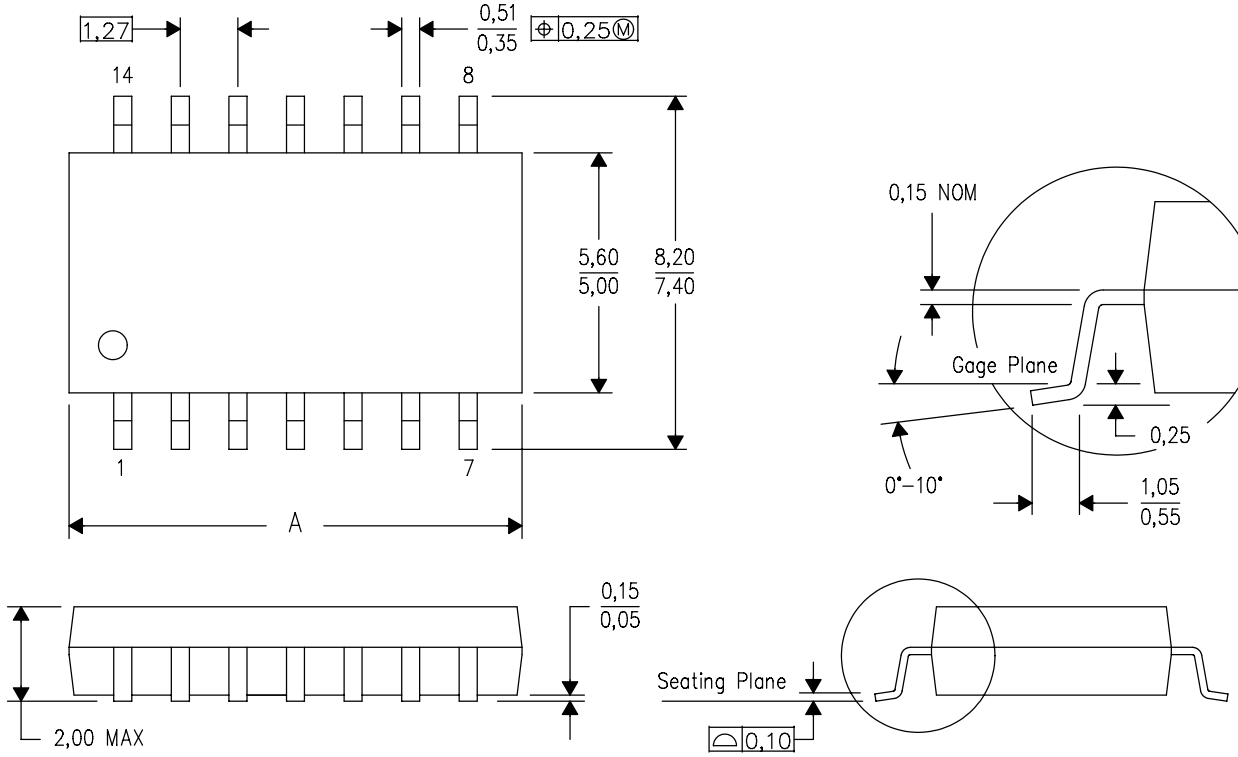
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

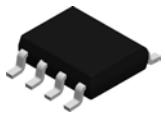
14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

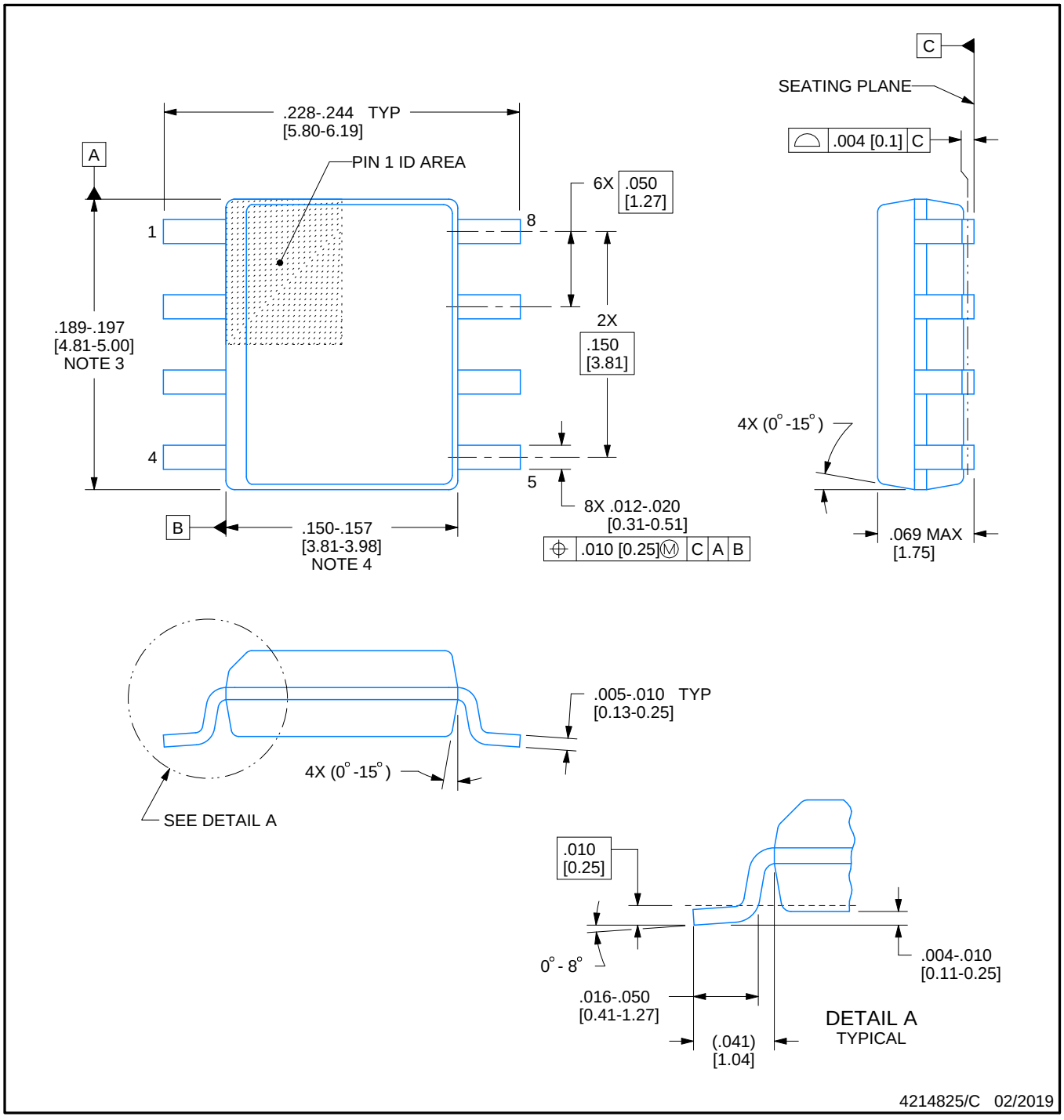


PACKAGE OUTLINE

D0008A

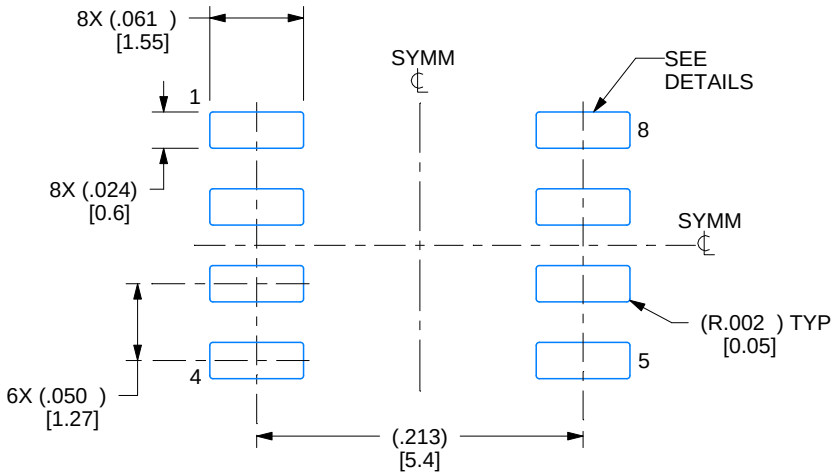
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

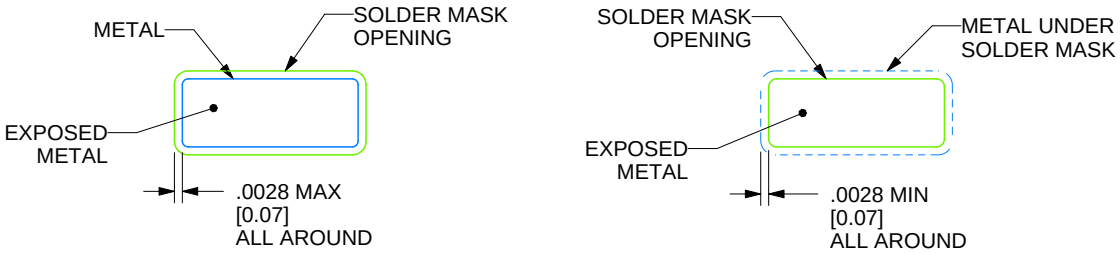


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

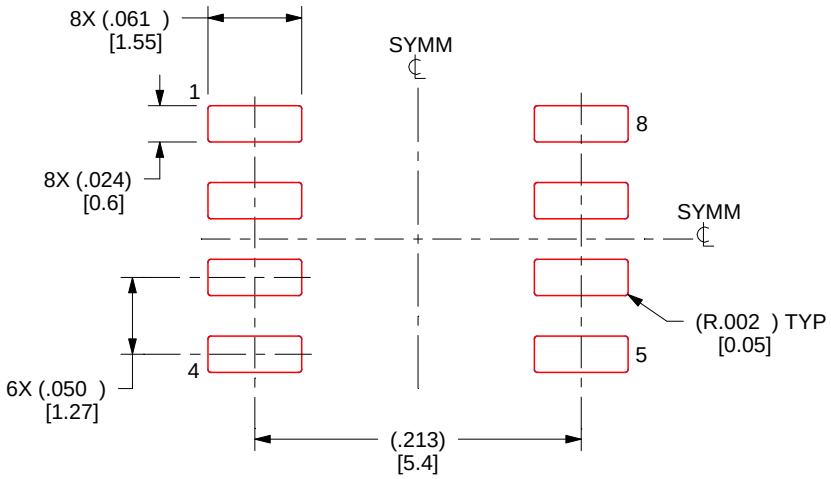
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

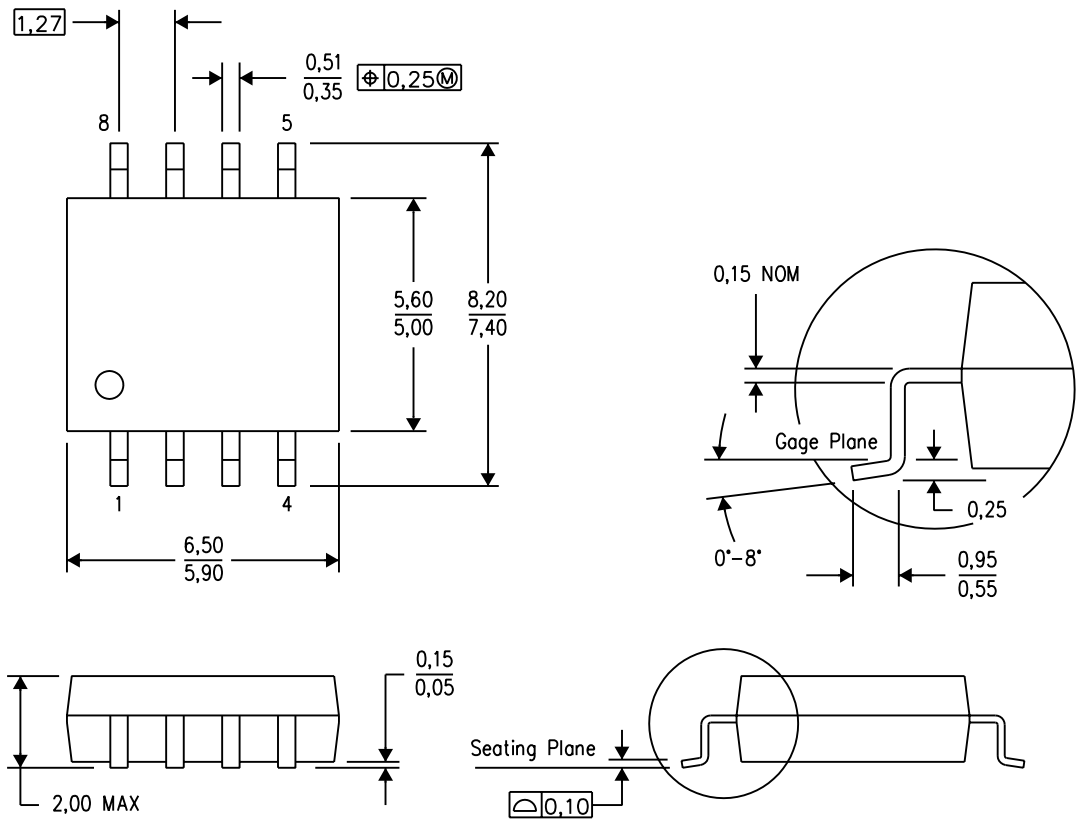
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

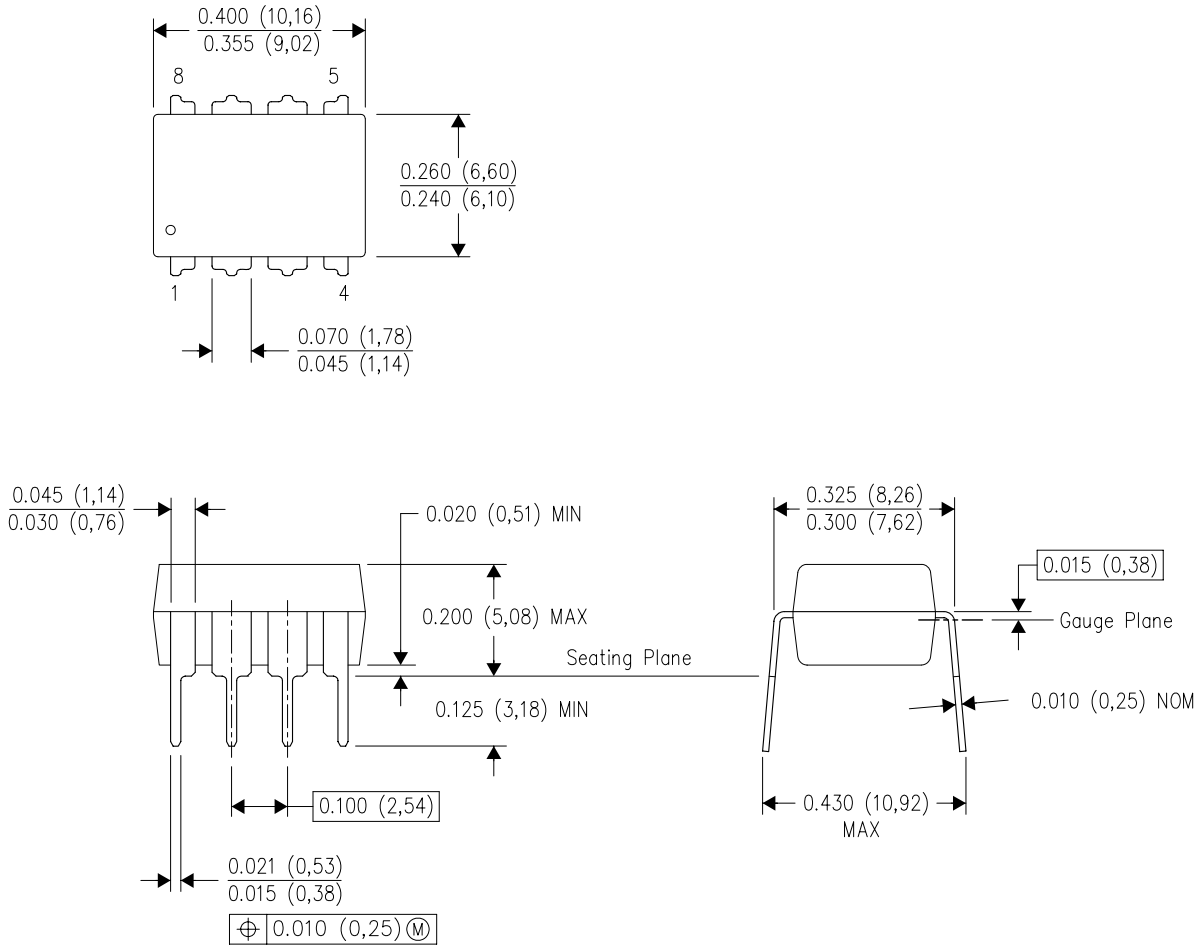
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

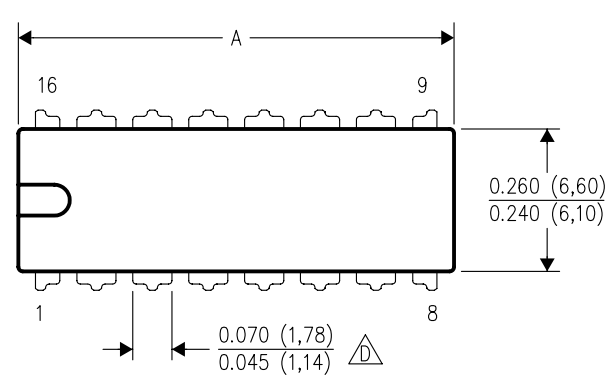


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

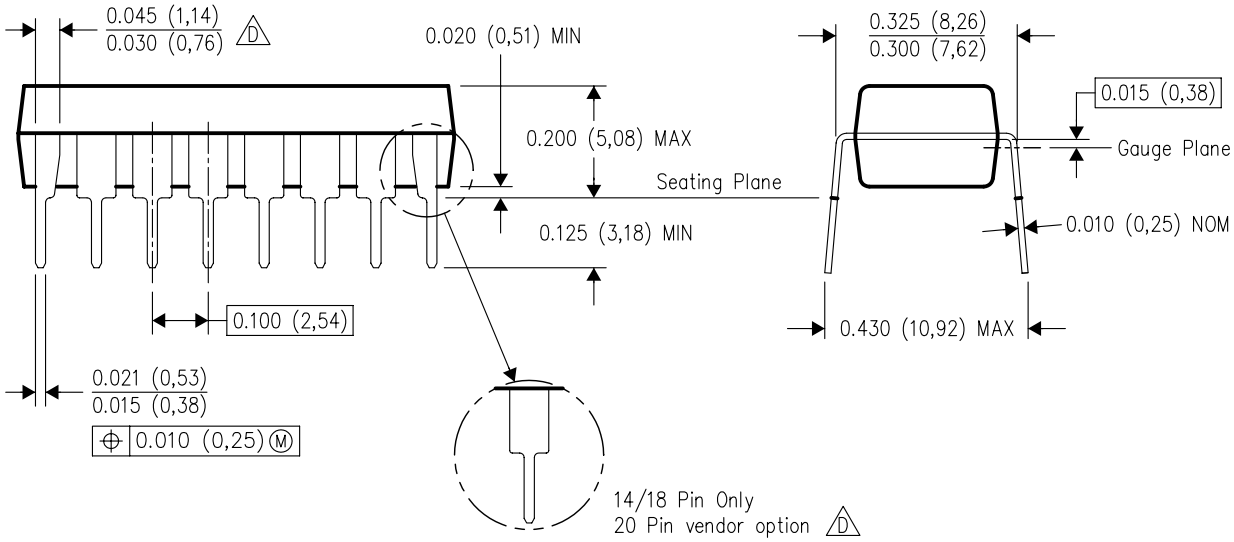
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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