THVD1520 10 Mbps RS-485 Transceiver With ±8-kV IEC ESD Protection

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- 4.5-V to 5.5-V supply voltage
- 10 Mbps, Half-Duplex RS-422/RS-485
- Bus I/O protection
  - ± 16-kV HBM ESD
  - ± 8-kV IEC 61000-4-2 contact discharge
  - ± 8-kV IEC 61000-4-2 air gap discharge
  - ± 4-kV IEC 61000-4-4 fast transient burst
- Extended industrial temperature range: -40°C to 125°C
- Large receiver hysteresis for noise rejection
- Low power consumption
  - Low standby supply current: < 1 µA
  - Quiescent during operation: < 840 µA
- Glitch-free power-up/down for hot plug-in capability
- Open, short and idle bus failsafe
- 1/8 unit load (up to 256 bus nodes)

2 Applications

- Factory Automation & Control
- Building Automation
- HVAC Systems
- Video Surveillance
- Smart Meters

3 Description

THVD1520 is a robust half-duplex RS-485 transceiver for industrial applications. The bus pins are immune to high levels of IEC contact discharge ESD events eliminating the need of additional system-level protection components.

The device operates from a single 5-V supply. The wide common-mode voltage range and low input leakage on bus pins make THVD1520 suitable for multi-point applications over long cable runs.

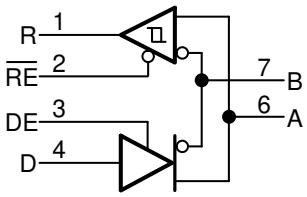
THVD1520 is available in industry standard 8-pin SOIC package for drop-in compatibility. The device is characterized for ambient temperatures from –40°C to 125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THVD1520	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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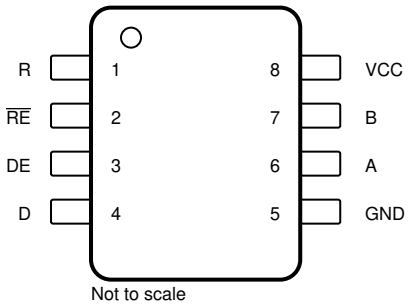
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2019	*	Initial release.

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low (internal 5-MΩ pull-up)
DE	3	Digital input	Driver enable, active high (internal 5-MΩ pull-down)
D	4	Digital input	Driver data input (internal 5-MΩ pull-up)
GND	5	Ground	Device ground
A	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	Bus input/output	Bus I/O port, B (complementary to A)
V_{CC}	8	Power	5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_L	Input voltage at any logic pin (D, DE or $\overline{RE}$)	–0.3	5.7	V
V_A, V_B	Voltage at A or B inputs, as differential or common-mode with respect to GND	–18	18	V
I_O	Receiver output current	–24	24	mA
T_J	Junction temperature		170	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals and GND	±16,000	V
			All other pins	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings [IEC]

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND	±8,000	V
		IEC 61000-4-2 ESD (Air-Gap Discharge), bus terminals and GND	±8,000	
		IEC 61000-4-4 EFT (Fast transient or burst), bus terminals and GND	±4,000	

6.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{ID}	Differential input voltage		–12		12	V
V_I	Input voltage at any bus terminal (1)		–7		12	V
V_{IH}	High-level input voltage (driver, driver-enable, and receiver-enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver-enable, and receiver-enable inputs)		0		0.8	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate				10	Mbps
T_J	Junction temperature		–40		150	°C
T_A (2)	Operating ambient temperature		–40		125	°C

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures upto 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shutdown (TSD) circuit which disables the device when the junction temperature reaches 170°C.

6.5 Thermal Information

THERMAL METRIC (1)		THVD1520 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\lvert V_{OD} \rvert$	Driver differential-output voltage magnitude	V_{test} from –7 to +12 V	See Figure 7	1.5	2.5		V
		R_L = 54 Ω (RS-485), C_L = 50 pF	See Figure 8	1.5	2.5		
		R_L = 100 Ω (RS-422), C_L = 50 pF		2	3		
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of driver differential-output voltage	R_L = 54 Ω or 100 Ω, C_L = 50 pF	See Figure 8	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω, C_L = 50 pF	See Figure 8	1	V_{CC} / 2	3	V
ΔV_{OC}	Change in differential driver common-mode output voltage			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				220		mV
$\lvert I_{OS} \rvert$	Driver short-circuit output current	DE = V_{CC}, -7 V ≤ [V_A or V_B] ≤ 12 V, or A pin shorted to B pin				150	mA
C_{OD}	Differential output capacitance				8		pF
Receiver							
I_I	Bus input current (driver disabled)	DE = 0 V, V_{CC} = 0 V or 5.5 V	V_I = 12 V		75	110	µA
			V_I = –7 V	–90	–70		
R_A, R_B	Bus input impedance	V_A = -7 V, V_B = 12 V and V_A = 12 V, V_B = -7 V	See Figure 12	96			kΩ
V_{IT+}	Positive-going receiver differential-input voltage threshold				–90	–50	mV
$V_{IT–}$	Negative-going receiver differential-input voltage threshold			–200	–150		mV
V_{HYS} (1)	Receiver differential-input voltage threshold hysteresis (V_{IT+} – $V_{IT–}$)			40	60		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_{OZ}	Receiver high-impedance output current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}		–1		1	µA
I_{OSR}	Receiver output short-circuit current	$\overline{RE}$ = 0, DE = 0	See Figure 13			95	mA
Logic							
I_{IN}	Input current (D, DE, $\overline{RE}$)			–2.5		2.5	µA
Supply							
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, $\overline{RE}$ = 0, no load		600	840	µA
		Driver enabled, receiver disabled	DE = V_{CC}, $\overline{RE}$ = V_{CC}, no load		440	580	
		Driver disabled, receiver enabled	DE = 0, $\overline{RE}$ = 0, no load		530	680	
		Driver and receiver disabled	DE = 0, $\overline{RE}$ = V_{CC}, no load		0.1	1	

(1) Under any specific conditions, V_{IT+} is specified to be at least V_{HYS} higher than $V_{IT–}$.

6.7 Power Dissipation Characteristics

PARAMETER			TEST CONDITIONS	VALUE	UNIT
PD	Power dissipation, driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125°C, 50% duty cycle square-wave signal at maximum signaling rate	Unterminated	R_L = 300 Ω, C_L = 50 pF	100	mW
		RS-422 load	R_L = 100 Ω, C_L = 50 pF	135	
		RS-485 load	R_L = 54 Ω, C_L = 50 pF	190	

6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Driver differential output rise and fall times		See Figure 9	10	17	30	ns
t_{PHL}, t_{PLH}	Driver propagation delay		See Figure 9		20	35	ns
$t_{SK(P)}$	Driver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$		See Figure 9		0.8	4	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 10 and Figure 11		25	100	ns
t_{PHZ}, t_{PLZ}	Driver enable time	Receiver enabled	See Figure 10 and Figure 11		25	100	ns
		Receiver disabled	See Figure 10 and Figure 11		1.5	3	µs
Receiver							
t_r, t_f	Receiver output rise and fall times		See Figure 14		5	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time		See Figure 14		50	95	ns
$t_{SK(P)}$	Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$		See Figure 14		3	15	ns
t_{PHZ}, t_{PLZ}	Receiver disable time		See Figure 15		15	30	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 15		25	170	ns
		Driver disabled	See Figure 16		1	5	µs

6.9 Typical Characteristics

V_{CC} = 5 V, T_A = 25^{0}C (unless otherwise noted)

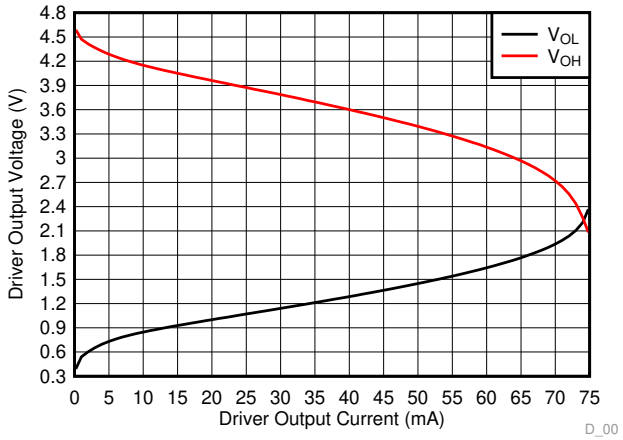


Figure 1. Driver Output Voltage vs Driver Output Current

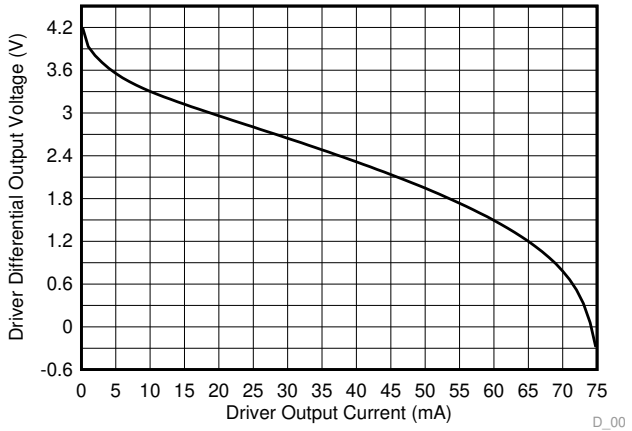


Figure 2. Driver Differential Output Voltage vs Driver Output Current

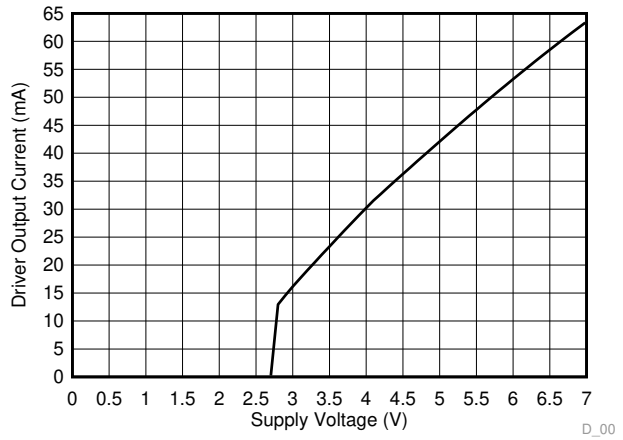


Figure 3. Driver Output Current vs Supply Voltage

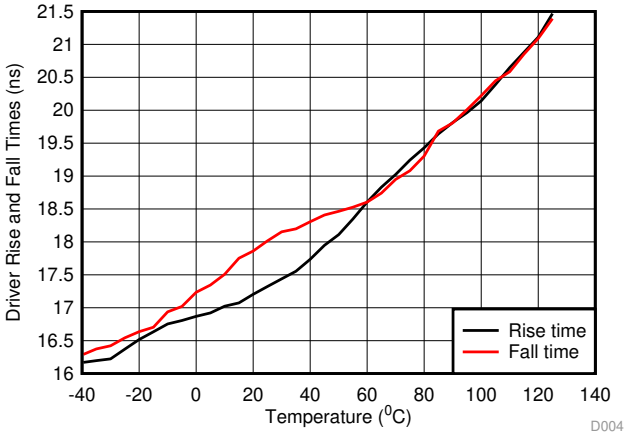


Figure 4. Driver Rise or Fall Time vs Temperature

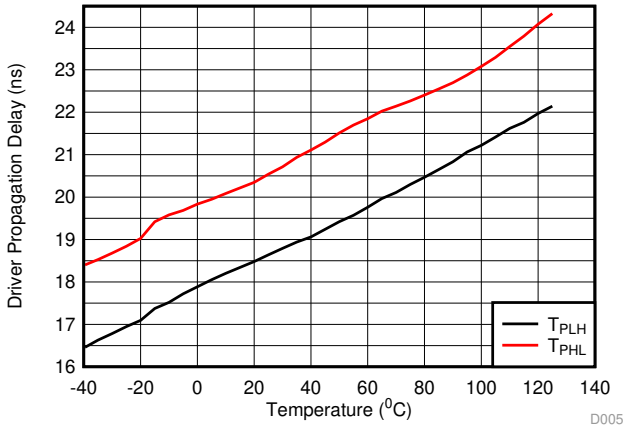
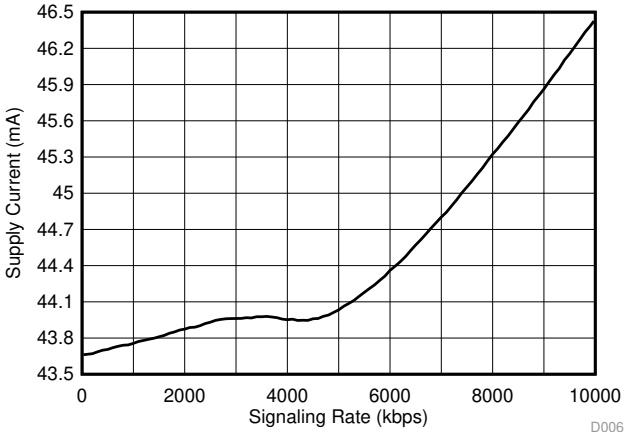


Figure 5. Driver Propagation Delay vs Temperature



50% duty cycle square-wave | R_L = 54 Ω | C_L = 50 pF | DE = V_{CC}, $\overline{RE}$ = GND

Figure 6. Supply Current vs Signaling Rate

7 Parameter Measurement Information

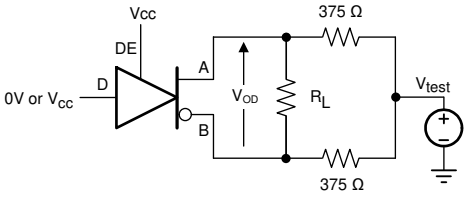


Figure 7. Measurement of Driver Differential Output Voltage With Common-Mode Load

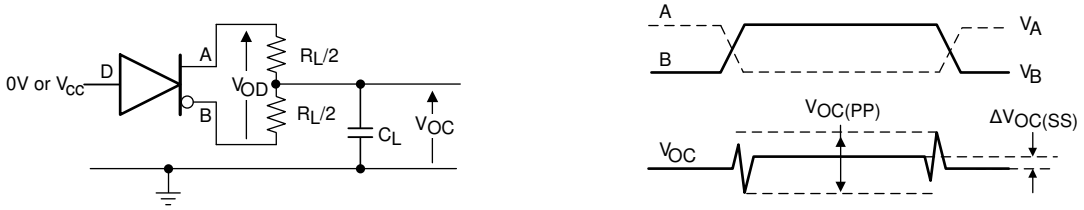


Figure 8. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

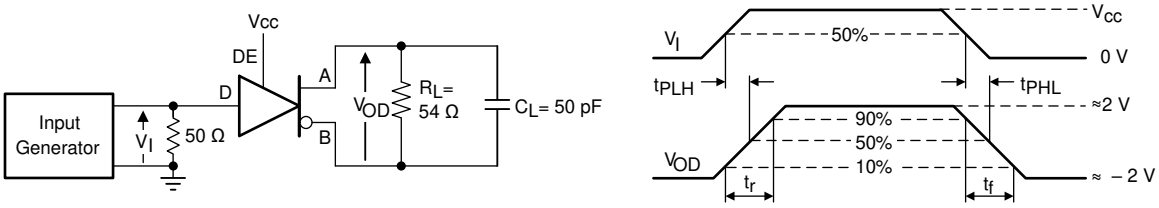


Figure 9. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

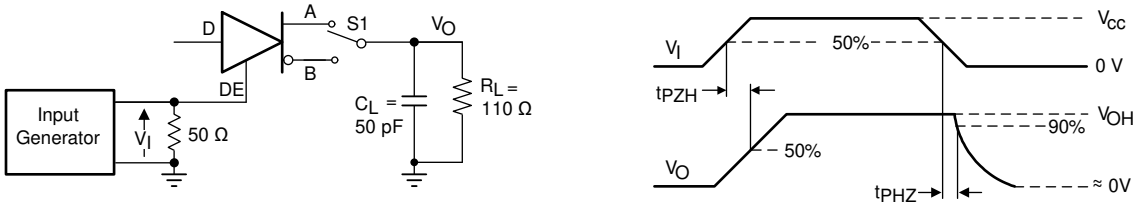


Figure 10. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

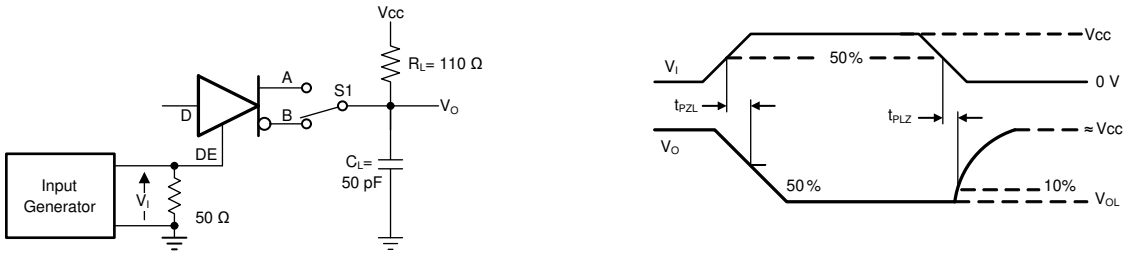


Figure 11. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

Parameter Measurement Information (continued)

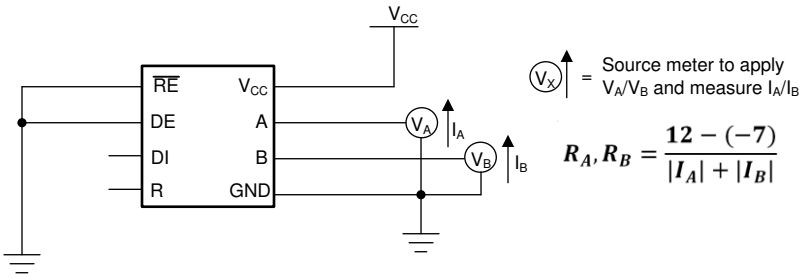


Figure 12. Measurement of Bus Impedance

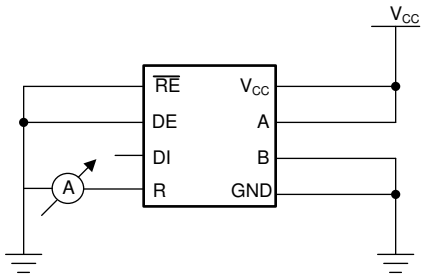


Figure 13. Measurement of Receiver Output Short Circuit Current

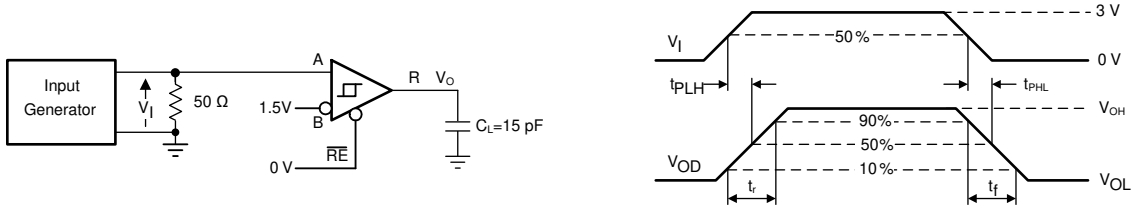


Figure 14. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

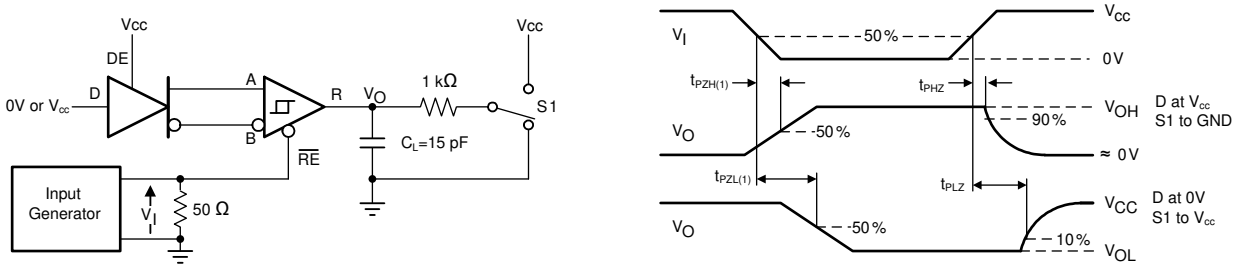


Figure 15. Measurement of Receiver Enable/Disable Times With Driver Enabled

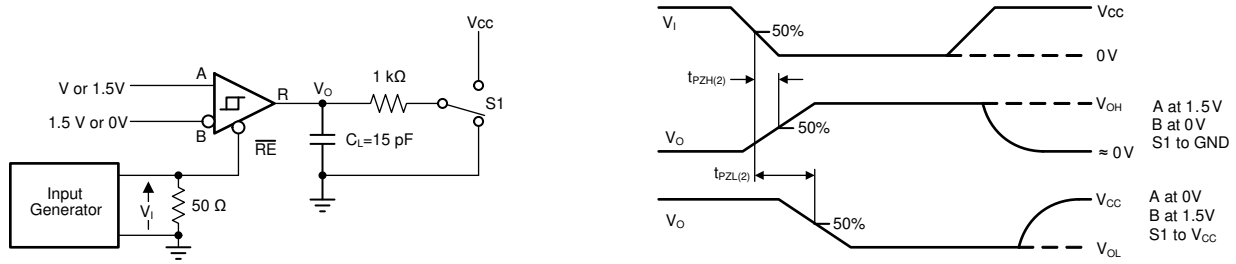


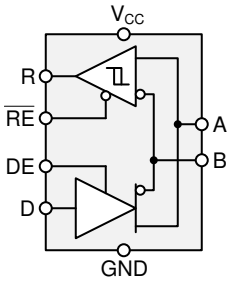
Figure 16. Measurement of Receiver Enable Times With Driver Disabled

8 Detailed Description

8.1 Overview

The THVD1520 is a low-power, half-duplex RS-485 transceiver suitable for data transmission up to 10 Mbps.

8.2 Functional Block Diagrams



8.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ±8 kV (contact discharge), ±8 kV (air gap discharge) and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The THVD1520 is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

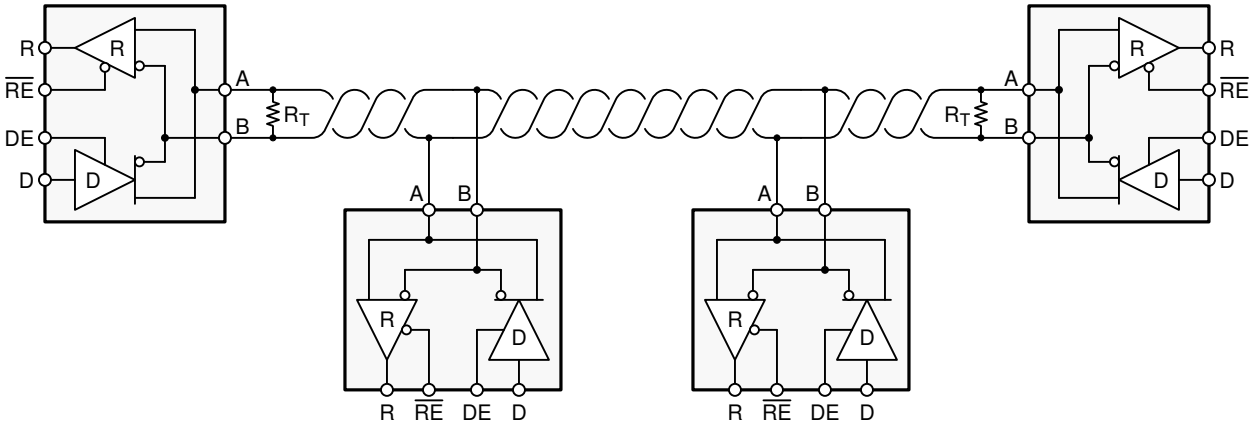


Figure 17. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

Typical Application (continued)

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD1520 consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

9.2.1.4 Receiver Failsafe

The differential receivers of the THVD1520 are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+}, $V_{IT–}$, and V_{HYS} (the separation between V_{IT+} and $V_{IT–}$). As shown in the table, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output will be high. Only when the differential input is more than V_{HYS} below V_{IT+} will the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{IT+}.

Typical Application (continued)

9.2.1.5 Transient Protection

The bus pins of the THVD1520 transceiver family include on-chip ESD protection against ±16-kV HBM and ±8-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.

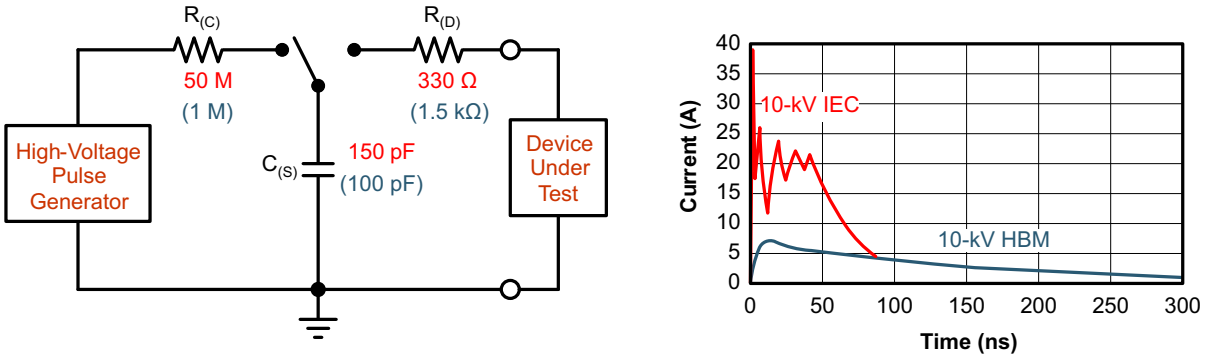


Figure 18. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 19 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

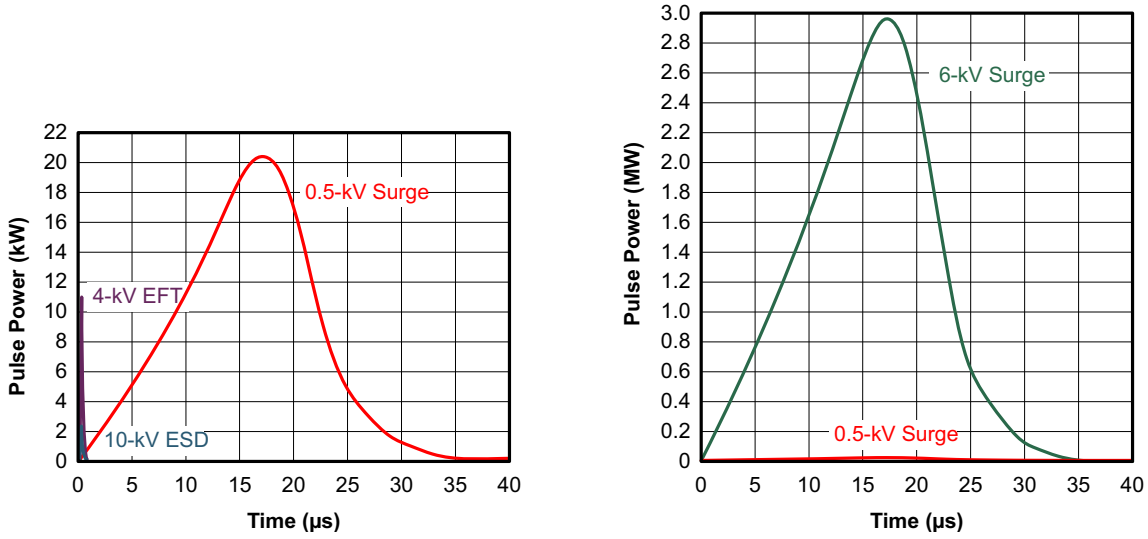


Figure 19. Power Comparison of ESD, EFT, and Surge Transients

Typical Application (continued)

In the event of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. Figure 20 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

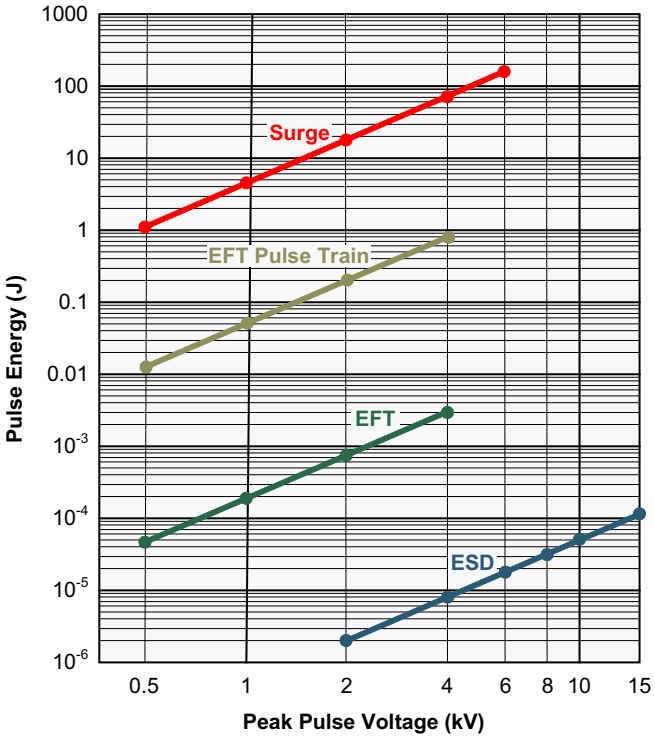


Figure 20. Comparison of Transient Energies

Typical Application (continued)

9.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary. Figure 21 suggests a protection circuit against 1 kV surge (IEC 61000-4-5) transients. Table 3 shows the associated bill of materials.

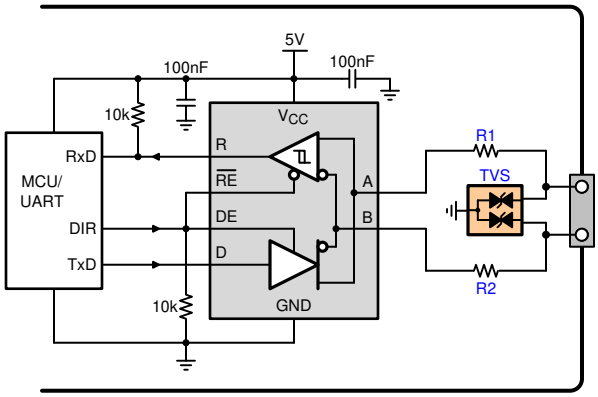


Figure 21. Transient Protection Against Surge Transients for Half-Duplex Devices

Table 3. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 transceiver	THVD1520	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

9.2.3 Application Curves

Figure 22. Waveforms at 10 Mbps Operation, PRBS7 Data Pattern

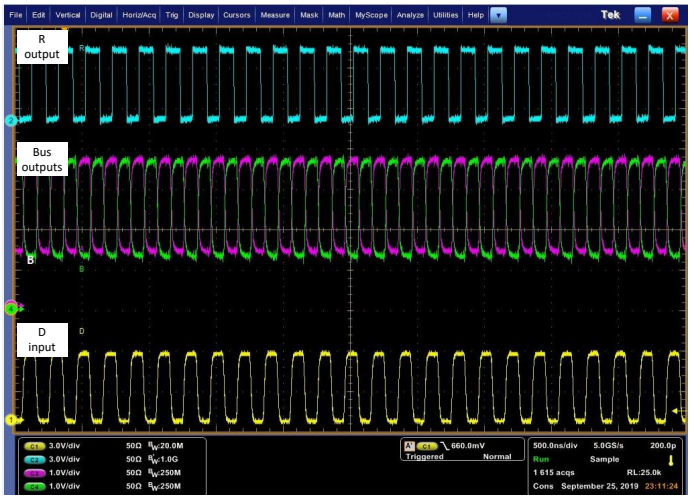


Figure 23. Waveforms at 10 Mbps Operation, Clock Data Pattern

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable lines to limit noise currents in theses lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

11.2 Layout Example

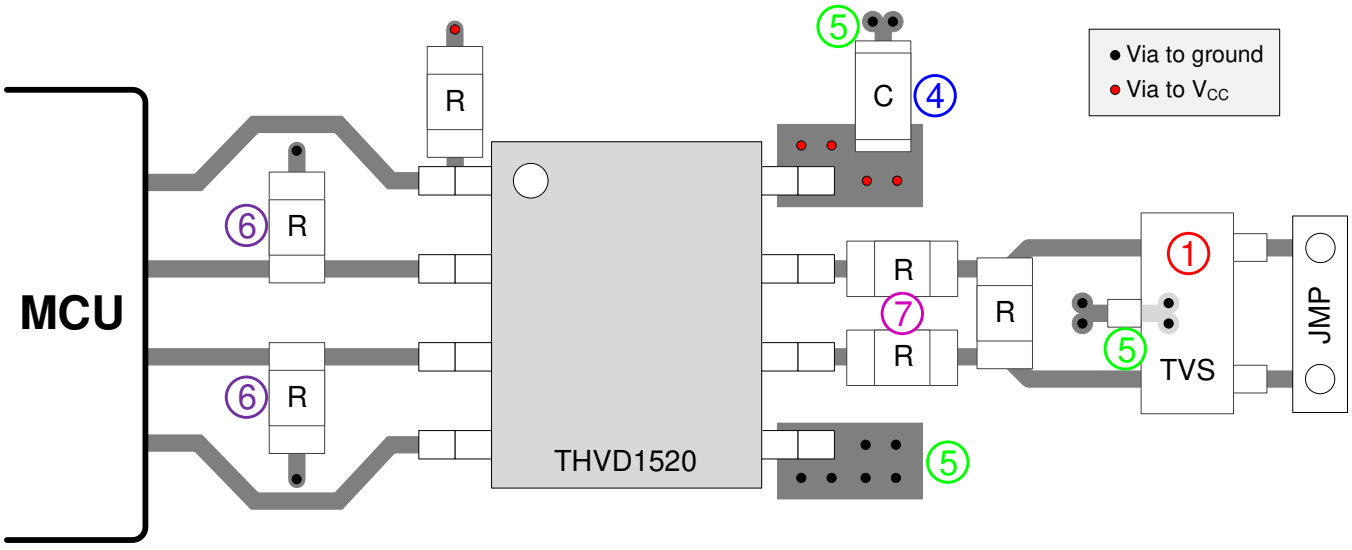


Figure 24. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.2 Third-Party Products Disclaimer

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12.3 Receiving Notification of Documentation Updates

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12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1520DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1520
THVD1520DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1520
THVD1520DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1520
THVD1520DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1520

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

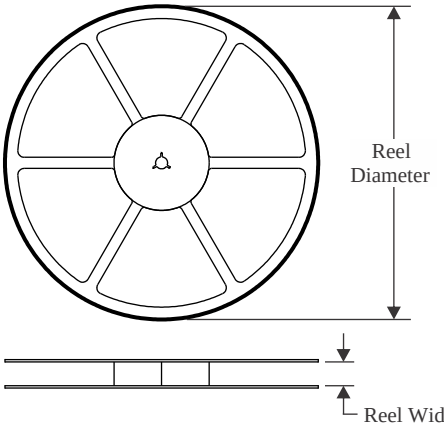
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

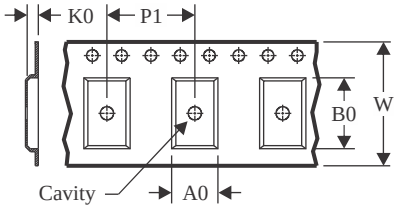
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

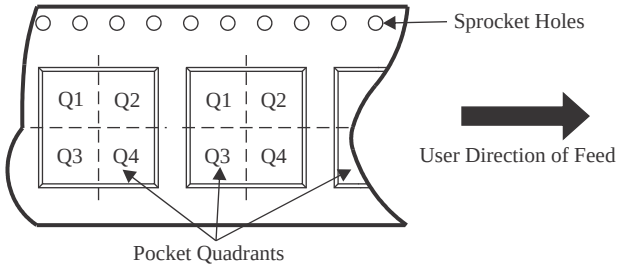


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

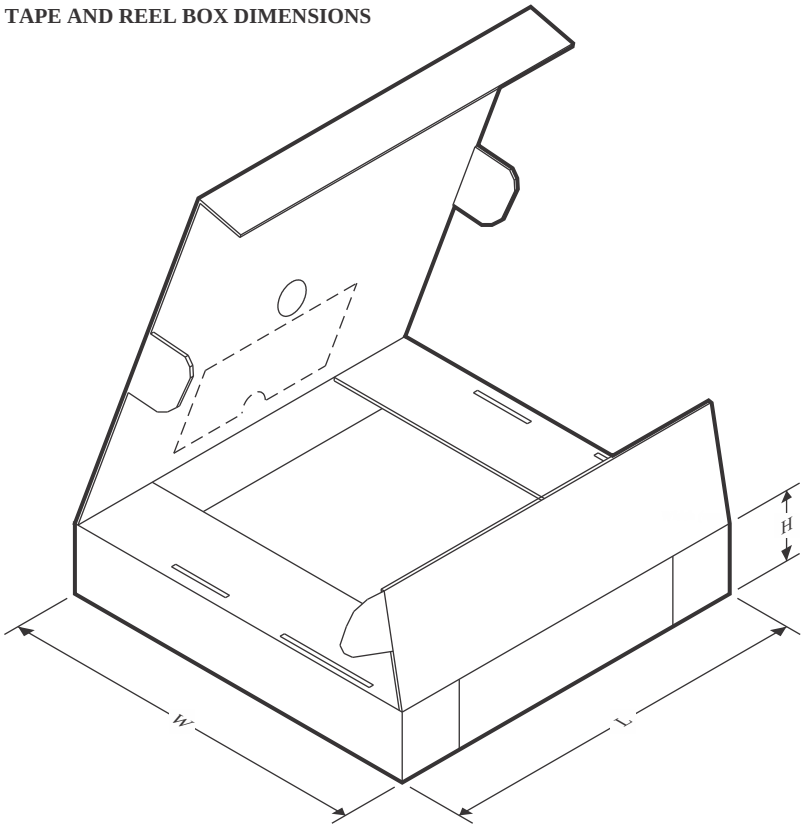
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

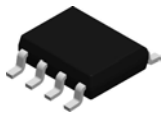
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1520DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1520DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1520DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1520DRG4	SOIC	D	8	2500	353.0	353.0	32.0

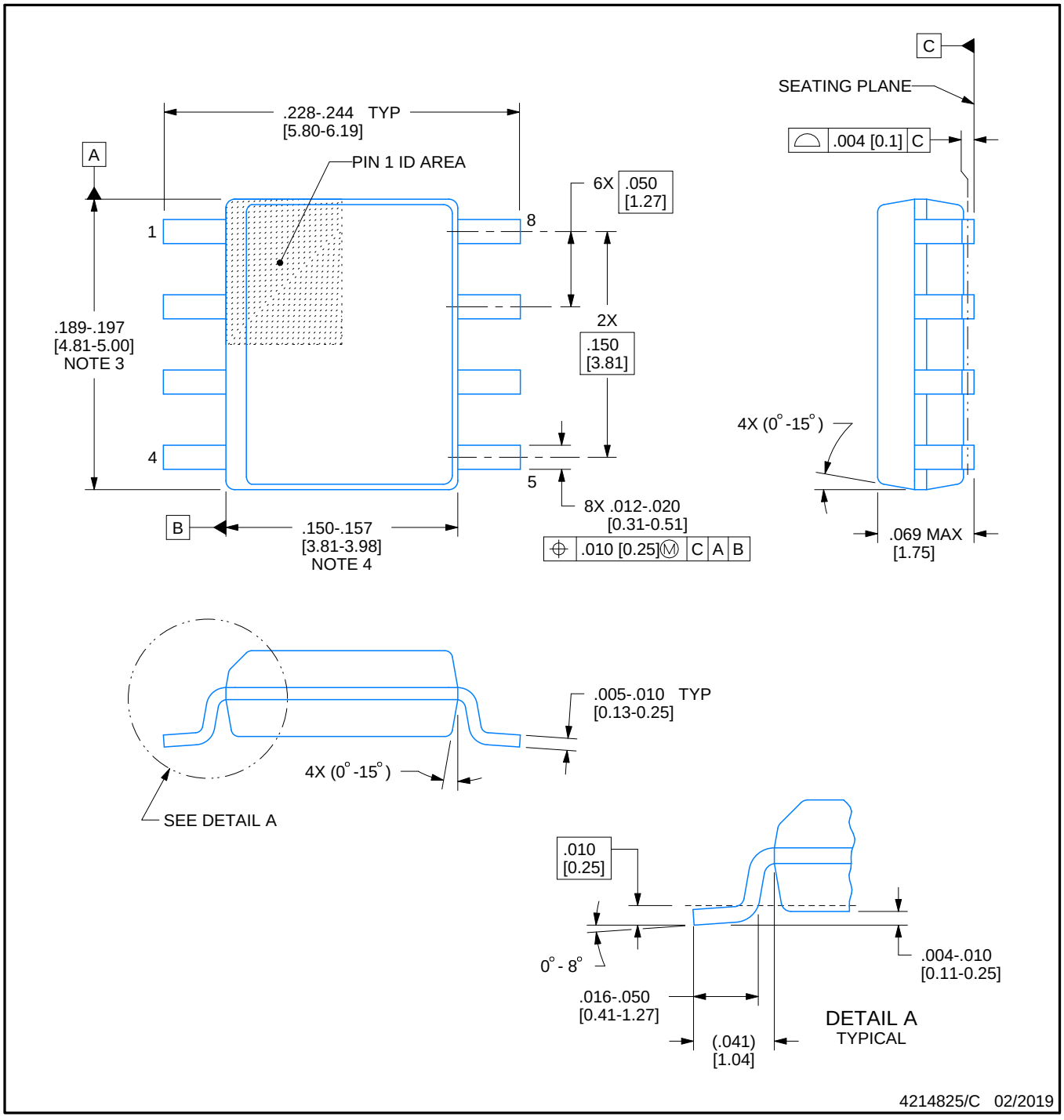


PACKAGE OUTLINE

D0008A

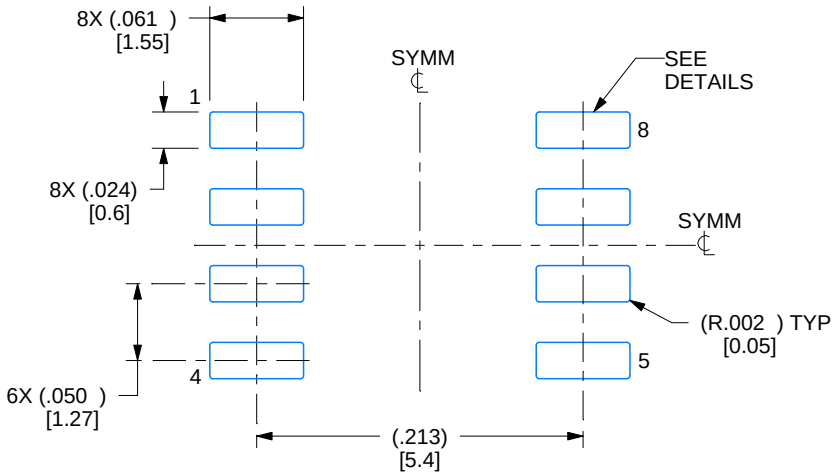
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

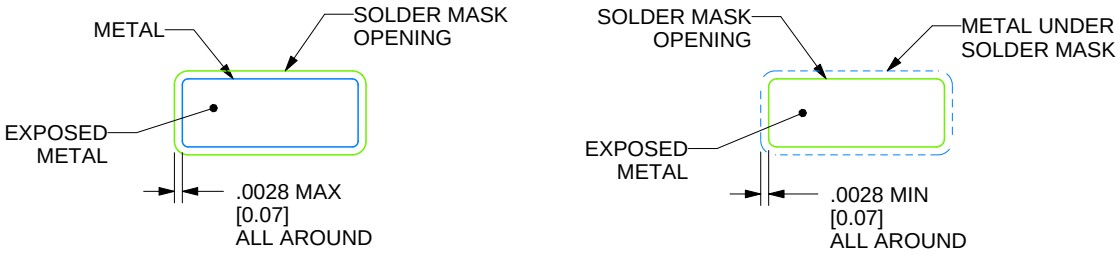


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

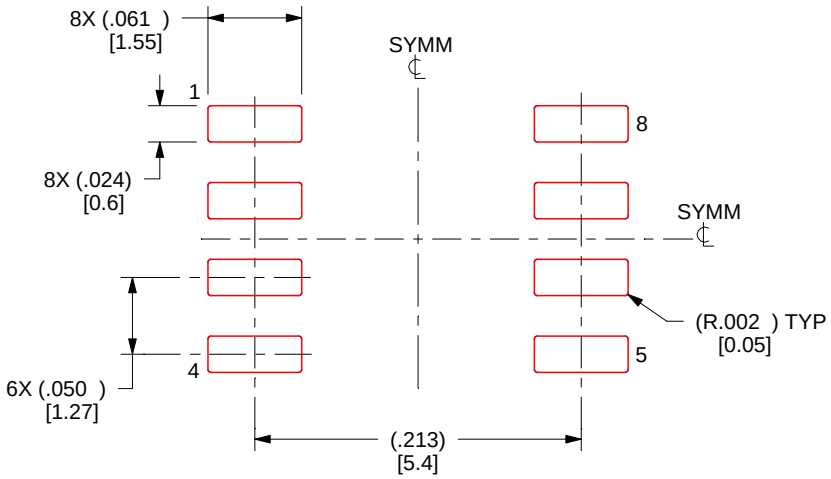
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025