OPAx182 36-V, 5-MHz, Low-Noise, Zero-Drift, MUX-Friendly, Precision Op Amps

1 Features

- Ultra-high precision:
  - Zero-drift: 0.003 µV/°C
  - Ultra-low offset voltage: 4 µV (maximum)
- Excellent dc precision:
  - CMRR: 168 dB
  - Open-loop gain: 170 dB
- Low noise:
  - e_n at 1 kHz: 5.7 nV/√Hz
  - 0.1-Hz to 10-Hz noise: 0.12 μV_{PP}
- Excellent dynamic performance:
  - Gain bandwidth: 5 MHz
  - Slew rate: 10 V/µs
  - Fast settling: 10-V step, 0.01% in 1.7 µs
- Robust design:
  - MUX-friendly inputs
  - RFI and EMI filtered inputs
- Wide supply: ±2.25 V to ±18 V, 4.5 V to 36 V
- Quiescent current: 0.85 mA
- Rail-to-rail output
- Input includes negative rail

2 Applications

- Battery test
- DC power supply, ac source, electronic load
- Data acquisition (DAQ)
- Semiconductor test
- Weigh scale
- Analog input module
- Flow transmitter

3 Description

The OPA182, OPA2182, and OPA4182 (OPAx182) are ultra-low noise, fast-settling, zero-drift, high-precision operational amplifiers, These devices provide rail-to-rail output operation and feature a unique MUX-friendly architecture and controlled start-up system. These devices also feature excellent ac performance combined with only 0.45 µV of offset voltage and 0.003 µV/°C of drift over temperature. All these features make the OPAx182 a great choice for data acquisition, battery test, analog input modules, weigh scales, and any other systems requiring high dc precision and low noise.

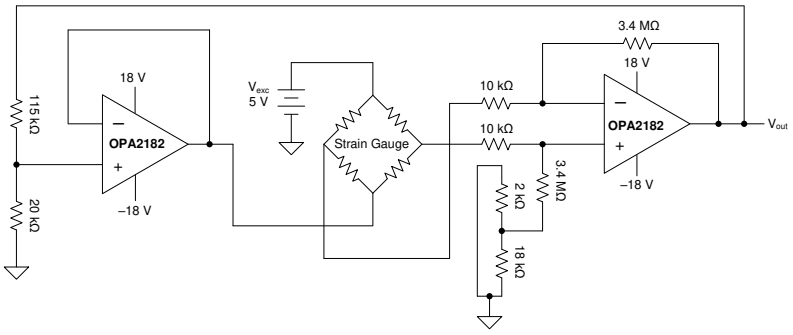
The MUX-friendly input architecture prevents inrush current when applying large input differential voltages and improves settling performance in multichannel systems. Moreover, the controlled start-up system rejects any inrush current when ramping up the supply rails, all while providing robust ESD protection during shipment, handling, and assembly.

The device is specified from –40°C to +125°C.

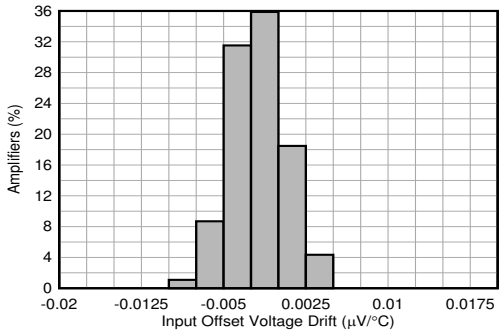
Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
OPA182	D (SOIC, 8)	4.90 mm x 3.90 mm
	DBV (SOT-23, 5)	2.90 mm x 1.60 mm
OPA2182	D (SOIC, 8)	4.90 mm x 3.90 mm
	DGK (VSSOP, 8)	3.00 mm x 3.00 mm
OPA4182	D (SOIC, 14)	8.65 mm x 3.91 mm
	PW (TSSOP, 14) Preview	5.00 mm x 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



OPA2182 Bridge Sensor Application



OPAx182 Offset Drift

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2021) to Revision E (August 2022)	Page
• Changed OPA182 DBV (SOT-23) package from preview to active and added associated content	1

Changes from Revision C (January 2021) to Revision D (December 2021)	Page
• Added OPA182 and OPA4182 production data (active) devices and associated content	1

Changes from Revision B (July 2020) to Revision C (January 2021)	Page
• Changed VSSOP-8 (DGK) package from preview to production data (active)	1

Changes from Revision A (May 2020) to Revision B (July 2020)	Page
• Added VSSOP-8 (DGK) preview package and associated content to data sheet	1
• Changed capacitive load drive specification from "TBD" to "See Typical Characteristics"	8

Changes from Revision * (December 2019) to Revision A (May 2020)	Page
• Changed device status from advanced information (preview) to production data (active)	1

5 Device Comparison Table

PRODUCT	FEATURES
OPA2189	0.4-µV offset, 0.005-µV/°C drift, 5.2-nV/√Hz, rail-to-rail output, 36-V, zero-drift, MUX-friendly CMOS
OPA2188	6-µV offset, 0.03-µV/°C drift, 8.8-nV/√Hz, rail-to-rail output, 36-V, zero-drift, MUX-friendly CMOS
OPA2187	1-µV offset, 0.001-µV/°C drift, 100-µA quiescent current, rail-to-rail output, 36-V, zero-drift CMOS
OPA2388	0.25-µV offset, 0.005-µV/°C drift, 7-nV/√Hz, 10-MHz, *true* rail-to-rail input/output, 5.5-V, zero-drift, zero-crossover CMOS
OPA2180	120-µV, 10-MHz, 5.1-nV/√Hz, 36-V JFET input industrial op amp

6 Pin Configuration and Functions

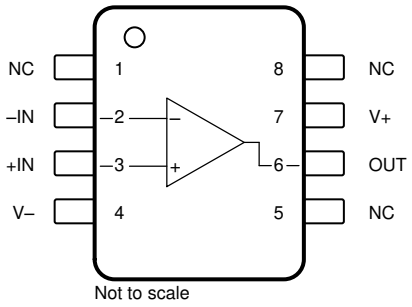


Figure 6-1. OPA182 D (8-Pin SOIC) Package, Top View

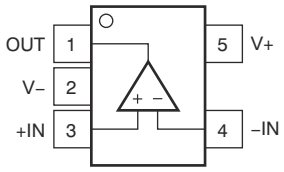


Figure 6-2. OPA182 DBV (5-Pin SOT-23) Package, Top View

Table 6-1. Pin Functions: OPA182

PIN			TYPE	DESCRIPTION
NAME	D (SOIC)	DBV (SOT-23)		
–IN	2	4	Input	Inverting input
+IN	3	3	Input	Noninverting input
NC	1, 5, 8	—	—	No internal connection; can be left floating.
OUT	6	1	Output	Output channel
V–	4	2	Power	Negative supply
V+	7	5	Power	Positive supply

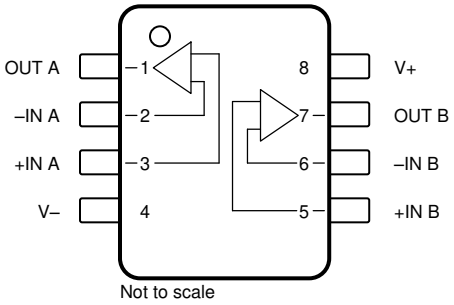


Figure 6-3. D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

Table 6-2. Pin Functions: OPA2182

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
+IN A	3	Input	Noninverting input channel A
–IN B	6	Input	Inverting input channel B
+IN B	5	Input	Noninverting input channel B
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
V–	4	Power	Negative supply
V+	8	Power	Positive supply

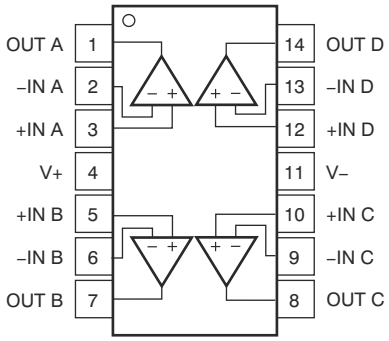


Figure 6-4. D (14-Pin SOIC) and PW (14-Pin TSSOP, Preview) Packages, Top View

Table 6-3. Pin Functions: OPA4182

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
+IN A	3	Input	Noninverting input channel A
–IN B	6	Input	Inverting input channel B
+IN B	5	Input	Noninverting input channel B
–IN C	9	Input	Inverting input channel C
+IN C	10	Input	Noninverting input channel C
–IN D	13	Input	Inverting input channel D
+IN D	12	Input	Noninverting input channel D
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
OUT C	8	Output	Output channel C
OUT D	14	Output	Output channel D
V–	11	Power	Negative supply
V+	4	Power	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Single-supply, V_S = (V+)		40	V
		Dual-supply, V_S = (V+) – (V–)		±20	
	Signal input voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
	Output short circuit(2)		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply, V_S = (V+)	4.5		36	V
		Dual-supply, V_S = (V+) – (V–)	±2.25		±18	
T_A	Operating temperature		–40		125	°C

7.4 Thermal Information: OPA182

THERMAL METRIC[1]		OPA182		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.9	138.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.8	63.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.2	35.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.1	17.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55.4	35.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2182

THERMAL METRIC[1]		OPA2182		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.1	150.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.8	43.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.3	71.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.2	2.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50.6	70.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA4182

THERMAL METRIC[1]		OPA4182	UNIT
		D (SOIC)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics,see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.45	±4	µV
		T_A = 0°C to 85°C				±4	
		T_A = –40°C to +125°C				±4	
dV_{OS}/dT	Input offset voltage drift	T_A = 0°C to 85°C	OPA182ID, OPA2182		±0.003	±0.012	µV/°C
			OPA182IDBV, OPA4182ID		±0.003	±0.020	
		T_A = –40°C to +125°C	OPA182ID, OPA2182		±0.003	±0.012	
			OPA182IDBV, OPA4182ID		±0.003	±0.020	
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C	OPA182		±0.005	±0.07	µV/V
			OPA2182, OPA4182ID		±0.005	±0.05	
INPUT BIAS CURRENT							
I_B	Input bias current	Z_{IN} = 100 kΩ || 500 pF			±50	±350	pA
			T_A = 0°C to 85°C			±1	nA
			T_A = –40°C to +125°C			±7	
I_{OS}	Input offset current	Z_{IN} = 100 kΩ || 500 pF			±140	±700	pA
			T_A = 0°C to 85°C			±2	nA
			T_A = –40°C to +125°C			±3	
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			18		nV_{RMS}
					0.119		$µV_{PP}$
e_n	Input voltage noise density	f = 10 Hz			5.7		nV/√Hz
		f = 100 Hz			5.7		
		f = 1 kHz			5.7		
		f = 10 kHz			5.7		
i_n	Input current noise density	f = 1 kHz			165		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) – 2.5	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V ≤ V_{CM} ≤ (V+) – 2.5 V	V_S = ±2.25 V	120	140		dB
			V_S = ±18 V, OPA182	141	168		
			V_S = ±18 V, OPA2182, OPA4182ID	143	168		
		(V–) – 0.1 V ≤ V_{CM} ≤ (V+) – 2.5 V, T_A = –40°C to +125°C	V_S = ±2.25 V	120			
			V_S = ±18 V, OPA182, OPA2182	140			
		(V–) ≤ V_{CM} ≤ (V+) – 2.5 V, T_A = –40°C to +125°C	V_S = ±18 V, OPA4182ID	130			

7.7 Electrical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT IMPEDANCE							
z_{id}	Differential input impedance				0.1 || 3.7		GΩ || pF
z_{ic}	Common-mode input impedance				60 || 2.3		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±18 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ	OPA182, OPA2182	150	170		dB
			OPA4182ID	145	170		
			T_A = –40°C to +125°C	146			
		V_S = ±18 V, (V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ	OPA182, OPA2182	150	170		
			OPA4182ID	145	170		
			T_A = –40°C to +125°C	140			
FREQUENCY RESPONSE							
UGB	Unity-gain bandwith	A_V = 1			3.6		MHz
GBW	Gain-bandwith product	A_V = 1000			5		MHz
SR	Slew rate	Gain = 1, 10-V step			10		V/µs
THD+N	Total harmonic distortion + noise	Gain = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00008%		
	Crosstalk	OPA2182	At dc		150		dB
			f = 10 kHz		120		
t_S	Settling time	To 0.1%	V_S = ±18 V, gain = 1, 10-V step		1.3		µs
		To 0.01%	V_S = ±18 V, gain = 1, 10-V step, falling		1.7		
			V_S = ±18 V, gain = 1, 10-V step, rising		3.4		
t_{OR}	Overload recovery time	V_{IN} × gain = V_S = ±18V			220		ns
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_{LOAD} = 10 kΩ		20	110	
			R_{LOAD} = 2 kΩ		80	500	
		Negative rail	No load		5	15	
			R_{LOAD} = 10 kΩ		20	110	
			R_{LOAD} = 2 kΩ		80	500	
		T_A = –40°C to +125°C, both rails			20	120	
I_{SC}	Short-circuit current				±65		mA
C_{LOAD}	Capacitive load drive				See Typical Characteristics		pF
Z_O	Open-loop output impedance	f = 1 MHz			320		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = ±2.25 V to ±18 V	T_A = 25°C		0.85	1	mA
			T_A = –40°C to +125°C			1.1	

7.8 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

Table 7-1. Typical Characteristic Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 7-1
Offset Voltage Drift Distribution From –40°C to 125°C	Figure 7-2
Input Bias Current Production Distribution	Figure 7-3
Input Offset Current Production Distribution	Figure 7-4
Offset Voltage vs Temperature	Figure 7-5
Offset Voltage vs Common-Mode Voltage	Figure 7-6
Offset Voltage vs Supply Voltage	Figure 7-7
Open-Loop Gain and Phase vs Frequency	Figure 7-8
Closed-Loop Gain vs Frequency	Figure 7-9
Input Bias Current vs Common-Mode Voltage	Figure 7-10
Input Bias Current and Offset vs Temperature	Figure 7-11
Output Voltage Swing vs Output Current (Sourcing)	Figure 7-12
Output Voltage Swing vs Output Current (Sinking)	Figure 7-13
CMRR and PSRR vs Frequency	Figure 7-14
CMRR vs Temperature	Figure 7-15
PSRR vs Temperature	Figure 7-16
0.1-Hz to 10-Hz Voltage Noise	Figure 7-17
Input Voltage Noise Spectral Density vs Frequency	Figure 7-18
THD+N Ratio vs Frequency	Figure 7-19
THD+N vs Output Amplitude	Figure 7-20
Quiescent Current vs Supply Voltage	Figure 7-21
Quiescent Current vs Temperature	Figure 7-22
Open-Loop Gain vs Temperature (10-kΩ)	Figure 7-23
Open-Loop Output Impedance vs Frequency	Figure 7-24
Small-Signal Overshoot vs Capacitive Load (10-mV Step)	Figure 7-25, Figure 7-26
No Phase Reversal	Figure 7-27
Positive Overload Recovery	Figure 7-28
Negative Overload Recovery	Figure 7-29
Small-Signal Step Response (10-mV Step)	Figure 7-30, Figure 7-31
Large-Signal Step Response (10-V Step)	Figure 7-32, Figure 7-33
Settling Time	Figure 7-34
Short Circuit Current vs Temperature	Figure 7-35
Maximum Output Voltage vs Frequency	Figure 7-36
EMIRR vs Frequency	Figure 7-37
Channel Separation	Figure 7-38

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

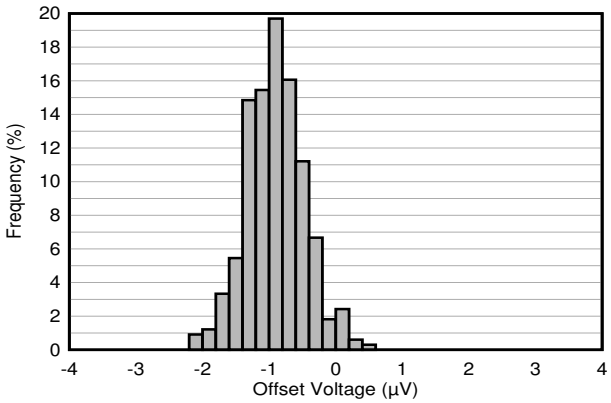


Figure 7-1. Offset Voltage Production Distribution

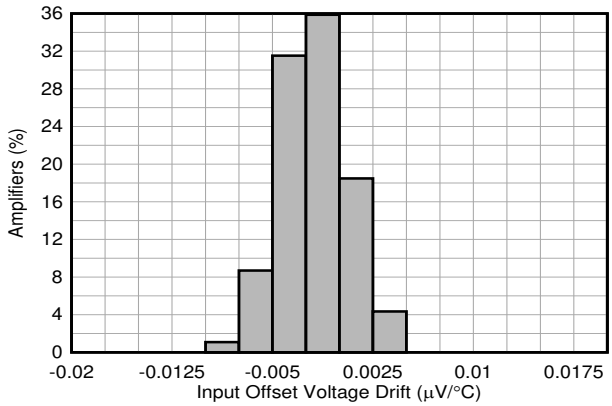


Figure 7-2. Offset Voltage Drift Distribution

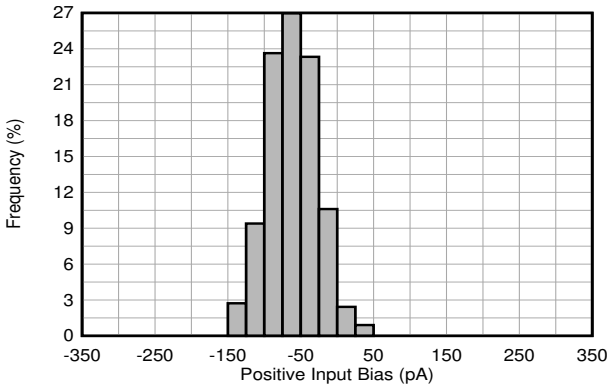


Figure 7-3. Input Bias Current Production Distribution

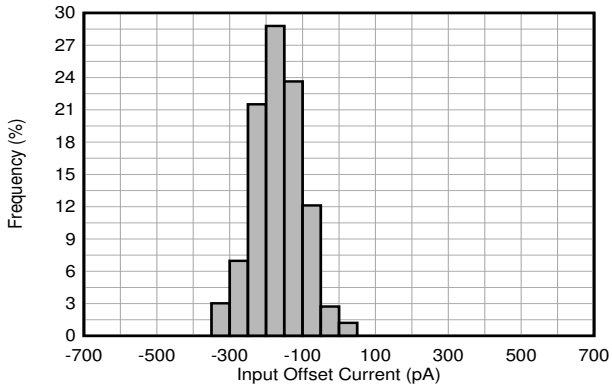


Figure 7-4. Input Offset Current Production Distribution

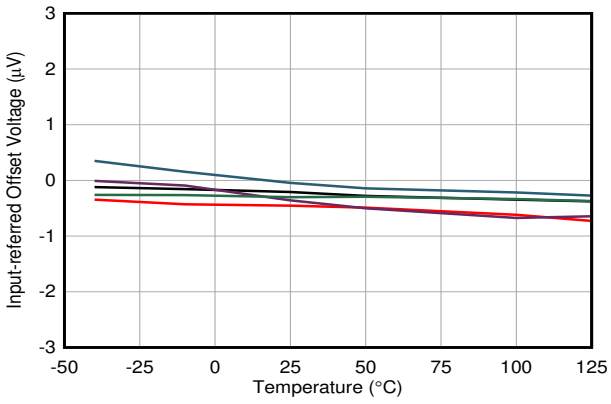


Figure 7-5. Offset Voltage vs Temperature

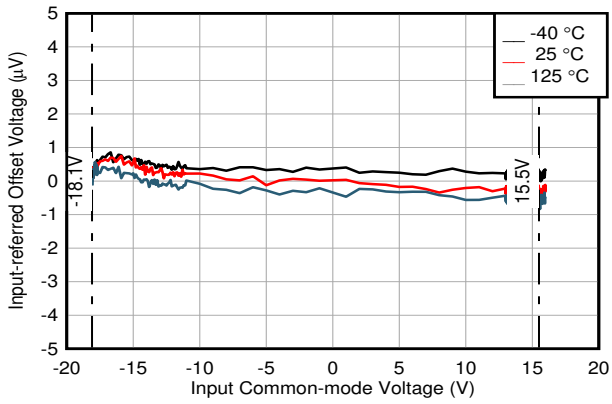


Figure 7-6. Offset Voltage vs Common-Mode Voltage

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

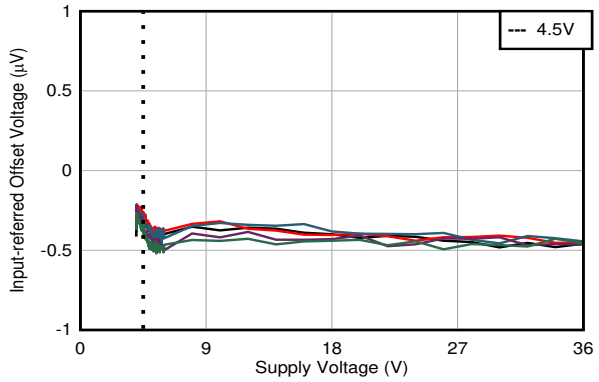


Figure 7-7. Offset Voltage vs Supply Voltage

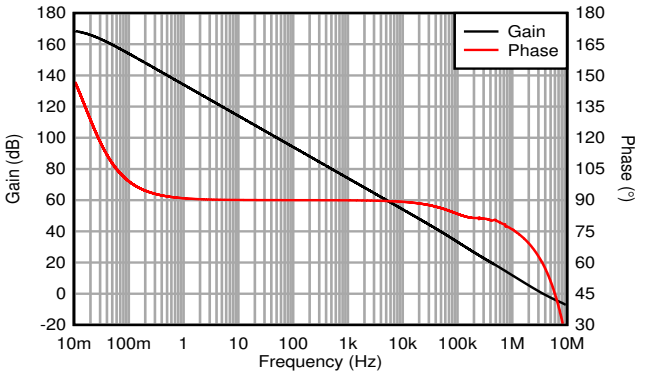


Figure 7-8. Open-Loop Gain and Phase vs Frequency

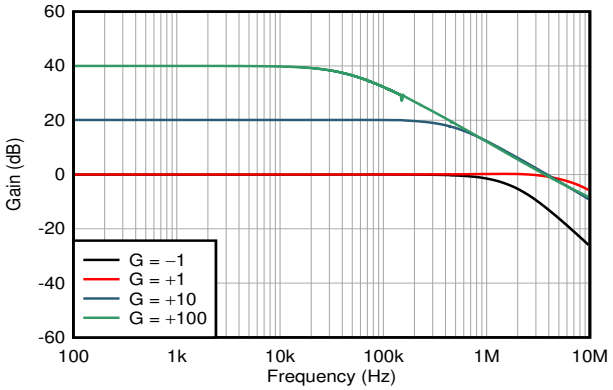


Figure 7-9. Closed-Loop Gain vs Frequency

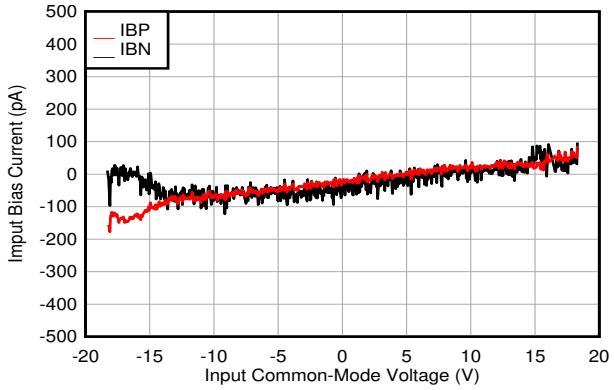


Figure 7-10. Input Bias Current vs Common-Mode Voltage

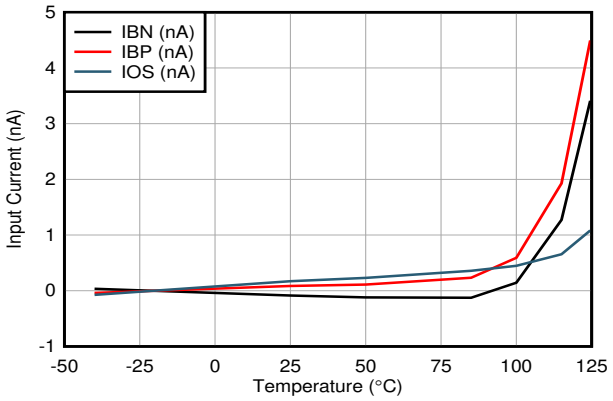


Figure 7-11. Input Bias Current and Offset vs Temperature

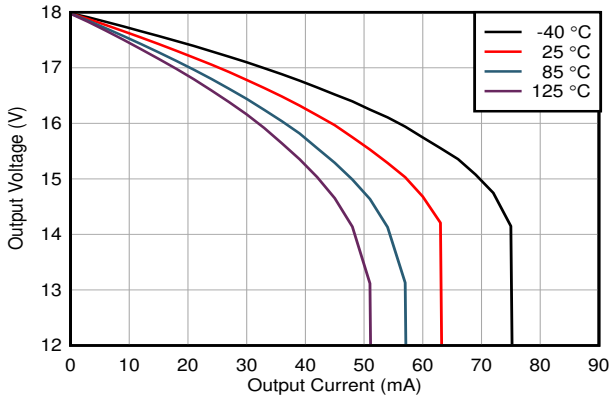


Figure 7-12. Output Voltage Swing vs Output Current (Sourcing)

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

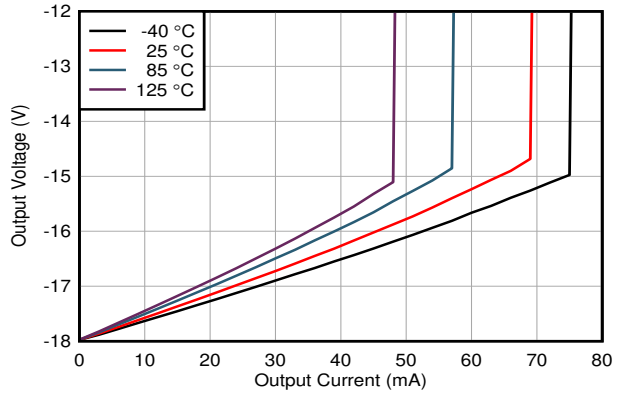


Figure 7-13. Output Voltage Swing vs Output Current (Sinking)

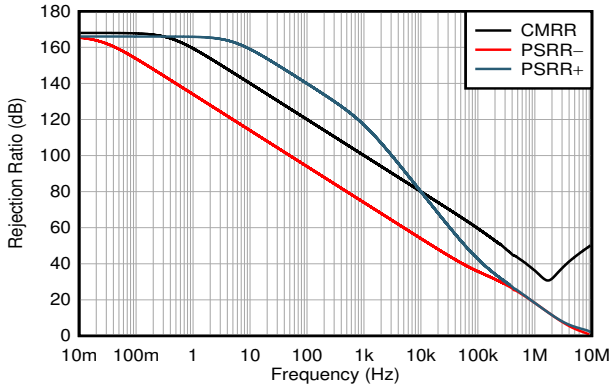


Figure 7-14. CMRR and PSRR vs Frequency

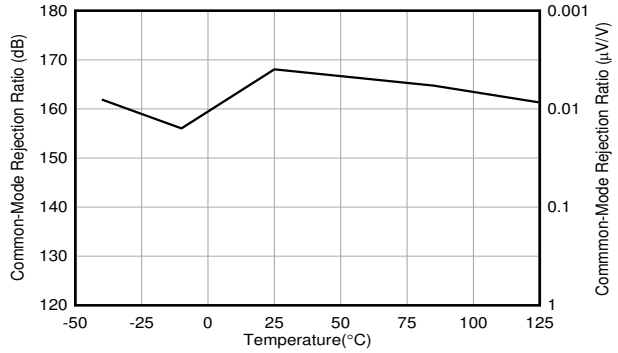


Figure 7-15. CMRR vs Temperature

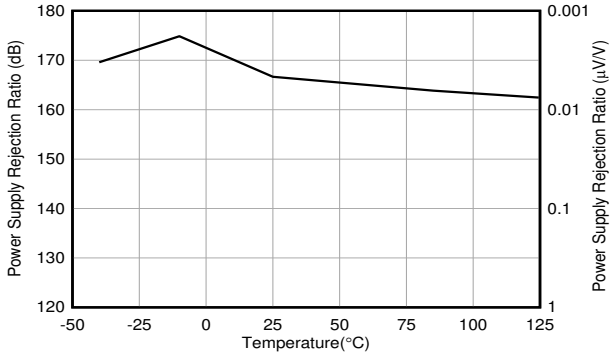


Figure 7-16. PSRR vs Temperature

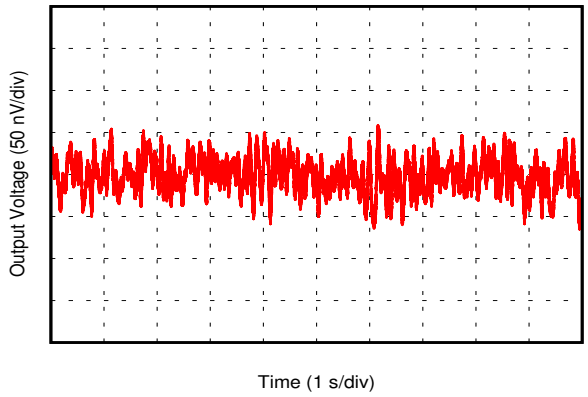


Figure 7-17. 0.1-Hz to 10-Hz Voltage Noise

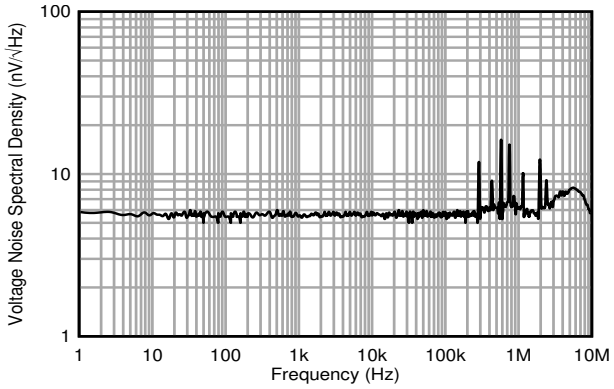


Figure 7-18. Input Voltage Noise Spectral Density vs Frequency

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

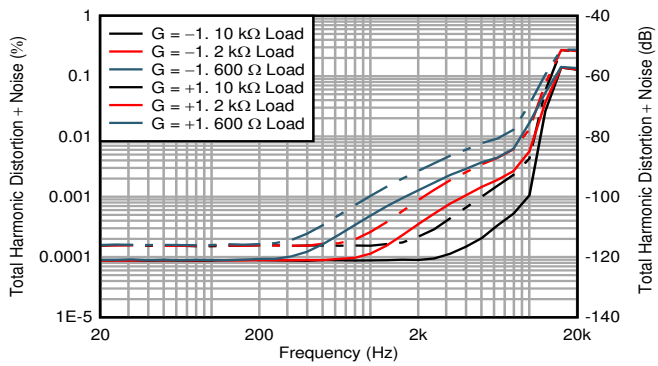


Figure 7-19. THD+N Ratio vs Frequency

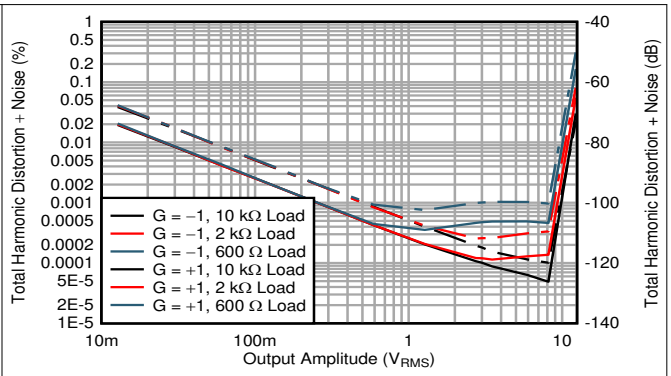


Figure 7-20. THD+N vs Output Amplitude

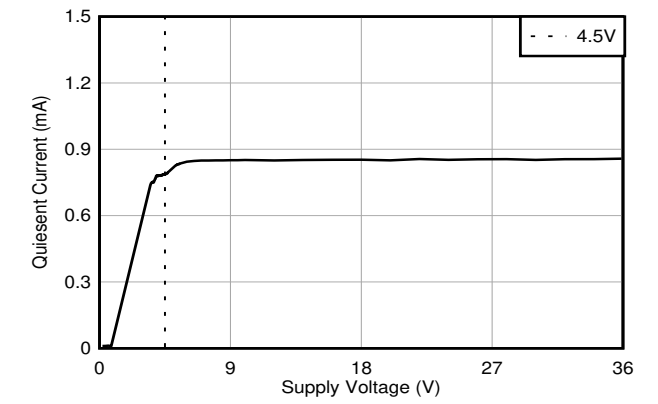


Figure 7-21. Quiescent Current vs Supply Voltage

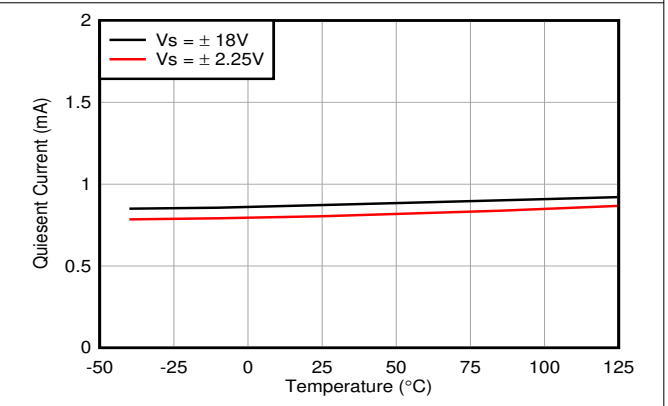


Figure 7-22. Quiescent Current vs Temperature

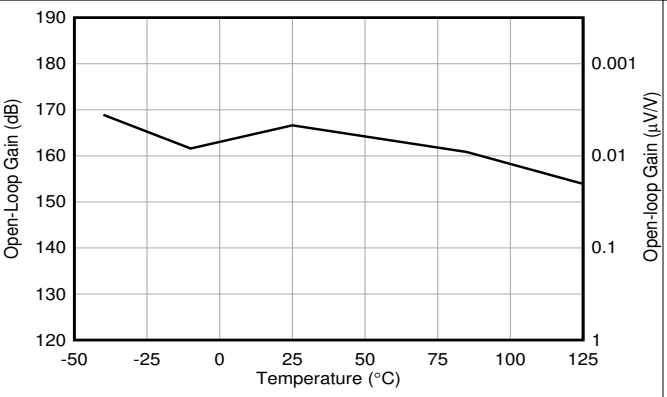


Figure 7-23. Open-Loop Gain vs Temperature (10-kΩ)

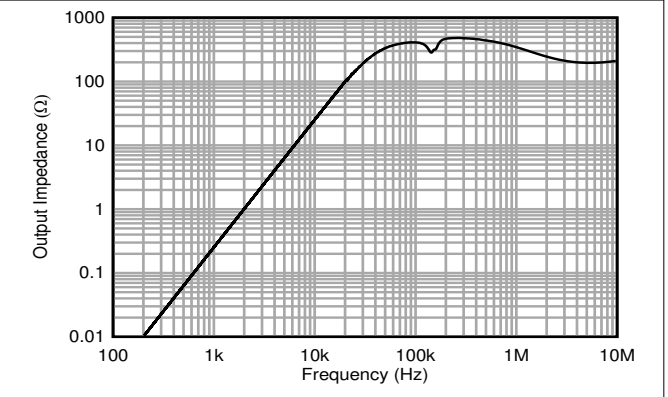


Figure 7-24. Open-Loop Output Impedance vs Frequency

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

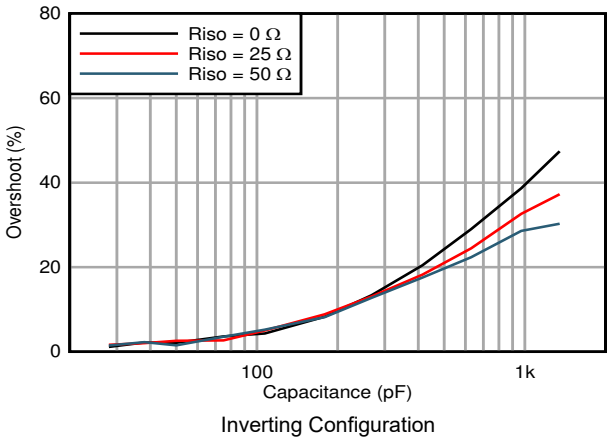


Figure 7-25. Small-Signal Overshoot vs Capacitive Load

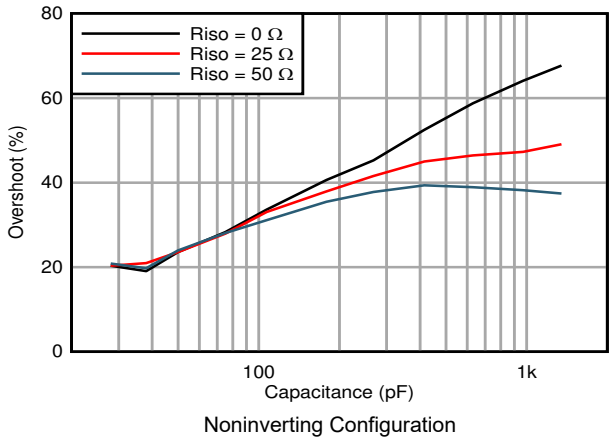


Figure 7-26. Small-Signal Overshoot vs Capacitive Load

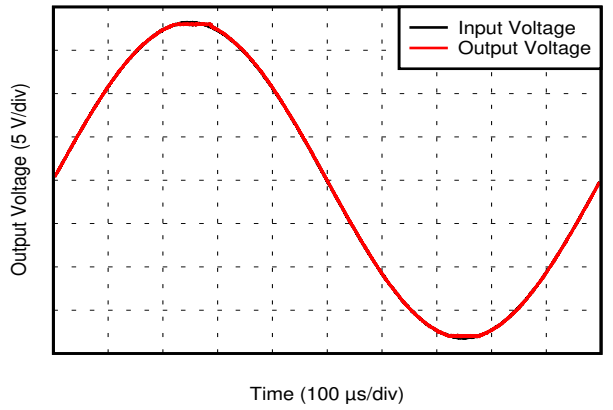


Figure 7-27. No Phase Reversal

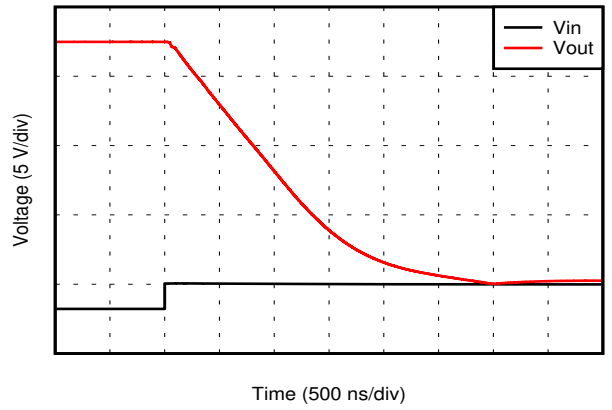


Figure 7-28. Positive Overload Recovery

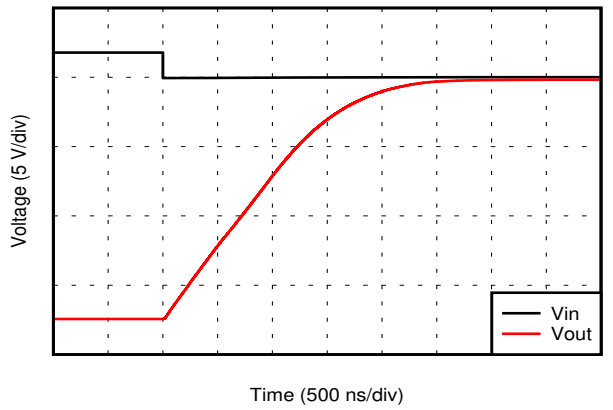


Figure 7-29. Negative Overload Recovery

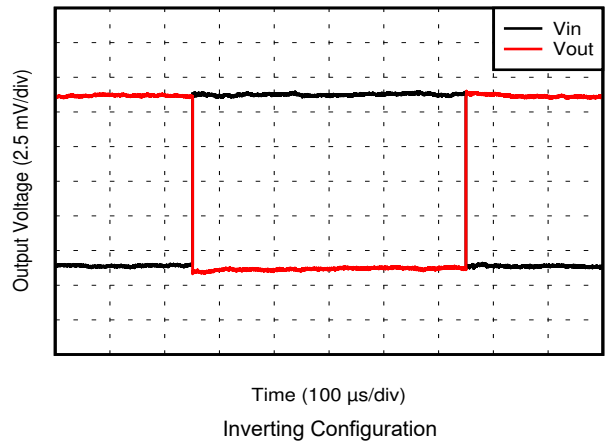
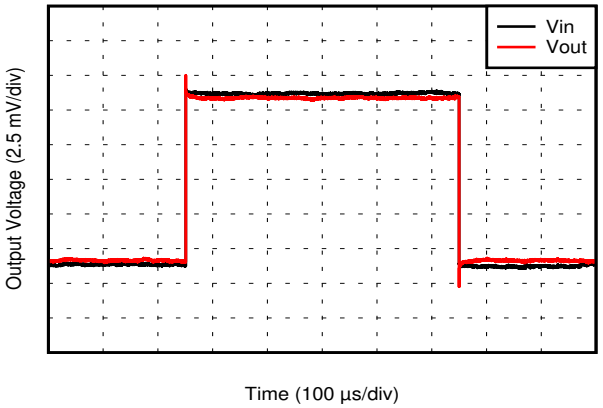


Figure 7-30. Small-Signal Step Response

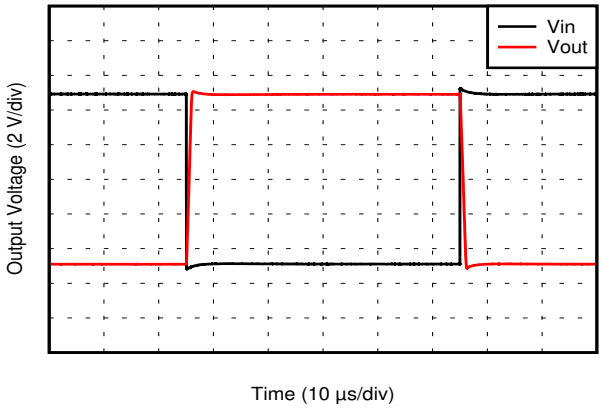
7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



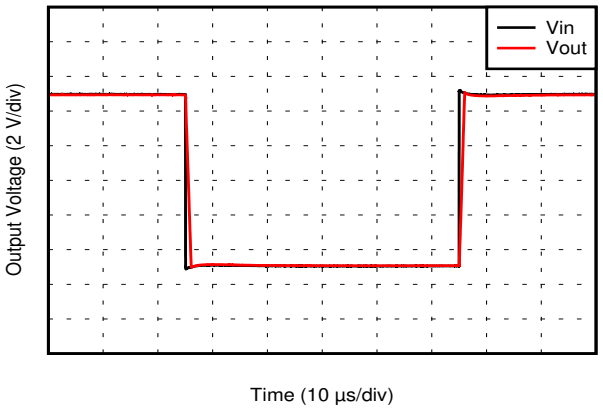
Noninverting Configuration

Figure 7-31. Small-Signal Step Response



Inverting Configuration

Figure 7-32. Large-Signal Step Response



Noninverting Configuration

Figure 7-33. Large-Signal Step Response

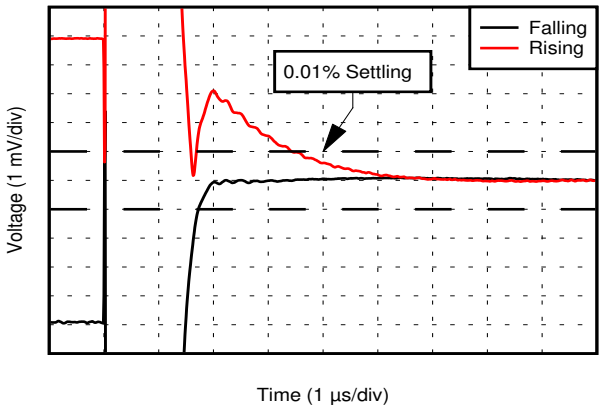


Figure 7-34. Settling Time

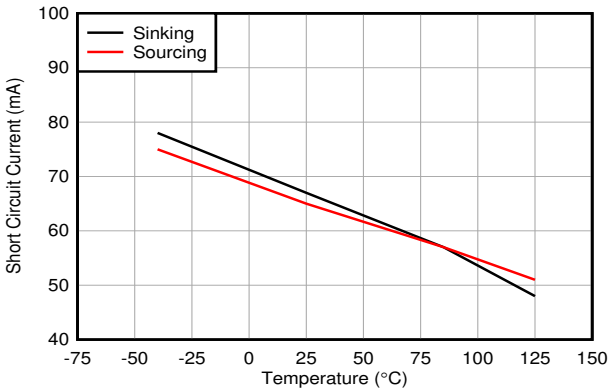


Figure 7-35. Short-Circuit Current vs Temperature

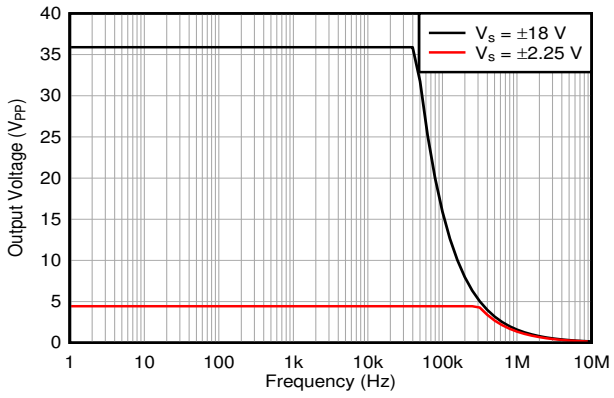


Figure 7-36. Maximum Output Voltage vs Frequency

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

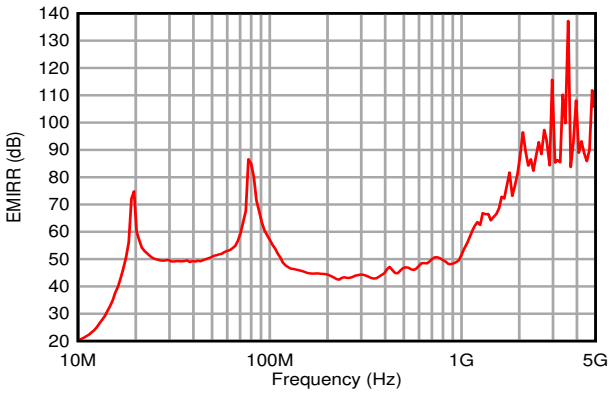


Figure 7-37. EMIRR vs Frequency

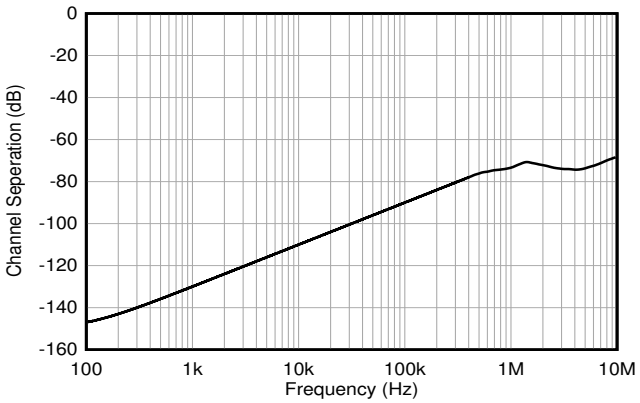


Figure 7-38. Channel Separation

8 Detailed Description

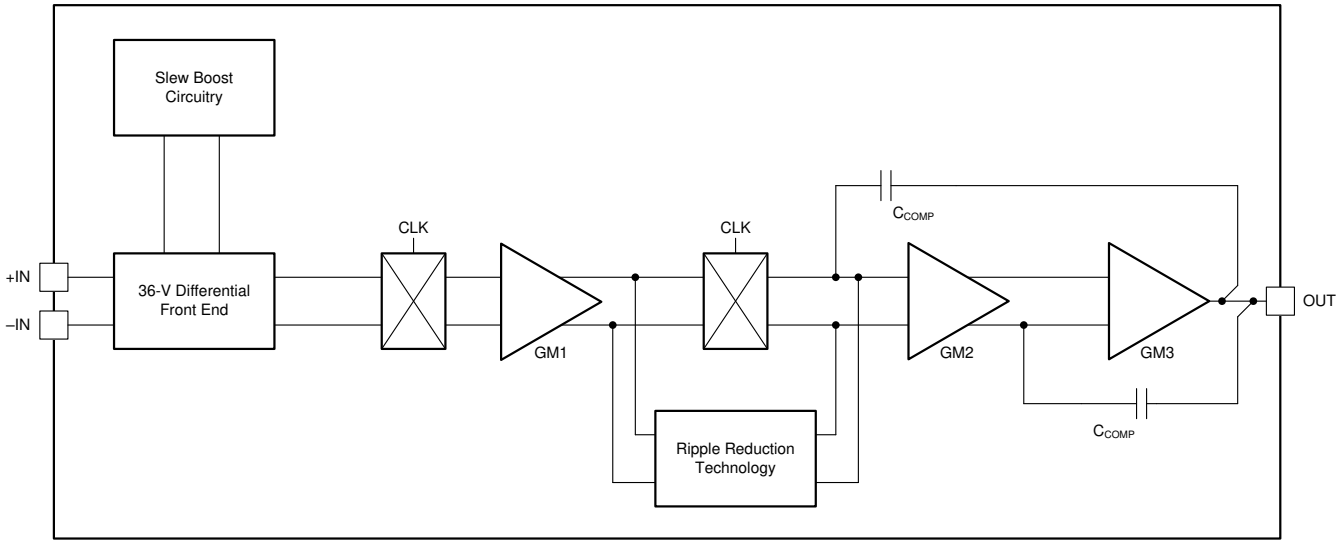
8.1 Overview

The OPAx182 family of operational amplifiers combine precision offset and drift with excellent overall performance, making these devices a great choice for many precision applications. The precision offset drift of only 0.005 µV/°C provides stability over the entire temperature range. In addition, these devices offer excellent linear performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate. See the *Layout Guidelines* section for details and a layout example.

The OPAx182 are zero-drift, MUX-friendly, rail-to-rail output operational amplifiers. The devices operate from 4.5 V to 36 V, are unity-gain stable, and a great choice for a wide range of general-purpose and precision applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise, zero flicker noise, and outstanding distortion performance when operating below the chopper frequency.

8.2 Functional Block Diagram

The functional block diagram shows a representation of the proprietary OPAx182 architecture.



8.3 Feature Description

The OPAx182 operational amplifiers have several integrated features that help maintain a high level of precision throughout all operating conditions. These features include phase-reversal protection, input bias current clock feedthrough and MUX-friendly inputs.

8.3.1 Phase-Reversal Protection

The OPAx182 have an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx182 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 8-1.

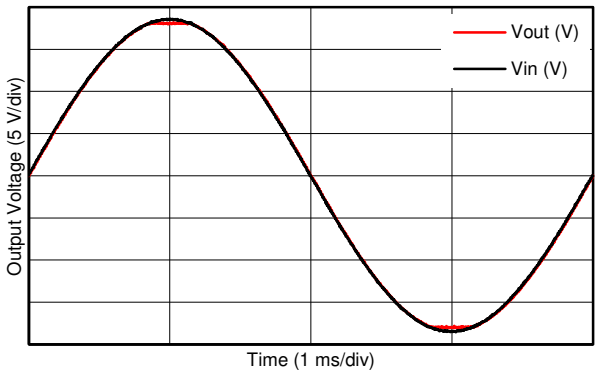


Figure 8-1. No Phase Reversal

8.3.2 Input Bias Current Clock Feedthrough

Zero-drift amplifiers such as the OPAx182 use switching on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the pulses from amplifying; however, the pulses can be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

8.3.3 EMI Rejection

The OPAx182 use integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx182 benefit from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 8-2 shows the results of this testing on the OPAx182. Table 8-1 lists the EMIRR +IN values for the OPAx182 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 8-1 can be centered on or operated near the particular frequency shown. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR +IN, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance
- EMIRR is more simple to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any op amp pin can result in adverse effects because there is insufficient amplifier loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output can result in unexpected dc offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

The EMIRR +IN of the OPAx182 is plotted versus frequency as shown in Figure 8-2. If available, any dual and quad op amp device versions have nearly similar EMIRR +IN performance. The OPAx182 gain bandwidth is 5 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the op amp bandwidth.

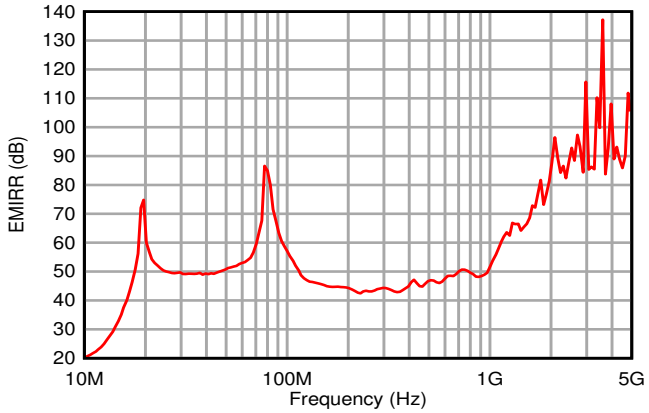


Figure 8-2. EMIRR Testing

Table 8-1. OPAx182 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	44.9 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	48.4 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	81.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	87.9 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	137.2 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	99.2 dB

8.3.4 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. See Figure 8-3 for an illustration of the ESD circuits contained in the OPAx182 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger or threshold voltage that is greater than the normal operating voltage of the OPAx182 but less than the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

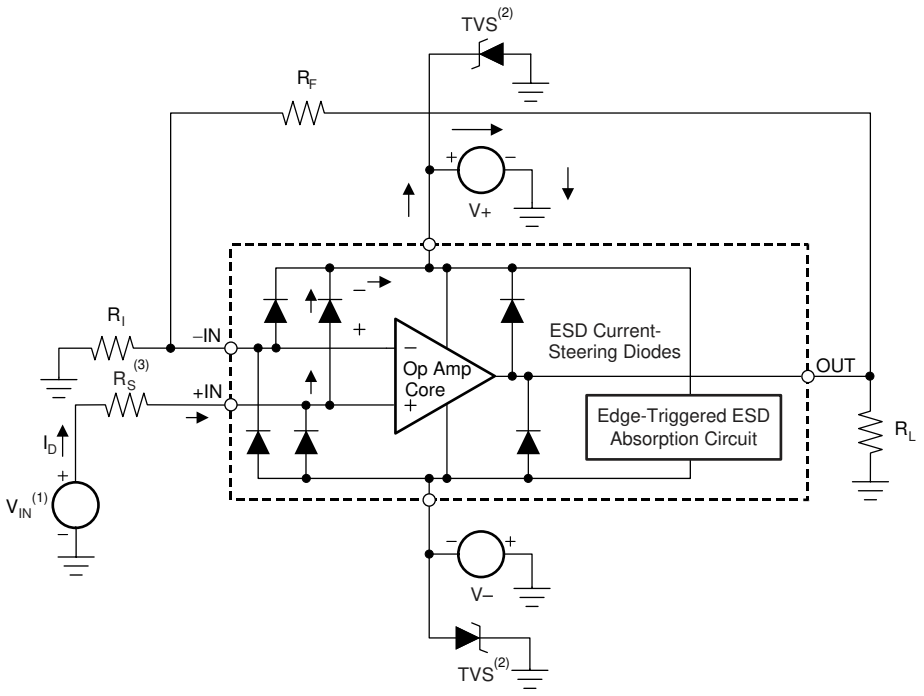
When the op amp connects into a circuit (as shown in Figure 8-3), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits are biased on, and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 8-3 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies V+ or V– are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current-steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, external Zener diodes must be added to the supply pins, as shown in Figure 8-3. The Zener voltage must be selected such that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) V_{IN} = V+ + 500 mV.
(2) TVS: 40 V > $V_{TVSBR\ (min)}$ > V+, where $V_{TVSBR\ (min)}$ is the minimum specified value for the transient voltage suppressor breakdown voltage.
(3) Suggested value is approximately 5 kΩ in overvoltage conditions.

Figure 8-3. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

8.3.5 MUX-Friendly Inputs

The OPAx182 feature a proprietary input stage design that allows an input differential voltage to be applied while maintaining high input impedance. Typically, high-voltage CMOS or bipolar-junction input amplifiers feature antiparallel diodes that protect input transistors from large V_{GS} voltages that can exceed the semiconductor process maximum and permanently damage the device. Large V_{GS} voltages can be forced when applying a large input step, switching between channels, or attempting to use the amplifier as a comparator. For more information, see the *MUX-Friendly Precision Operational Amplifiers* application brief.

The OPAx182 solve these problems with a switched-input technique that prevents large input bias currents when large differential voltages are applied. This input architecture solves many issues seen in switched or multiplexed applications, where large disruptions to RC filtering networks are caused by fast switching between large potentials. The OPAx182 offer outstanding settling performance because of these design innovations, along with built-in slew rate boost and wide bandwidth. The OPAx182 can also be used as a comparator. Differential and common-mode *Absolute Maximum Ratings* still apply relative to the power supplies.

8.4 Device Functional Modes

The OPAx182 have a single functional mode, and are operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage is 36 V (±18 V).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPAx182 operational amplifiers combine precision offset and drift with excellent overall performance, making these devices a great choice for many precision applications. The precision offset drift of only 0.005 µV/°C provides stability over the entire temperature range. In addition, the devices combine excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPAx182 can be used.

9.2 Typical Applications

9.2.1 Strain Gauge Analog Linearization

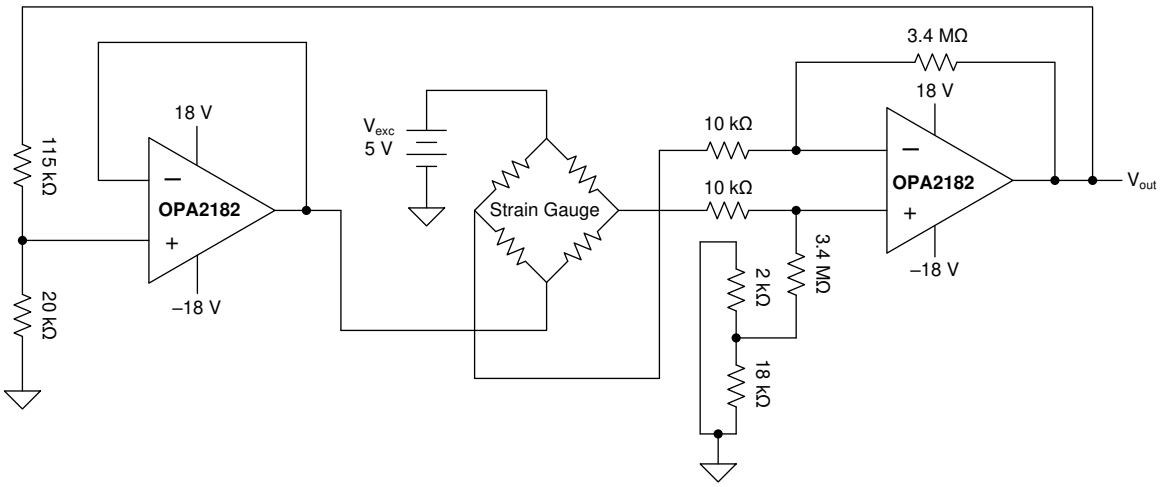


Figure 9-1. Bridge Sensor Analog Linearization With the OPA2182

9.2.1.1 Design Requirements

A strain gauge is used to measure an alteration due to external force through the use of electrical resistance in a Wheatstone-bridge configuration. The Wheatstone bridge is used to precisely measure very low values of resistances down in the mΩ range. An excitation voltage is applied to the bridge, and the output voltage across the middle of the bridge is measured. The total change in output voltage is relatively small, typically in the mV range. Therefore, an op amp is used to amplify the signal. The OPA2182 is designed to construct high-precision amplification.

Use the following parameters for this design example:

- Use the op-amp linear output operating range, which is usually specified under the AOL test conditions. The common-mode voltage is equal to the input signal.
- Use an op amp that does not add significant noise to the system or else the small output voltage from the Wheatstone bridge will be lost.
- The input signal must be gained; therefore, use an op amp with low input offset voltage (V_{OS})
- The input signal must be gained; therefore, use an op amp with enough open-loop gain to provide the required amplification

9.2.1.2 Detailed Design Procedure

The bridge sensor signal flow model is shown in Figure 9-2.

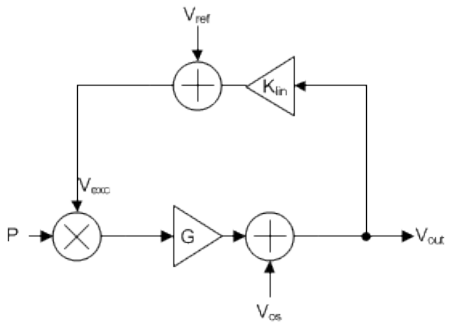


Figure 9-2. Bridge Sensor Signal Flow Model

The bridge sensor is modeled as a multiplier, with inputs from an excitation voltage and pressure sensor producing an output voltage given in Equation 1:

$$V_{bridge}(P, V_{exc}) = V_{exc} \times K_p(P) \tag{1}$$

K_p is the sensitivity of the bridge sensor, and is usually specified in mV/V. P represents the pressure relative to the range of the sensor, normalized to a scale from 0 to 1. Solving this equation with the variables given in the signal flow model and solving for V_{out} results in Equation 2:

$$V_{out}(P) = \frac{V_{OS} + V_{ref} \times G \times K_p(P)}{1 - G \times K_{lin} \times K_p(P)} \tag{2}$$

This equation has three variables, V_{OS}, G and K_{lin}, that require three equations to solve. To solve these equations. values of K_p at no load, midscale and full load conditions are needed for the sensor. With these values, the system can be linearized.

With known values for K_p, K_{lin} is calculated as shown in Equation 3:

$$K_{lin} = \frac{4 \times B_v \times V_{ref}}{(V_{out\_high} - V_{out\_low}) - 2 \times B_v \times (V_{out\_high} + V_{out\_low})} \tag{3}$$

In this equation, B_v represents the bridge nonlinearity, which is calculated as shown in Equation 4:

$$B_v = \frac{K_p(0.5) - \frac{K_p(1) + K_p(0)}{2}}{K_p(1) - K_p(0)} \tag{4}$$

B_v is solved based on the sensor specifications, and the equation is then used to solve for K_{lin}. Next, the system gain is calculated using Equation 5 and Equation 6.

$$V_{out\_high} = \frac{V_{OS} + V_{ref} \times G \times K_p(1)}{1 - G \times K_{lin} \times K_p(1)} \tag{5}$$

$$V_{out\_high} = \frac{V_{OS} + V_{ref} \times G \times K_p(0)}{1 - G \times K_{lin} \times K_p(0)} \tag{6}$$

Solving for V_{OS} in both equations and combining results in Equation 7.

$$V_{out\_high}(1-G\times K_{lin}\times K_p(1))-V_{ref}\times G\times K_p(1)=V_{out\_low}(1-G\times K_{lin}\times K_p(0))-V_{ref}\times G\times K_p(0) \quad (7)$$

Solving for G gives Equation 8.

$$G=\frac{V_{out\_high}-V_{out\_low}}{K_p(1)\times(K_{lin}\times V_{out\_high}+V_{ref})-K_p(0)\times(K_{lin}\times V_{out\_low}+V_{ref})} \quad (8)$$

With both K_{lin} and G now calculated, V_{OS} is solved as shown in Equation 9.

$$V_{OS}=V_{out\_low}(1-G\times K_{lin}\times K_p(0))-V_{ref}\times G\times K_p(0) \quad (9)$$

For a sensor with a K_P of 0.0003 mV/V at no load, 0.0017 mV/V midscale and 0.00289 mV/V, the corresponding nonlinearity is approximately 4%. Solving for K_{lin}, G, and V_{OS} gives the values shown in Table 9-1.

Table 9-1. Example Bridge Calculations

K_{lin}	0.173913
G	323.8178
VOS	-0.48573

9.2.1.3 Application Curves

Using the same K_P values used previously, the bridge nonlinearity is simulated as 4% peak, the output is linear from 0 V to 5 V, and the corrected system nonlinearity is approximately ±0.1%.

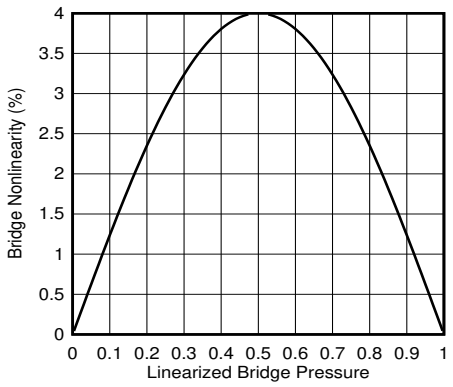


Figure 9-3. Bridge Nonlinearity

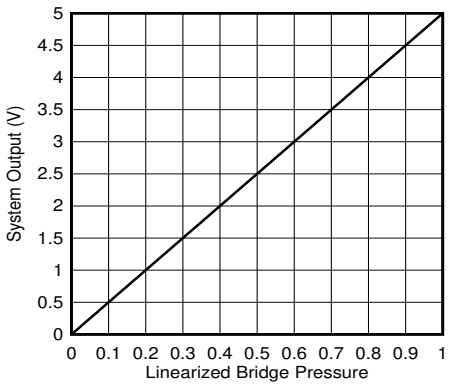


Figure 9-4. Bridge Output

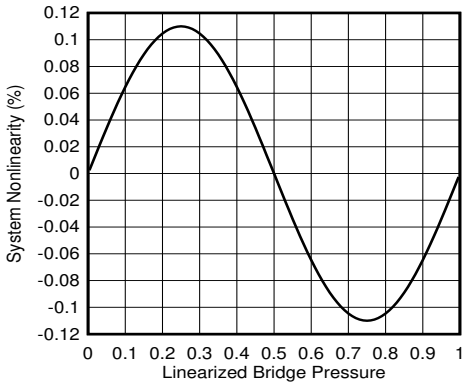


Figure 9-5. System Nonlinearity

9.2.2 Rogowski Coil Integrator

Figure 9-6 shows the OPA2182 configured as an active integrator, level shifter and precision voltage reference buffer for a Rogowski coil used to indirectly measure the current of a protection relay with high accuracy. This design has two main signal paths: the first path is used to accurately measure the current flowing through the Rogowski coil, and a second high-speed path is used to detect a fast transient such as a short circuit. The OPA2182 is selected for this application thanks to the low offset voltage (0.45 µV) and offset drift (0.003 µV/°C) that minimize calibration requirements and maintain higher accuracy across the full temperature range. This device also features flat noise across a wide frequency range which includes dc which improves accuracy and repeatability across a wide range of input currents from the Rogowski coil. Additional information on this design can be found in the *Active Integrator for Rogowski Coil Reference Design with Improved Accuracy for Relay and Breaker*.

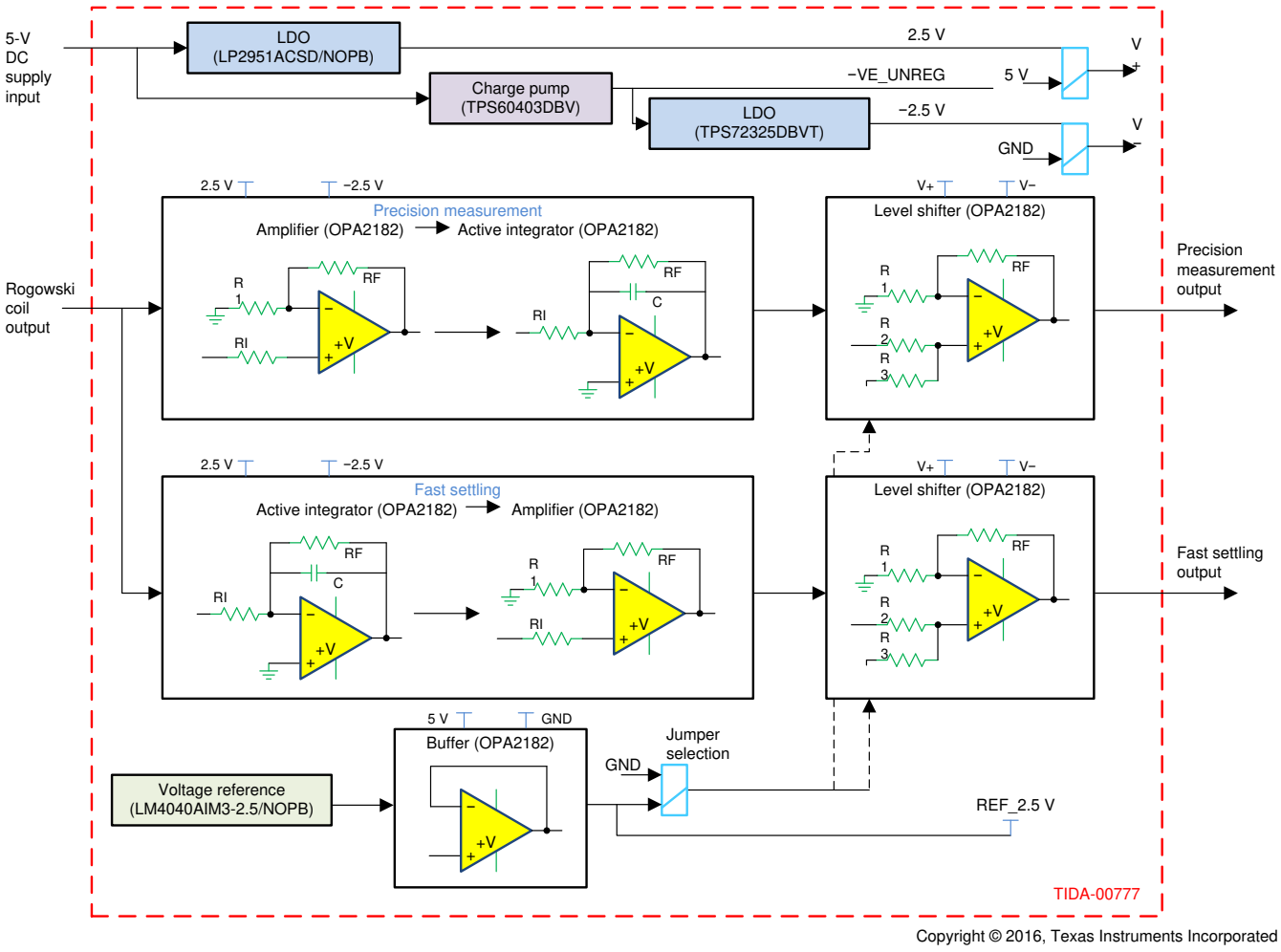


Figure 9-6. Programmable Power Supply

9.2.3 System Examples

9.2.3.1 24-Bit, Delta-Sigma, Differential Load Cell or Strain Gauge Sensor Signal Conditioning

The OPA2182 is used in a 24-bit, differential load cell or strain gauge sensor signal conditioning system alongside the ADS1225. The OPA2182 amplifier is configured in a two-amp instrumentation-amplifier (IA) configuration, and is band-limited to reduce noise and allow heavy capacitive drive. The load cell is powered by an excitation voltage (denoted V_{EX}) of 5 V and provides a differential voltage proportional to force applied. The differential voltage can be quite small and both outputs are biased to V_{EX} / 2.

In this example, the OPA2182 is employed here because of the excellent input offset voltage (0.45 µV) and input offset voltage drift (0.003 µV/°C), the low broadband noise (5.7 nV/√Hz) and zero-flicker noise, and excellent linearity and high input impedance. The two-amp IA configuration removes the dc bias and amplifies the differential signal of interest and drives the 24-bit, delta-sigma ADS1225 analog-to-digital converter (ADC) for acquisition and conversion. The ADS1225 features a 100-SPS data rate, single-cycle settling, and simple conversion control with a dedicated START pin.

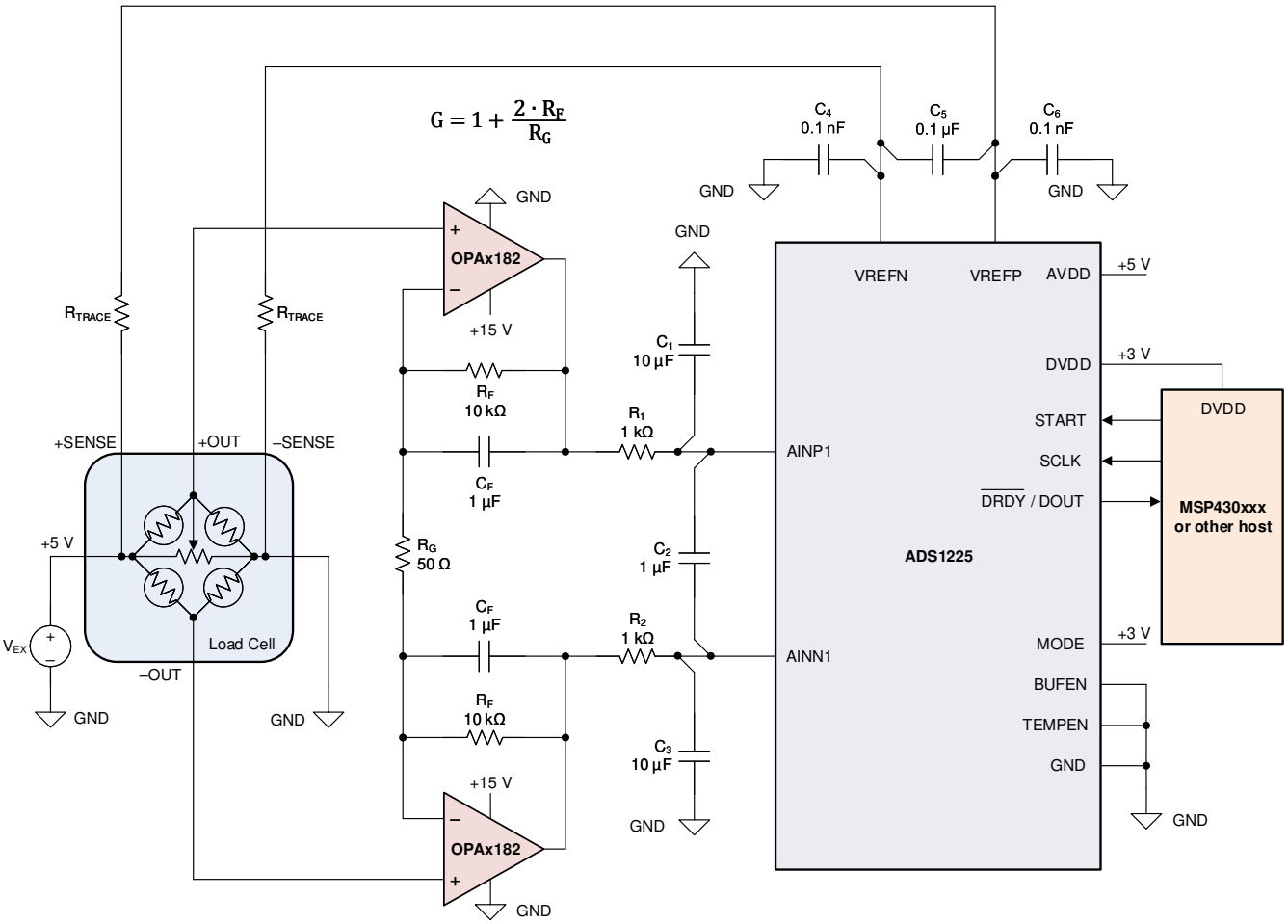


Figure 9-7. 24-Bit Differential Load Cell or Strain Gauge Sensor Signal Conditioning Schematic

9.2.4 Programmable Power Supply

Figure 9-6 shows the OPAx182 configured as a precision programmable power supply using the 16-bit, voltage output DAC8581 and the OPA548 high-current amplifier. This application amplifies the digital-to-analog converter (DAC) voltage by a value of five, and handles a large variety of capacitive and current loads. The OPAx182 in the front-end provides precision and low drift across a wide range of inputs and conditions. Click the following link to download the TINA-TI™ software file: Programmable Power-Supply Circuit.

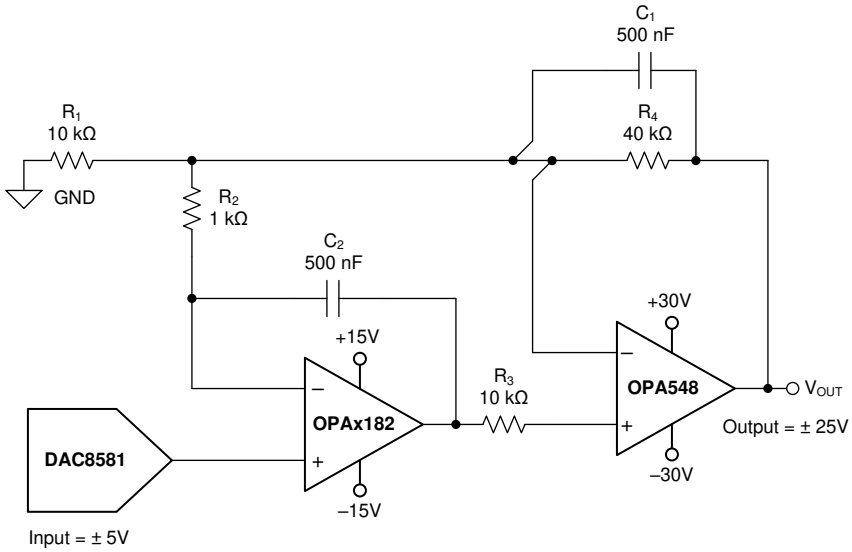
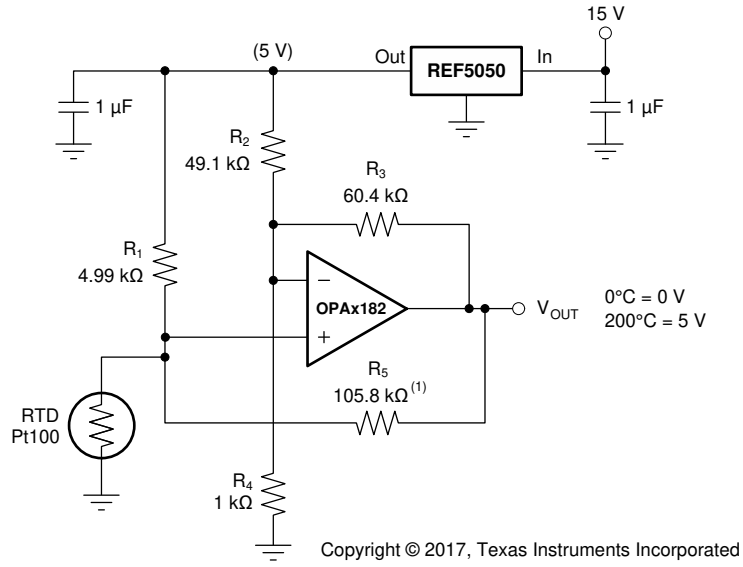


Figure 9-8. Programmable Power Supply

9.2.5 RTD Amplifier With Linearization

See the *Analog Linearization of Resistance Temperature Detectors* analog design journal for an in-depth analysis of Figure 9-9. Click the following link to download the TINA-TI™ software file: RTD Amplifier with Linearization.



(1) R_5 provides positive-varying excitation to linearize output.

Figure 9-9. RTD Amplifier With Linearization

9.3 Power Supply Recommendations

The OPAx182 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the *Aboslute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

9.4 Layout

9.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *The PCB is a component of op amp design*.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in Figure 9-10, keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

For the lowest offset voltage, avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors.

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

9.4.2 Layout Example

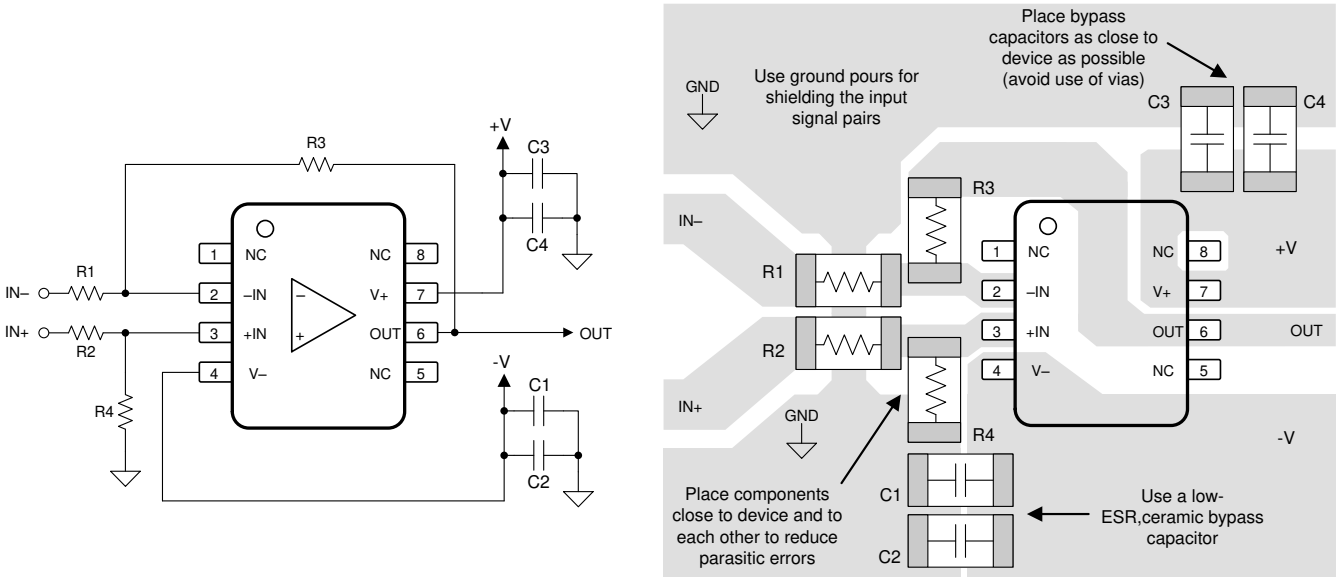


Figure 9-10. Operational Amplifier Board Layout for Difference Amplifier Configuration

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

10.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

10.1.1.3 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Zero-drift Amplifiers: Features and Benefits* application report
- Texas Instruments, *The PCB is a component of op amp design* technical brief
- Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis* technical brief
- Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis* technical brief
- Texas Instruments, *Using infinite-gain, MFB filter topology in fully differential active filters* technical brief
- Texas Instruments, *Op Amp Performance Analysis* application bulletin
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application bulletin
- Texas Instruments, *Tuning in Amplifiers* application bulletin
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes* application report
- Texas Instruments, *Feedback Plots Define Op Amp AC Performance* application bulletin
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Analog Linearization of Resistance Temperature Detectors* technical brief
- Texas Instruments, *TI Precision Design TIPD102 High-Side Voltage-to-Current (V-I) Converter* reference guide

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA182IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2RXQ
OPA182IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2RXQ
OPA182IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2RXQ
OPA182IDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2RXQ
OPA182IDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP182
OPA182IDR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP182
OPA182IDT	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP182
OPA182IDT.B	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP182
OPA2182ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP2182
OPA2182ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP2182
OPA2182IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	26RQ
OPA2182IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	26RQ
OPA2182IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	26RQ
OPA2182IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	26RQ
OPA2182IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP2182
OPA2182IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP2182
OPA4182IDR	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP4182
OPA4182IDR.B	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP4182
OPA4182IDT	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP4182
OPA4182IDT.B	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP4182

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

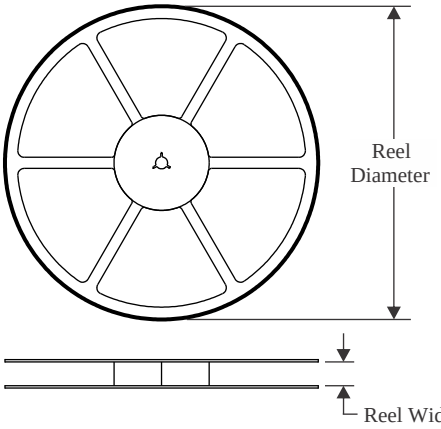
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

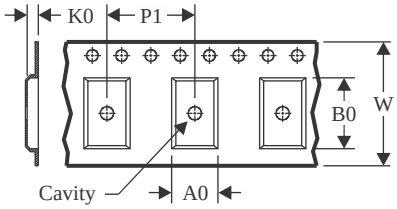
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

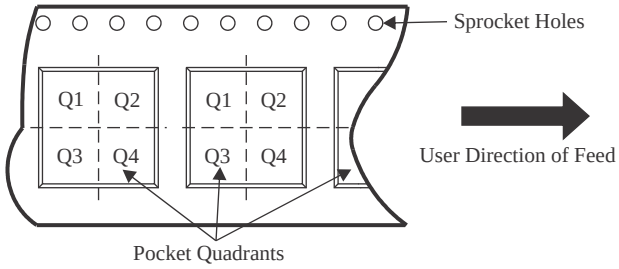


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

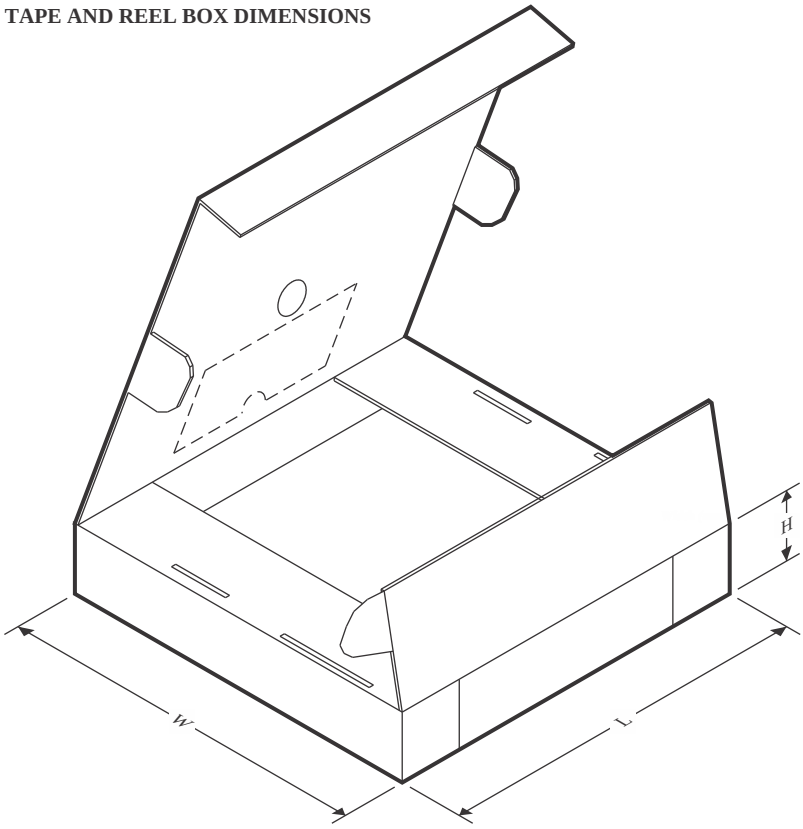
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA182IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA182IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA182IDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA182IDT	SOIC	D	8	250	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2182IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2182IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2182IDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
OPA4182IDR	SOIC	D	14	3000	330.0	16.4	6.5	9.5	2.3	8.0	16.0	Q1
OPA4182IDT	SOIC	D	14	250	330.0	16.4	6.5	9.5	2.3	8.0	16.0	Q1

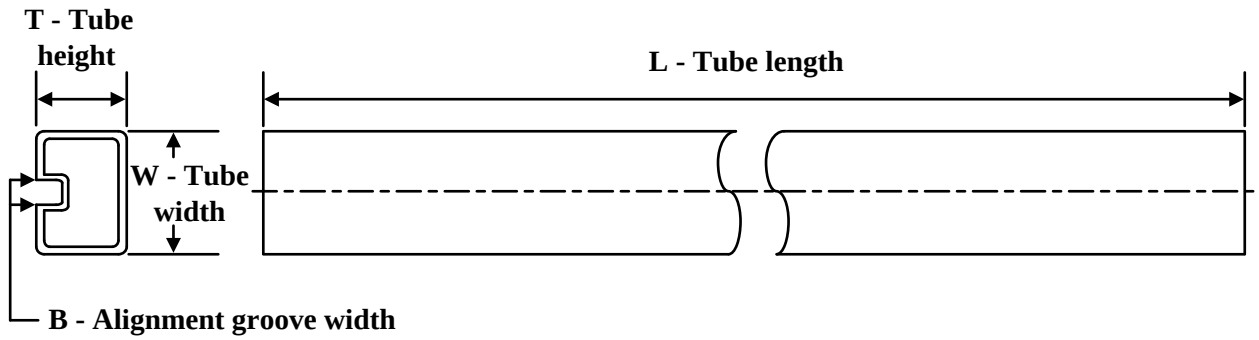
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA182IDBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
OPA182IDBVT	SOT-23	DBV	5	250	190.0	190.0	30.0
OPA182IDR	SOIC	D	8	3000	366.0	364.0	50.0
OPA182IDT	SOIC	D	8	250	366.0	364.0	50.0
OPA2182IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2182IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2182IDR	SOIC	D	8	2500	366.0	364.0	50.0
OPA4182IDR	SOIC	D	14	3000	366.0	364.0	50.0
OPA4182IDT	SOIC	D	14	250	366.0	364.0	50.0

TUBE



*All dimensions are nominal

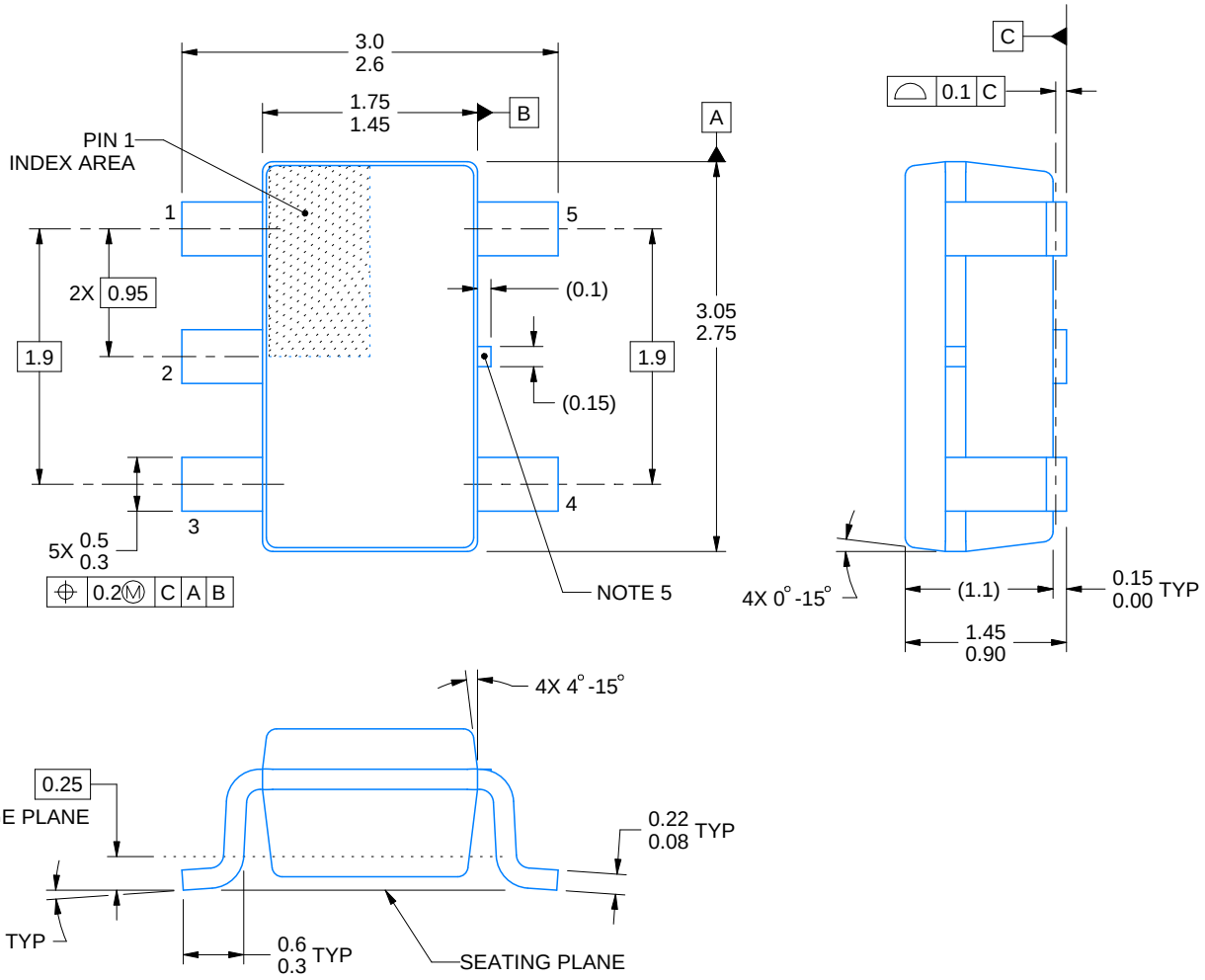
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2182ID	D	SOIC	8	75	509	7.9	3800	2.81
OPA2182ID.B	D	SOIC	8	75	509	7.9	3800	2.81

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

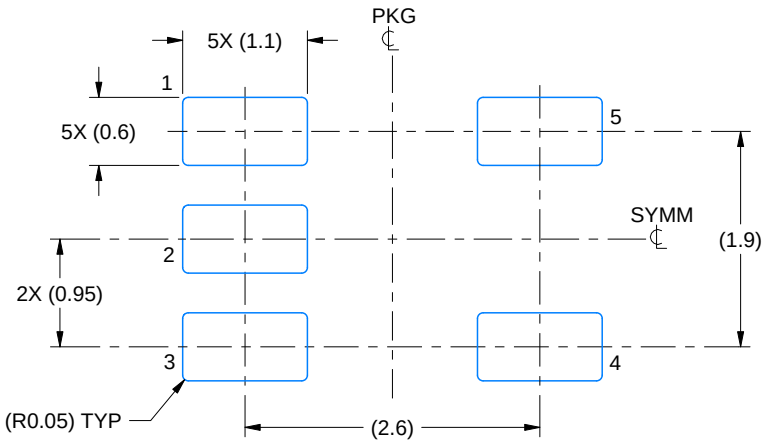
SMALL OUTLINE TRANSISTOR



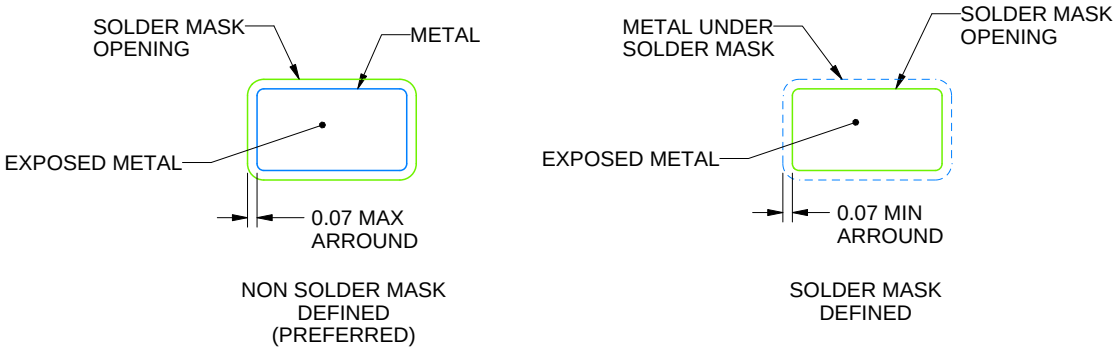
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

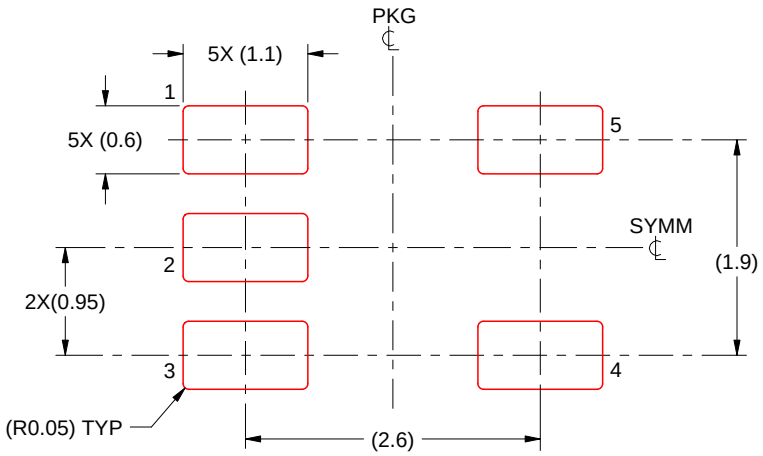


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

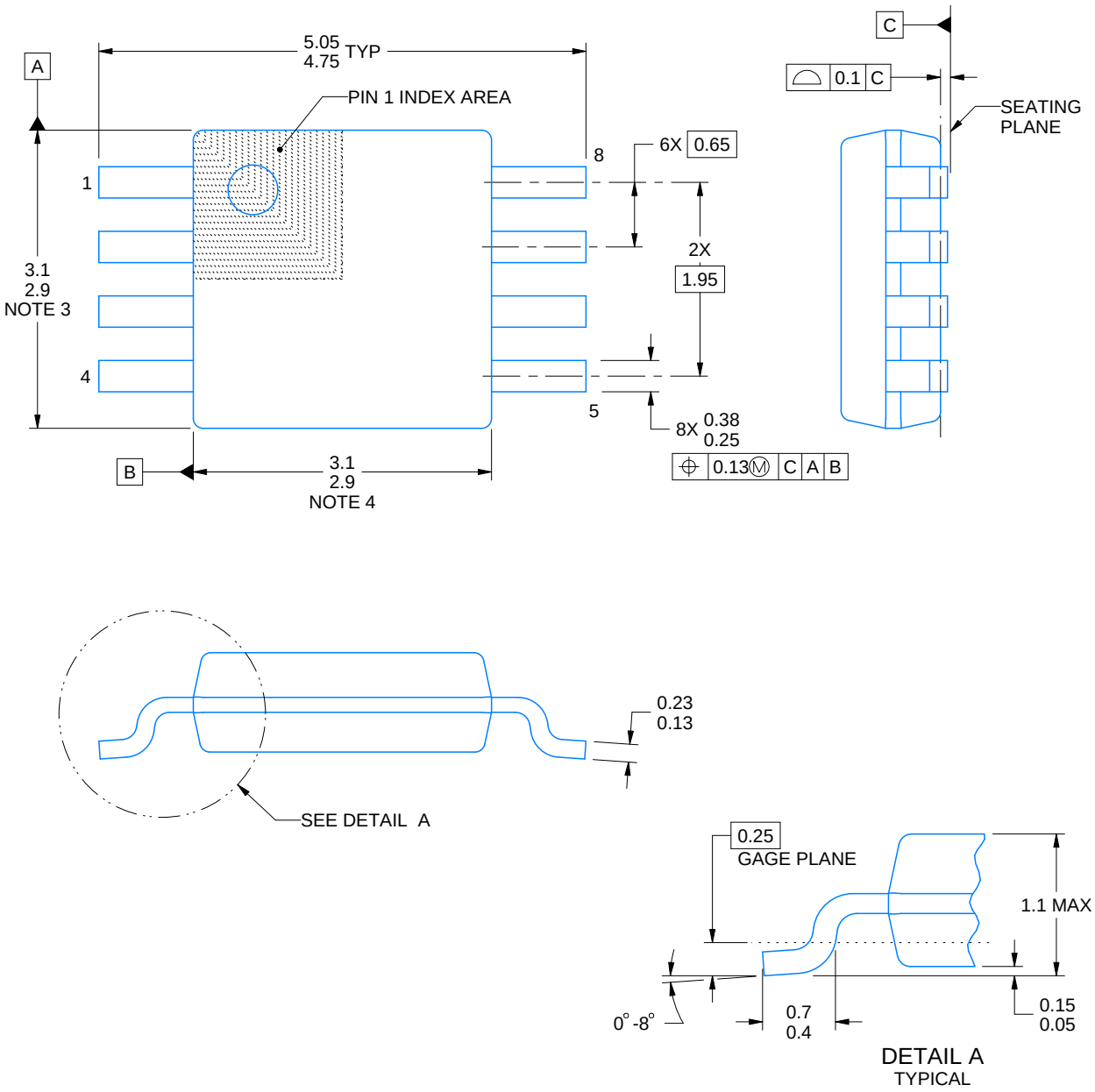
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

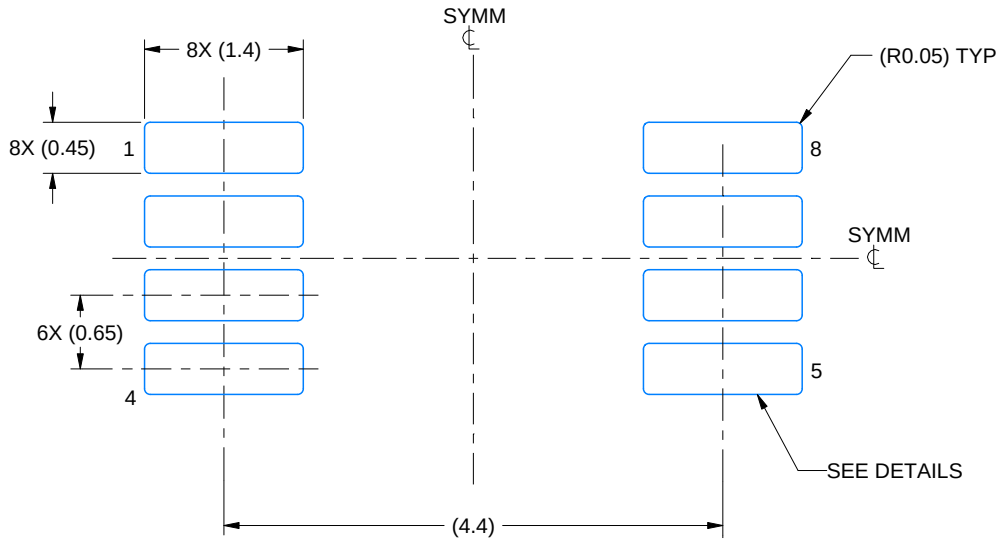
SMALL OUTLINE PACKAGE



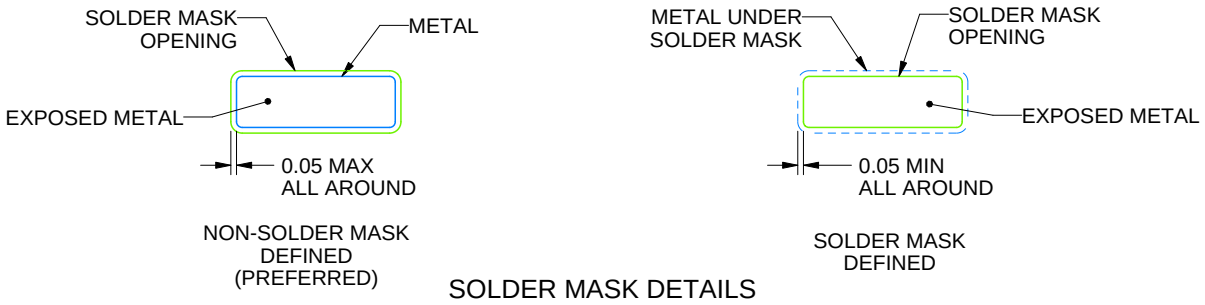
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

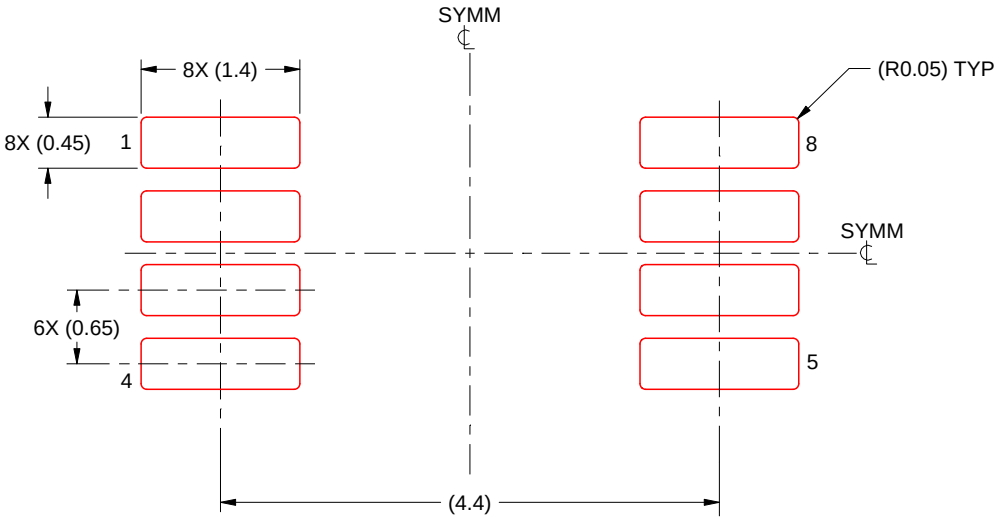


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

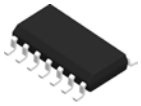


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

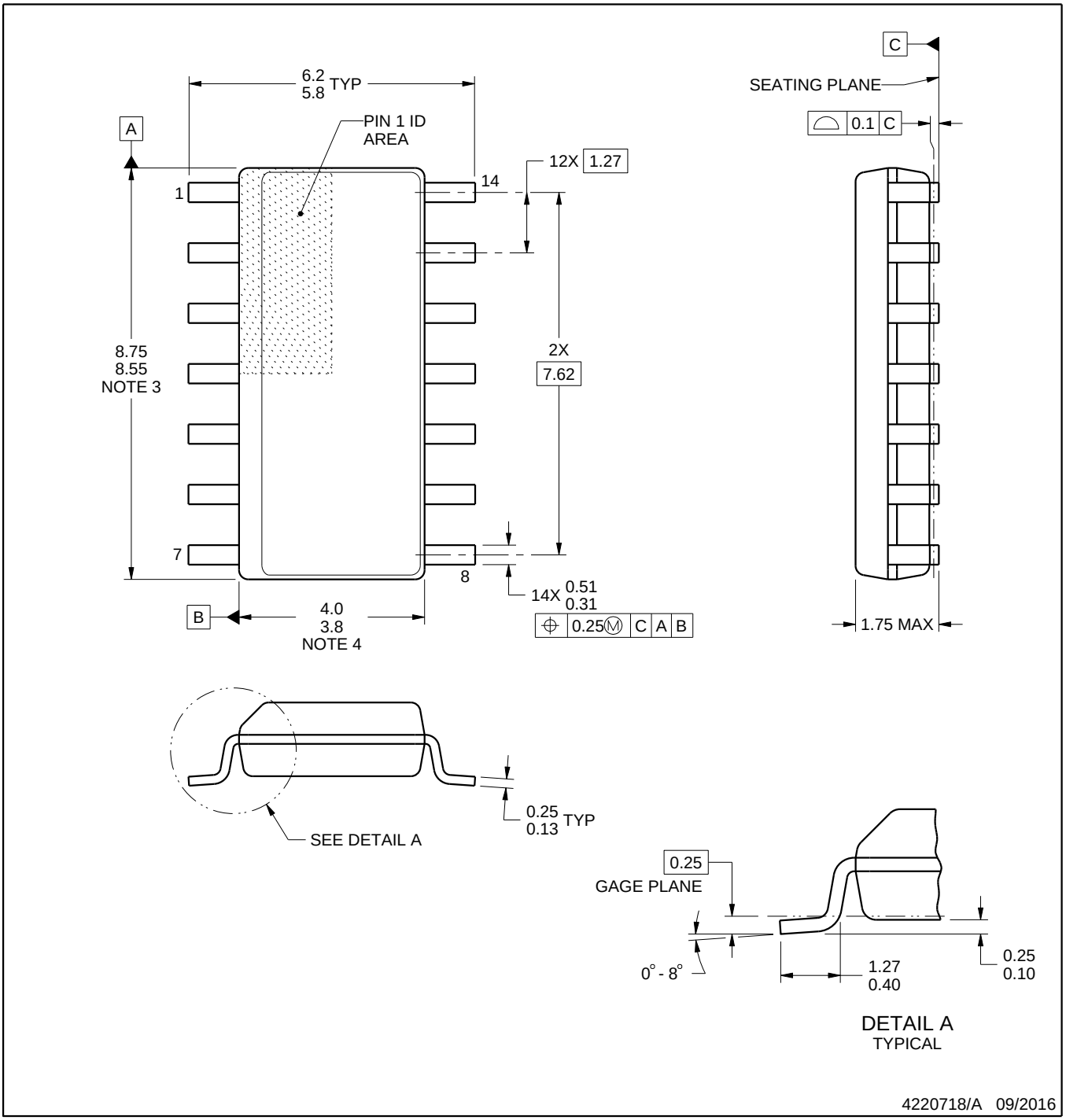


PACKAGE OUTLINE

D0014A

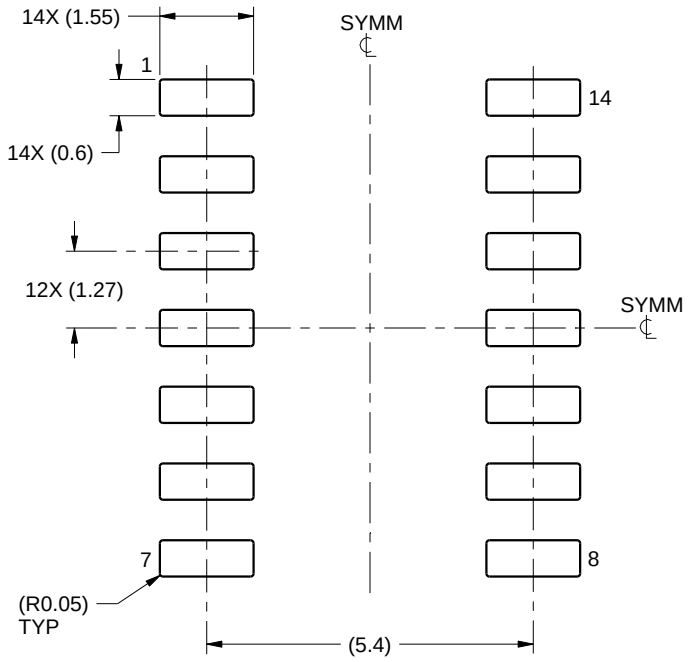
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

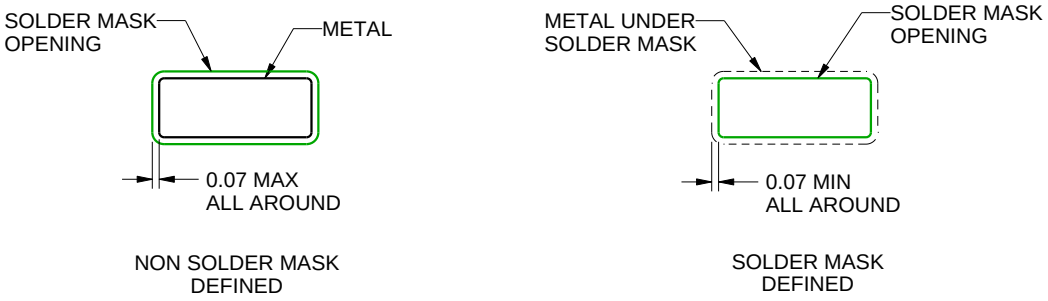


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

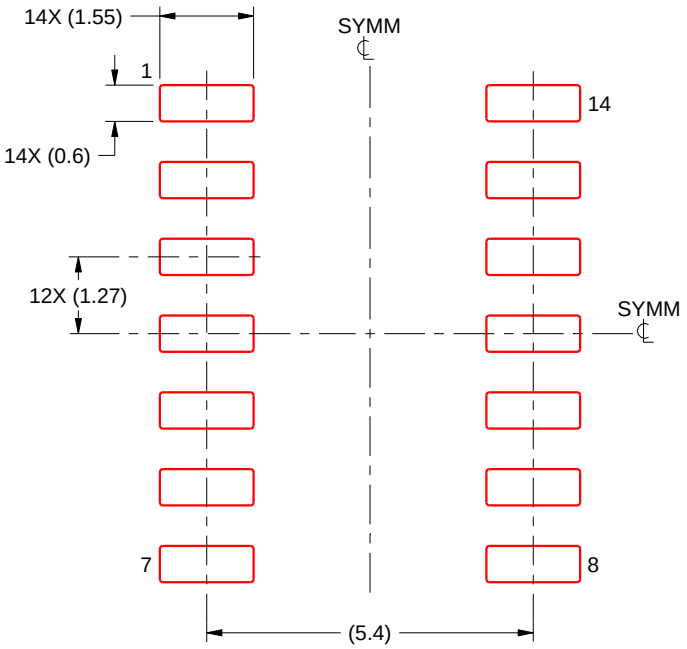
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

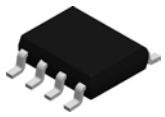


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

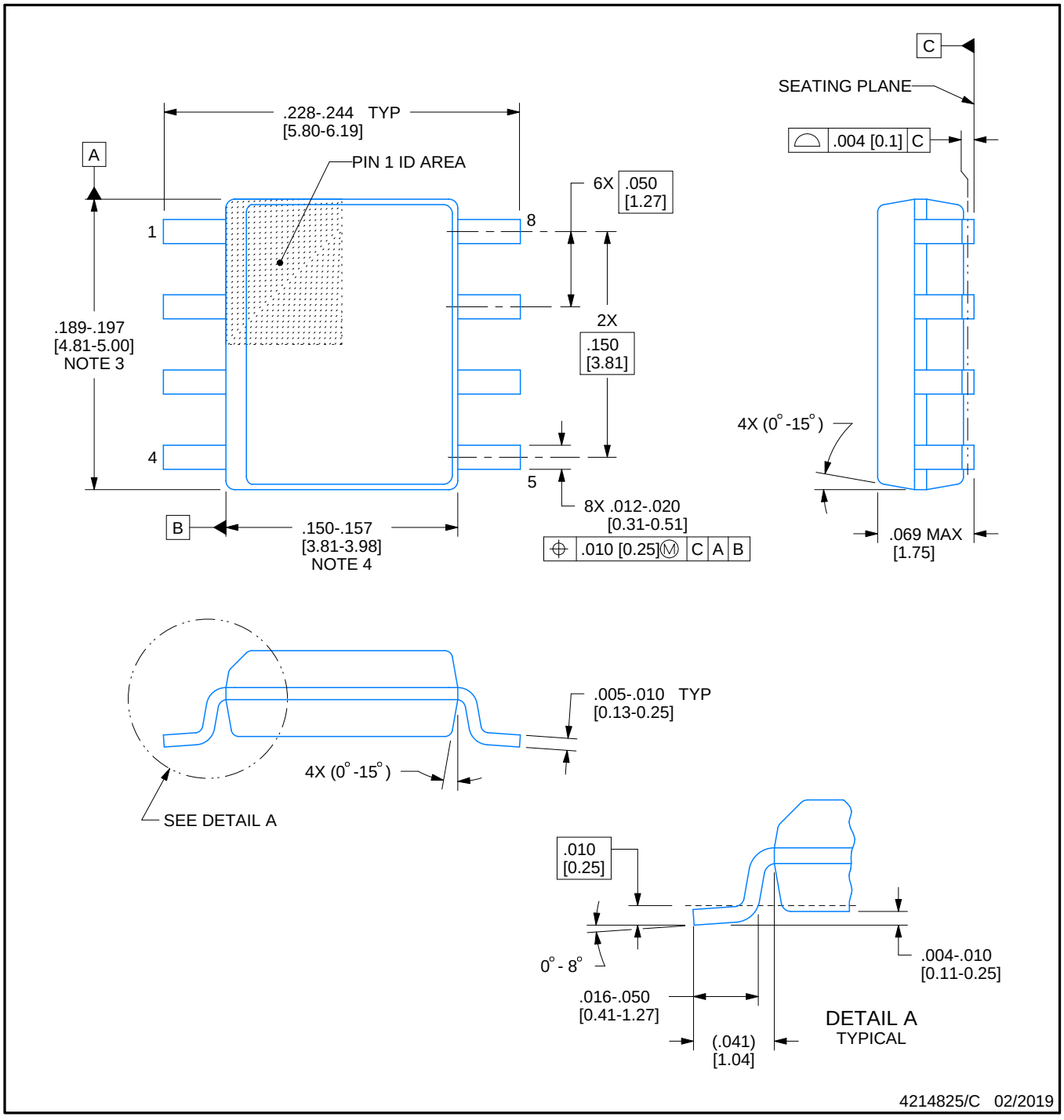


PACKAGE OUTLINE

D0008A

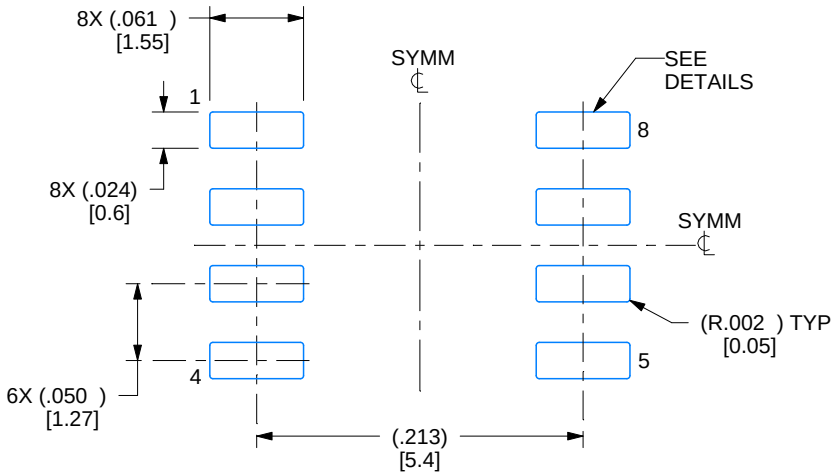
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

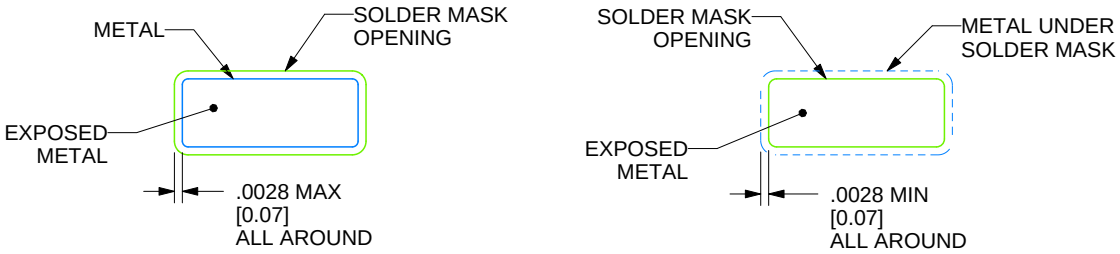


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

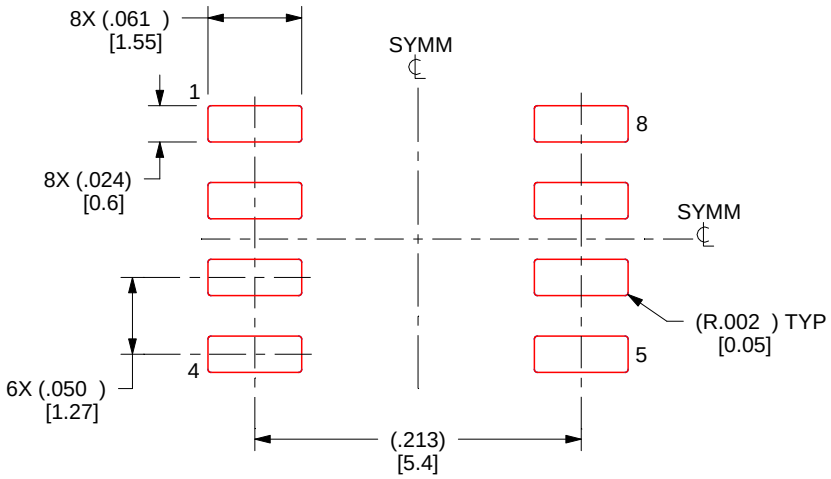
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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