MC121-Q1 Automotive 40V, Single Phase BLDC Driver with Integrated Hall Sensor

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature Grade-1 : –40°C ≤ T_A ≤ 125°C
- N-channel H-bridge driver with internal Hall sensor
- $R_{DS(ON)}$: 850mΩ (HS+LS)
- Current rating
  - Configurable current limit up to 1.21A
  - 0.5A rms (T_A = 105ºC, $R_{\theta JA}$ = 100 ºC/W)
- Integrated supply (VM) clamp
- Configurable speed curve and starting duty cycle
- Commutation schemes: square or soft (up to 90º)
  - Square: maximum torque/speed
  - Soft: optimized speed and acoustics
- Configurable speed reference input: PWM or DC
  - Input PWM frequency range: 20 Hz to 90 kHz
  - Input DC voltage range: (0-3)V
- Configurable output PWM frequency: 25 or 50kHz
- Closed loop speed control accuracy: ±3%
- PWM dithering to reduce EMI
- Configurable soft start time
- Configurable hall offset angle and time
- Speed output with 0.5x, 1x, 2/3x, or 2x multipliers
- Rotor lock detection output (RD)
- Configurable PWM modes
  - Synchronous, asynchronous and hybrid
- Auto-demag for high efficiency across speed
- One-time programming (2 pages) over I^2C
- Protection features
  - Overcurrent protection for short between VM/GND and OUTx
  - Locked rotor protection (LRP) with auto-restart
  - VM undervoltage lockout (UVLO)
  - VM overvoltage protection (OVP)
  - Thermal shutdown (TSD)
  - Configurable fault retry time
- Functional features (Opeartion continues)
  - when short between FG/RD and GND
  - 100% input during short between PWM/DC and VM

2 Applications

- LED headlamp cooling fans
- Infotainment cooling fans
- ADAS and ECU/sensor cooling fans
- Wireless charger cooling fans

3 Description

The MC121-Q1 is a 40V, 850mΩ rated motor driver with integrated N-channel full-bridge, charge pump, Hall sensor, commutation control logic, and protection circuitry for single phase brushless DC motors. The Hall sensor provides rotor position information to the commutation logic to maintain continuous rotor motion. The commutation logic can be programmed for square and soft PWM waveforms to reduce acoustic noise or maximize speed/efficiency.

The duty cycle of a pulse-width modulated signal or a (0-3)V DC voltage on the PWM/DC pin controls the motor speed. FG/RD pin can be configured to report the motor speed or a locked rotor condition to an external controller. The PWM/DC and FG/RD pins can be temporarily configured as an I^2C interface to support a programming (OTP) mode to configure the OTP during production.

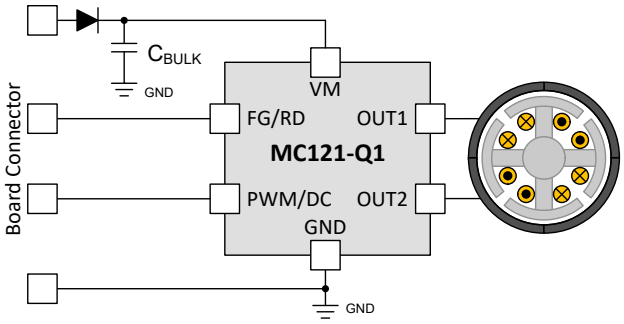
The MC121-Q1 integrates protection features for motor and device protection. These include supply undervoltage lockout, overvoltage protection, output overcurrent protection, device overtemperature shutdown, and locked rotor protection.

The MC121-Q1 is available in two 6-pin packages: SOT23-FL and X2SON. SOT23-FL is a flat lead package with a maximum height of 1.1mm. X2SON is a non-leaded package with a max. height of 0.4mm.

Packaging Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
MC121QDEZRQ1	X2SON (6)	2.50 mm x 2.00 mm
MC121QDYMRQ1	SOT23 (6)	3.80 mm x 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Pin Configuration and Functions

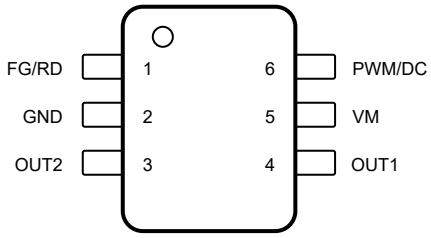

Figure 4-1. MC121-Q1, 6-Pin SOT-23, Top View

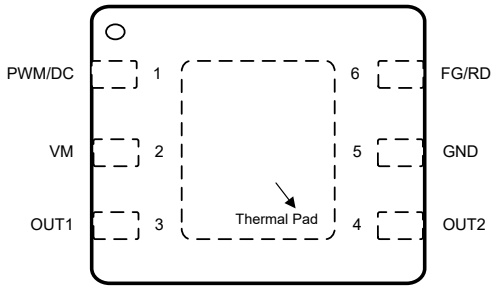

Figure 4-2. MC121-Q1, 6-Pin X2SON, Top View

Table 4-1. Pin Functions

PIN	PACKAGE		TYPE[1]	DESCRIPTION
NAME	SOT-23	X2SON		
FG/RD	1	6	O	Motor speed or rotor lock indicator output. Open-drain output that requires an external pull-up resistor to desired logic-high voltage. In test/programming mode, this pin becomes the SDA pin for I^2C interface.
GND	2	5	G	Device ground. Connect to system ground.
OUT1	4	3	O	Half-bridge output. Connect to motor winding.
OUT2	3	4	O	Half-bridge output. Connect to motor winding.
VM	5	2	P	Device and motor power supply. Connect to motor supply voltage; bypass to GND with one 0.1-µF capacitor and one bulk capacitor. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
PWM/DC	6	1	I	Motor speed control pin - can take a PWM or DC signal. This pin is internally pulled up to 100% duty cycle input when left floating in PWM input mode (PWMDC_MODE = 0x0). In test/programming mode, this pin becomes the SCL pin for I^2C interface.
Thermal pad			G	Must be connected to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = no connect.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.5	VM_{CLAMP}	V
Power supply transient voltage ramp	VM	0	2	V/µs
Logic pin voltage	PWM/DC	-0.5	VM + 0.5	V
Open drain pin voltage	FG/RD	-0.5	VM + 0.5	V
Output pin voltage	OUTx	-1	VM + 1	V
Peak Output Current (OUTx)	OUTx		1.44	A
Open drain output current	FG/RD		25	mA
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings Auto

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 3A	±6000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C3	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	VM	3.2		35	V
V_{IN}	Logic input voltage	PWM/DC (when configured in PWM mode)	0		VM	V
V_{IN}	Analog input voltage	PWM/DC (when configured in DC mode)	0		3.2	V
f_{PWM_IN}	PWM frequency	PWM	0.02		90	kHz
V_{OD}	Open drain pullup voltage	FG/RD	0		VM	V
I_{OD}	Open drain output current	FG/RD			20	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

5.4 Thermal Information

THERMAL METRIC(1)		MC121-Q1 SOT23 (DYM) 6 PINS	MC121-Q1 X2SON (DEZ) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	156.1	74.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.1	39.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.6	45.3	°C/W

THERMAL METRIC(1)		MC121-Q1 SOT23 (DYM) 6 PINS	MC121-Q1 X2SON (DEZ) 6 PINS	UNIT
Ψ_{JT}	Junction-to-top characterization parameter	10.1	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.5	45.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	16.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

MC121-Q1: 3.2V ≤ V_{VM} ≤ 35V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)
Typical values are at T_J = 25°C and V_{VM} = 12V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM)						
I_{VMQ}	VM sleep mode current	$V_{PWM/DC}$ = 0V, SLEEP_EN = 0x1		0.08	0.14	mA
I_{VM}	VM active mode current	$V_{PWM/DC}$ = 3V (PWMDC_MODE = 0x1) or floating (PWM_DC = 0x0), no load across OUTx		3.9	5	mA
t_{WAKE}	Turn-on time from standby/sleep mode	Time taken from PWM duty = 0% to 100% to OUTx switching, PWM input (PWMDC_MODE = 0x0), PWM_IN_RANGE = 0x0			16	ms
		Time taken from PWM duty = 0% to 100% to OUTx switching, PWM input (PWMDC_MODE = 0x0), PWM_IN_RANGE = 0x1			64	ms
	Turn-on time from standby/sleep mode	Time taken from DC input = 0V to 3V to OUTx switching, DC input (PWMDC_MODE = 0x1)			1	ms
t_{STOP_DET}	Time taken to detect DIN = 0%	Time take from PWM duty = 100% to 0% to initiate motor stop as per RAMP_ON_STOP_DIS, PWM input (PWMDC_MODE = 0x0, PWM_IN_RANGE = 0x0)			16	ms
		Time take from PWM duty = 100% to 0% to initiate motor stop as per RAMP_ON_STOP_DIS, PWM input (PWMDC_MODE = 0x0, PWM_IN_RANGE = 0x1)			64	ms
	Time taken to detect DIN = 0%	Time take from DC input = 3V to 0V to initiate motor stop as per RAMP_ON_STOP_DIS, DC input (PWMDC_MODE =0x1)			1.3	ms
PWM/DC (SCL) and FG (SDA)						
V_{IL}	Input logic low voltage	PWM/DC pin in PWM input mode (PWMDC_MODE =0x0) during active or standby state or SCL mode, FG pin in SDA mode			0.8	V
V_{IH}	Input logic high voltage		2			V
V_{HYS}	Input hysteresis		0.15	0.2	0.26	V
V_{SLEEP_DC}	Voltage threshold on PWM/DC pin for sleep entry in DC input mode	Voltage applied on PWM/DC pin, SLEEP_EN = 0x1, PWMDC_MODE = 0x1	0		0.1	V

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Typical values are at T_J = 25°C and V_{VM} = 12V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL} (PWM/DC)	Input logic low current	V_I = 0V, SLEEP_EN = 0x0, PWM/DC pin in PWM input mode (PWMDC_MODE = 0x0) or SCL mode	225	245	265	µA
		V_I = 0V, SLEEP_EN = 0x0, PWM/DC pin in DC input mode (PWMDC_MODE = 0x1)			1	µA
		V_I = 0V, SLEEP_EN = 0x1, PWM/DC pin in PWM input mode (PWMDC_MODE = 0x0) or DC input mode (PWMDC_MODE = 0x1) or SCL mode	20	50	70	µA
I_{IH} (PWM/DC)	Input logic high current	V_I = 3.3V, PWM/DC pin in PWM input mode (PWMDC_MODE = 0x0) or DC input mode (PWMDC_MODE = 0x1) or SCL mode	-1		0	µA
		V_I = V_{VM}, PWM/DC pin in PWM input mode (PWMDC_MODE = 0x0) or DC input mode (PWMDC_MODE = 0x1) or SCL mode	-1		0	µA
V_{PU} (PWM/DC)	Internal pull-up voltage	PWM input mode (PWMDC_MODE = 0x0), VM ≥ 3.6V	2.7	2.9	3.2	V
		PWM input mode (PWMDC_MODE = 0x0), VM < 3.6V	2.55		VM	V
f_{PWM_IN}	Input PWM frequency range for duty/ speed reference	PWM input (PWMDC_MODE = 0x0), PWM_IN_RANGE = 0x0	0.08		90	kHz
		PWM input (PWMDC_MODE = 0x0), PWM_IN_RANGE = 0x1	0.02		22	kHz
V_{PWM_ACC}	Duty/speed reference accuracy from PWM input	20Hz ≤ f_{PWM_IN} ≤ 45kHz			0.4	%
		45kHz < f_{PWM_IN} ≤ 90kHz			0.8	%
V_{DC}	DC input range for duty/speed reference	DC input (PWMDC_MODE = 0x1), 3.2V ≤ VM < 4.5V	0		VM - 1.4	V
		DC input (PWMDC_MODE = 0x1), 4.5V ≤ VM ≤ 35V	0		3.1	V
$V_{DC\_DIN\_0\%}$	DC input threshold for 0% duty/speed reference (DIN = 0%)	DC input (PWMDC_MODE = 0x1)			0.1	V
$V_{DC\_DIN\_100\%}$	DC input threshold for 100% duty/speed reference (DIN = 100%)	DC input (PWMDC_MODE = 0x1), 3.2V ≤ VM < 4.5V	VM - 1.4		3.2	V
		DC input (PWMDC_MODE = 0x1), 4.5V ≤ VM ≤ 35V	2.9	3	3.2	V
V_{DC_ACC}	Duty/speed reference accuracy from DC input	DC input (PWMDC_MODE = 0x1), 4.5V ≤ VM ≤ 35V			3	%
V_{OL} (FG)	Output logic low voltage	I_{OD} = 20mA			0.4	V
I_{OZ} (FG)	Output logic high current	V_{OD} = 3.3V	-1		1	µA
I_{OZ} (FG)	Output logic high current	V_{OD} = VM	-1		1	µA
DRIVER OUTPUTS (OUTx)						
$R_{DS(on)}$ (H+L)	High-side+Low-side MOSFET on resistance	V_{VM} = 3.2V, I_O = 500mA, T_A = 25°C		0.85	1.02	Ω
$R_{DS(on)}$ (H+L)	High-side+Low-side MOSFET on resistance	V_{VM} = 12V, I_O = 500mA, T_A = 25°C		0.8	0.95	Ω
$R_{DS(on)}$ (H+L)	High-side+Low-side MOSFET on resistance	V_{VM} = 12V, I_O = 500mA, T_A = 150°C		1.3	1.5	Ω
f_{PWM_OUT}	PWM output frequency	PWM_OUT_FREQ = 0x0, DITHER_EN = 0x0	23.5	25	26.25	kHz

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Typical values are at T_J = 25°C and V_{VM} = 12V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM_OUT}	PWM output frequency	PWM_OUT_FREQ = 0x1, DITHER_EN = 0x0	45	50	55	kHz
DIGITAL-LATCH HALL EFFECT SENSOR						
B_{OP}	Operate point		0.4	0.8	1.6	mT
B_{RP}	Release point		-1.6	-0.7	-0.4	mT
B_{HYS}	Hysteresis; $B_{HYS} = (B_{OP} – B_{RP})$		1.2	1.6	3.2	mT
B_{OF}	Magnetic offset; $B_{OF} = (B_{OP} + B_{RP}) / 2$		-1	0	1	mT
OSCILLATOR						
f_{osc}	Internal oscillator frequency	V_{VM} = 12V, T_J = 25ºC	24.625	25	25.375	MHz
f_{osc}	Internal oscillator frequency		24.25	25	25.75	MHz
DUTY CURVE						
D_{OUT_RES}	Output duty cycle resolution per LSB	Measured at 50% voltage level, 0.4% ≤ DOUT ≤ 99.6%		0.4		%
D_{HYS}	Speed curve hysteresis for rising D_{IN}	DIN_HYS = 0x0. Sweep DIN from 0% to DIN0+DIN_HYS. Output DOUT changes from DOUT0 to target duty cycle.		0		%
		DIN_HYS = 0x1. Sweep DIN from 0% to DIN0+DIN_HYS. Output DOUT changes from DOUT0 to target duty cycle.		1.2		%
		DIN_HYS = 0x2. Sweep DIN from 0% to DIN0+DIN_HYS. Output DOUT changes from DOUT0 to target duty cycle.		2.4		%
		DIN_HYS = 0x3. Sweep DIN from 0% to DIN0+DIN_HYS. Output DOUT changes from DOUT0 to target duty cycle.		4.8		%
$SPEED_{ERR}$	Closed loop speed accuracy	T_J = 25ºC, SPEED_LOOP_EN = 0x1, 12.5% x MAX_SPEED ≤ SPEED_REF ≤ MAX_SPEED	-1		1	%
		SPEED_LOOP_EN = 0x1, 12.5% x MAX_SPEED ≤ SPEED_REF ≤ MAX_SPEED	-3		3	%
COMMUTATION						
$\theta_{HALL\_OS\_ANGLE}$	Minimum Hall offset angle	HALL_OS_ANGLE = 0x00		0		deg
	Maximum Hall offset angle	HALL_OS_ANGLE = 0x1F		43.8		deg
$\theta_{HALL\_OS\_ANGLE\_LSB}$	Hall offset angle resolution per LSB	HALL_OS_ANGLE LSB		1.4		deg
t_{HALL_OS}	Minimum Hall offset signal lead/lag time	HALL_OS_TIME = 0x00		0		µs
	Maximum Hall offset signal lead/lag time	HALL_OS_TIME = 0xFF		2.55		ms
$t_{HALL\_OS\_LSB}$	Hall offset signal lead/lag time resolution per LSB	HALL_OS_TIME LSB		10		µs
t_{DEMAG}	Minimum time for demagnetization period	DEMAG_TIME = 0x00		0		µs
	Maximum time for demagnetization period	DEMAG_TIME = 0x20		1.29		ms
t_{DEMAG_LSB}	DEMAG_TIME time resolution per LSB	DEMAG_TIME LSB		10.24		µs
θ_{SRISE}	Minimum angle for soft rise	SRISE = 0x00		2.8		deg
	Maximum angle for soft rise	SRISE = 0x10		90		deg
θ_{SRISE_LSB}	SRISE angle resolution per LSB	SRISE LSB		2.8		deg
θ_{SFALL}	Minimum angle for soft fall	SFALL = 0x00		2.8		deg
	Maximum angle for soft fall	SFALL = 0x1F		90		deg

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Typical values are at T_J = 25°C and V_{VM} = 12V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{SFALL_LSB}	SFALL angle resolution per LSB	SRISE LSB		2.8		deg
PRESTART AND PWM RAMP/SOFT START						
PWM_RAMP_RATE	Output duty cycle ramp rate for soft start and speed changes	PWM_RAMP_SEL = 0x0 (1.3s for 0 to 100%)		77		%/s
		PWM_RAMP_SEL = 0x1 (2.6s for 0 to 100%)		38.5		%/s
		PWM_RAMP_SEL = 0x2 (5.2s for 0 to 100%)		19.2		%/s
		PWM_RAMP_SEL = 0x3 (10.4s for 0 to 100%)		9.6		%/s
PROTECTION CIRCUITS						
VM_{CLAMP}	VM clamping voltage	I_{clamp} = 20mA	37		43	V
VM_{POR}	VM power on reset threshold to power-up the device	Supply rising	2.3	2.55	2.7	V
VM_{POR_HYS}	VM power on reset threshold hysteresis	Rising to falling threshold	0.04	0.09	0.13	V
V_{UVLO}	Supply undervoltage lockout threshold to start/stop driving the motor	Supply rising (UVLO_SEL = 0x0)	2.85	3	3.15	V
		Supply falling (UVLO_SEL = 0x0)	2.55	2.7	2.85	V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold (UVLO_SEL = 0x0)		0.3		V
V_{UVLO}	Supply undervoltage lockout threshold to start/stop driving the motor	Supply rising (UVLO_SEL = 0x1)	3.97	4.2	4.5	V
		Supply falling (UVLO_SEL = 0x1)	2.55	2.7	2.85	V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold (UVLO_SEL = 0x1)		1.5		V
V_{UVLO}	Supply undervoltage lockout threshold to start/stop driving the motor	Supply rising (UVLO_SEL = 0x2)	5.42	5.7	6	V
		Supply falling (UVLO_SEL = 0x2)	2.55	2.7	2.85	V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold (UVLO_SEL = 0x2)		3		V
V_{UVLO}	Supply undervoltage lockout threshold to start/stop driving the motor	Supply rising (UVLO_SEL = 0x3)	7.2	7.6	8	V
		Supply falling (UVLO_SEL = 0x3)	2.55	2.7	2.85	V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold (UVLO_SEL = 0x3)		4.9		V
V_{OVP}	Supply overvoltage lockout (OVP)	Supply rising (OVP_SEL = 0x0)	32.7	34.5	36.3	V
V_{OVP}	Supply overvoltage lockout (OVP)	Supply falling (OVP_SEL = 0x0)	31.4	33.2	34.9	V
V_{OVP}	Supply overvoltage lockout (OVP)	Supply rising (OVP_SEL = 0x1)	21.5	22.7	23.9	V
V_{OVP}	Supply overvoltage lockout (OVP)	Supply falling (OVP_SEL = 0x1)	20.1	21.2	22.3	V
V_{OVP}	Supply overvoltage lockout (OVP)	Supply rising (OVP_SEL = 0x2)	17.5	18.4	19.3	V
V_{OVP}	Supply overvoltage lockout (OVP)	Supply falling (OVP_SEL = 0x2)	15.9	16.9	17.9	V
V_{OVP_HYS}	Supply overvoltage hysteresis			1.5		V
t_{OVP_DEG}	Supply overvoltage deglitch time		70	80	90	µs
t_{OVP_BLANK}	Supply overvoltage blanking time	OVP_BLANK_EN = 0x1, OVP_BLANK_TIME = 0x0		1		ms
		OVP_BLANK_EN = 0x1, OVP_BLANK_TIME = 0x1		4		ms

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Typical values are at T_J = 25°C and V_{VM} = 12V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIMIT}	Current limit threshold	ILIMIT_SEL = 0x0	0.29	0.32	0.37	A
		ILIMIT_SEL = 0x1	0.38	0.43	0.49	A
		ILIMIT_SEL = 0x2	0.48	0.53	0.61	A
		ILIMIT_SEL = 0x3	0.58	0.63	0.73	A
		ILIMIT_SEL = 0x4	0.67	0.73	0.85	A
		ILIMIT_SEL = 0x5	0.76	0.83	0.97	A
		ILIMIT_SEL = 0x6	0.85	0.94	1.09	A
		ILIMIT_SEL = 0x7	0.94	1.03	1.21	A
		ILIMIT_SEL = 0x8	1.03	1.12	1.33	A
		ILIMIT_SEL = 0x9	1.11	1.21	1.44	A
t_{ILIMIT_BLANK}	Current limit blanking time (applied from most recent rising edge PWM (FET) signal)	ILIM_BLANK_SEL = 0x0		0.5		µs
		ILIM_BLANK_SEL = 0x1		1		µs
t_{ILIMIT_DEG}	Current limit deglitch time	ILIM_DEGLITCH_SEL = 0x0		0.6		µs
	Current limit deglitch time	ILIM_DEGLITCH_SEL = 0x1		1.1		µs
I_{OCP}	Overcurrent protection trip point (HS_FET)		1.3 * I_{LIMIT}	1.7 * I_{LIMIT}	2.2 * I_{LIMIT}	A
I_{OCP}	Overcurrent protection trip point (LS_FET)		1.5 * I_{LIMIT}	1.7 * I_{LIMIT}	1.85 * I_{LIMIT}	A
t_{OCP_DEG}	Overcurrent protection deglitch time			0.6		µs
t_{LRD_START}	Locked rotor detection time at start-up	LRD_TIME_STARTUP = 0x0	0.31	0.32	0.34	s
		LRD_TIME_STARTUP = 0x1	0.42	0.44	0.46	s
		LRD_TIME_STARTUP = 0x2	0.5	0.52	0.55	s
		LRD_TIME_STARTUP = 0x3	1	1.05	1.1	s
N_{RETRY}	Long retry time ratio for locked rotor and overcurrent. Long retry time = N_{RETRY} x t_{LRD_START}	LRD_LONG_RETRY_SEL = 0x0		2		
		LRD_LONG_RETRY_SEL = 0x1		4		
		LRD_LONG_RETRY_SEL = 0x2		8		
		LRD_LONG_RETRY_SEL = 0x3		10		
		LRD_LONG_RETRY_SEL = 0x4		12		
		LRD_LONG_RETRY_SEL = 0x5		16		
		LRD_LONG_RETRY_SEL = 0x6		24		
		LRD_LONG_RETRY_SEL = 0x7		28		
t_{LRD_RUN}	Locked rotor detection time at start-up	Locked rotor during motor run	0.29	0.32	0.35	s
T_{TSD}	Thermal shutdown temperature		155	170	185	°C
T_{HYS}	Thermal shutdown hysteresis			24		°C

5.6 I2C Timing Requirements

		MIN	NOM	MAX	UNIT
STANDARD MODE					
f_{SCL}	SCL Clock frequency	0		100	kHz
$t_{HD,STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4			µs
t_{LOW}	LOW period of the SCL clock	4.7			µs
t_{HIGH}	HIGH period of the SCL clock	4			µs
$t_{SU,STA}$	Setup time for a repeated START condition	4.7			µs

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		MIN	NOM	MAX	UNIT
$t_{HD,DAT}$	Data hold time: For I2C bus devices	0.01		3.45	µs
$t_{SU,DAT}$	Data set-up time	250			ns
t_R	SDA and SCL rise time			1000	ns
t_F	SDA and SCL fall time			300	ns
$t_{SU,STO}$	Set-up time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
FAST MODE					
f_{SCL}	SCL Clock frequency	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
$t_{SU,STA}$	Setup time for a repeated START condition	0.6			µs
$t_{HD,DAT}$	Data hold time: For I2C bus devices	0.01		0.9	µs
$t_{SU,DAT}$	Data set-up time	50			ns
t_R	SDA and SCL rise time			300	ns
t_F	SDA and SCL fall time			300	ns
$t_{SU,STO}$	Set-up time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{SP}	Pulse width of spikes to be supressed by input noise filter		50		ns

5.7 Timing Diagrams

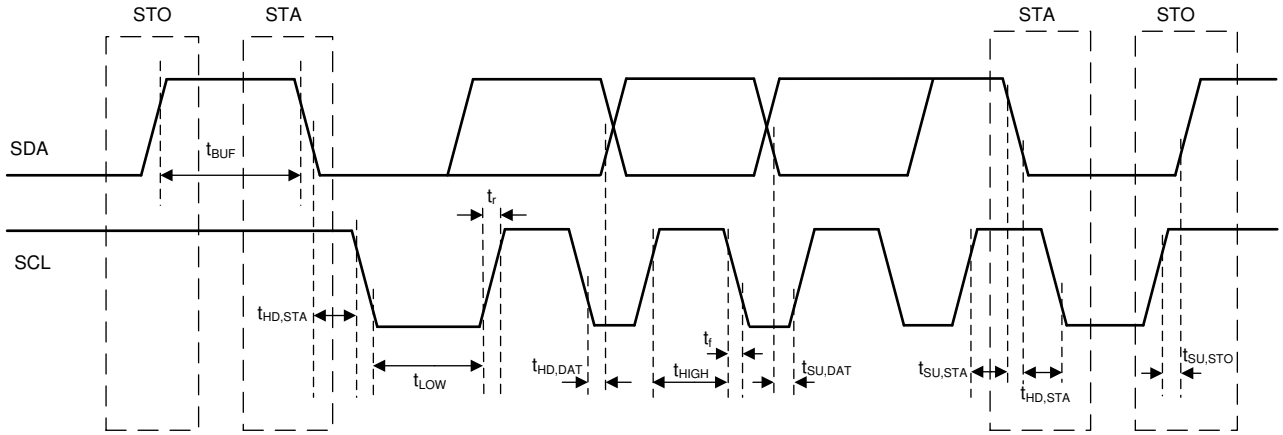

Figure 5-1. I²C Timing Diagram

6 Detailed Description

6.1 Overview

The MC121-Q1 is a 40V, 850mΩ rated, 1.25A peak, single phase BLDC motor driver with integrated N-channel full-bridge FETs, charge pump, Hall sensor, commutation control logic, and protection circuitry. The Hall sensor provides rotor position information to the commutation logic to maintain continuous rotor motion. The commutation logic can be programmed for square and soft PWM waveforms to reduce acoustic noise or maximize speed/efficiency.

6.2 Functional Block Diagram

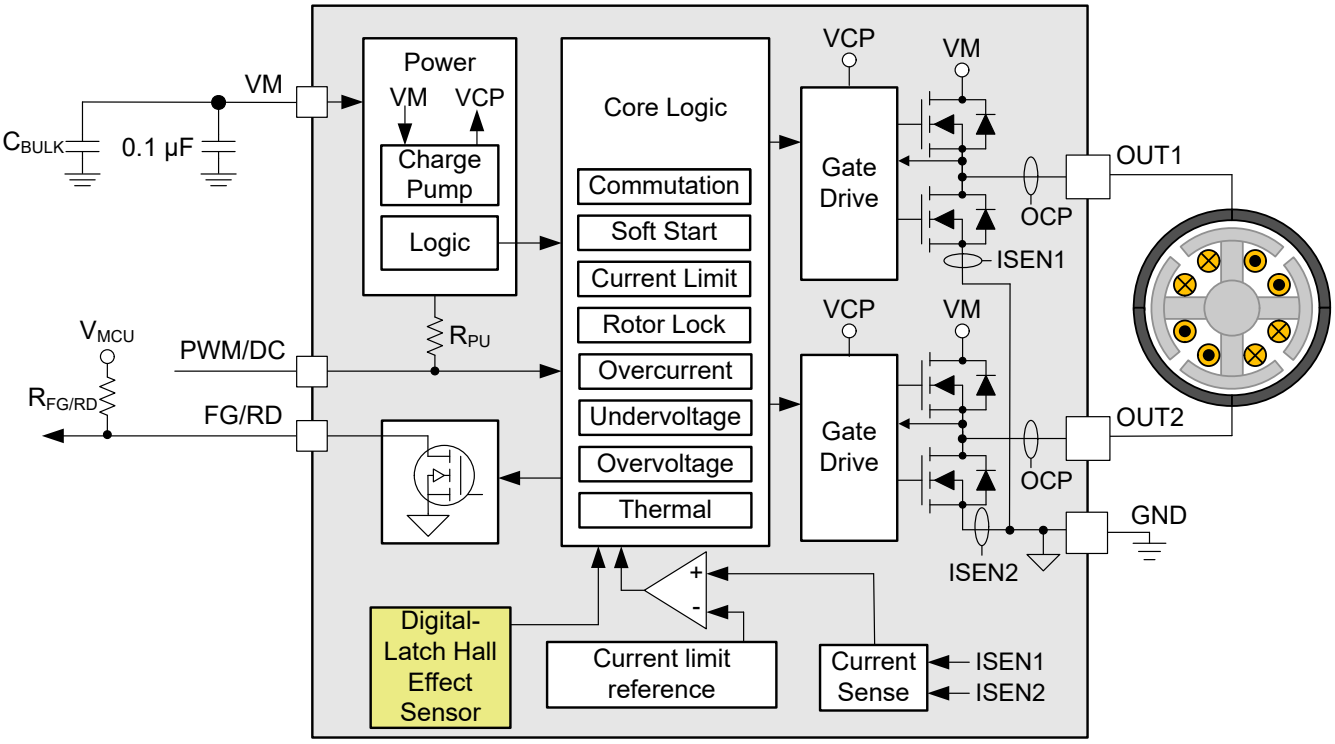

Figure 6-1. MC121-Q1 Functional Block Diagram

6.3 Feature Description

6.3.1 Motor Control

MC121-Q1 accepts a pulse-width modulated (PWM) or a DC (analog) input on the PWM/DC pin to control the motor speed. The MC121-Q1 provides a configurable duty curve to map the input duty (DIN in Figure 6-2) to a user configured target output duty cycle (DOUT_TARGET in Figure 6-2). The MC121-Q1 also provides a user configurable duty ramp to smoothly increase/decrease the output duty cycle (DOUT in Figure 6-2) to reach DOUT_TARGET. The MC121-Q1 supports both open-loop (duty cycle) and closed-loop (speed) control. In open-loop (duty cycle) control, the applied duty cycle is directly set by DOUT while in closed-loop (speed) control, the applied duty cycle is set by the speed loop. An integrated digital-latch Hall sensor provides rotor position and timing information to the commutation algorithm. The MC121-Q1 supports square and output PWM waveshaping schemes to optimize between efficiency/motor speed and acoustic noise. The MC121-Q1 provides synchronous, asynchronous, and hybrid output PWM modulation modes on the H-bridge. Configurable hall lead/lag angle and time adjustment is available to improve the efficiency across both lower and higher speeds. In addition, MC121-Q1 provides a configurable demagnetization (auto or manual) feature to reduce the motor winding current to zero before a commutation to minimize the DC bus (VM) voltage spike, acoustic noise and improve efficiency.

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Figure 6-2 shows the motor control block diagram of MC121-Q1.

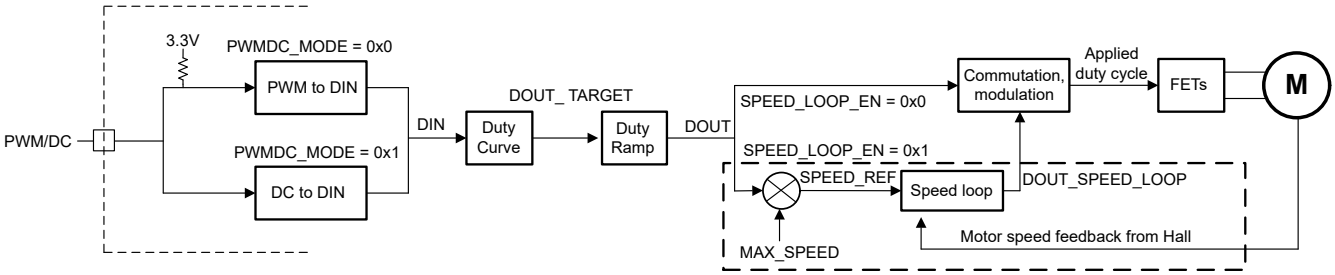

Figure 6-2. MC121-Q1 Motor Control Block Diagram

6.3.1.1 Duty Input

MC121-Q1 receives the duty input (DIN) from the PWM/DC pin. The PWM/DC input can either be a PWM or DC (analog) signal and is selected by PWMDC_MODE bit. The input PWM frequency can range between 20 Hz and 90 kHz (input PWM frequency range configured by PWM_IN_RANGE bit), while the DC input can range between (0-3)V. The PWM/DC pin integrates a pull-up feature to set the duty input (DIN) to 100% when the pin is left floating/unconnected for applications that need only ON/OFF control.

Note

When PWRUP_PWMDC_MASK is set to 0x1, MC121-Q1 waits for 1s after power-up before reacting to duty input from PWM/DC pin. There is no wait time on power-up when PWRUP_PWMDC_MASK is set to 0x0.

6.3.1.2 Duty Curve

MC121-Q1 supports configurable duty curve as shown in Figure 6-3. This allows user to set the target output duty cycle (DOUT_TARGET) as a function of input duty (DIN) depending on the specific use-case enabling a single platform (MC121-Q1) BLDC driver designs for different end applications.

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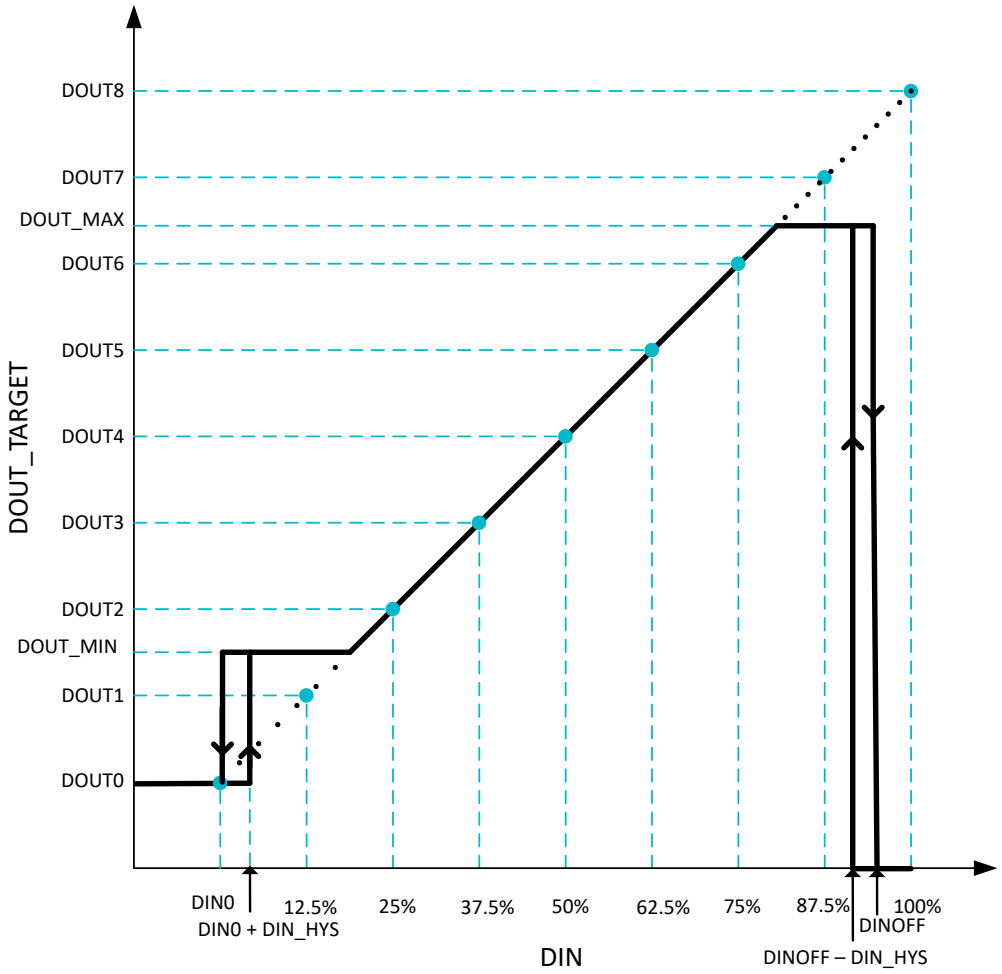

Figure 6-3. Duty Curve

The configurable points on the duty curve are as follows,

- **DIN0, DOUT0**: DIN0 can be used to set the minimum input (starting) duty cycle to start driving the motor - when STBY_EN = 0x1, motor is not driven till DIN ≥ (DIN0 + DINHYS). DINHYS sets the hysteresis around DIN0 to start/stop driving the motor. MC121-Q1 also provides the option of driving the motor even when DIN < DIN0 by setting STBY_EN to 0x0 and DOUT0 to a non-zero value. The device state when DIN = 0% is set by SLEEP_EN and STBY_EN bits as listed in Table 6-5.
- **DINOFF**: DINOFF sets the maximum input duty cycle (DIN) above which target output duty cycle (DOUT_TARGET) is set to zero to stop driving the motor, DOUT_TARGET = 0% when DIN ≥ DINOFF. The motor driving resumes when DIN < (DINOFF - DINHYS).
- **DOUT_MIN**: DOUT_MIN sets the minimum target output duty cycle (DOUT_TARGET) when DIN0 < DIN < DINOFF.
- **DOUT_MAX**: DOUT_MAX sets the maximum target output duty cycle (DOUT_TARGET) when DIN < DINOFF.
- **DOUTx**: DOUTx sets the output duty at fixed intervals of input duty. DOUT1 sets the target output duty at DIN = 12.5%, DOUT2 sets the target output duty at DIN = 25% and so forth such that DOUT8 sets the target output duty at DIN = 100% . DOUTx can be used to configure positive slope duty curve as shown in Duty Curve. DOUTx can be also used to configure negative slope as shown in Figure 6-4. DOUTx can also be used to configure mixed slope (positive, negative and zero) as shown in Figure 6-5.

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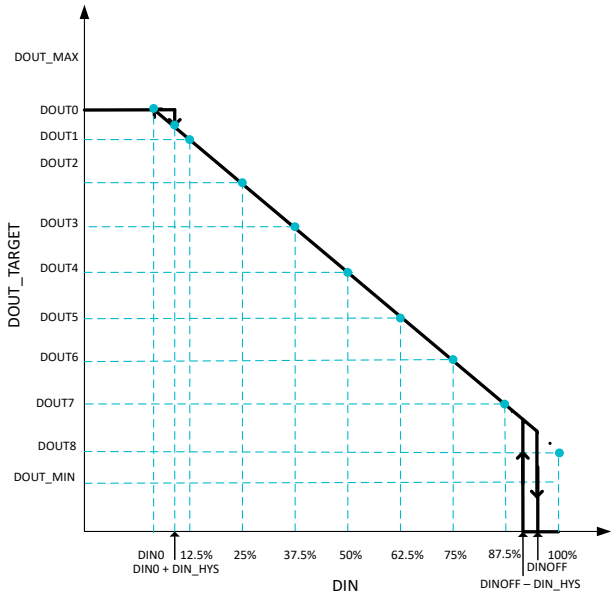

Figure 6-4. Duty Curve - Negative Slope

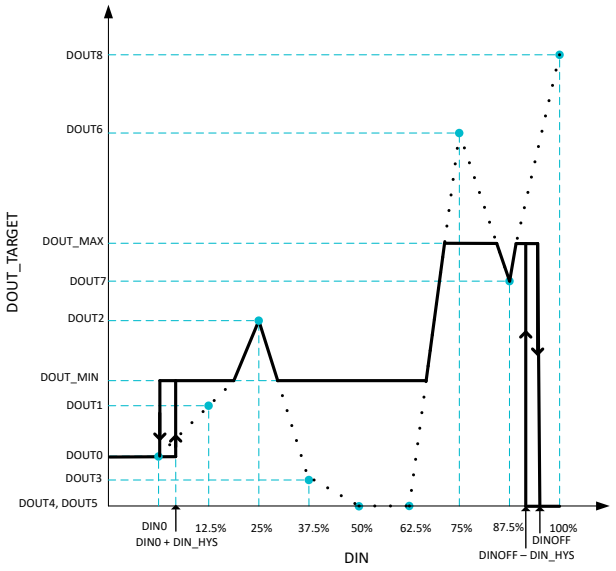

Figure 6-5. Duty Curve - Mixed Slope

6.3.1.3 Motor Start, Speed Change, and Stop

Motor Start

The MC121-Q1 implements a user configured two-slope ramp to reach the target output duty cycle (DOUT_TARGET in Figure 6-2) during motor start-up as shown in Figure 6-6. The two slope ramp (pre-start followed by soft start) enables a reliable start-up and reduces motor noise.

The MC121-Q1 enters the pre-start phase when the device exits standby mode, sleep mode, or fault mode. During the pre-start phase, the MC121-Q1 always uses square commutation to drive the motor. When PWM_RAMP_EN is set to 0x1, the output duty cycle (DOUT in Figure 6-2) increases linearly from starting duty cycle (DOUT_START x DOUT_MAX when speed loop is disabled and DOUT_START when speed loop is enabled) at the rate set by PWM_RAMP_SEL. When PWM_RAMP_EN is set to 0x0, then DOUT is updated directly by the DOUT_TARGET. The pre-start phase continues till four electrical cycles (eight Hall edges) are observed. When the fourth electrical cycle is completed, the device enters the soft start phase to ramp up DOUT to DOUT_TARGET; if DOUT has reached DOUT_TARGET by the end of pre-start phase, the soft start phase is skipped and device enters steady state directly. If the MC121-Q1 does not detect a Hall signal transition within t_{LRD}, the device enters the locked rotor protection fault state. During start-up sequence, locked rotor detection time (t_{LRD_START}) is user configured by LRD_TIME_STARTUP. During steady state, locked rotor detection time (t_{LRD_RUN}) is fixed at 320ms. Hall offset (angle and time) is disabled during the pre-start phase.

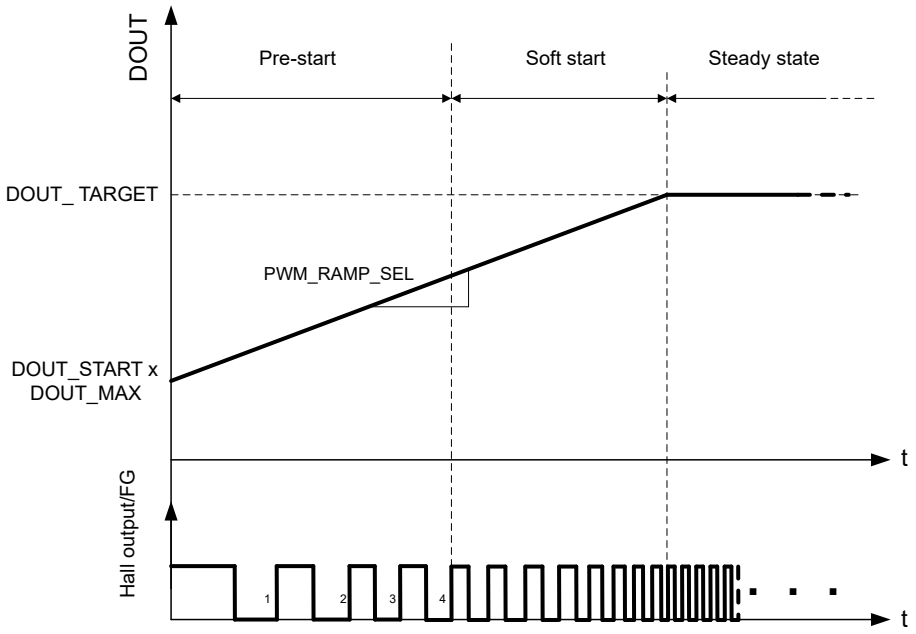

Figure 6-6. Output duty cycle during motor start

During the soft start phase, DOUT is ramped at the rate set by the PWM_RAMP_SEL. In this phase, Hall offset and demagnetization are applied and MC121-Q1 uses the commutation scheme set by the COMMUTATION_MODE, SRISE, and SFALL bits. The soft start phase ends when DOUT reaches output duty or speed target.

Speed Change

During motor operation, when DIN changes, the MC121-Q1 ramps the output duty cycle (DOUT in Figure 6-2) from previous target duty cycle (DOUT_TARGET_PREV) to the new target duty cycle (DOUT_TARGET) using user configured ramp rate. During acceleration (DOUT_TARGET > DOUT_TARGET_PREV), the ramp rate is set by PWM_RAMP_SEL and during deceleration (DOUT_TARGET < DOUT_TARGET_PREV), the ramp rate is either PWM_RAMP_SEL (when PWM_DECEL_SEL = 0x0) or 0.5 x PWM_RAMP_SEL (when PWM_DECEL_SEL = 0x1). PWM_DECEL_SEL = 0x1 provides a slower ramp during deceleration to avoid DC bus spikes due to regenerative energy push-back from motor. Figure 6-7 shows examples of DOUT increasing and decreasing according to PWM_RAMP_SEL.

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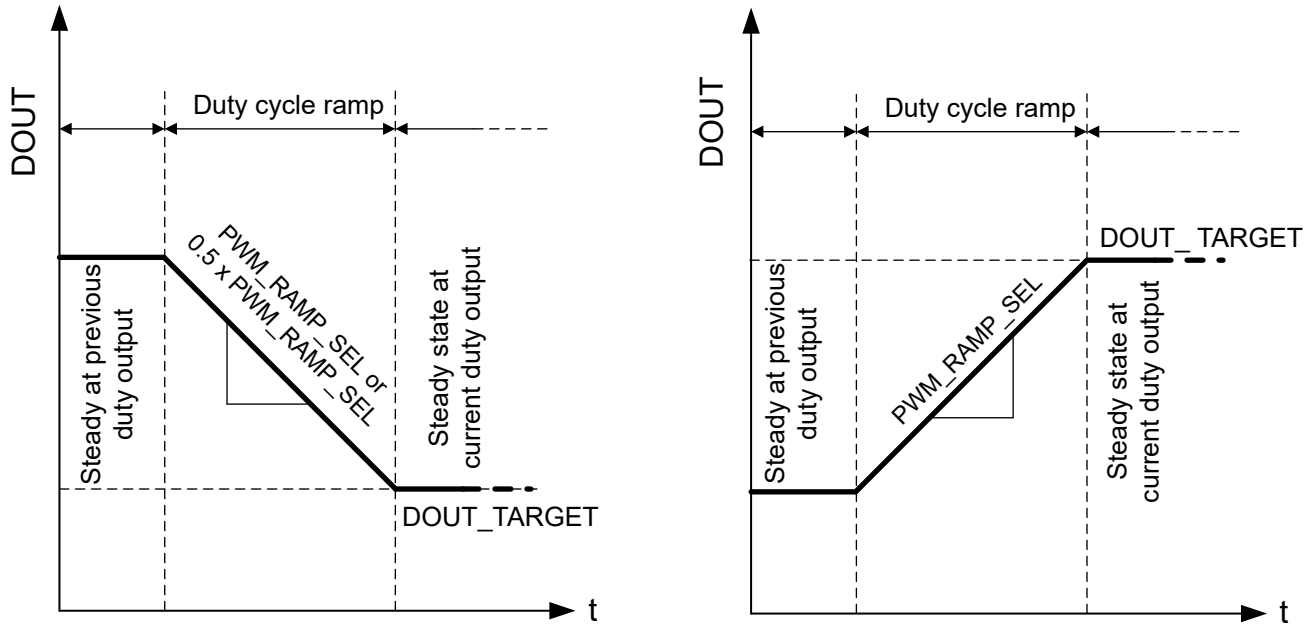

Figure 6-7. Duty Cycle Ramp

Stop

When a motor stop (DOUT_TARGET = 0%) is received, MC121-Q1 stops the motor based on RAMP_ON_STOP_DIS setting. When RAMP_ON_STOP_DIS is set to 0x1, all FETs are placed in Hi-Z on detecting motor stop (within t_{STOP_DET}). When RAMP_ON_STOP_DIS is set to 0x0, the device ramps down DOUT (at the rate set by PWM_DECEL_SEL) to zero followed by Hi-Z of all FETs. Once the FETs are in Hi-Z, depending on the STBY_EN and SLEEP_EN bits, MC121-Q1 continues in standby state or enters low-power sleep state. The motor stop sequence to enter sleep state when DIN is set to 0% as shown in Figure 6-8.

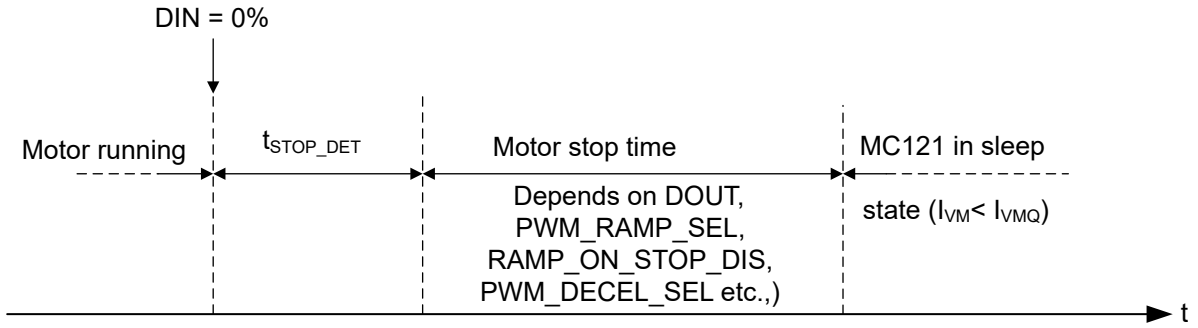

Figure 6-8. Sleep Entry Sequence when DIN is set to 0%

Note

Setting the PWM_RAMP_EN bit to 0x0 disables the duty cycle ramp. Disabling the duty cycle ramp results in a step change in the DOUT (when DIN changes), that can result in high motor phase currents or DC bus voltage spikes. TI recommends setting PWM_RAMP_EN to 0x1 to avoid any current or voltage spikes.

6.3.1.4 Open-Loop (Duty Cycle) Control

In open-loop control mode (SPEED_LOOP_EN set to 0x0), the input duty from the PWM/DC pin (DIN) and duty curve determine the peak output duty cycle of the commutation waveform (motor phase voltage applied

across OUTx pins), DOUT, as shown in Figure 6-9. The applied duty cycle to the H-bridge FETs depends on the commutation mode (COMMUTATION_MODE) and modulation mode (PWM_MODE) configurations.

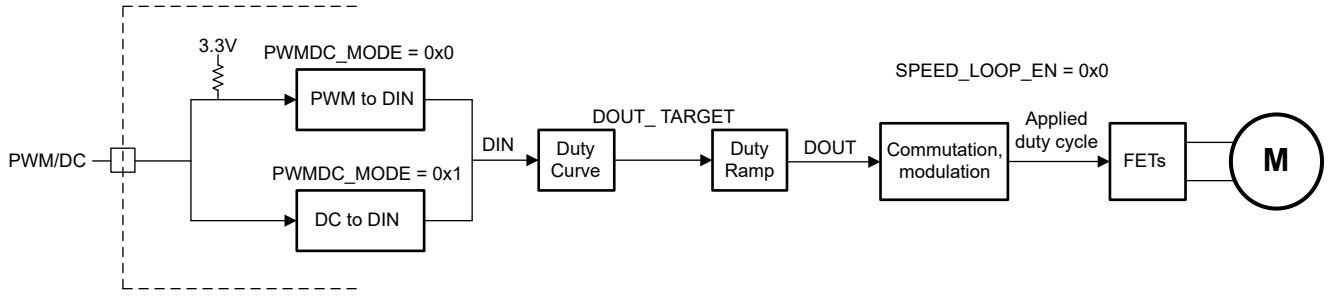

Figure 6-9. Open (Duty) Loop Control

6.3.1.5 Closed-Loop (Speed) Control

The MC121-Q1 has a closed loop (speed) control mode which can be used to maintain constant speed under varying operating conditions (VM, load) as shown in Figure 6-10. Speed loop is enabled by setting SPEED_LOOP_EN to 0x1 and the speed reference/target (SPEED_REF) is set by (DOUT x MAX_SPEED). The motor speed feedback from integrated Hall sensor is compared with the SPEED_REF and the error is fed into a PI loop. The PI loop Kp and Ki coefficients are configured through KP_RATIO and KI_RATIO. The output of speed loop (DOUT_SPEED_LOOP) sets the peak applied duty cycle. When output of the speed loop (DOUT_SPEED_LOOP) saturates, the integrator is disabled to prevent integral wind-up.

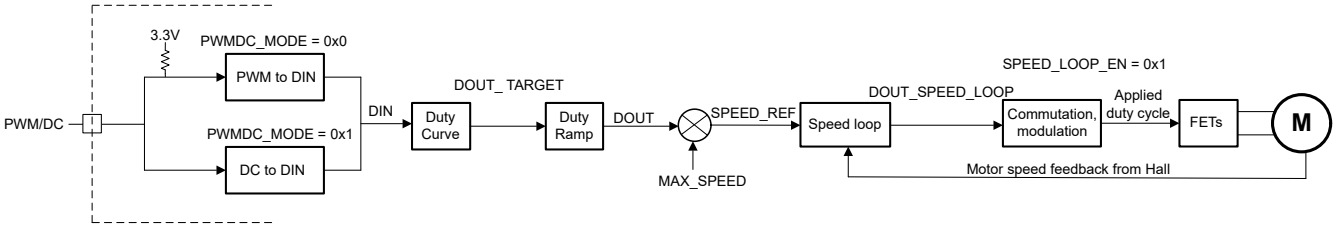

Figure 6-10. Closed (Speed) Loop Control

6.3.1.6 Commutation

In motors, commutation is the process of orienting stator and rotor magnetic fields to maintain continuous rotor motion. The rotor of a single phase BLDC motor contains a permanent magnet with alternating poles. The stator has one phase winding which attracts and repels the rotor magnet poles when energized. A Hall sensor integrated in the MC121-Q1 determines which direction to drive the current through the stator winding to commutate the motor. Figure 6-11 shows an example of single-phase motor commutation using the MC121-Q1. For proper motor commutation, the MC121-Q1 must be placed between two of the stator poles with the Hall element directly beneath the rotor magnet.

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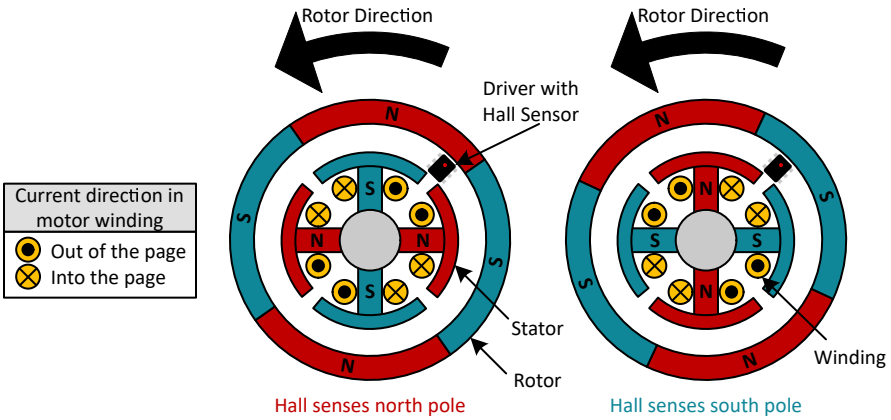

Figure 6-11. Example of Single Phase Motor Commutation

The MC121-Q1 driver integrates the following functions for commutation of a single-phase BLDC motor.

- Digital-latch Hall sensor for rotor position sensing
- Hall sensor offset angle setting for lead or lag angle adjustment using the HALL_OS_ANGLE and HALL_ANGLE_MODE bits
- Hall sensor delay setting for lead or lag time adjustment using the HALL_OS_TIME and HALL_TIME_MODE bits
- Hall offset signal inversion with the HALL_INVERT bit to change motor rotation direction or accommodate various Hall sensor orientation
- Square and soft PWM duty cycle waveshaping selected by COMMUTATION_MODE bit

6.3.1.6.1 Hall Sensor

The MC121-Q1 integrates a digital-latch Hall sensor to provide rotor position information to the commutation algorithm. The following sections highlight the details for device orientation and internal Hall signals to the commutation algorithm.

6.3.1.6.1.1 Field Direction Definition

The Hall sensor detects a positive magnetic field (B > 0 mT) when the magnetic field lines exit through the surface of the Hall sensor indicated in yellow in Figure 6-12. The SOT package uses a flipped-chip-on-lead construction, so the Hall sensor surface points away from the magnetic rotor. In this orientation, the Hall sensor detects a positive magnetic field when a north pole passes below the package.

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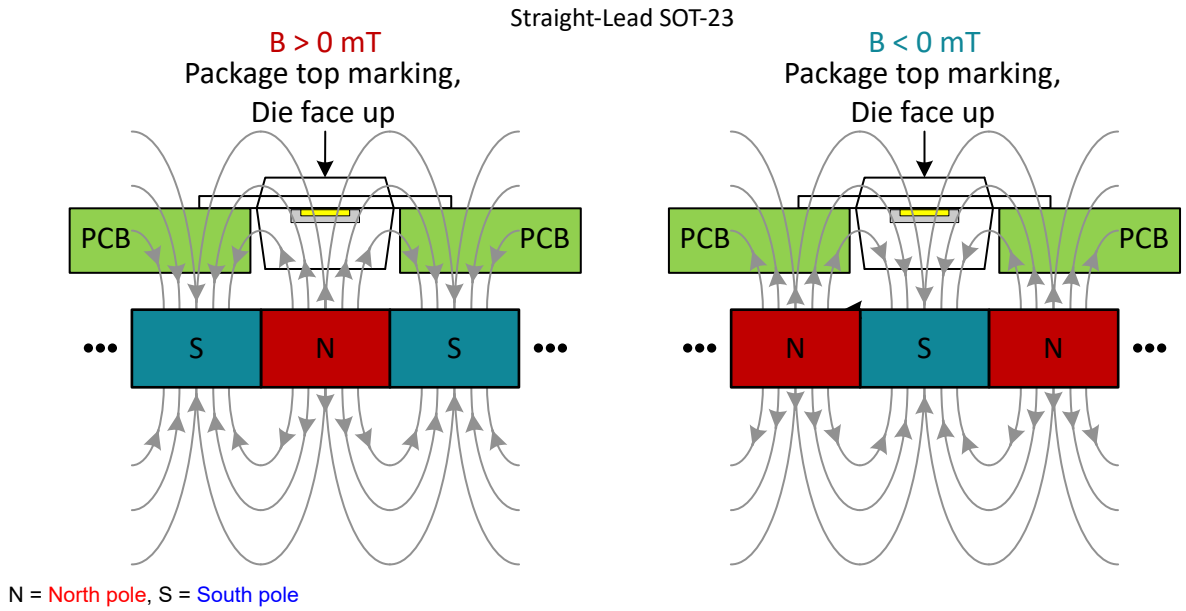

Figure 6-12. Field Direction Definition With Respect To Rotor Magnet And Driver

6.3.1.6.1.2 Internal Hall Latch Sensor Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP}, then the internal Hall latch output signal is indeterminate. If the field strength is greater than B_{OP}, then the internal Hall latch output signal is low. If the field strength is less than B_{RP}, then the internal Hall latch output signal is high.

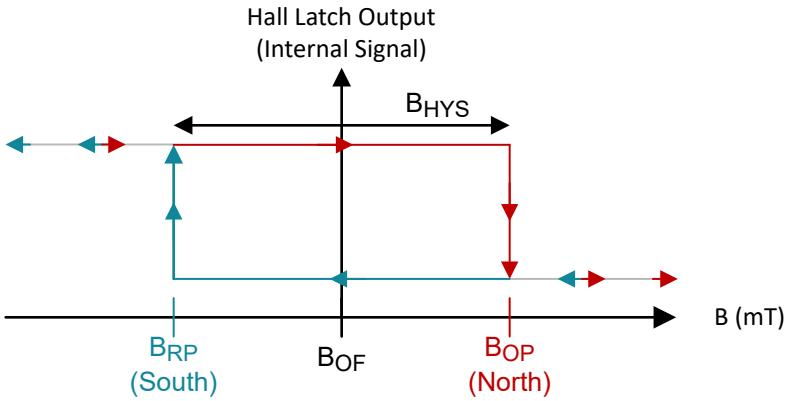

Figure 6-13. Internal Hall Output Signal

6.3.1.6.2 Hall Offset

MC121-Q1 provides the option of compensating the offset between Hall sensor and BEMF zero cross due to the relative location of the Hall sensor (in MC121-Q1) with respect to the BEMF zero cross. HALL_OS_ANGLE can be used to set the magnitude of the Hall offset angle ranging from 0º to 43.6º in steps of 1.4º. The polarity of this offset with respect to zero cross (lead or lag) can be set using HALL_ANGLE_MODE.

A lead or lag time with respect to the Hall sensor output is needed to maximize the motor efficiency across speeds by aligning the motor phase current with BEMF. The lead/lag time ($t_{HALL\_OS\_TIME}$) can be set by HALL_OS_TIME from 0 to 2.55ms in steps of 10µs; the polarity of this time (lead or lag) can be set using HALL_TIME_MODE.

MC121-Q1 aggregates the total lead or lag time that needs to be applied as per HALL_OS_ANGLE, HALL_ANGLE_MODE, HALL_OS_TIME and HALL_TIME_MODE and applies the computed lead or lag time

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around commutation region. For example, when HALL_OS_ANGLE is set to -15.4°, HALL_OS_TIME is set to 150µs, motor is operating at 500Hz, the applied lead time is approximately 64µs. 15.4° at 500Hz corresponds to 85.5µs, so effective lead/lag time is (150-85.5)µs = ~64µs.

6.3.1.6.3 Square Commutation

Square commutation is a simple commutation scheme provided by MC121-Q1 for maximum torque/speed operation. Figure 6-14 shows the driver output voltage relative to the Hall sensor signal in square commutation.

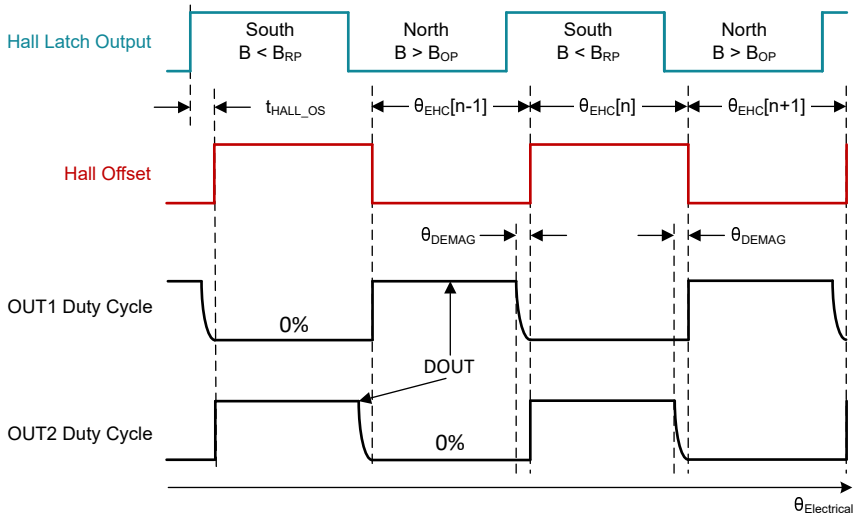

Figure 6-14. Square Commutation Timing Waveform

In square commutation, the output duty cycle remains constant at DOUT with respect to the electrical angle ($\theta_{Electrical}$). The signal from the Hall sensor and HALL_INVERT bit determines the OUTx terminal that switches at the commanded duty cycle and the OUTx terminal that is pulled to GND during the 180° electrical half cycle, θ_{EHC}.

The demagnetization state, θ_{DEMAG}, occurs at the end of the electrical half cycle and is determined by the DEMAG_TIME bits. The purpose of demagnetization is to reduce the motor current to zero and demagnetize the stator windings before reversing the OUTx voltage polarity due to a commutation event. Demagnetization minimizes voltage spikes on the VM supply and OUTx during commutation. Demagnetization also improves efficiency by reducing motor current spikes around the commutation region when back-EMF is minimal. PWM_MODE sets synchronous, asynchronous, or hybrid modulation for motor current during PWM OFF time and θ_{DEMAG} time, as described in Section 6.3.1.7. Figure 6-15, Figure 6-16, and Figure 6-17 show timing diagrams for asynchronous, synchronous, and hybrid recirculation states during θ_{DEMAG} respectively.

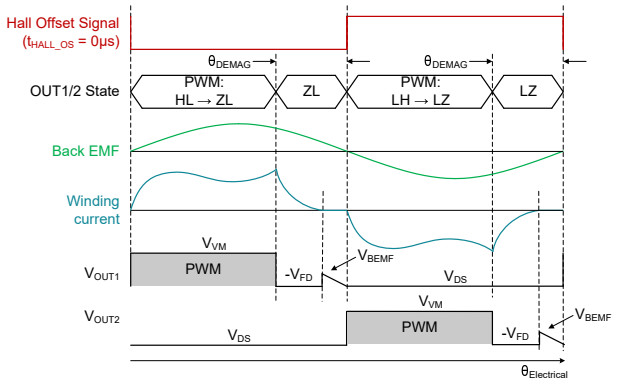

Figure 6-15. Detailed Timing Diagram for Square Commutation Using Asynchronous Mode for θ_{DEMAG}

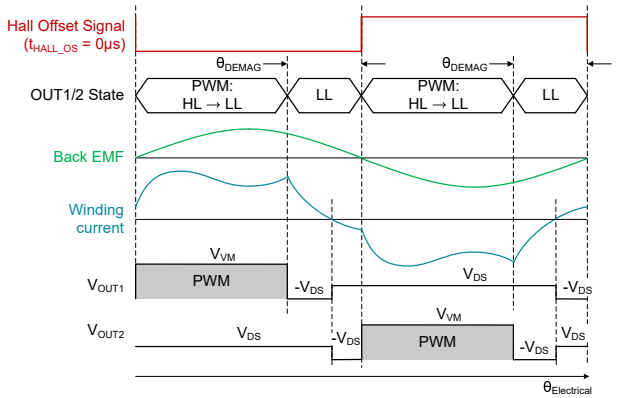

Figure 6-16. Detailed Timing Diagram for Square Commutation Using Synchronous Mode for θ_{DEMAG}

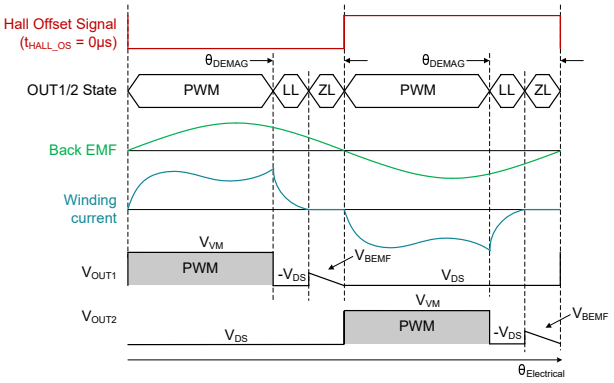

Figure 6-17. Detailed Timing Diagram for Square Commutation Using Hybrid Mode for θ_{DEMAG}

The demag time (DEMAG_TIME) can be set to a fixed time or can be automatically determined. When the AUTO_DEMAG_EN is set to 0x0, the demagnatization time is constant across operating conditions, and the DEMAG_TIME bits determine the θ_{DEMAG} based on speed of the motor. When the AUTO_DEMAG_EN is set to 0x1, the driver automatically adjusts the θ_{DEMAG} angle to optimize the demagnetization duration based on the speed of the motor.

6.3.1.6.4 Soft Commutation

In soft commutation scheme, after a commutation event, the PWM duty cycle ramps up to D_{OUT} during θ_{SRISE} and ramps back down to 0% during θ_{SFALL} as shown in Figure 6-18. The purpose of soft commutation is to reduce acoustic noise compared to square commutation. The timing of the Hall sensor signal transitions determines the timings of the θ_{SRISE} and θ_{SFALL} angles during the electrical half cycle. The θ_{SRISE} and θ_{SFALL} angles can be programmed using the SRISE and SFALL bits.

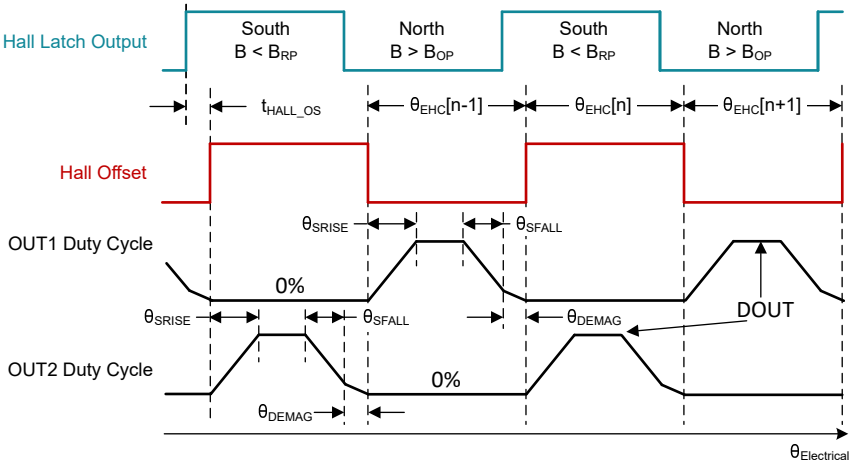

Figure 6-18. Soft Commutation Timing Waveform

When programming the SRISE, SFALL, and DEMAG_TIME bits, if the sum of θ_{SRISE}, θ_{SFALL}, and θ_{DEMAG} is greater than 180°, then θ_{SRISE} angle is reduced.

6.3.1.7 PWM Modulation Modes

The MC121-Q1 provides three PWM modulation modes: synchronous, asynchronous and hybrid. The PWM_MODE bit configures the PWM modulation mode. During synchronous mode, both low-side FETs turn on during the PWM OFF time. Synchronous mode reduces power loss by conducting the freewheeling current through the FET instead of the body diode. However, depending on turn-off current and motor winding inductance, there can be reverse current conduction during synchronous modulation resulting in negative torque and lower motor speed. During asynchronous mode, only one low-side FET remains on during the PWM OFF

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time while all other FETs are disabled and the freewheeling current is conducted through the body diode of a LS FET. In asynchronous mode, there is no reverse current flow during PWM off time but the power loss can be higher due to body diode conduction. Hybrid combines both modes - synchronous till the freewheeling current drops to < 13mA followed by asynchronous to prevent reverse current flow.

Table 6-1 shows the H-bridge states for the output PWM - H indicates HS FET in given OUTx leg is ON, L indicates LS FET in given OUTx leg is ON, Z indicates both FETs in given OUTx legs are in Hi-Z. The Hall offset signal is the internal signal determined from the Hall sensor state and device settings. The Hall offset signal determines the output switching states in the commutation algorithm state machine. The input PWM duty cycle and commutation mode (square/soft) determine the instantaneous output PWM duty cycle, D_{OUT}.

Table 6-1. Output State Table

Driver State	Description	Modulation mode set by PWM_MODE	Hall Offset Signal	OUT1	OUT2
DOUT	PWM ON time/duty cycle	X	L	L	H
		X	H	H	L
(1-DOUT), Current Limiting, θ_{DEMAG}	Motor current recirculation during PWM OFF time/ duty or during current limiting off time, or phase demagnetization before a commutation event	Asynchronous mode	L	L	Z
			H	Z	L
		Synchronous mode	X	L	L

Figure 6-19 shows the motor current flow through the H-bridge during PWM ON time, PWM OFF time, and demagnetization states. Refer to Section 6.3.1.6.3 for more details on demagnetization state.

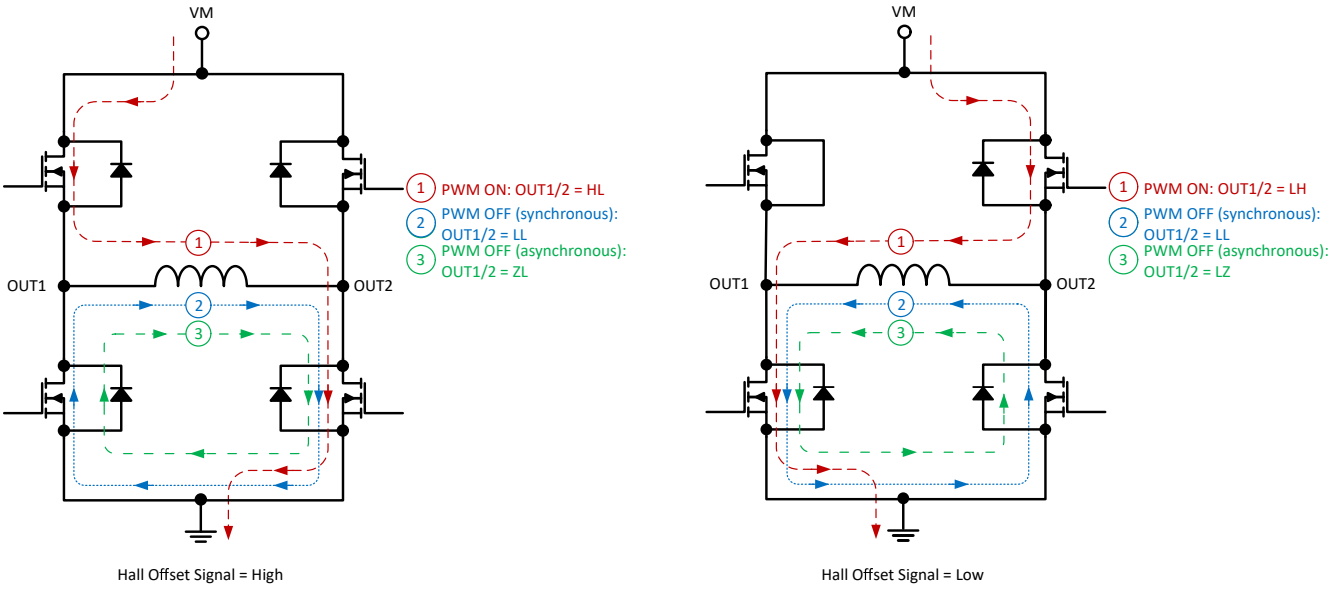

Figure 6-19. Motor Current and Output States

The hybrid PWM mode enables both low-side FETs during the PWM OFF time (same as synchronous mode) to avoid recirculating the motor current through the body diode. Once the motor current reaches <13mA, a zero-current detector disables the acceptable low-side FET to place the H-bridge in the asynchronous mode. By automatically switching between synchronous and asynchronous modes, the MC121-Q1 reduces device power loss while avoiding back EMF generating unintended negative current in the motor winding.

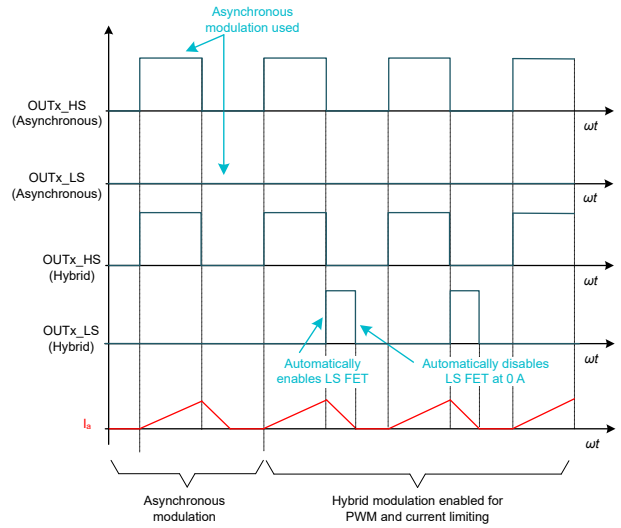

Figure 6-20. Asynchronous and Hybrid Modulation

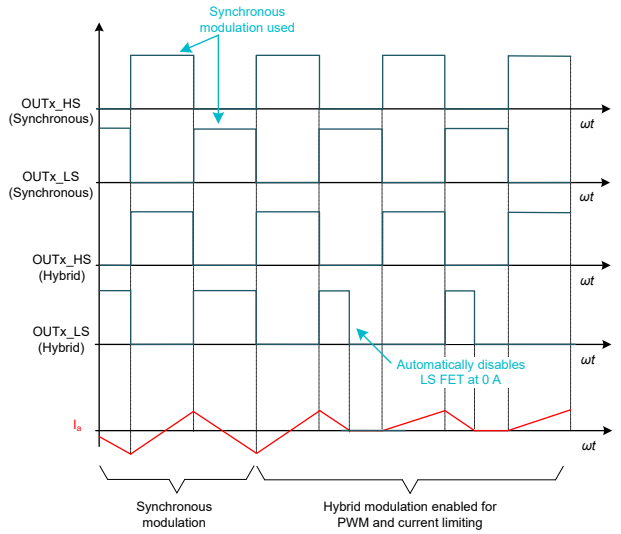

Figure 6-21. Synchronous and Hybrid Modulation

Table 6-2 shows the settings for the PWM_MODE bitfield to configure the PWM modulation mode.

Table 6-2. Modulation Mode with PWM_MODE

PWM_MODE Bits	PWM and Current Limiting OFF Time	Demagnetization State
000b	Asynchronous	Asynchronous
001b	Asynchronous	Synchronous
010b	Synchronous	Asynchronous
011b	Synchronous	Synchronous
100b	Synchronous	Hybrid
101b	Asynchronous	Hybrid
110b	Hybrid	Asynchronous
111b	Hybrid	Hybrid

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6.3.2 Protections

MC121-Q1 integrates protections for rotor lock, current limiting, overcurrent, VM undervoltage, VM overvoltage, and overtemperature events. Table 6-3 indicates fault mode entry and recovery to active mode.

Table 6-3. Device Fault Action and Response

FAULT	CONDITION	H-BRIDGE	DEVICE LOGIC	FG/RD Indication?	RECOVERY
Locked rotor protection	Hall transition not detected for t_{LRD} and LRD_RETRY_DIS = 0x0	All FETs disabled (Hi-Z)	Enabled	Yes	Auto retry after $t_{lock\_long\_retry}$ or $t_{lock\_quick\_retry}$
	Motor stall: Hall transition not detected for t_{LRD} for 5 consecutive start attempts and LRD_RETRY_DIS = 0x1	All FETs disabled (Hi-Z)			Latched; latched fault cleared only by power reset or wake-up
Current limit	$I_{OUTx,LS} > I_{LIMIT}$	HS FETs disabled and current recirculation through LS FETs based on PWM_MODE		No	$I_{OUTx,LS} < I_{LIMIT}$ at the start of next output PWM duty cycle
Overvoltage protection	$V_{VM} > V_{OVP}$ rising and OVP_EN=0x1	All FETs disabled (Hi-Z)		Yes, if FGRD_FAULT_SEL = 0x1	$V_{VM} < V_{OVP}$ falling
Overcurrent protection	$I_{OUTx} > I_{OCP}$ and OCP_MODE = 0x0	All FETs disabled (Hi-Z)			Auto retry after $t_{lock\_long\_retry}$
	$I_{OUTx} > I_{OCP}$ and OCP_RETRY_MODE = 0x1				Latched after 3 consecutive OCP events; latched fault cleared only by power reset or wake-up
Thermal Shutdown	$T_J > T_{TSD}$	All FETs disabled (Hi-Z)			$T_J < T_{TSD} - T_{HYS}$
Undervoltage protection	$V_{VM} < V_{UVLO}$ falling	All FETs disabled (Hi-Z)	Disabled	No	$V_{VM} > V_{UVLO}$ rising
Integrated supply clamp	$V_{VM} > VM_{CLAMP}$ and VM_CLAMP_DIS = 0x0	HS FETs disabled (Hi-Z)	Enabled		$V_{VM} < VM_{CLAMP}$

The FG/RD pin supports feedback to the fan controller for motor speed or rotor lock detection. Setting the FGRD_MODE bit to 0x0 configures the FG/RD pin for the frequency generator (FG) output. The transitions of the internal Hall sensor signal determine the frequency of the FG signal. By setting the FG_MULTIPLIER bits, the FG pin toggles with a factor of 1/2, 1, 2/3, or 2 times the internal Hall sensor frequency. The FG_MULTIPLIER bits help minimize system design and firmware changes when swapping motors with different number of magnetic pole pairs. When FG_HALL_RAW_EN is set to 0x0, the FG pin signal corresponds to the Hall offset signal. When FG_HALL_RAW_EN = 0x1, the FG pin signal corresponds to the Hall sensor signal directly. The device does not support the 2/3 FG_MULTIPLIER setting when FG_HALL_RAW_EN = 0x1.

The FG/RD pin indicates device fault mode, locked rotor condition and active mode status according to Table 6-4. The state of the FG pin when motor is in stationary/idle (stopped by DIN = 0% or DOUT_TARGET = 0%) is always complementary to the state used to indicate a locked rotor or device fault condition. For example, if a combination of FGRD_MODE, FGRD_INVERT and FGRD_FAULT_SEL bits indicate locked rotor as an active low signal on FG pin, the state of the FG pin is high (through external pull-up) when the motor is in stationary/idle state.

Table 6-4. FG/RD Pin Behavior

FGRD_MODE bit	FGRD_INVERT bit	FGRD_FAULT_SEL bit	Active Mode Indication	Locked rotor indication	Fault mode indication
0x0	0x0	0x0	FG = toggling	FG = asserted low	FG = previous state
	0x0	0x1			FG = asserted low
	0x1	0x0		FG = pulled high	FG = previous state
	0x1	0x1			FG = pulled high
0x1	0x0	0x0	RD = pulled high	RD = asserted low	RD = previous state
		0x1			RD = asserted low
	0x1	0x0	RD = asserted low	RD = pulled high	RD = previous state
		0x1			RD = pulled high

6.3.2.1 Locked Rotor Protection

When the MC121-Q1 does not detect a Hall transition for longer than the locked rotor detection time (t_{LRD}), a locked rotor fault is recognized, all FETs are disabled (Hi-Z) and the FG/RD pin indicates the locked rotor fault according to Table 6-4. t_{LRD} is set by t_{LRD_START} during start-up sequence, while t_{LRD} is set by t_{LRD_RUN} during motor run (steady state). The locked rotor retry sequence (when LRD_RETRY_DIS = 0x0) during start-up is as shown in Figure 6-22. During the first start-up after power-up/wake-up, the number of quick retry attempts is set by LRD_NRETRY_STARTUP; the quick retry time is same as the locked rotor detection time (t_{LRD_START}). If the locked rotor condition persists after LRD_NRETRY_START attempts are completed, MC121-Q1 enters a long retry time ($t_{lock\_long\_retry}$) which is (LRD_LONG_RETRY_SEL x t_{LRD_START}). Once the long retry time lapses, MC121-Q1 attempts to spin the motor again; on the second start-up attempt after power-up/wake-up, the number of quick retry attempts is set by LRD_NRETRY_RUN while the locked rotor detection time (t_{LRD_START}) and quick retry time remain the same. If the locked rotor condition persists after LRD_NRETRY_RUN attempts are completed, MC121-Q1 enters a long retry time ($t_{lock\_long\_retry}$) again. Subsequent motor start-up sequences uses the same retry pattern as the second start-up cycle as shown in Figure 6-22. Every motor start-up attempt after retry time lapse (quick or long retry) is initiated from the pre-start phase as shown in Figure 6-6.

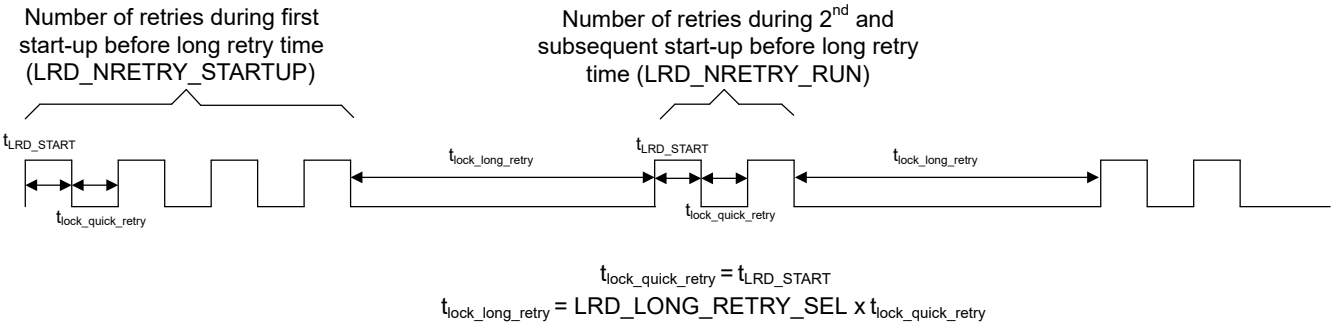

Figure 6-22. Locked rotor retry sequence and timing during start-up when LRD_RETRY_DIS = 0x0

When a locked rotor condition is detected during motor run (no Hall transition for t_{LRD_RUN}), all FETs are in disabled (Hi-Z) and the FG/RD pin indicates the locked rotor fault according to Table 6-4. MC121-Q1 waits for one interval of long retry time before starting the locked rotor retry sequence as shown in Figure 6-23.

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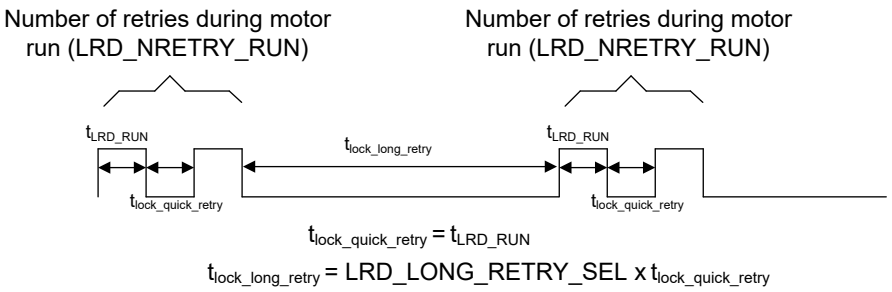

Figure 6-23. Locked rotor retry sequence and timing during run when LRD_RETRY_DIS = 0x0

MC121-Q1 provides the option of latching a locked rotor fault after 5 consecutive start attempts result in a locked rotor by setting LRD_RETRY_DIS = 0x1 as shown in Figure 6-24. Motor operation can resumed either by a power reset or wake-up (sleep exit).

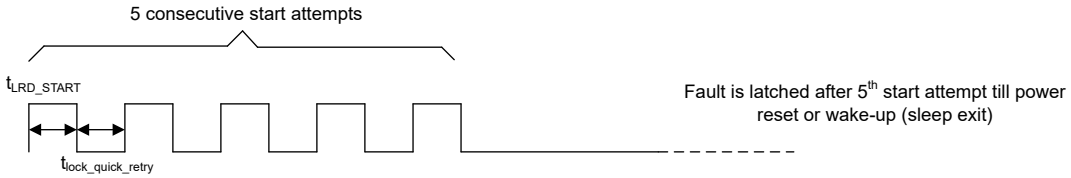

Figure 6-24. Locked rotor retry sequence and timing when LRD_RETRY_DIS = 0x1

6.3.2.2 Current Limit

Current limit feature protects the motor from overcurrent operation during start-up, overload and stall conditions. When the motor phase current exceeds the I_{LIMIT} threshold, the MC121-Q1 uses a cycle-by-cycle current limit scheme by turning off the high-side FET. ILIMIT_SEL sets the current limit threshold. The PWM_MODE bits set synchronous, asynchronous, or hybrid recirculation states for motor current during the current limiting OFF time, similar to the PWM OFF time described in Section 6.3.1.7.

If the motor current remains above the I_{LIMIT} threshold at the start of the next PWM period, then the low-side FETs remain enabled for another PWM period. If the motor current drops below I_{LIMIT} by the start of the next PWM period, the outputs return to the driving state determined by the commutation algorithm state machine as shown in Table 6-1.

Current limiting provides an upper limit to the motor torque by reducing the output PWM duty cycle when motor current is above the I_{LIMIT} threshold. The current limit function takes priority over the PWM duty cycle determined by the commutation state machine. When the motor current drops below the I_{LIMIT} threshold, the commutation state machine has full control of the output duty cycle. Figure 6-25and Figure 6-26 show example waveforms of the cycle-by-cycle current limiting scheme.

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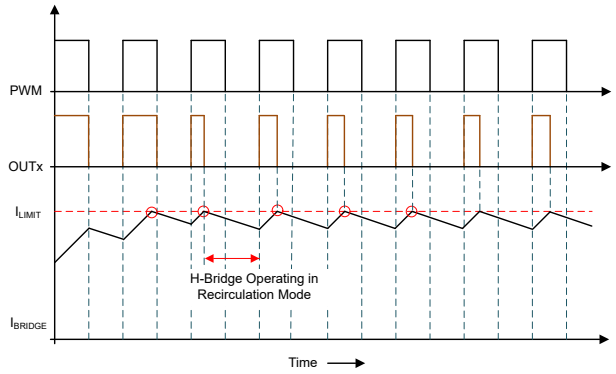

Figure 6-25. Cycle-by-Cycle Current-Limit Operation

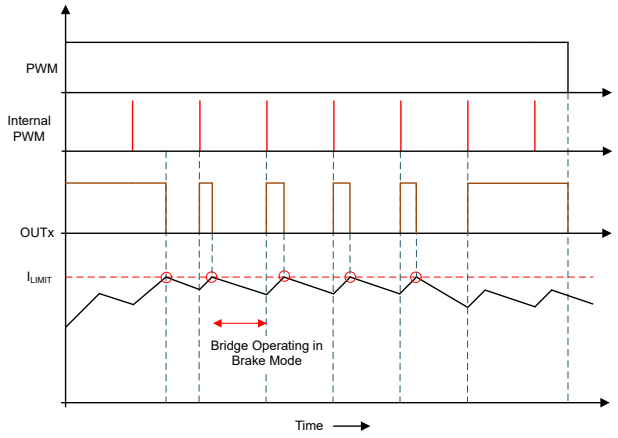

Figure 6-26. Cycle-by-Cycle Current-Limit Operation with 100% PWM Duty Cycle

6.3.2.3 Overcurrent Protection (OCP)

The overcurrent protection (OCP) feature protects the integrated power FETs on the OUTx pins from shorts to the supply (VM), ground, and between the OUTx pins. When the current through a FET stays higher than the OCP threshold (I_{OCP}) for longer than the OCP deglitch time (t_{OCP}) as shown in Figure 6-27, all FETs in the H-bridge are disabled (Hi-Z) and the FG/RD pin indicates the locked rotor fault according to Table 6-4. The OCP fault recovery is set by OCP_RETRY_MODE.

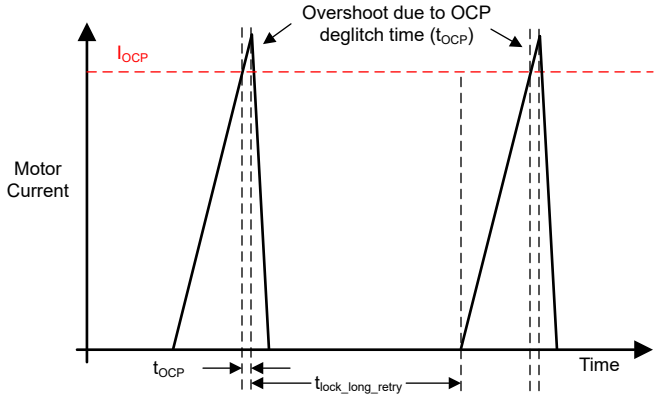

Figure 6-27. OCP Operation

When OCP_RETRY_MODE is set to 0x0, MC121-Q1 starts driving the motor (from pre-start phase) after $t_{lock\_long\_retry}$ lapses as shown in Figure 6-28. $t_{lock\_long\_retry}$ is set by (LRD_LONG_RETRY_SEL x t_{LRD_START}). When OCP_RETRY_MODE is set to 0x1, MC121-Q1 latches the fault after 3 retry attempts (retry time is set by $t_{lock\_long\_retry}$); subsequent motor operation is possible only after a subsequent power reset or wake-up (sleep exit) to clear the fault condition.

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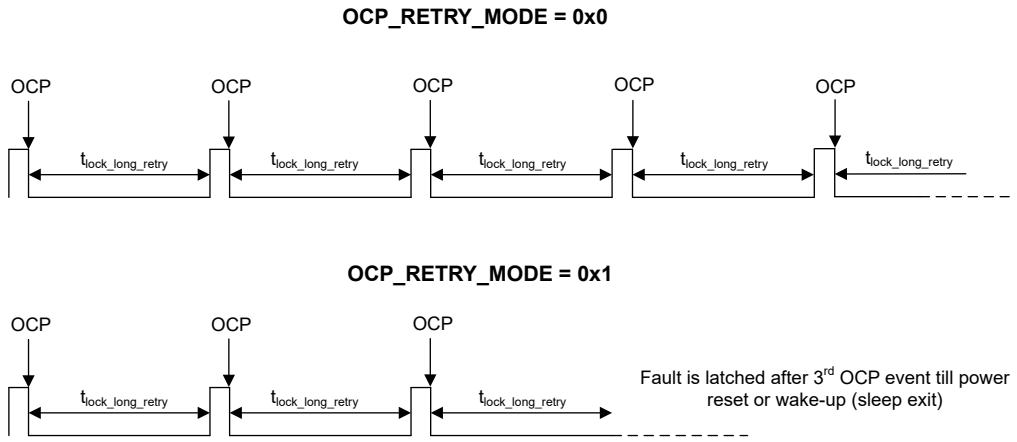

Figure 6-28. OCP retry Modes

6.3.2.4 VM Undervoltage Lockout (UVLO)

When the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled and the internal logic is reset. When UVLO_SEL = 0x0, device powers up and motor operation resumes when the V_{VM} voltage rises above the UVLO rising threshold as shown in Figure 6-29. When UVLO_SEL ≠ 0x0, device always powers-up at UVLO rising threshold corresponding to UVP_SEL = 0x0 but the motor operation begins only when VM rises above the UVLO rising threshold set by the UVLO_SEL. When UVLO_SEL ≠ 0x0 and 3.15 < VM < V_{UVLO} (rising) (corresponding to set UVLO_SEL), VM UVLO fault is active, all FETs are disabled and the FG/RD pin indicates the locked rotor fault according to Table 6-4.

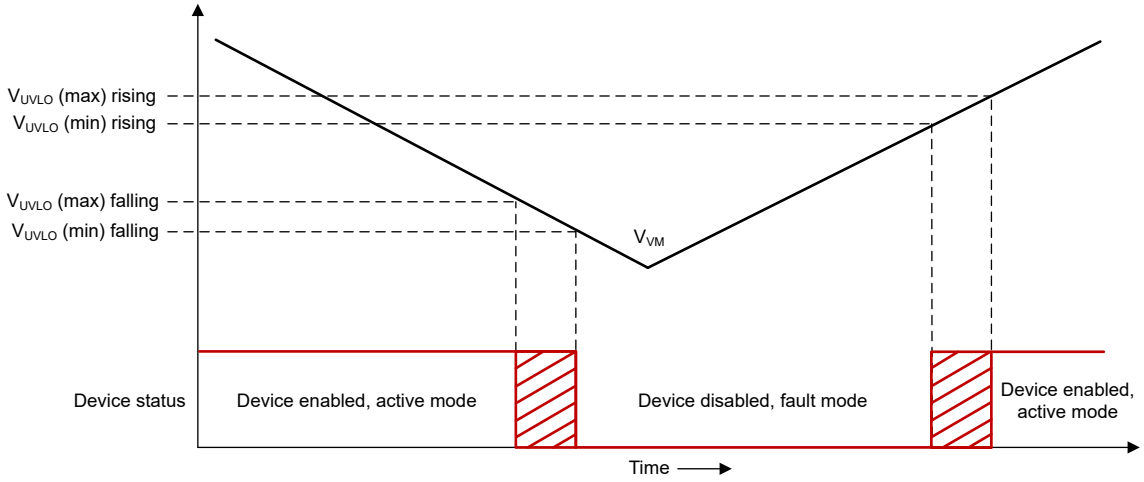

Figure 6-29. VM UVLO Operation

6.3.2.5 VM Over Voltage Protection (OVP)

When the VM voltage exceeds the V_{OVP} rising threshold, all FETs are in Hi-Z and the FG/RD pin indicates the locked rotor fault according to Table 6-4. When the VM voltage drops below the V_{OVP} falling threshold, normal device operation resumes. The OVP threshold is set by OVP_SEL and can be disabled by setting OVP_EN to 0x0. Overvoltage protection has a fixed deglitch time of 80µs to eliminate spurious OVP triggers. To avoid false OVP triggers due to transient VM spikes during normal motor operation, the overvoltage protection is disabled during the rise and fall intervals of soft commutation. In addition, OVP is always disabled during the demagnetization interval. Also, an optional (enabled by setting OVP_BLANK_EN to 0x1) blanking time set by OVP_BLANK_SEL (1ms or 4ms) is provided during the peak duty cycle interval to improve OVP detection robustness. Figure 6-30 shows the OVP detection operation in different intervals of soft commutation. In square commutation, there are no rise/fall intervals and the blanking time, when enabled, is applied from the commutation instant.

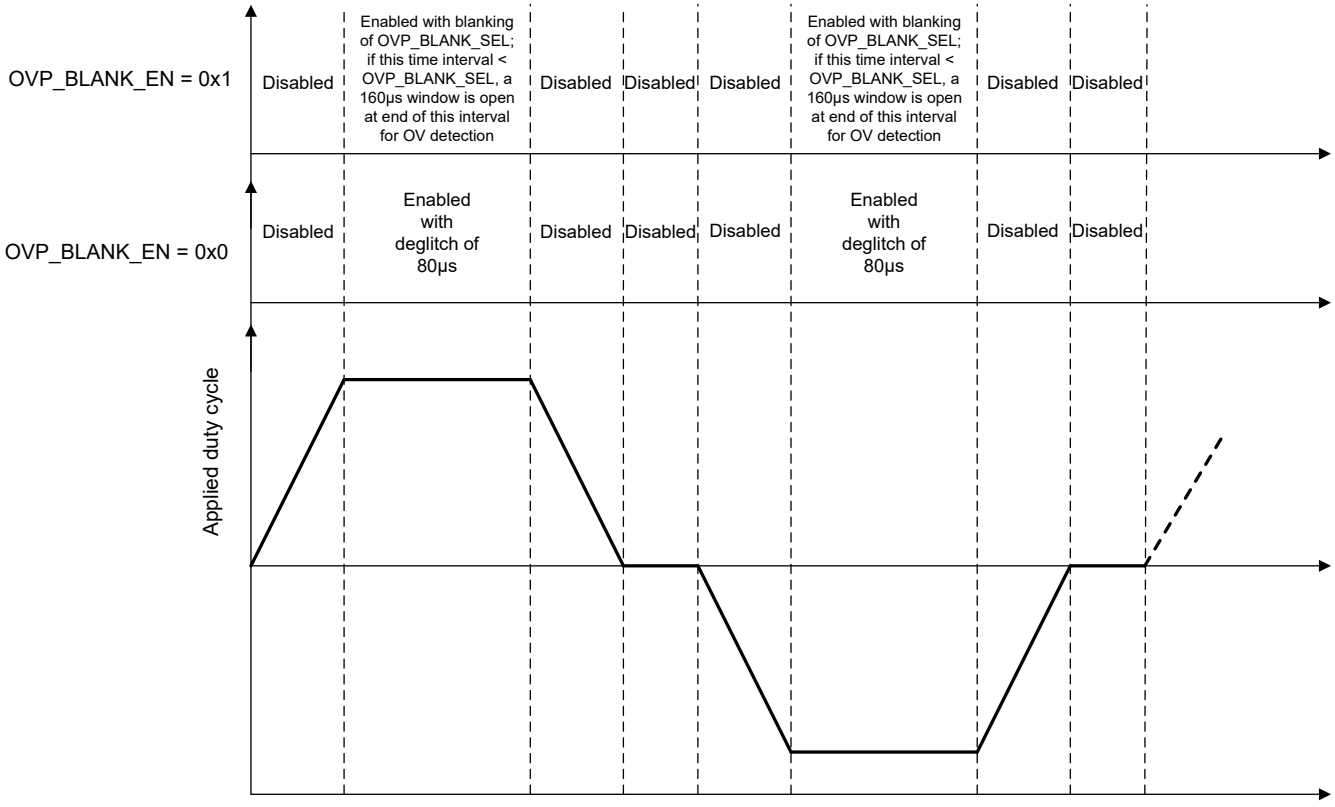

Figure 6-30. OVP Detection

6.3.2.6 Thermal Shutdown (TSD)

If the die temperature exceeds T_{TSD}, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level (T_{TSD} - T_{HYS}), device operation automatically resumes.

6.3.2.7 Integrated Supply (VM) Clamp

MC121-Q1 provides an integrated clamp on the supply (VM) pin to limit the voltage spikes on VM pin due to regenerative energy push-back from the motor; the clamp is disabled when VM_CLAMP_DIS is set to 0x1. When the VM voltage reaches VM_{CLAMP} level, the device activates the clamp to limit the VM voltage. When the clamp is active, HS FETs are in Hi-Z and motor driving is stopped; the clamp circuit is able to absorb the energy till the clamp citcuit reaches the limits specified by the Safe Operating Area. When the SOA limits are exceeded, the clamp is deactivated; in case higher energy (than specified by SOA) is needed to be clamped a acceptable external TVS diode is added.

Note

During the clamp operation, if any faults like overcurrent protection (OCP) or overtemperature (TSD) are encountered, the clamp is deactivated.

6.4 Device Functional Modes

6.4.1 Active Mode

When the V_{VM} voltage is greater than the V_{UVLO} voltage and D_{IN} > 0%, the device goes to active mode. The t_{WAKE} time must elapse before the device responds to inputs.

6.4.2 Sleep and Standby Mode

SLEEP is used to enable the sleep (low power) mode. In sleep mode (SLEEP_EN = 0x1 and D_{IN} = 0%), the device draws very low quiescent current from the VM pin (I_{VMQ}) - this is done by disabling internal circuitry

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including FETs, Hall sensor, current sense, digital core, internal regulators, and charge pump. The device wakes up and enters active (STBY_EN = 0x0) or standby (STBY_EN = 0x1) mode, when D_{IN} > 0% for t_{WAKE}.

When sleep mode is disabled (SLEEP = 0x0), STBY_EN decides the device operation across D_{IN}. When D_{IN} < DIN0 and STBY_EN = 0x0, MC121-Q1 drives the motor at duty or speed corresponding to DOUT0; when D_{IN} < DIN0 and STBY_EN = 0x1, MC121-Q1 stops the motor operation (DOUT = 0%) and is in standby state.

Irrespective of SLEEP_EN and STBY_EN values, when D_{IN} ≥ (DIN0 + DHYS), MC121-Q1 drives the motor at duty or speed set by the duty curve. Table 6-5 summarizes sleep and standby mode operation.

Note

D_{IN} = 0% corresponds to duty cycle of 0% in PWM input mode (PWM_DC = 0x0) and a DC voltage < 100mV in DC (analog) input mode (PWM_DC = 0x1)

Table 6-5. Summary of sleep/standby mode operation

SLEEP_EN	STBY_EN	Condition for Device Status Change	Device Status	D_{OUT}	H-Bridge
0x0	0x0	D_{IN} < DIN0	Active Mode	DOUT0	PWM
	0x1		Standby Mode	0%	Hi-Z
X	X	DINOFF > D_{IN} ≥ (DIN0 + DHYS)	Active Mode	Set by D_{IN} as per duty curve	PWM
0x1	X	D_{IN} = 0%; refer Figure 6-8	Sleep Mode	0%	Hi-Z
0x1	0x0	0% < D_{IN} < DIN0	Active Mode	DOUT0	PWM
	0x1		Standby Mode	0%	Hi-Z

6.4.3 Fault Mode

The MC121-Q1 is protected against system faults described in Section 6.3.2. In some cases, the commutation algorithm can be interrupted, and the device needs to restart the motor.

6.4.4 Test Mode and One-Time Programmable Memory

The MC121-Q1 integrates a test and programming mode where the PWM/DC and FG/RD pins support an I^2C interface for device configuration and testing. The I^2C interface also gives access to the one-time programmable (OTP) memory. Programming the registers selects the device configurations described in the previous sections. Figure 6-31 shows the basic hardware configuration for configuring and programming the MC121-Q1.

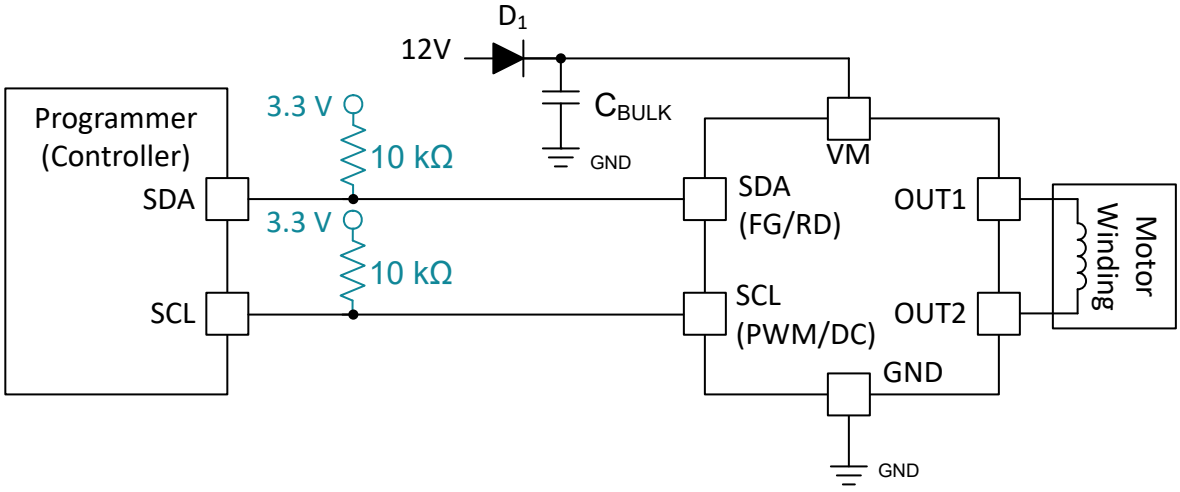

Figure 6-31. I^2C Programmer and Fan Module

The MC121-Q1 enters test mode and OTP mode with the following procedure.

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1. Pull the FG/RD pin low and apply a high frequency signal in the range of (416-833) kHz at any duty between (20-80)% for 15 to 20 cycles to the PWM/DC pin to enter the test mode. The I²C interface is active in test mode.
2. Communicate with MC121-Q1 over I²C to read and write to the registers in Section 7 to configure the registers.
3. To maintain reliable OTP memory programming through I²C communication, maintain the MC121-Q1 power supply pin voltage (VM) above 8V throughout the entire duration of the communication.
4. Write the OTP mode entry key 02h, 01h, 04h to the USR_OTP_PRG_UNLOCK register in successive write-frames to unlock OTP mode.
5. To burn the OTP memory, write 1b to the USR_OTP_PROG_ALL bit in USR_OTP_CFG Register.

6.5 Programming

The MC121-Q1 supports I²C programming in test mode. Section 6.4.4 describes the method to enter test mode to read and write to the registers and to program the OTP memory during system prototyping and production. External programming hardware or an on-board microcontroller can interface with the MC121-Q1 over the I²C interface. The following sections describe the details of the I²C communication protocol.

6.5.1 I²C Communication

The I²C bus consists of a data line (SDA) and a clock line (SCL) with off-chip pull-up resistors. When the bus is idle, both SDA and SCL lines are pulled high.

A controller device, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A peripheral device receives and/or transmits data on the bus under control of the controller device. The MC121-Q1 is the peripheral device on the I²C bus in this context.

The device address of the MC121-Q1 is 0x65.

6.5.1.1 I²C Read

The I²C read operation begins similarly to a write operation. The controller device sends a START condition on the bus with the 7-bit address of the peripheral device and the R/W bit set to 0b. After the peripheral device responds with an acknowledge signal (ACK), the controller device sends the 8-bit address of the register intended to receive the data. After the peripheral device responds with an ACK signal again, the controller device re-sends the START command, RSTRT, followed by the peripheral address with the R/W bit set to 1b to signify a read operation. The controller device releases the SDA line to receive the register data from the peripheral device. The peripheral responds with an ACK signal to indicate that the peripheral is ready to transmit the register data.

The controller device continues providing a clock signal to the peripheral device. The peripheral device sends the 8-bit register data on the SDA line each clock cycle. At the end of the byte, the controller device sends a negative-acknowledge (NACK) signal, signaling to the peripheral device to stop communications and release the bus. The controller device then sends a STOP condition.

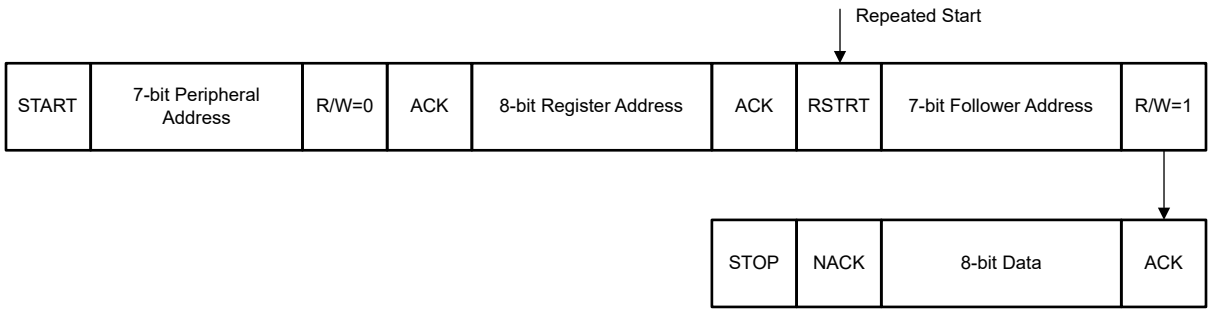

Figure 6-32. I²C Read Sequence

6.5.1.2 I²C Write

To write on the I²C bus, the controller device sends a START condition on the bus with the 7-bit address of the peripheral device and the R/W bit set to 0b to signify a write operation. After the peripheral device responds with an acknowledge bit (ACK), the controller device sends the 8-bit address of the register intended to receive the data. After the peripheral device responds with an ACK bit again, the controller device sends the 8-bit data. The peripheral device responds with a final ACK bit, and the controller terminates the transmission with a STOP condition.

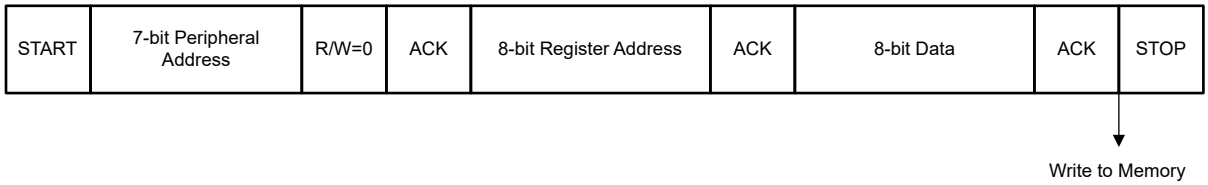

Figure 6-33. I²C Write Sequence

7 Register Map

Table 7-1 list the register maps for one-time programmable memory (OTP) and test mode accessible by I^2C test mode in the MC121-Q1. The USER_OTP map (addresses 0x00 to 0x1B) includes OTP registers available for device programming during end-system production. The USR_TM register map (addresses 0x20 to 0x26) offer test mode configuration to allow system designers to experiment with device settings during system prototyping and development. Burned OTP registers keep written data after power cycle. After burning OTP, the registers may receive new data in test mode, but the burned OTP values are the device defaults when the device power cycles. The test mode registers, USR_TM are not OTP memory registers and are reset during a power cycle.

7.1 USR_OTP Registers

Table 7-1 lists the memory-mapped registers for the USR_OTP registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. USR_OTP Registers

Offset	Acronym	Register Name	Section
0h	INTERFACE_CONFIG0	Interface Configuration Register 0	Section 7.1.1
1h	INTERFACE_CONFIG1	Interface Configuration Register 1	Section 7.1.2
2h	START_STOP_CONFIG	Start and Stop Configuration Register	Section 7.1.3
3h	DIN0	DIN0 Setting	Section 7.1.4
4h	DOUT0	DOUT0 Setting	Section 7.1.5
5h	DOUT1	DOUT1 Setting	Section 7.1.6
6h	DOUT2	DOUT2 Setting	Section 7.1.7
7h	DOUT3	DOUT3 Setting	Section 7.1.8
8h	DOUT4	DOUT4 Setting	Section 7.1.9
9h	DOUT5	DOUT5 Setting	Section 7.1.10
Ah	DOUT6	DOUT6 Setting	Section 7.1.11
Bh	DOUT7	DOUT7 Setting	Section 7.1.12
Ch	DOUT8	DOUT8 Setting	Section 7.1.13
Dh	HALL_TIME_CONFIG	Configuration Register for Hall Offset Time	Section 7.1.14
Eh	COMMUTATION_CONFIG0	Commutation Configuration Register 0	Section 7.1.15
Fh	COMMUTATION_CONFIG1	Commutation Configuration Register 1	Section 7.1.16
10h	COMMUTATION_CONFIG2	Commutation Configuration Register 2	Section 7.1.17
11h	COMMUTATION_CONFIG3	Commutation Configuration Register 3	Section 7.1.18
12h	PROTECTION_CONFIG0	Configuration Register for Protection Settings	Section 7.1.19
13h	CLOSED_LOOP_CONFIG0	Least Significant byte of MAX_SPEED	Section 7.1.20
14h	CLOSED_LOOP_CONFIG1	KI_RATIO and MSN of MAX_SPEED in closed loop and DOUT_MAX in Open loop	Section 7.1.21
15h	CLOSED_LOOP_CONFIG2	KP_RATIO in closed loop and LRD settings	Section 7.1.22
16h	PROTECTION_CONFIG1	Register for Protections and PWM Dithering	Section 7.1.23
17h	GENERAL_CONFIG1	Register for ILIM_SEL, Hall and LRD settings	Section 7.1.24
18h	GENERAL_CONFIG2	Register for VM clamp, Prestart ramp and Hall Settings	Section 7.1.25
19h	GENERAL_CONFIG3	Register for Silence, Pole pair, LRD settings	Section 7.1.26
1Ah	GENERAL_CONFIG4	Configuration Register for DEMAG and Silence settings	Section 7.1.27
1Bh	USR_OTP_CRC	Register for CRC calculated over USR_OTP	Section 7.1.28

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. USR_OTP Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 INTERFACE_CONFIG0 Register (Offset = 0h) [Reset = 00h]

INTERFACE_CONFIG0 is shown in Table 7-3.

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Table 7-3. INTERFACE_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HALL_DEGLITCH_EN	R/W	0h	Enables HALL signal from HALL sensor to be deglitched for 0h = HALL deglitch disabled 1h = HALL deglitch enabled
6	PWM_IN_RANGE	R/W	0h	Selects the input PWM signal frequency detection range 0h = 80Hz to 90kHz 1h = 20Hz to 22kHz
5	PWM_OUT_FREQ	R/W	0h	Selects the PWM switching Frequency on the OUTx 0h = Output PWM freq is 25kHz 1h = Output PWM freq is 50kHz
4-3	ILIM_BLANK_SEL	R/W	0h	Selects additional blanking time for current limit (ILIM) on top of deadtime and default blanking 0h = No additional blanking 1h = 160ns (nominal) additional blanking 2h = 320ns additional iLim blanking 3h = 640ns additional iLim blanking
2	ILIM_DEGLITCH_SEL	R/W	0h	Selects the deglitch time for cycle by cycle current limit (ILIMIT). 0h = deglitch time between 481ns to 732ns 1h = deglitch time between 925ns to 1.419us
1-0	UVLO_SEL	R/W	0h	Selects the threshold at which UVLO gets triggered 0h = Rising threshold 3V and falling threshold 2.7V 1h = Rising threshold 4.2V and falling threshold 2.7V 2h = Rising threshold 5.7V and falling threshold 2.7V 3h = Rising threshold 7.6V and falling threshold 2.7V

7.1.2 INTERFACE_CONFIG1 Register (Offset = 1h) [Reset = 60h]

INTERFACE_CONFIG1 is shown in Table 7-4.

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Table 7-4. INTERFACE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DIN_HYS	R/W	1h	Selects duty cycle hysteresis DIN_HYS for speed curve. 0h = 0%, no hysteresis 1h = 1.2% 2h = 2.4% 3h = 4.8%
5	STBY_EN	R/W	1h	Selects OUTx behavior at DIN = 0%. 0h = The driver commutates the motor at the DOUT0 duty cycle. 1h = The driver disables the outputs after t_{SLEEP}, but all internal circuitry remains active for faster re-enable.
4	SLEEP_EN	R/W	0h	Enables sleep mode when DIN = 0%. 0h = Sleep mode is disabled. The driver state is determined by the STBY_EN bit. 1h = Sleep mode is enabled. DOUT ramps down to 0% output duty cycle, and the driver goes into a low-power sleep mode after receiving no Hall edge for t_{SLEEP}.
3	PWMDC_MODE	R/W	0h	Selects input mode between PWM or analog. 0h = The PWM pin accepts a logic PWM duty cycle to control speed. 1h = The PWM pin accepts and analog voltage to control motor speed.

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Table 7-4. INTERFACE_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	FGRD_INVERT	R/W	0h	Selects FG/RD pin logic level during rotor lock or device fault. 0h = FG/RD pin asserted low during rotor lock or device fault. 1h = FG/RD pin asserted high during rotor lock or device fault.
1	FGRD_MODE	R/W	0h	Selects functionality of FG/RD pin. 0h = FG speed feedback output 1h = RD rotor lock detection feedback output
0	FGRD_FAULT_SEL	R/W	0h	Selects whether FG/RD pin reports device faults. 0h = FG/RD pin reports rotor lock faults only 1h = FG/RD reports rotor lock, overvoltage, overcurrent, thermal shutdown, and undervoltage fault conditions

7.1.3 START_STOP_CONFIG Register (Offset = 2h) [Reset = 89h]

START_STOP_CONFIG is shown in Table 7-5.

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Table 7-5. START_STOP_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RAMP_ON_STOP_DIS	R/W	1h	Selects whether to ramp duty cycle down to zero while stopping or immediately apply zero duty cycle 0h = Ramp duty cycle down to zero based based on PWM_RAMP_EN, PWM_RAMP_SEL and PWM_DECEL_SEL bits 1h = Immediately Set FETs to HiZ when motor stop command is received
6-5	DINOFF	R/W	0h	Selects threshold of input DC above which output duty cycle will be zero 0h = disabled, no value of input dyty cycle above which DOUT will be 0 1h = When input duty cycle ≥ 90% DOUT will be mapped to 0% 2h = When input duty cycle ≥ 95% DOUT will be mapped to 0% 3h = When input duty cycle equals 100% DOUT will be mapped to 0%
4-2	DOUT_MIN	R/W	2h	Selects minimum value DOUT will be clamped to, if input duty cycle is between DIN0 and DINOFF 0h = 0% 1h = 5% 2h = 10% 3h = 12.5% 4h = 15% 5h = 20% 6h = 25% 7h = 30%
1-0	DOUT_START	R/W	1h	Selects DOUT to be applied when motor starts up. DOUT will be ramped to target duty cycle from this initial value. 0h = 12.5% of DOUT_MAX in Open Loop and 12.5% in Closed Loop 1h = 25% of DOUT_MAX in Open Loop and 25% in Closed Loop 2h = 50% of DOUT_MAX in Open Loop and 50% in Closed Loop 3h = 100% of DOUT_MAX in Open Loop and 100% in Closed Loop

7.1.4 DIN0 Register (Offset = 3h) [Reset = 16h]

DIN0 is shown in Table 7-6.

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Table 7-6. DIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIN0	R/W	16h	Sets the minimum input duty cycle DIN, that the speed curve accepts. DIN = 100%*DIN0/255 0h = 0% 1h = 0.39126% 16h = 8.8% (default) FFh = 100%

7.1.5 DOUT0 Register (Offset = 4h) [Reset = 1Ah]

DOUT0 is shown in Table 7-7.

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Table 7-7. DOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DOUT0	R/W	1Ah	Sets the output duty DOUT when DIN ≤ DIN0 DOUT = 100%*DOUT0/255 0h = 0%, all FETs off, putting the driver in a HiZ state 1h = 0.39126% 1Ah = 10.2% (default) FFh = 100%

7.1.6 DOUT1 Register (Offset = 5h) [Reset = 20h]

DOUT1 is shown in Table 7-8.

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Table 7-8. DOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DOUT1	R/W	20h	Sets the output duty DOUT when DIN = 12.5% DOUT = 100%*DOUT1/255 0h = 0%, both outputs remain low, putting the driver in a brake state 20h = 12.5% (default) FFh = 100%

7.1.7 DOUT2 Register (Offset = 6h) [Reset = 40h]

DOUT2 is shown in Table 7-9.

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Table 7-9. DOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DOUT2	R/W	40h	Sets the output duty DOUT when DIN = 25% DOUT = 100%*DOUT1/255 0h = 0%, both outputs remain low, putting the driver in a brake state 40h = 25% (default) FFh = 100%

7.1.8 DOUT3 Register (Offset = 7h) [Reset = 60h]

DOUT3 is shown in Table 7-10.

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Table 7-10. DOUT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DOUT3	R/W	60h	Sets the output duty DOUT when DIN = 37.5% DOUT = 100%*DOUT1/255 0h = 0%, both outputs remain low, putting the driver in a brake state 60h = 37.5% (default) FFh = 100%

7.1.9 DOUT4 Register (Offset = 8h) [Reset = 80h]

DOUT4 is shown in Table 7-11.

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Table 7-11. DOUT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DOUT4	R/W	80h	Sets the output duty DOUT when DIN = 50% DOUT = 100%*DOUT1/255 0h = 0%, both outputs remain low, putting the driver in a brake state 80h = 50% (default) FFh = 100%

7.1.10 DOUT5 Register (Offset = 9h) [Reset = A0h]

DOUT5 is shown in Table 7-12.

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Table 7-12. DOUT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DOUT5	R/W	A0h	Sets the output duty DOUT when DIN = 62.5% DOUT = 100%*DOUT1/255 0h = 0%, both outputs remain low, putting the driver in a brake state A0h = 62.5% (default) FFh = 100%

7.1.11 DOUT6 Register (Offset = Ah) [Reset = C0h]

DOUT6 is shown in Table 7-13.

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Table 7-13. DOUT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DOUT6	R/W	C0h	Sets the output duty DOUT when DIN = 75% DOUT = 100%*DOUT1/255 0h = 0%, both outputs remain low, putting the driver in a brake state C0h = 75% (default) FFh = 100%

7.1.12 DOUT7 Register (Offset = Bh) [Reset = E0h]

DOUT7 is shown in Table 7-14.

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Table 7-14. DOUT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DOUT7	R/W	E0h	Sets the output duty DOUT when DIN = 87.5% DOUT = 100%*DOUT1/255 0h = 0%, both outputs remain low, putting the driver in a brake state E0h = 87.5% (default) FFh = 100%

7.1.13 DOUT8 Register (Offset = Ch) [Reset = FFh]

DOUT8 is shown in Table 7-15.

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Table 7-15. DOUT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DOUT8	R/W	FFh	Sets the output duty DOUT when DIN = 100% DOUT = 100%*DOUT1/255 0h = 0%, both outputs remain low, putting the driver in a brake state FFh = 100% (default)

7.1.14 HALL_TIME_CONFIG Register (Offset = Dh) [Reset = 00h]

HALL_TIME_CONFIG is shown in Table 7-16.

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Table 7-16. HALL_TIME_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HALL_OS_TIME	R/W	0h	Hall lead/lag time offset. t_{HALL_OS} = HALL_OS*10.24 us, 10.24 us/step 00h = 0 01h = 10.24us 02h = 20.48us

7.1.15 COMMUTATION_CONFIG0 Register (Offset = Eh) [Reset = 00h]

COMMUTATION_CONFIG0 is shown in Table 7-17.

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Table 7-17. COMMUTATION_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FG_MULTIPLIER	R/W	0h	This factor multiplies FG output frequency to keep speed feedback frequency the same when motor pole count changes. 0h = 1/2x 1h = 2/3x 2h = 1x 3h = 2x
5	FG_HALL_RAW_EN	R/W	0h	If this bit is high, then the FG_MULTIPLIER field is applied to the RAW_HALL signal instead of the HALL_OFFSET signal, to drive the FG_RD pin. 0h = HALL_OFFSET signal drives FG_RD pin, based on FG_MULTIPLIER factor 1h = HALL_RAW drives FG_RD pin, based on FG_MULTIPLIER factor. Note: 2/3x option is not valid for HALL_RAW signal.
4-3	COMMUTATION_MODE	R/W	0h	Selects commutation mode for output PWM waveshape. 0h = Square commutation 1h = Soft commutation

Table 7-17. COMMUTATION_CONFIG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	PWM_MODE	R/W	0h	Selects output behavior during OFF times for PWM, current limiting, and demagnetization 0h = Asynchronous mode for PWM, current limiting, and demagnetization 1h = Asynchronous mode for PWM and current limiting; Synchronous mode for demagnetization 2h = Synchronous mode for PWM and current limiting; Asynchronous mode for demagnetization 3h = Synchronous mode for PWM, current limiting, and demagnetization 4h = Synchronous mode for PWM and current limiting; Hybrid mode for demagnetization 5h = Asynchronous mode for PWM and current limiting; Hybrid mode for demagnetization 6h = Hybrid mode for PWM and current limiting; Asynchronous mode for demagnetization 7h = Hybrid mode for PWM, current limiting, and demagnetization

7.1.16 COMMUTATION_CONFIG1 Register (Offset = Fh) [Reset = A0h]

COMMUTATION_CONFIG1 is shown in Table 7-18.

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Table 7-18. COMMUTATION_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM_RAMP_EN	R/W	1h	Enables PWM ramp function 0h = PWM ramp function disabled, input duty cycle applied instantly to DOUT 1h = PWM ramp function enabled, ramp rate set according to PWM_RAMP_SEL bits
6-5	PWM_RAMP_SEL	R/W	1h	The overall time from motor startup for DOUT to ramp from 0 to 100%. This also controls the ramp rate when increasing or decreasing input PWM duty cycle to change speed. 0h = 10.4s (9.6%/s duty cycle ramp rate) 1h = 5.2s (19.2%/s duty cycle ramp rate) 2h = 2.6s (38.5%/s duty cycle ramp rate) 3h = 1.3s (77%/s duty cycle ramp rate)
4-0	SRISE	R/W	0h	Sets the rising ramp for soft commutation. Default is 0 degrees for square commutation. θ_{SRISE} = (SRISE*2.8 degrees)+2.8 degrees 00h = 2.8 degrees 01h = 5.6 degrees 1Fh = 90 degrees

7.1.17 COMMUTATION_CONFIG2 Register (Offset = 10h) [Reset = 20h]

COMMUTATION_CONFIG2 is shown in Table 7-19.

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Table 7-19. COMMUTATION_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	Reserved
5	PWM_DECEL_SEL	R/W	1h	Selects whetehr the ramp rate during deceleration is same as PWM_RAMP_SEL setting or half of that 0h = Deceleration ramp rate set by PWM_RAMP_SEL 1h = Deceleration ramp rate is half of PWM_RAMP_SEL

Table 7-19. COMMUTATION_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	SFALL	R/W	0h	Sets the falling ramp for soft commutation. Default is 0 degrees for square commutation. θ_{SFALL} = (SFALL*2.8 degrees)+2.8 degrees 00h = 2.8 degrees 01h = 5.6 degrees 1Fh = 90 degrees

7.1.18 COMMUTATION_CONFIG3 Register (Offset = 11h) [Reset = 46h]

COMMUTATION_CONFIG3 is shown in Table 7-20.

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Table 7-20. COMMUTATION_CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	AUTO_DEMAG_EN	R/W	1h	Selects fixed or automatic t_{DEMAG} time 0h = Sets t_{DEMAG} according to DEMAG bits 1h = Automatically determines duration of t_{DEMAG} time by detecting the current zero crossing 2h = Reserved 3h = Reserved
5-4	AUTO_DEMAG_STEP	R/W	0h	Step resolution for Auto Demag 0h = 2.56us 1h = 5.12us 2h = 10.24us 3h = 20.48us
3	RESERVED	R/W	0h	Reserved
2-1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

7.1.19 PROTECTION_CONFIG0 Register (Offset = 12h) [Reset = 04h]

PROTECTION_CONFIG0 is shown in Table 7-21.

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Table 7-21. PROTECTION_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPEED_LOOP_EN	R/W	0h	Enables or disables Closed Loop speed control operation 0h = Open Loop operation with input command being target DutyCycle 1h = Closed Loop operation with input command being target Speed
6	OVP_EN	R/W	0h	Enables or disables overvoltage protection 0h = Overvoltage protection disabled 1h = Overvoltage protection enabled
5-4	OVP_SEL	R/W	0h	Selects threshold past which OVP is asserted 0h = 34.5V rising and 33.1V falling 1h = 22.6V rising and 21.1V falling 2h = 18.1V rising and 16.6V falling 3h = No OVP
3	OCP_RETRY_MODE	R/W	0h	Controls whether to retry indefinitely after OCP or stop after 3 consecutive retries 0h = retry indefinitely 1h = retry only 3 times consecutively

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Table 7-21. PROTECTION_CONFIG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	LRD_LONG_RETRY_SEL	R/W	4h	Selects multiplicatier to calculate $t_{lock\_long\_retry}$ from t_{LRD_START} 0h = x 2 1h = x 4 2h = x 8 3h = x 10 4h = x 12 5h = x 16 6h = x 24 7h = x 28

7.1.20 CLOSED_LOOP_CONFIG0 Register (Offset = 13h) [Reset = 00h]

CLOSED_LOOP_CONFIG0 is shown in Table 7-22.

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Table 7-22. CLOSED_LOOP_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_SPEED_LSB	R/W	0h	Sets the 8 LSBs of the 12 bit value representing the maximum electrical speed in Hz device should target, when operating at 100% DutyCycle in Closed loop. Used for calculating the target speed based on the input Duty Cycle observed on the PWM pin as per the equation Target elecrical speed (Hz) = Input duty cycle * MAX_SPEED

7.1.21 CLOSED_LOOP_CONFIG1 Register (Offset = 14h) [Reset = FFh]

CLOSED_LOOP_CONFIG1 is shown in Table 7-23.

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Table 7-23. CLOSED_LOOP_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DOUT_MAX_MSN OR KI_RATIO	R/W	Fh	Open Loop: Sets the Most Significant Nibble of DOUT_MAX, the maximum value DOUT will be clamped to if DIN is between DIN0 and DINOFF. DOUT_MAX has a min clamp of 25% Closed Loop: Sets the 3 bits for KI_RATIO 0h = Kp * 8 1h = Kp * 4 2h = Kp * 2 3h = Kp * 1 4h = Kp/2 5h = Kp/4 6h = Kp/8 7h = Kp/16
3-0	DOUT_MAX_LSN OR MAX_SPEED_MSN	R/W	Fh	Open Loop: Sets the Least Significant Nibble of DOUT_MAX, the maximum value DOUT will be clamped to if DIN is between DIN0 and DINOFF. DOUT_MAX has a min clamp of 25% Closed Loop: Sets the 4 MSBs of the 12 bit value representing the maximum electrical speed in Hz device should target, when operating at 100% DutyCycle in Closed loop. Used for calculating the target speed based on the input Duty Cycle observed on the PWM pin as per the equation Target elecrical speed (Hz) = Input duty cycle * MAX_SPEED

7.1.22 CLOSED_LOOP_CONFIG2 Register (Offset = 15h) [Reset = 02h]

CLOSED_LOOP_CONFIG2 is shown in Table 7-24.

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Table 7-24. CLOSED_LOOP_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LRD_NRETRY_STARTUP	R/W	0h	Number of retries for very first start-up attempt after wakeup from reset or SLEEP or STBY, before enforcing a long retry period tlock_long_retry. 0h = Just one retry attempt in first set of retry attempts 1h = Two retry attempts in first set of retry attempts 2h = Three retry attempts in first set of retry attempts 3h = Four retry attempts in first set of retry attempts
5-4	LRD_NRETRY_RUN	R/W	0h	Number of retries for subsequent start-up attempts after first start-up attempt, post wakeup from reset or SLEEP or STBY, before enforcing a long retry period tlock_long_retry. 0h = Just one retry attempt in subsequent set of retry attempts 1h = Two retry attempts in subsequent set of retry attempts 2h = Three retry attempts in subsequent set of retry attempts 3h = Four retry attempts in subsequent set of retry attempts
3	DEADTIME_SEL	R/W	0h	Reduced deadtime duration from 600ns to 520ns 0h = Deadtime is 600ns 1h = Deadtime is 520ns
2-0	KP_RATIO	R/W	2h	Proportional component in the Closed Loop Speed Controller. 0h = 8/fMax 1h = 4/fMax 2h = 2/fMax 3h = 1/fMax 4h = 1/(2*fMax) 5h = 1/(4*fMax) 6h = 1/(8*fMax) 7h = 1/(16*fMax)

7.1.23 PROTECTION_CONFIG1 Register (Offset = 16h) [Reset = 44h]

PROTECTION_CONFIG1 is shown in Table 7-25.

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Table 7-25. PROTECTION_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OVP_BLANK_SEL	R/W	0h	Selects the duration of blanking to be applied in during peak duty cycle phase. 0h = Blanking active after 1ms 1h = Blanking active after 4ms
6	OVP_BLANK_EN	R/W	1h	Enables or disables the OVP Blanking time duting the peak duty cycle phase 0h = No OVP blanking in Peak duty cycle phase and blanking will only be active for SRISE and SFALL phases 1h = OVP blanking in Peak duty cycle phase according to OVP_BLANK_SEL in addition to SRISE and SFALL phases
5	OCP_DEGLITCH_SEL	R/W	0h	Selects deglitch time for OCP 0h = OCP deglitch time is 500ns 1h = OCP deglitch time is 1us
4	RESERVED	R/W	0h	Reserved
3-2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	DITHER_EN	R/W	0h	Enables dithering of internal oscillator and therefore output PWM when set high 0h = Dithering disabled 1h = Dithering enabled

7.1.24 GENERAL_CONFIG1 Register (Offset = 17h) [Reset = 46h]

GENERAL_CONFIG1 is shown in Table 7-26.

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Table 7-26. GENERAL_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HALL_INVERT	R/W	0h	This bit inverts the Hall offset signal to the commutation block. 0h = Non-inverted Hall latch signal 1h = Inverted Hall latch signal
6	HALL_TIME_MODE	R/W	1h	Hall offset time lead/lag select bit 0h = The Hall offset signal lags the Hall latch output signal by t_{HALL_OS} 1h = The Hall offset signal leads the Hall latch output signal by t_{HALL_OS}
5-4	LRD_TIME_STARTUP	R/W	0h	Selects the locked rotor detection time t_{LRD_START} at start-up. Also used to calculate $t_{lock\_long\_retry}$ from 0h = 325ms 1h = 440ms Ah = 524ms Bh = 1.05s
3-0	ILIMIT_SEL	R/W	6h	Selects the current limit threshold. Only values from 0h to 9h are valid. 0h = 0.33 A 1h = 0.44 A 2h = 0.55 A 3h = 0.66 A 4h = 0.77 A 5h = 0.88 A 6h = 0.99 A 7h = 1.10 A 8h = 1.21 A 9h = 1.32 A

7.1.25 GENERAL_CONFIG2 Register (Offset = 18h) [Reset = 81h]

GENERAL_CONFIG2 is shown in Table 7-27.

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Table 7-27. GENERAL_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VM_CLAMP_DIS	R/W	1h	Disables the VM Clamp feature 0h = VM Clamp enabled 1h = VM Clamp disabled
6	HALL_ANGLE_MODE	R/W	0h	Selects whether the angle component of Hall Offset is to be applied in leading or lagging direction 0h = The Hall offset signal leads the Hall latch output signal by $\theta_{HALL\_OS\_ANGLE}$ 1h = The Hall offset signal lags the Hall latch output signal by $\theta_{HALL\_OS\_ANGLE}$
5-1	HALL_OS_ANGLE	R/W	0h	The angle component of Hall Offset 0h = 0 degrees 1h = 1.4 degrees 1Fh = 43.6 degrees
0	PRESTART_RAMP_EN	R/W	1h	Enables prestart PWM ramp function 0h = Prestart ramp function disabled, input duty cycle applied instantly to DOUT 1h = Prestart ramp function enabled, ramp rate set according to PWM_RAMP_SEL bits

7.1.26 GENERAL_CONFIG3 Register (Offset = 19h) [Reset = 24h]

GENERAL_CONFIG3 is shown in Table 7-28.

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Table 7-28. GENERAL_CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SILENCE_ANGLE	R/W	2h	Sets the angle duration for silence at beginning of commutation 0h = 0.0 1h = 1.4 2h = 2.8 3h = 4.2 4h = 5.6 5h = 7.0 6h = 8.4 7h = 9.8 8h = 11.3 9h = 12.7 10h = 14.1 11h = 15.5 12h = 16.9 13h = 18.3 14h = 19.7 15h = 21.1
3-2	POLE_PAIR	R/W	1h	Indicates number of pole pairs in the rotor 0h = One pole pair 1h = Two pole pairs 2h = Three pole pairs 3h = Four pole pairs
1	LRD_RETRY_DIS	R/W	0h	Disables retries after 5 consecutive attempts whrn locked rotor is detected 0h = Infinite number of retries 1h = Retries limited to 5
0	PWRUP_PWMDC_MASK	R/W	0h	Masks input speed command at the PWM pin for 1s during initial power up from reset condition 0h = No masking at PWM pin input 1h = Masks PWM pin input for 1s during initial power up enabled

7.1.27 GENERAL_CONFIG4 Register (Offset = 1Ah) [Reset = 08h]

GENERAL_CONFIG4 is shown in Table 7-29.

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Table 7-29. GENERAL_CONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	DEMAG_TIME	R/W	4h	Sets the DEMAG time 0h = 0us 1h = 10.24us 2h = 20.48us 3Fh = 645.12us 7Fh = 1.29ms
0	SILENCE_MODE	R/W	0h	Selects the state of output FETs during silence phase 0h = All FETs in HiZ during silence phase 1h = Asyncronous mode in SILENCE phase

7.1.28 USR_OTP_CRC Register (Offset = 1Bh) [Reset = 00h]

USR_OTP_CRC is shown in Table 7-30.

Return to the Summary Table.

Table 7-30. USR_OTP_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	USR_OTP_CRC	R/W	0h	CRC value calculated over USR_OTP registers

7.2 USR_TM Registers

Table 7-31 lists the memory-mapped registers for the USR_TM registers. All register offset addresses not listed in Table 7-31 should be considered as reserved locations and the register contents should not be modified.

Table 7-31. USR_TM Registers

Offset	Acronym	Register Name	Section
20h	TEST_FAULT	Register to test for Fault	Section 7.2.1
21h	TEST_DIN	Input Duty Cycle Control	Section 7.2.2
22h	TEST_FAULT_STATUS	Register to indicate Fault type	Section 7.2.3
23h	TEST_SPEED_MSB	Speed Feedback	Section 7.2.4
24h	TEST_SPEED_LSB	Speed Feedback	Section 7.2.5
25h	USR_OTP_CFG	Register to configure USR_OTP Programming	Section 7.2.6
26h	USR_OTP_PRG_UNLOCK	Unlock access to program or verify USR_OTP	Section 7.2.7

Complex bit access types are encoded to fit into small table cells. Table 7-32 shows the codes that are used for access types in this section.

Table 7-32. USR_TM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W0C	W 0C	Write 0 to clear
Reset or Default Value		
-n		Value after reset or the default value

7.2.1 TEST_FAULT Register (Offset = 20h) [Reset = 00h]

TEST_FAULT is shown in Table 7-33.

Return to the Summary Table.

Table 7-33. TEST_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FAULT	R	0h	Reading this bit indicates that the device is in a fault mode (OCP, OVP, UVLO, Rotor Lock, TSD). Current limiting operation does not report on this bit. 0h = Active mode 1h = Fault mode
6-0	RESERVED	R	0h	Reserved

7.2.2 TEST_DIN Register (Offset = 21h) [Reset = 01h]

TEST_DIN is shown in Table 7-34.

Return to the Summary Table.

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Table 7-34. TEST_DIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIN_CNTRL	R/W	1h	Writing to this register sets the inpit duty cycle DIN to control speed while the PWM pin is not available in I2C. DIN = DIN_CTRL/255 0h = 0% (default) A0h = 62.5% FFh = 100%

7.2.3 TEST_FAULT_STATUS Register (Offset = 22h) [Reset = 00h]

TEST_FAULT_STATUS is shown in Table 7-35.

Return to the Summary Table.

Table 7-35. TEST_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	RESERVED	R/W0C	0h	Reserved
4	TSD	R/W0C	0h	Reading this bit indicates that the device is in temperature shutdown (TSD) protection. 0h = Normal operation 1h = TSD fault
3	UVLO	R	0h	Reading this bit indicates that the device is in undervoltage (UVLO). 0h = Normal operation 1h = UVLO fault
2	OVP	R/W0C	0h	Reading this bit indicates that the device is in overvoltage protection (OVP). 0h = Normal operation 1h = OVP fault
1	LRP	R	0h	Reading this bit indicates that the device is in locked rotor protection (LRP). 0h = Normal operation 1h = LRP fault
0	OCP	R/W0C	0h	Reading this bit indicates that the device in overcurrent protection. 0h = Normal operation 1h = OCP fault

7.2.4 TEST_SPEED_MSB Register (Offset = 23h) [Reset = 00h]

TEST_SPEED_MSB is shown in Table 7-36.

Return to the Summary Table.

Table 7-36. TEST_SPEED_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ELECTRICAL_PERIOD_MSB	R	0h	Reading this register provides the period of the motor's electrical cycle. This helps provide speed feedback during test mode since the FG pin is not available. Formula for Electrical Half Cycle Duration is 10.24us * ((ELECTRICAL_PERIOD_MSB << 8) + (ELECTRICAL_PERIOD)) Total Electrical Period would be twice the value calculated above

7.2.5 TEST_SPEED_LSB Register (Offset = 24h) [Reset = 00h]

TEST_SPEED_LSB is shown in Table 7-37.

Return to the Summary Table.

Table 7-37. TEST_SPEED_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ELECTRICAL_PERIOD_LSB	R	0h	Reading this register provides the period of the motor's electrical cycle. This helps provide speed feedback during test mode since the FG pin is not available. Formula in ELECTRICAL_PERIOD_MSB bit field description..

7.2.6 USR_OTP_CFG Register (Offset = 25h) [Reset = 00h]

USR_OTP_CFG is shown in Table 7-38.

Return to the Summary Table.

Table 7-38. USR_OTP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	USR_OTP_CRC_ERR	R	0h	Status of USR_OTP_CRC check 0h = No CRC error 1h = CRC err
6	DEVICE_OTP_CRC_ERR	R	0h	Status of DEVICE OTP CRC computed for DEVICE OTP contents 0h = No CRC error 1h = CRC err
5	RESERVED	R/W	0h	Reserved
4-3	USR_OTP_PAGE_USED	R	0h	Indicates the origin of the data used for any loading of USR_OTP Shadow Registers 0h = Shadow Registers not loaded from either of the USR_OTPs so far. This implies that USR_OTP1 was sensed to be unprogrammed on power-up. 1h = Latest load of Shadow Registers was from USR_OTP1 2h = Latest load of Shadow Registers was from USR_OTP2. 3h = Invalid combination which is not expected.
2	USR_OTP_PAGE_SEL	R/W	0h	This bit indicates whether first USR_OTP page (USR_OTP1) is targeted for commanded operation, or second USR_OTP page (USR_OTP2) is targeted. 0h = USR_OTP1 1h = USR_OTP2
1	USR_OTP_PROG_VERIFY	R/W	0h	Reserved
0	USR_OTP_PROG_ALL	R/W	0h	Write 1h to this bit to program the USR_OTP page according to USR_OTP_PAGE_SEL

7.2.7 USR_OTP_PRG_UNLOCK Register (Offset = 26h) [Reset = 00h]

USR_OTP_PRG_UNLOCK is shown in Table 7-39.

Return to the Summary Table.

Table 7-39. USR_OTP_PRG_UNLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2-0	USR_OTP_PROG_UNLOCK	R	0h	User needs to write a sequence of 2h,1h,4h to this bits in successive write-frames, to unlock access to USR_OTP programming or program-verify operations

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The MC121-Q1 can be used to drive Single Phase Brushless-DC motors. The following design procedure can be used to interface the MC121-Q1.

8.1.1 External Components

This section presents recommended external components for the MC121-Q1 in a fan application.

Supply Components

Figure 8-1 shows typical components used on the supply connection in a fan module. The D_1 diode in series with the power supply protects the MC121-Q1 in case of accidental reverse supply connection. A power supply decoupling capacitor is required for proper functioning of MC121-Q1 and a minimum value of 0.1 uF is recommended. The optional bulk capacitor, C_{BULK}, placed near the VM pin helps to stabilize the V_{VM} supply voltage during motor operation. A ceramic capacitor with low electrical series resistance (ESR) and a voltage rating twice the supply voltage is recommended to provide margin during transients. A capacitance value between 1 µF and 10 µF based on application is recommended.

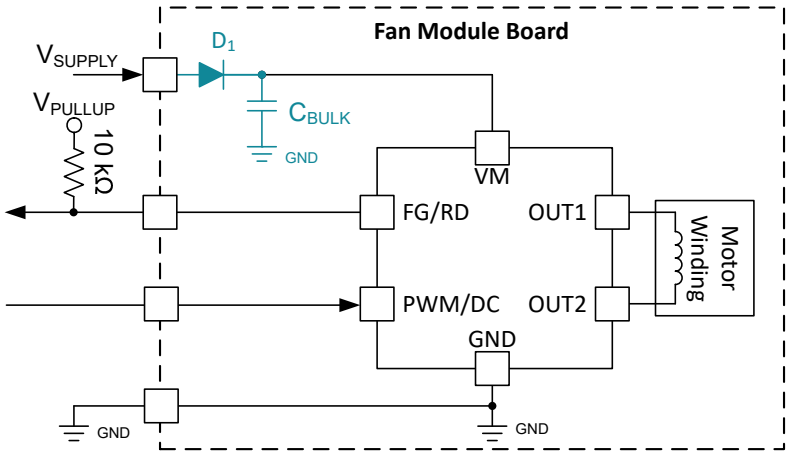

Figure 8-1. Typical Fan Module External Components

Motor systems requiring large motor currents and high rotor inertia can experience high currents flowing into the VM node from the H-bridge due to stored inductor energy during commutation. The additional charge in the C_{BULK} capacitor increases the V_{VM} supply voltage. Although the MC121-Q1 has overvoltage protection, adding protective clamp components on the supply rail can reduce the magnitude of voltage spikes. These components can also help protect against ESD strikes on the supply.

Figure 8-2 shows an example using a Zener diode or TVS diode (D_2) on the VM node. The diode clamping voltage needs to be higher than the fan system maximum operating voltage and lower than the MC121-Q1 maximum operating voltage from the Recommended Operating Conditions table. An RC snubber on the supply also can protect the driver against voltage spikes and ESD (Figure 8-3). TI recommends using 1 µF for $C_{SNUBBER}$ and 2 Ω for $R_{SNUBBER}$. Alternatively, an electrolyic capacitor can be used in parallel with C_{BULK}.

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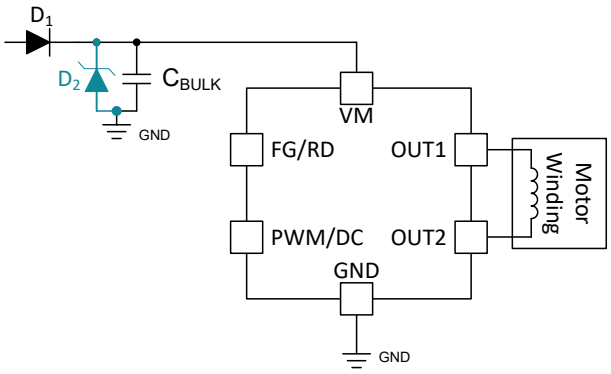

Figure 8-2. Clamping Diode on VM

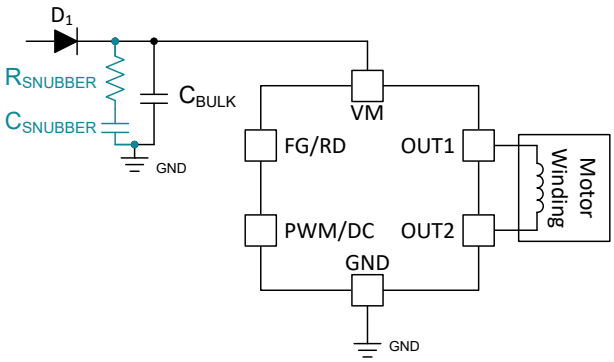

Figure 8-3. Snubber on VM

PWM and FG/RD Pin Components

Figure 8-1 shows the minimal external components needed for fan module PWM control and speed/fault feedback. The FG/RD pin is an open drain output and requires an external pull-up resistor to provide an output signal at the proper voltage. The pull-up resistor value must be chosen to limit the current into the FG/RD pin to less than 5 mA when the open drain output asserts low. Adding resistors inline with the PWM input and FG/RD output can help protect the driver from ESD strikes on the connector wires, as shown in Figure 8-4. Clamping or TVS diodes on the FG/RD and PWM signals provides additional protection against ESD strikes as shown in Figure 8-5.

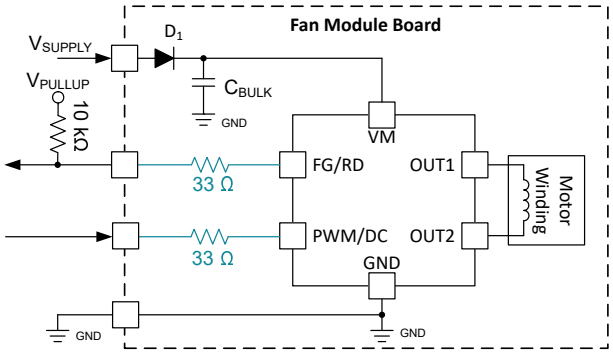

Figure 8-4. Resistors on PWM and FG/RD

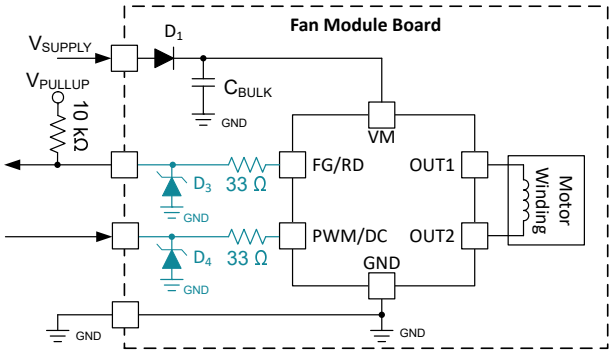

Figure 8-5. Resistors and zener diodes on PWM and FG/RD

Some single phase fan modules require an open-collector interface for the FG/RD and PWM pins. Figure 8-6 and Figure 8-7 show examples for connecting components inside and outside of the fan module for the open-collector interface.

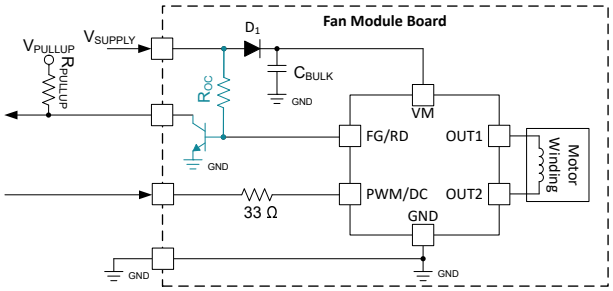

Figure 8-6. Open Collector on FG/RD

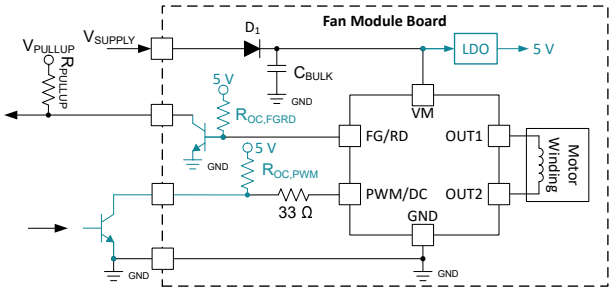

Figure 8-7. Open Collector on PWM and FG/RD

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OTP and Test Mode Programming

The MC121-Q1 supports an I²C interface on the FG/RD and PWM pins in OTP (one-time programmable) mode. The OTP mode allows the designer to test various device settings and program the device OTP in production. Figure 8-8 shows an example of the external component connections for the MC121-Q1 for device programming. Additional details on OTP and test mode programming are in Section 6.4.4.

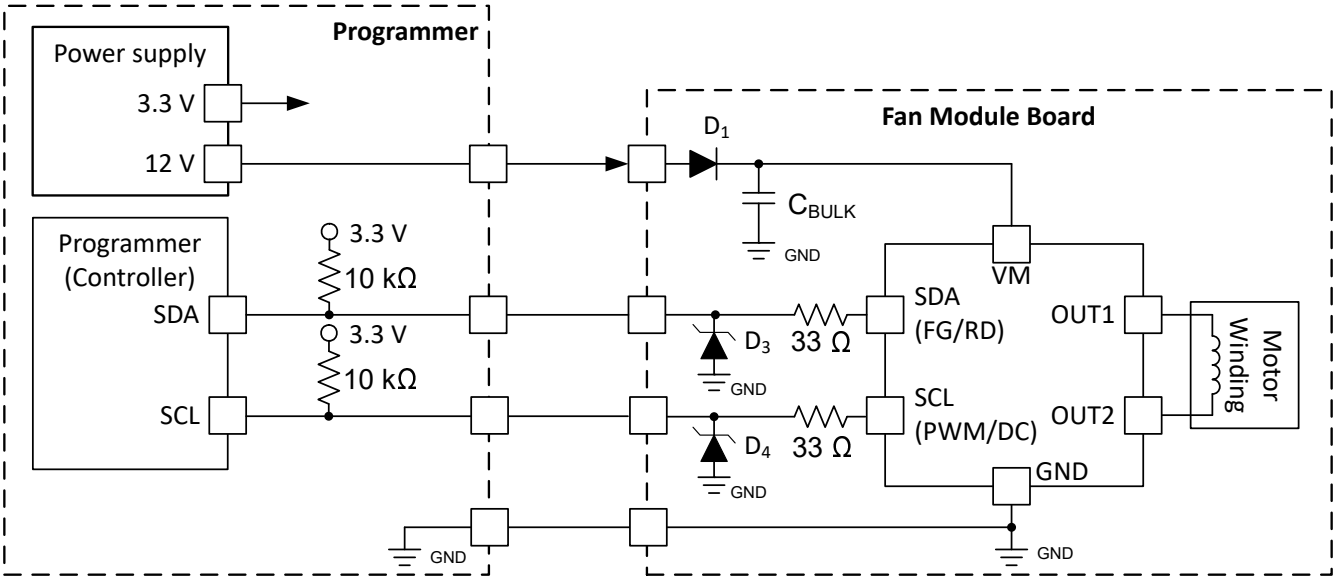

Figure 8-8. OTP Memory Programmer and Fan Module

8.2 Typical Application

8.2.1 Design Requirements

Single Phase Brushless-DC Motor Control With Current Limit

In this application, the MC121-Q1 is used to drive a single phase brushless-DC motor with current limit up to 100% duty cycle. The following design procedure can be used to configure the MC121-Q1 in current limit mode.

Table 8-1 lists the example input parameters for the system design.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage	12V
Motor peak current	1.2A
Speed Input type	PWM (0% to 100% duty), 50Hz
FG/RD pin function	Assert high when rotor lock fault
Commutation shape	Square

8.2.2 Detailed Design Procedure

Motor Voltage

Single phase Brushless-DC motors are typically rated for a certain voltage (for example 12 V or 24 V). Operating a motor at a higher voltage corresponds to a lower drive current to obtain the same motor power. A higher operating voltage also corresponds to a higher obtainable rpm. The MC121-Q1 allows for a range of possible operating voltages from 3.2V to 35V.

Device configuration settings

Default OTP configuration for MC121-Q1 is listed in Table 7-1 . Default values are chosen for reliable motor startup and closed loop operation. Refer toMC121-Q1 tuning and programming guide which provides step by step procedure to tune a single-phase BLDC motor in both open loop and closed loop configurations, and explore features in the device.

Table 8-2. Recommended OTP configuration Values (changes from default)

Register Values Name	Recommended Value
PWM_IN_RANGE	1h
FGRD_INVERT	1h
FGRD_MODE	1h
PWM_MODE	7h
SILENCE_ANGLE	4h
ILIMIT_SEL	9h

Once the device OTP is programmed with the desired configuration, device can be operated stand-alone and I^2C serial interface is not required anymore. Speed can be commanded using PWM/DC pin and locked rotor faults can be monitored using the FG/RD pin.

Power Dissipation and Junction Temperature Losses

To calculate the junction temperature of the MC121-Q1 from power losses, use Equation 1. Note that the thermal resistance θ_{JA} depends on PCB configurations such as the ambient temperature, numbers of PCB layers, copper thickness on top and bottom layers, and the PCB area.

$$T_J[℃] = P_{loss}[W] \times \theta_{JA}\left[\frac{℃}{W}\right] + T_A[℃] \quad (1)$$

8.2.3 Application Curves

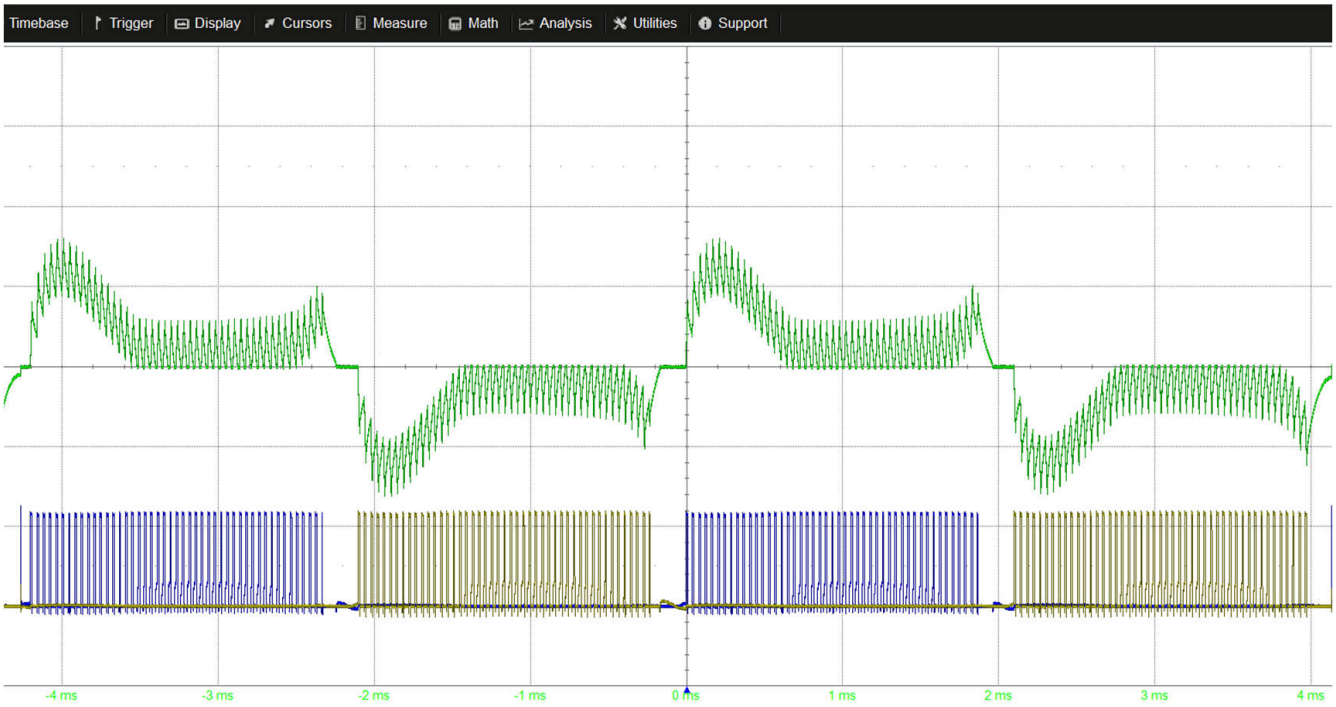

Figure 8-9. OUTx voltage and phase current at PWM input = 25%

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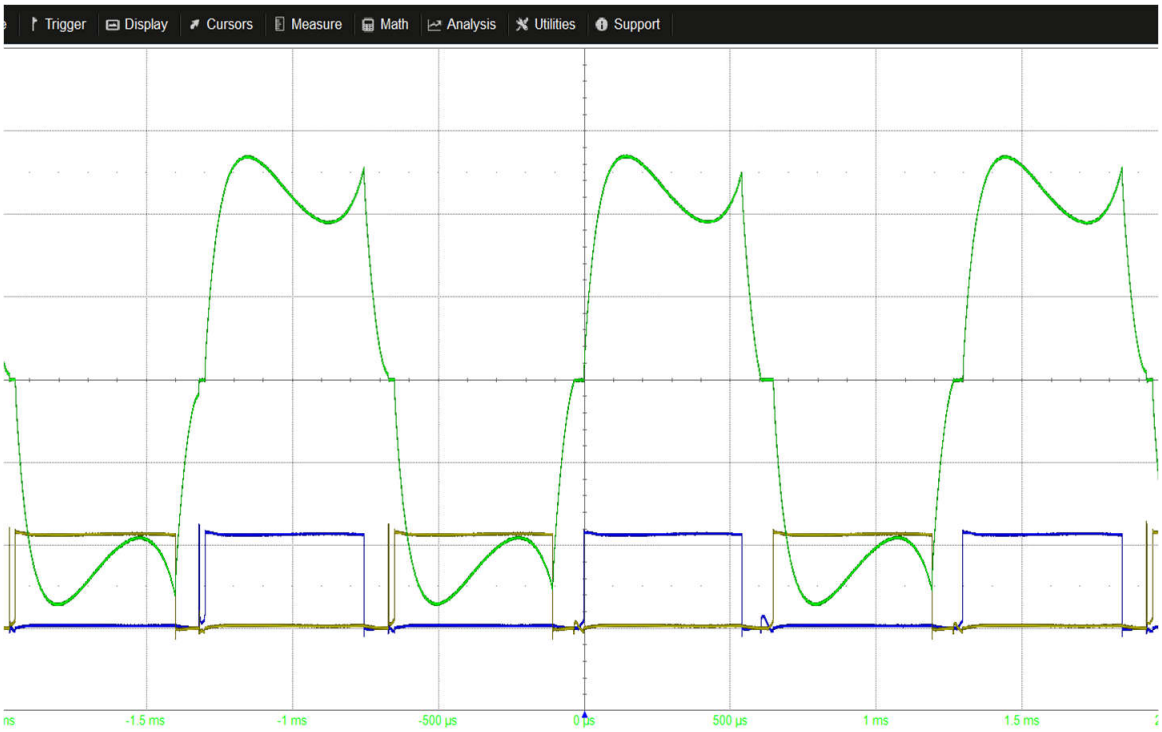

Figure 8-10. OUTx voltage and phase current at PWM input = 100%

8.3 Power Supply Recommendations

8.3.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The motor stop or braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

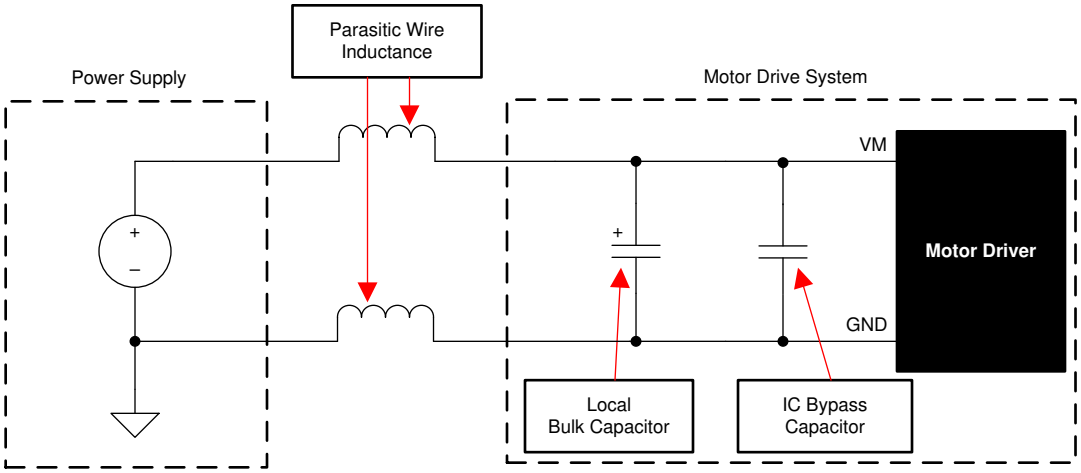

Figure 8-11. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors can be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

8.4 Layout

8.4.1 Layout Guidelines

The bulk capacitor can be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize parasitic inductance and allow the bulk capacitor to deliver high current.

The device bypass capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Figure 8-12 shows a layout example for the MC121-Q1 in DEX package. For proper motor commutation, the MC121-Q1 must be placed between two of the stator poles with the Hall element directly beneath the rotor magnet. Figure 8-13 shows the placement example for DYM package

ADVANCE INFORMATION

8.4.2 Layout Example

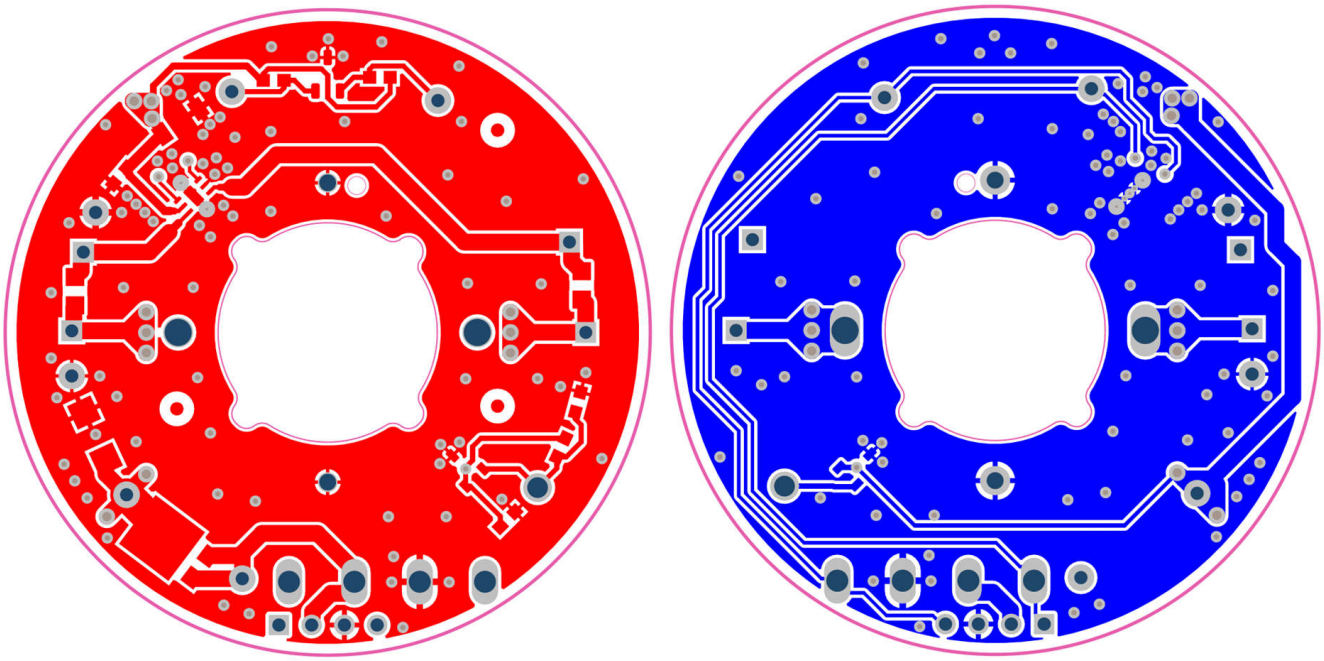

Figure 8-12. Recommended Example Layout for DEZ package

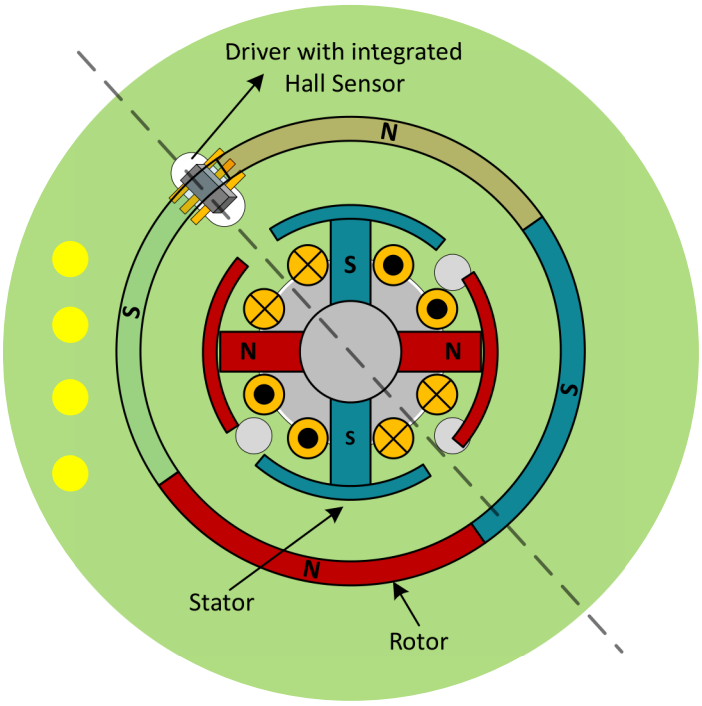

Figure 8-13. Recommended Example Placement for DYM package

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

9.1 Device Support

9.2 Documentation Support

9.2.1 Related Documentation

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2025	*	Initial Release

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PMC121QDEZRQ1	Active	Preproduction	X2SON (DEZ) | 6	5000 | LARGE T&R	-	Call TI	Level-1-260C-UNLIM	-40 to 125	P2BQ
PMC121QDYMRQ1	Active	Preproduction	SOT-23-THIN (DYM) | 6	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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Last updated 10/2025