

## PRECISION MICROPOWER SHUNT VOLTAGE REFERENCE

Check for Samples: [LM4040-EP](#)

### FEATURES

- Fixed Output Voltage of 2.5 V
- Tight Output Tolerances and Low Temperature Coefficient
  - Max 0.65%, 100 ppm/ $^{\circ}\text{C}$
- Low Output Noise: 35  $\mu\text{V}_{\text{RMS}}$  Typ
- Wide Operating Current Range: 45  $\mu\text{A}$  Typ to 15 mA
- Stable With All Capacitive Loads; No Output Capacitor Required

### APPLICATIONS

- Data-Acquisition Systems
- Power Supplies and Power-Supply Monitors
- Instrumentation and Test Equipment
- Process Controls
- Precision Audio
- Automotive Electronics
- Energy Management
- Battery-Powered Equipment

### DESCRIPTION/ORDERING INFORMATION

The LM4040 series of shunt voltage references are versatile, easy-to-use references that cater to a vast array of applications. The 2-pin fixed-output device requires no external capacitors for operation and is stable with all capacitive loads. Additionally, the reference offers low dynamic impedance, low noise, and low temperature coefficient to ensure a stable output voltage over a wide range of operating currents and temperatures. The LM4040 uses fuse and Zener-zap reverse breakdown voltage trim during wafer sort to offer an output voltage tolerance of 0.65%.

Packaged in a space-saving SOT-23-3 package and requiring a minimum current of 45  $\mu\text{A}$  (typ), the LM4040 also is ideal for portable applications. The LM4040C25 is characterized for operation over an ambient temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	DEVICE GRADE	$V_{KA}$	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	0.65% initial accuracy and 100 ppm/ $^{\circ}\text{C}$ temperature coefficient	2.5 V	SOT-23-3 (DBZ)	Reel of 250	LM4040C25MDBZTEP	SAGU

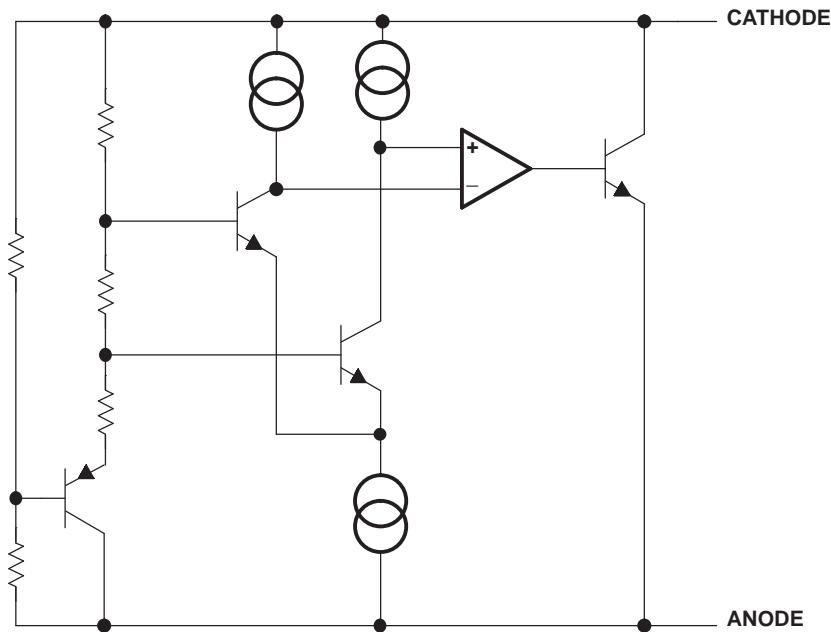
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) The actual top-side marking has one additional character that designates the wafer fab/assembly site.



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## FUNCTIONAL BLOCK DIAGRAM



## Absolute Maximum Ratings<sup>(1)</sup>

over free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$I_Z$	Continuous cathode current	–10	25	mA
$T_J$	Operating virtual junction temperature		150	°C
$T_{stg}$	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>	LM4040	UNITS
	DBZ	
	3 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	320.8
$\theta_{JC}$	Junction-to-case thermal resistance	98.2
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(3)</sup>	53.3
$\Psi_{JT}$	Junction-to-top characterization parameter <sup>(4)</sup>	3.3
$\Psi_{JB}$	Junction-to-board characterization parameter <sup>(5)</sup>	51.8

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).

## Recommended Operating Conditions

		MIN	MAX	UNIT
I <sub>Z</sub>	Cathode current	See <sup>(1)</sup>	15	mA
T <sub>A</sub>	Free-air temperature	–55	125	°C

(1) See parametric tables

## Electrical Characteristics

at extended temperature range, full-range T<sub>A</sub> = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
V <sub>Z</sub>	I <sub>Z</sub> = 100 μA	25°C		2.5		V
ΔV <sub>Z</sub>	I <sub>Z</sub> = 100 μA	25°C	–16	16		mV
		Full range	–42	42		
I <sub>Z,min</sub>		25°C		45	75	μA
		Full range			82	
α <sub>VZ</sub>	I <sub>Z</sub> = 10 mA	25°C		±20		ppm/°C
		25°C		±15		
		Full range			±100	
		25°C		±15		
ΔV <sub>Z</sub> ΔI <sub>Z</sub>	I <sub>Z,min</sub> < I <sub>Z</sub> < 1 mA	25°C	0.3	0.8		mV
		Full range		1.1		
		25°C	2.5	6		
		Full range		9		
Z <sub>Z</sub>	I <sub>Z</sub> = 1 mA, f = 120 Hz, I <sub>AC</sub> = 0.1 I <sub>Z</sub>	25°C		0.3		Ω
e <sub>N</sub>	I <sub>Z</sub> = 100 μA, 10 Hz ≤ f ≤ 10 kHz	25°C		35		μV <sub>RMS</sub>
	t = 1000 h, T <sub>A</sub> = 25°C ± 0.1°C, I <sub>Z</sub> = 100 μA				120	ppm
V <sub>HYST</sub>	Thermal hysteresis <sup>(1)</sup>	ΔT <sub>A</sub> = –55°C to 125°C			0.08	%

(1) Thermal hysteresis is defined as V<sub>Z,25°C</sub> (after cycling to –55°C) – V<sub>Z,25°C</sub> (after cycling to 125°C).

### TYPICAL CHARACTERISTICS

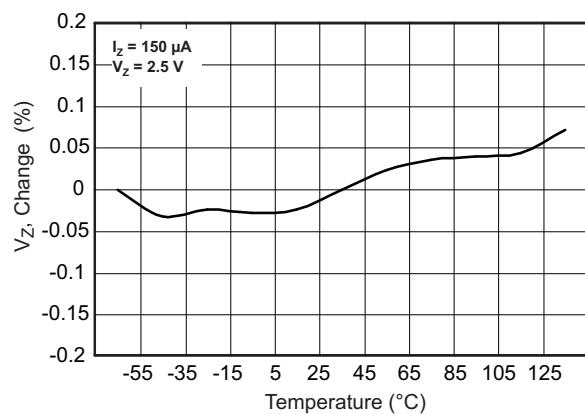
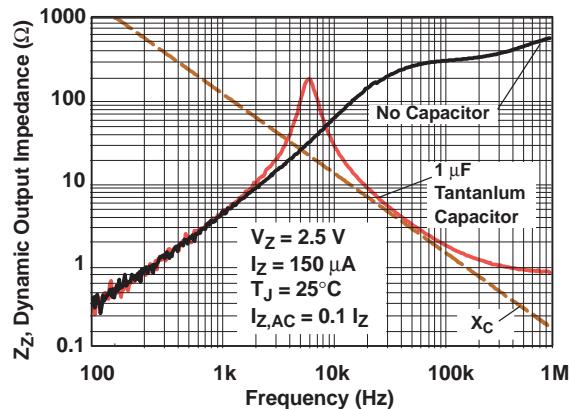
Figure 1. Change in  $V_Z$  vs Change in Temperature

Figure 2. Output Impedance vs Frequency

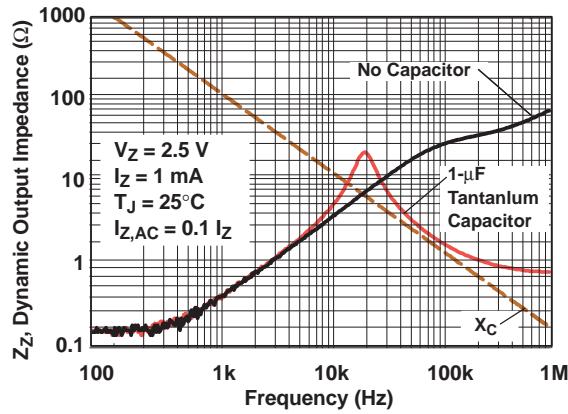


Figure 3. Output Impedance vs Frequency

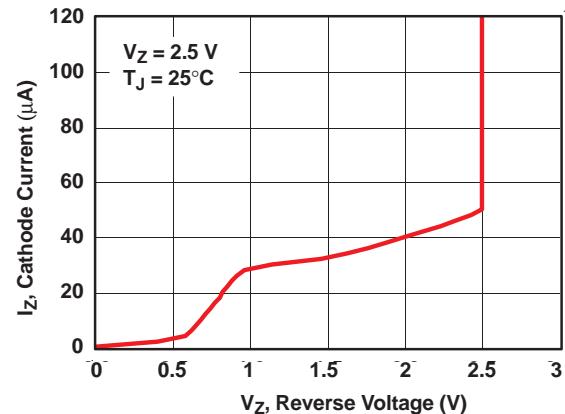


Figure 4. Cathode Current vs Reverse Voltage

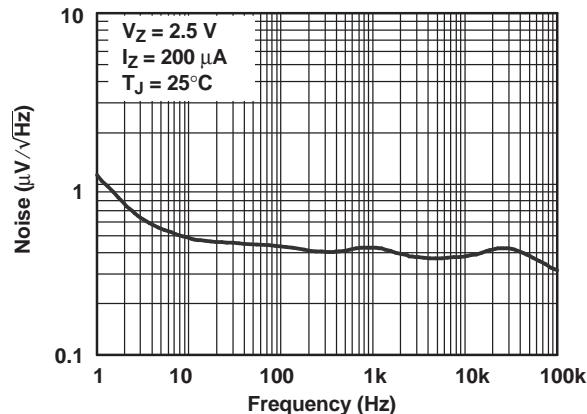


Figure 5. Noise Voltage vs Frequency

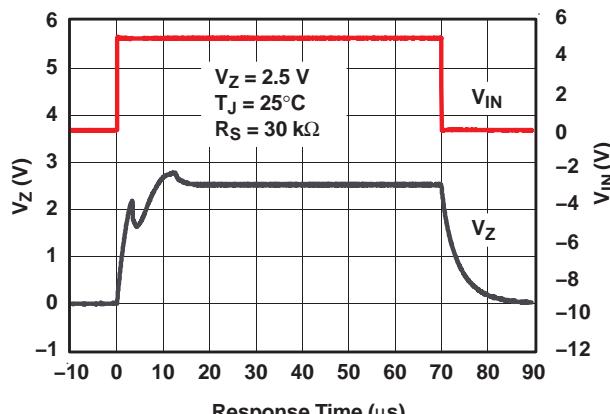
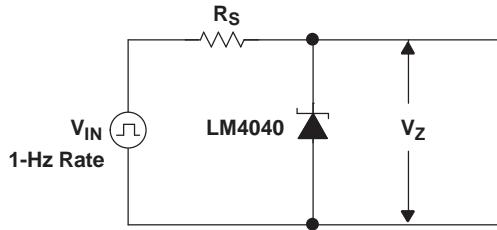


Figure 6. Start-Up Characteristics

## APPLICATION INFORMATION

### Start-Up Characteristics



**Figure 7. Test Circuit**

### Output Capacitor

The LM4040 does not require an output capacitor across cathode and anode for stability. However, if an output bypass capacitor is desired, the LM4040 is designed to be stable with all capacitive loads.

### SOT-23 Connections

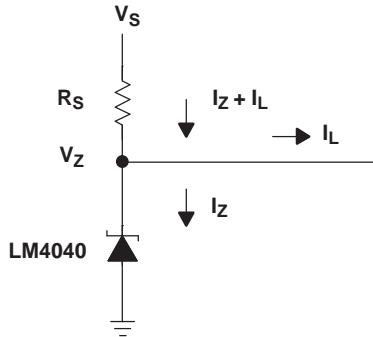
There is a parasitic Schottky diode connected between pins 2 and 3 of the SOT-23 packaged device. Thus, pin 3 of the SOT-23 package must be left floating or connected to pin 2.

### Cathode and Load Currents

In a typical shunt-regulator configuration (see [Figure 8](#)), an external resistor,  $R_S$ , is connected between the supply and the cathode of the LM4040.  $R_S$  must be set properly, as it sets the total current available to supply the load ( $I_L$ ) and bias the LM4040 ( $I_Z$ ). In all cases,  $I_Z$  must stay within a specified range for proper operation of the reference. Taking into consideration one extreme in the variation of the load and supply voltage (maximum  $I_L$  and minimum  $V_S$ ),  $R_S$  must be small enough to supply the minimum  $I_Z$  required for operation of the regulator, as given by data-sheet parameters. At the other extreme, maximum  $V_S$  and minimum  $I_L$ ,  $R_S$  must be large enough to limit  $I_Z$  to less than its maximum-rated value of 15 mA.

$R_S$  is calculated according to [Equation 1](#):

$$R_S = \frac{(V_S - V_Z)}{(I_L + I_Z)} \quad (1)$$



**Figure 8. Shunt Regulator**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4040C25MDBZTEP	Active	Production	SOT-23 (DBZ)   3	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SAGU
LM4040C25MDBZTEP.A	Active	Production	SOT-23 (DBZ)   3	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SAGU
V62/11615-01XE	Active	Production	SOT-23 (DBZ)   3	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SAGU

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

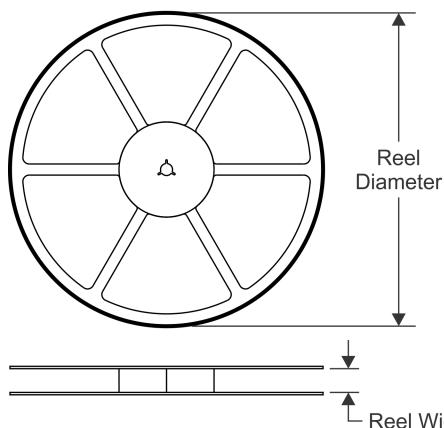
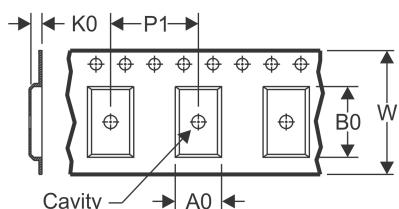
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

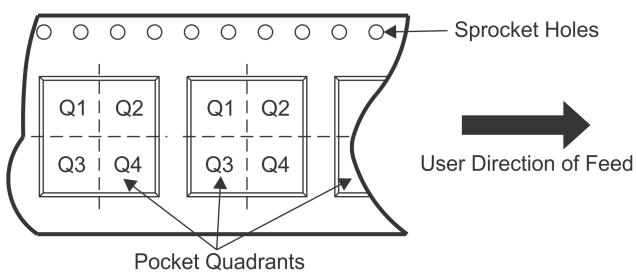
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4040C25MDBZTEP	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

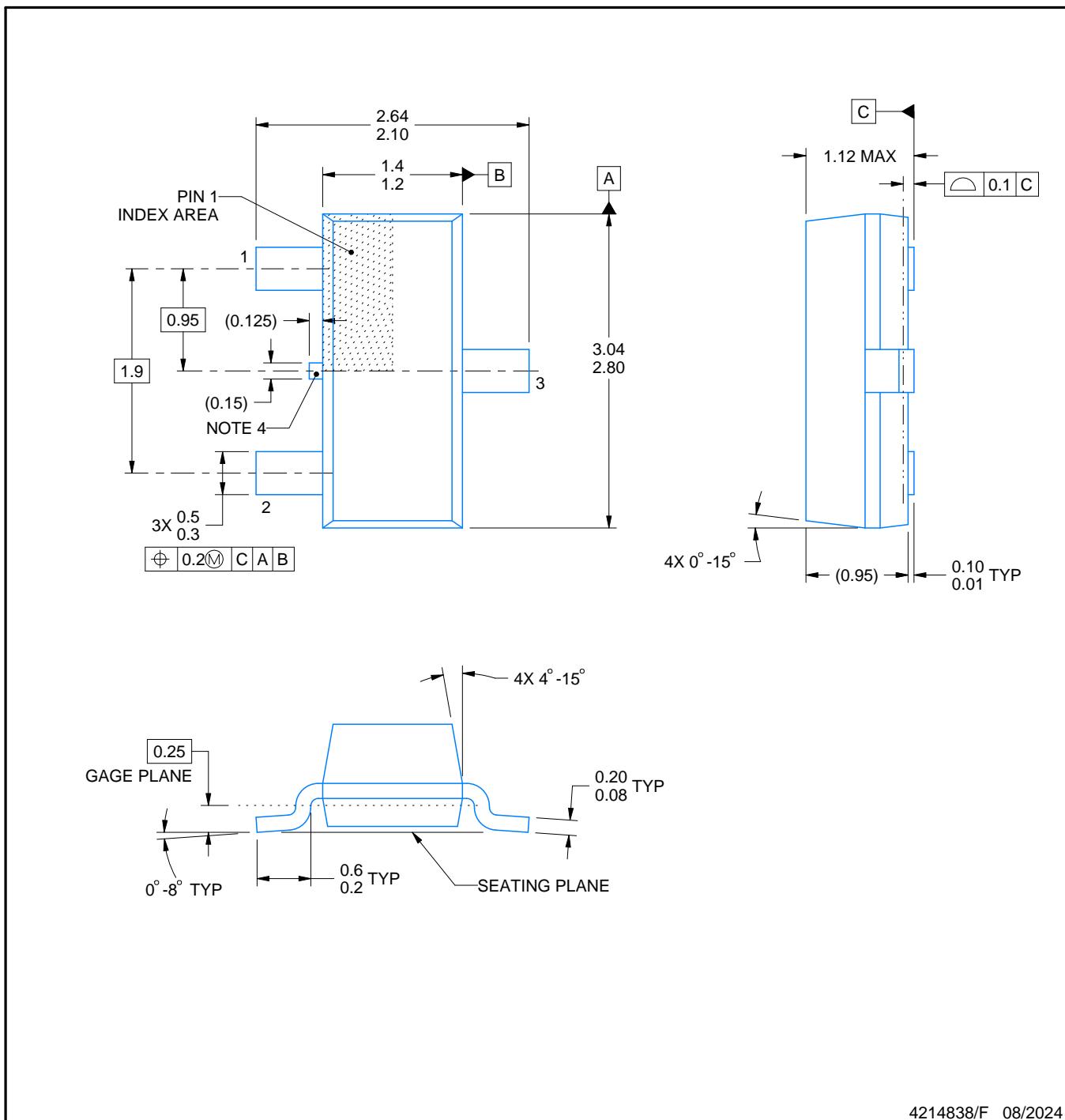
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4040C25MDBZTEP	SOT-23	DBZ	3	250	200.0	183.0	25.0

# PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

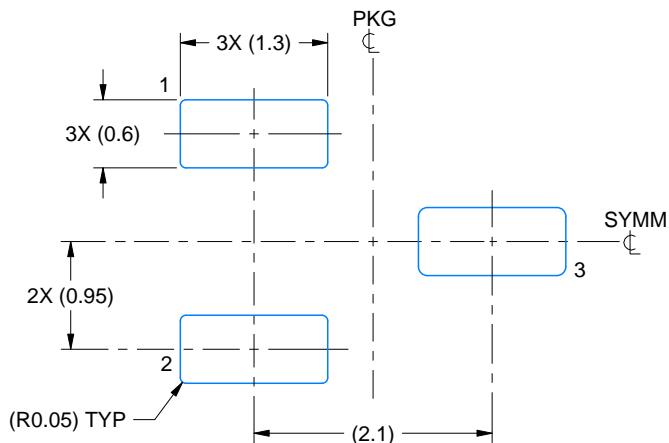
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

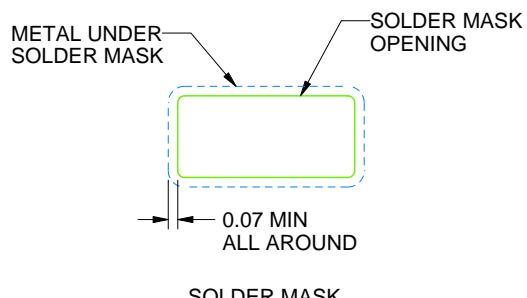
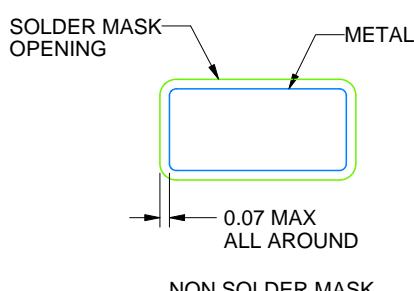
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

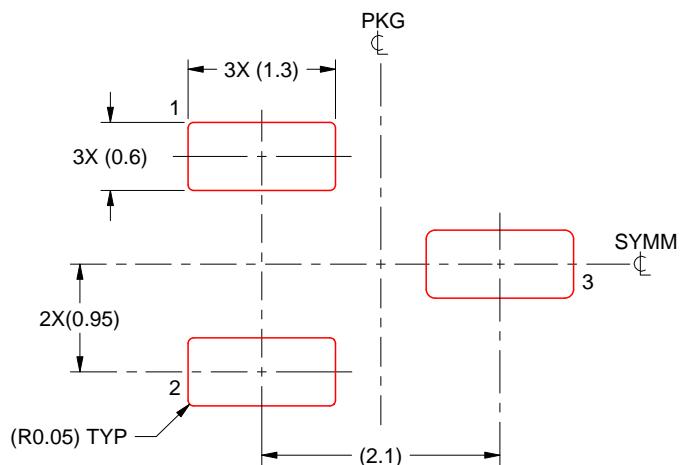
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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