LM3017 High Efficiency Low-Side Controller With True Shutdown

1 Features

- Fully Compliant to Thunderbolt™ Technology Specifications
- True Shutdown for Short-Circuit Protection
- Input Side Current Limit
- Single Enable Pin With Three Modes of Operation: Boost, Pass-Through, or Shutdown
- Built-in Charge Pump for High-Side NFET Disconnect Switch
- 1-A Push-Pull Driver for Low-Side NFET
- Peak Current Mode Control
- Simple Slope Compensation
- Protection Features: Thermal Shutdown, Cycle-by-Cycle Current Limit, Short-Circuit Protection, Output Overvoltage Protection, and Latch-Off
- Internal Soft Start
- Input Voltage Range: 5 V to 18 V
- 600-kHz Fixed Frequency Operation
- ±1% Reference Voltage Accuracy Over Temperature
- Low Shutdown Current (< 1 µA), 40 nA Typical
- 2.4 mm × 2.7 mm × 0.8 mm, 10-Pin WQFN Package

2 Applications

- Thunderbolt™ Technology Host Ports
- Notebook and Desktop Computers, Tablets, and Other Portable Consumer Electronics
- Hard Disc Drives, Solid-State Drives
- Offline Power Supplies
- Set-Top Boxes

3 Description

The LM3017 device is a versatile low-side NFET controller incorporating true shutdown and input side current limiting. The LM3017 is designed for simple implementation of boost conversions in Thunderbolt™ Technology. The LM3017 can also be configured for flyback or SEPIC designs. The input voltage range of 5 V to 18 V accommodates a two- or three-cell lithium ion battery or a 12-V rail. The enable pin accepts a single input to drive three different modes of operation: boost, pass-through, or shutdown mode. The LM3017 draws very low current in shutdown mode, typically 40 nA from the input supply.

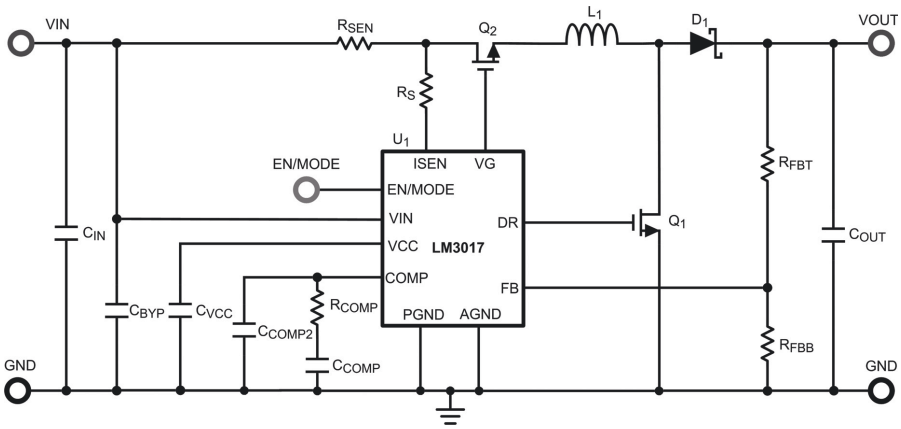
The LM3017 provides an adjustable output to drive the Power Load Switch or MUX for the host Thunderbolt™ port. The ability to drive an external high-side NMOS provides for true isolation of the load from the input. Current limiting on the input ensures that inrush and short-circuit currents are always under control. The LM3017 incorporates built-in thermal shutdown, cycle-by-cycle current limit, short-circuit protection, output overvoltage protection, and soft start. It is available in a 10-pin WQFN package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3017	WQFN (10)	2.40 mm × 2.70 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D **Page**

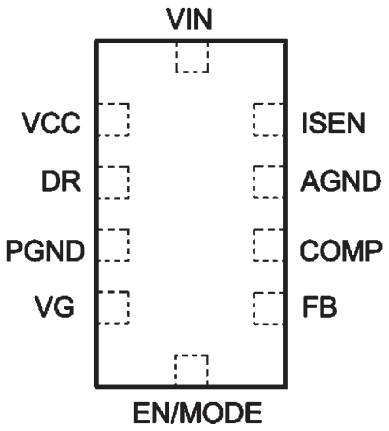
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed $R_{\theta JA}$ value in the *Thermal Information* table From: 36 To: 79.2 ... 4

Changes from Revision B (November 2012) to Revision C **Page**

- Added Updated to Rev C as Rev A and B were SVA Confidentials ... 1

5 Pin Configuration and Functions

NKL Package
10-Pin WQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VCC	O	Driver supply voltage pin: output of internal regulator powering low side NMOS driver. A minimum of 0.47 µF must be connected from this pin to PGND for proper operation.
2	DR	O	Low-side NMOS gate driver output: output gate drive to low side NMOS gate.
3	PGND	G	Power ground: ground for power section. External power circuit reference. Must be connected to AGND at a single point.
4	VG	O	High side NMOS gate driver output: output gate drive to high side NMOS gate.
5	EN/MODE	A	Multi-function input pin: this input provides for chip enable, and mode selection. See *Device Functional Modes* for details.
6	FB	A	Feed-back input pin: negative input to error amplifier. Connect to feedback resistor tap to regulate output.
7	COMP	A	Compensation pin: a resistor and capacitor combination connected to this pin provides frequency compensation for the regulator control loop.
8	AGND	G	Analog ground: ground for analog control circuitry. Reference point for all stated voltages.
9	ISEN	A	Current sense input: current sense input, with respect to V_{IN}, for all current limit functions.
10	VIN	P	Power supply input pin: input supply to regulator. See *Application and Implementation* for recommendations on bypass capacitors on this pin.

(1) A = Analog, G = Ground, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
VIN to PGND, AGND	–0.3	20	V
FB, COMP, VCC,DR to PGND, AGND	–0.2	6	V
EN/MODE	–0.2	5.5	V
VG	–0.3	VIN + 6	V
ISEN to PGND, AGND	VIN – 0.3	VIN	V
Peak low side driver output current		1	A
Power dissipation	Internally limited		
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply voltage	5.4	18	V
T_J	Junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM3017 NKL (WQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Minimum and maximum limits are specified through test, design, or statistical correlation, and apply over the junction temperature range at T_J = –40°C to 125°C. Typical values are provided for reference purposes only, and represent the most likely parametric norm at T_J = 25°C. V_{IN} = 12 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{FB}	Feedback voltage	Vcomp = 1.4 V	1.256	1.27	1.282	V
ΔV_{LINE}	Feedback voltage line regulation	5 V ≤ V_{IN} ≤ 18 V		0.33%		
V_{UVLO}	Input undervoltage lockout voltage	Rising	4.6	4.82	4.9	V
	Input undervoltage lockout hysteresis	Falling, below V_{UVLO}		280		mV
F_{SW}	Nominal switching frequency	EN/MODE = 1.6 V	550	600	635	kHz
$R_{DS(ON)}$	Low-side NMOS driver resistance, top driver FET	V_{IN} = 5 V, I_{DR} = 0.2 A		3.4		Ω
	Low-side NMOS driver resistance, bottom driver FET	V_{IN} = 5 V, I_{DR} = 0.2 A		1		
VCC	Driver voltage supply	V_{IN} < 6 V		V_{IN}		V
		V_{IN} ≥ 6 V		5.6		
D_{max}	Maximum duty cycle			86%		
$T_{min(on)}$	Minimum on-time			125		ns
$I_{Q\text{-}boost}$	Supply current in boost mode, no switching	EN/MODE = 1.6 V, FB = 1.4 V		5.2	9	mA
$I_{Q\text{-}SD}$	Supply current in shutdown mode	EN/MODE pin = 0.4 V		0.025	1	µA
$I_{Q\text{-}pass}$	Supply current in pass-through mode	EN/MODE = 2.6 V, FB = 1.4 V		1.4	2.3	mA
$V_{en\text{-}pass}$	Pass-through mode threshold(3)	Rising	2.19	2.4	2.56	V
$V_{mode\text{-}hyst}$	Mode change hysteresis, falling(3)	Falling	65	107	165	V
$V_{en\text{-}shutdown}$	Shutdown mode threshold(3)	Falling	0.2	0.4	0.59	V
$V_{en\text{-}boost}$	Boost mode enable window(3)	Rising	0.65	1.22	1.6	V
I_{en}	EN/MODE pin bias current(4)	EN/MODE = 1.6 V		±1		µA
V_{SENSE}	Cycle-by-cycle current limit threshold during boost mode	EN/MODE = 1.6 V, FB = 50 V	142	170	182	mV
ΔV_{SC}	Short-circuit current limit threshold during boost mode	EN/MODE = 1.6 V, FB = 0 V	18	30	42	mV
V_{SL}	Internal ramp compensation voltage			90		mV
V_{LIM1}	Input current limit threshold voltage in pass-through mode during T_{LIM1}(3)	EN/MODE = 2.6 V	70	85	95	mV
ΔV_{LIM2}	Input current limit threshold voltage in pass-through mode during T_{LIM2}(3)	EN/MODE = 2.6 V	14.5	18	21	mV
T_{LIM1}	Curent limit time at T_{LIM1}(3)			900		µs
T_{LIM2}	Current limit time at T_{LIM2}(3)			3.6		ms
T_{SC}	Current limit time at T_{SC}(3)			900		µs
V_{OVP}	Upper-output overvoltage protection threshold	Rising threshold measured at FB pin with respect to FB pin, VCOMP = 1.45 V		40		mV
	Lower-output overvoltage protection threshold	Falling threshold measured at FB pin with respect to FB pin, VCOMP = 1.45 V		26		
$V_{GS\text{-}on}$	On-state drive voltage at VG pin(5)	V_{IN} = 5 V, ISEN = 5 V, I_G = 0 A	3.8	4.9		V
$V_{GS\text{-}off}$	Off-state drive voltage at VG pin(6)	Vin = 5 V, ISEN = V_{IN} – 200 mV, I_G = 0 A		5		mV
I_G	Maximum drive current at VG pin	V_{IN} = 5 V, ISEN = 5 V, V_G = V_{IN}		20		µA
G_m	Error amplifier transconductance	V_{COM} = 1.4 V, I_{COMP} = ±50 µA	340	522	900	µA/V

(1) All limits are specified at room temperature and at temperature extremes. All room temperatures are 100% production tested. All limits at temperature extremes are specified through correlation using Statistical Quality Control (SQD) methods. All limits are used to calculate Average Outgoing Quaity Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) See *Device Functional Modes* and *Overvoltage Protection*.
(4) The bias current flowing through this pin is compensated and can flow either into or out-of this pin.
(5) This is the gate-to-source voltage drive of Q2, when the controller turns on this FET.
(6) This voltage is measured from the VG pin to AGND, when the controller fully turns off Q2.

Electrical Characteristics (continued)

Minimum and maximum limits are specified through test, design, or statistical correlation, and apply over the junction temperature range at T_J = –40°C to 125°C. Typical values are provided for reference purposes only, and represent the most likely parametric norm at T_J = 25°C. V_{IN} = 12 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
A_{VOL}	Error amplifier open-loop voltage gain	V_{COM} = 1.2 V to 1.8 V, I_{COMP} = 0 A	190	313	450	V/V
R_O	Error amplifier open-loop output resistance(7)			600		kΩ
I_{EAO}	Error amplifier output current swings	Sourcing: V_{COMP} = 1.4 V, V_{FB} = 1.1 V	27	66	115	µA
		Sinking: V_{COMP} = 1.4 V, V_{FB} = 1.4 V	49	68	125	
V_{EAO}	Error amplifier output voltage limits	Upper: V_{FB} = 0 V, COMP pin floating		2.3		V
		Lower: V_{FB} = 1.4 V		0.82		
T_r	Drive pin rise time	C_{load} = 3 nF, V_{DR} = 0 V to 3 V		25		ns
T_f	Drive pin fall time	C_{load} = 3 nF, V_{DR} = 3 V to 0 V		25		ns
T_{SD}	Thermal shutdown threshold			165		°C
$T_{SD\text{-}hyst}$	Thermal shutdown threshold hysteresis			10		°C

(7) This parameter is calculated from the error amplified G_m and A_{VOL}, and is not tested.

6.6 Typical Characteristics

V_{IN} = 12 V, T_J = 25°C, and see Figure 16 (unless otherwise noted).

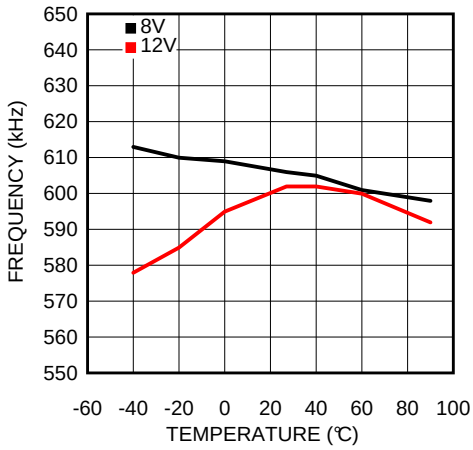


Figure 1. Switching Frequency vs Temperature

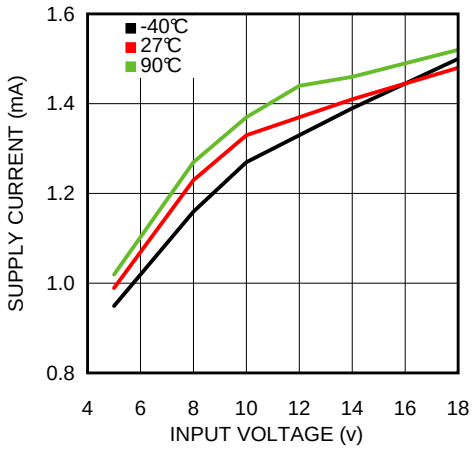


Figure 2. Supply Current in Pass-Through Mode ($I_{G\text{-}pass}$)

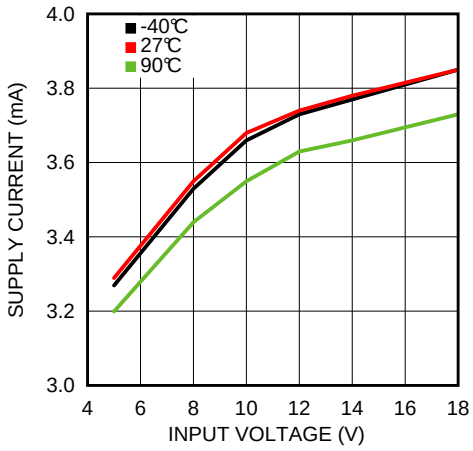


Figure 3. Supply Current in Boost Mode ($I_{Q\text{-}boost}$)

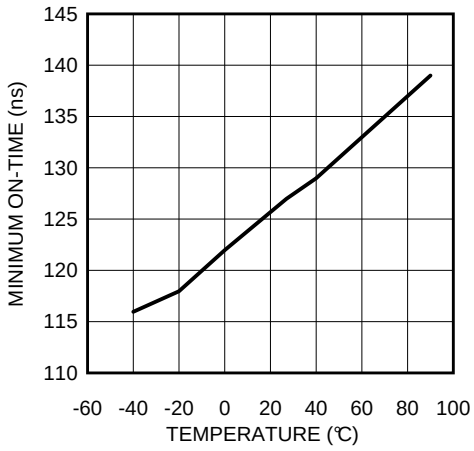


Figure 4. Minimum ON-Time vs Temperature

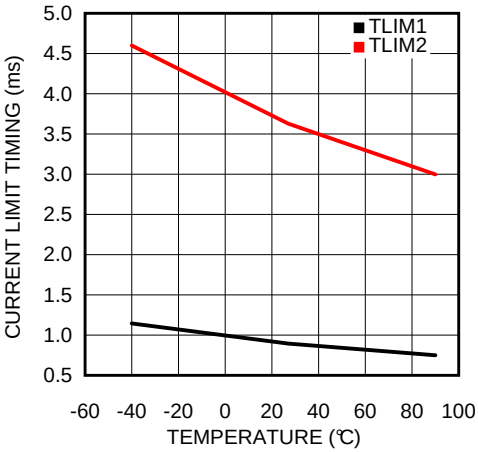


Figure 5. Current Limit Timing vs Temperature

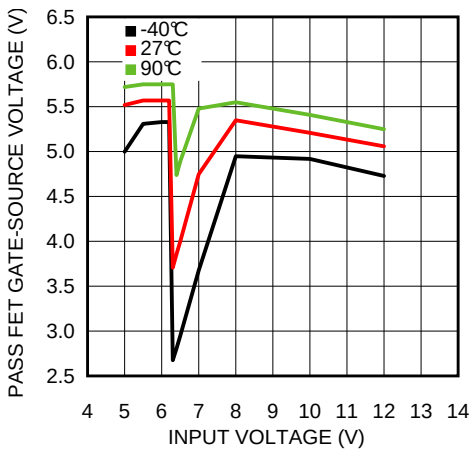


Figure 6. Pass FET Drive Voltage vs Input Voltage ($V_{GS\text{-}on}$)

Typical Characteristics (continued)

V_{IN} = 12 V, T_J = 25°C, and see Figure 16 (unless otherwise noted).

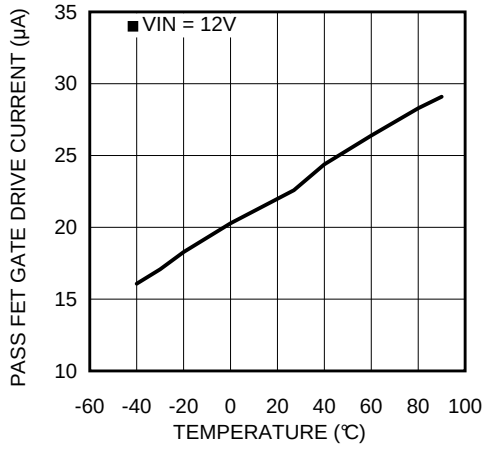


Figure 7. Pass FET Drive Current vs Temperature

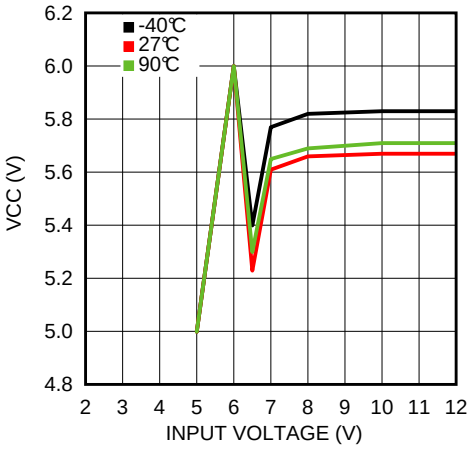
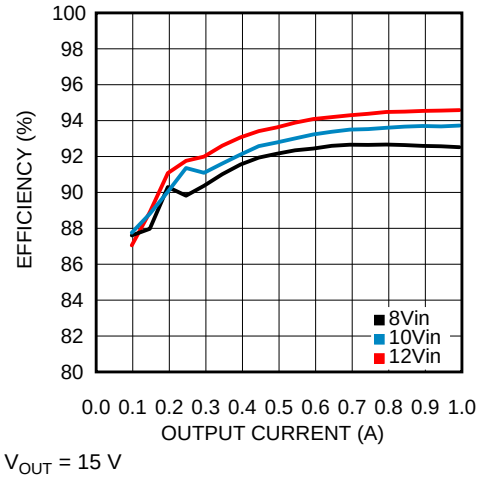


Figure 8. VCC Voltage vs Input Voltage



V_{OUT} = 15 V

Figure 9. Efficiency

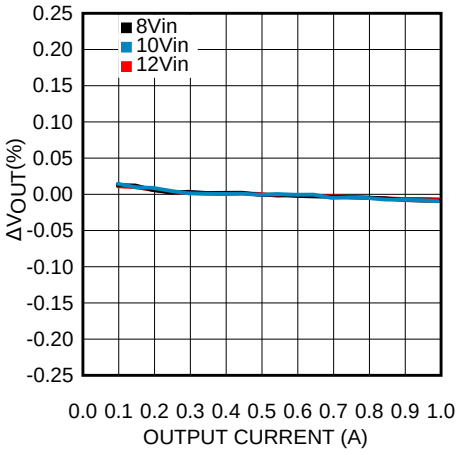


Figure 10. Load Regulation

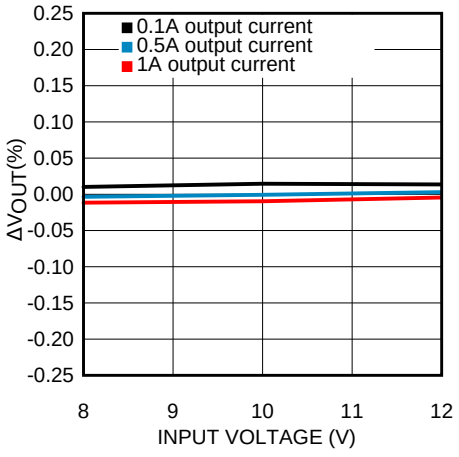
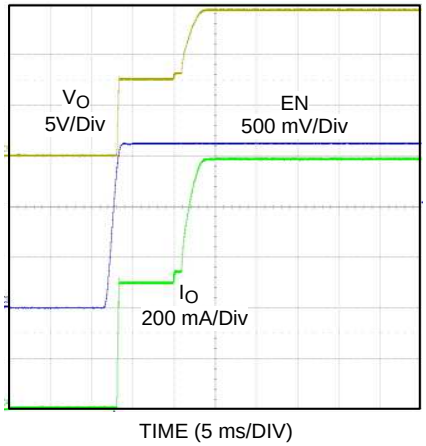


Figure 11. Line Regulation



V_{IN} = 8 V

Figure 12. Start-Up Waveforms

7 Detailed Description

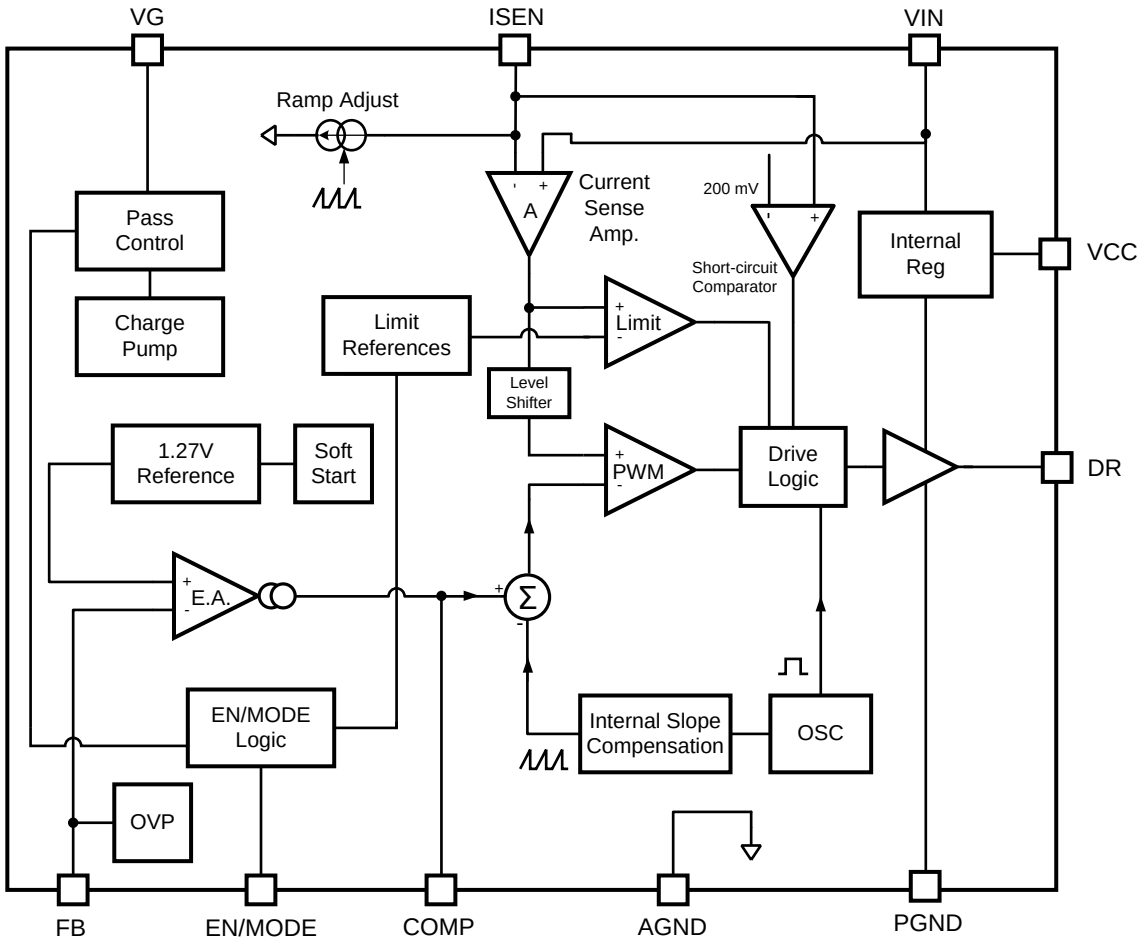
7.1 Overview

The LM3017 uses a fixed frequency, Pulse Width Modulated (PWM), current mode control architecture. A high-side current sense amplifier provides inductor current information by sensing the voltage drop across R_{SEN}. The voltage across this resistor is fed into the I_{SEN} pin. This voltage is then level shifted and fed into the positive input of the PWM comparator. As with all architectures of this type, a compensation ramp is required to ensure stability of the current control loop under all operating conditions. A nominal value of the ramp is provided internally while additional ramp can be added through the ISEN pin. The output voltage is sensed through an external feedback resistor divider network and fed into the error amplifier (EA) negative input (feedback pin, FB). The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator.

At the start of any switching cycle, the oscillator sets a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the Drive Logic is reset and the external MOSFET turns off.

Under extremely light load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET is on during the minimum on time is more than what is delivered to the load. An overvoltage comparator inside the LM3017 prevents the output voltage from rising under these conditions by sensing the feedback (FB pin) voltage and resetting the RS latch. The latch remains in a reset state until the output decays to the nominal value. Thus the operating frequency decreases at light loads, resulting in excellent efficiency.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 True Shutdown

The LM3017 incorporates circuitry to control a high side NMOS transistor in series with the inductor. This feature is used to disconnect the load from the input supply and protect the system from shorts on the output. Using an NMOS, rather than a PMOS transistor, saves the use of a diode from the inductor to ground. When the NMOS is turned off, the inductor brings the source belowground, keeping it on until the current is safely brought to zero. A built-in charge pump supplies typically V_{IN}+ 5 V to drive the gate of this NMOS.

7.3.2 Operation of the EN/MODE Pin

The EN/MODE pin is used to control the modes of the regulator by driving the high side gate (VG pin) to enable or disable the output through the pass MOSFET. Furthermore, it defines the current limit for each operation mode (see *Device Functional Modes*). Table 1 shows the modes versus the voltage on the EN/MODE pin.

Table 1. EN/MODE Voltage

EN/MODE PIN VOLTAGE	MODE
≤ 0.4 V	Shutdown
1.6 V to 2.2 V	Boost
≥ 2.6 V	Pass-through

Figure 13 shows the output voltage behavior in the various operation modes.

7.3.3 EN/MODE Control

As stated previously, the EN/MODE pin controls the state of the LM3017. As with any digital input, the voltage on this pin must not be allowed to slowly cross the various thresholds. Although hysteresis is used on this input, slowly varying signal may cause unpredictable behavior. Also, the EN/MODE pin must not be allowed to float. One way to control the LM3017, from digital logic, is to use the circuit shown in Figure 14. The resistor values are adjusted based on the above table and the logic supply used. The MOSFET can be any small signal device, such as the 2N7002.

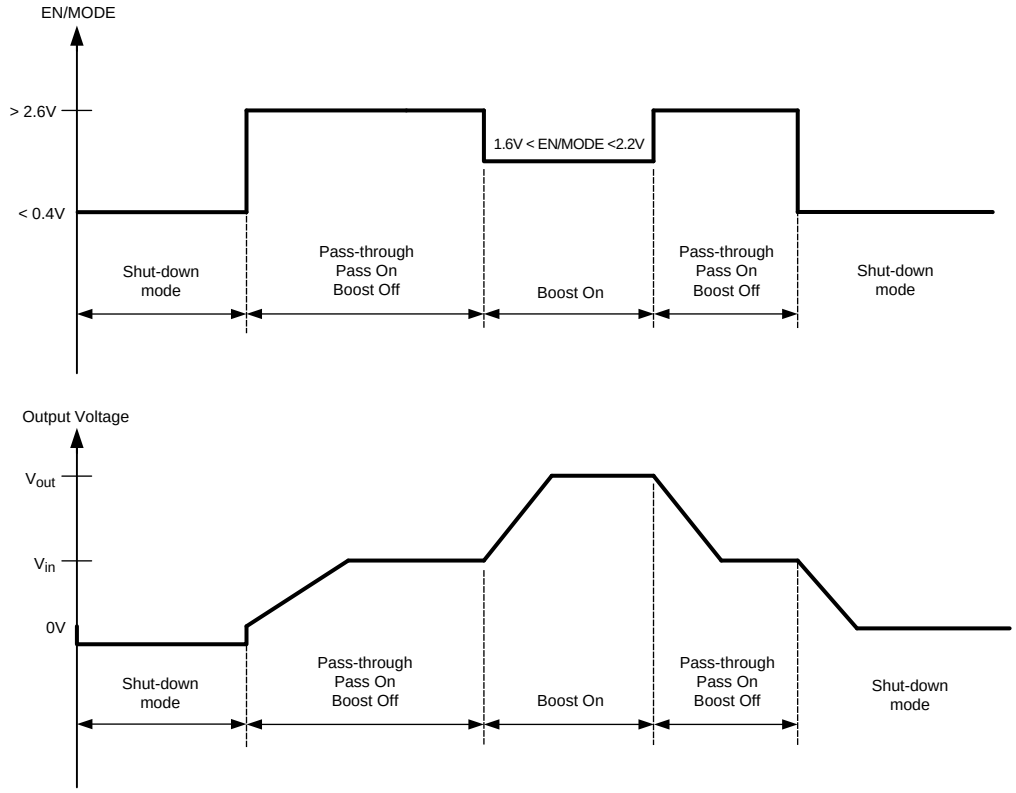


Figure 13. Typical EN/MODE Operation

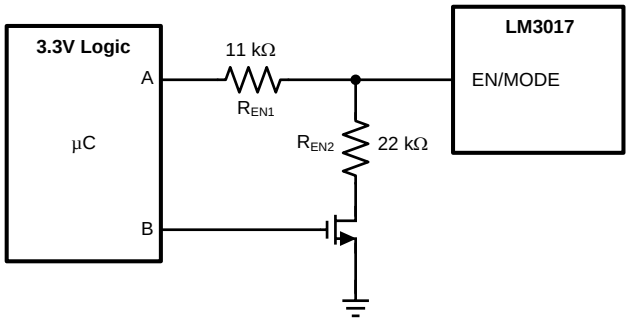


Figure 14. Typical EN/MODE Control Circuit

7.3.4 Overvoltage Protection

The LM3017 incorporates output overvoltage protection (OVP). At light, or no load the minimum switch on-time may not be short enough to allow regulation in constant frequency PWM mode. In these cases, the output voltage (and therefore the voltage on the FB pin) tries to rise. When the voltage on the FB pin reaches approximately 20 mV higher than the regulation point, the power switch (Q1) is turned off. Q1 remains off until the FB voltage drops back to the regulation point, at which time normal switching begins again. In this way, the LM3017 prevents the output voltage from rising too high with no load on the output.

7.3.5 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the LM3017 in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low-power standby state, disabling the output driver and the VCC regulator. After the temperature is reduced (typical hysteresis is 10°C), the VCC regulator is re-enabled and the LM3017 performs a soft start.

7.3.6 Current Limit Protection

The LM3017 implements current limit protection by controlling the pass FET, Q2.

In boost mode the LM3017 features both cycle-by-cycle current limit and short-circuit protection. Unlike most boost regulators, the LM3017 can protect itself from short circuits on the output by shutting off the pass FET. The boost current limit, defined by V_{CL}= 170 mV in *Electrical Characteristics*, turns off the boost FET for normal overloads on a cycle-by-cycle basis. The current is limited to V_{CL} / R_{SEN} until the overload is removed. If the output must be shorted, or otherwise pulled below V_{IN}, the inductor current has a tendency to *run-away*. This is prevented by the short-circuit protection feature, defined as V_{SC} = 200 mV in *Electrical Characteristics*. When this current limit is tripped, the current is limited to V_{SC} / R_{SEN} by controlling the pass FET. If the short persists for T_{SC} > 450 µs the pass FET is latched off. In this way, the current is limited to V_{SC} / R_{sen} until the short is removed or the time of T_{SC} = 450 µs is completed. Pulling the EN/MODE pin low (< 0.4 V, typical) is required to reset this short-circuit latch-off mode. The delay of T_{SC} = 450 µs helps to prevent nuisance latch-off during a momentary short on the output.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

Pulling the EN/MODE pin to less than 0.4 V (typical), during any mode of operation, places the part in full shutdown mode. The boost regulator and the pass FET is off and the load is disconnected from the input supply. In this mode, the regulator draws a maximum of 1 µA from the input supply.

7.4.2 Boost Mode

The boost regulator can be turned on by bringing the EN/MODE pin to greater than 1.6 V, but less than 2.2 V. This is the run mode for the boost regulator. Note that the LM3017 always starts in pass-through and transitions to boost mode.

7.4.3 Standby Mode

Setting the EN/MODE pin to greater than 2.6 V (typical), places the part in pass-through mode. The boost regulator is off and the pass MOSFET is on. During this mode, the load is connected to the input supply through the inductor and power diode, and is fully protected from output short circuits.

7.4.4 Start-Up Boost Mode

During start-up in boost mode, peak inductor current may be higher compared to normal operation. To allow for this, current limit levels and timing are different during start-up. The current limit is defined by V_{LIM2} = 100 mV (typical) in *Electrical Characteristics*, for the first T_{LIM2} = 3.6 ms (typical). The current is limited to V_{LIM2} / R_{SEN}, for this period. Once the T_{LIM2} = 3.6 ms (typical) timer has finished, the current limit is increased to V_{SC} = 200 mV (typical). For the first T_{LIM2} = 3.6 ms (typical) of the start-up, the latch-off feature is not enabled; however, the current is always limited to V_{LIM2} / R_{SEN}. This allows the part to start up normally. If the current limit is still tripped at the end of T_{LIM2} = 3.6 ms (typical) , the T_{SC} = 900 µs (typical) timer is started. Once the T_{SC} = 900 µs (typical) time has expired, the pass FET (Q2) is latched off. This gives a total current-limited time of T_{SC} + T_{LIM2} = 4.05 ms (typical), in cases where the LM3017 is started into a short circuit at the output.

7.4.5 Pass-Through Mode

In pass-through mode the power path is protected from shorts and overloads by the current limit defined as V_{LIM1} = 85 mV (typical) in *Electrical Characteristics*. When this current limit is tripped, the current is limited to V_{LIM1} / R_{SEN} by controlling the pass FET. If the short persists for T_{LIM1} > 900 µs (typical) the pass FET (Q2) is latched off. In this way, the current is limited to V_{LIM1} / R_{SEN} until the short is removed or the time of T_{LIM1} = 900 µs (typical) is completed. Pulling the EN/MODE pin low (0.4 V, typical) is required to reset this latch-off mode.

Device Functional Modes (continued)

7.4.6 Start-Up Pass-Through Mode

During start-up in pass mode, the current limit is defined by V_{LIM2} = 100 mV (typical) in *Electrical Characteristics*, for the first T_{LIM2} = 3.6 ms (typical). The current is limited to V_{LIM2} / R_{SEN}, for this period. Once the T_{LIM2} = 3.6 ms (typical) timer has finished, the current limit is reduced to V_{LIM1} = 85 mV (typical). For the first T_{LIM2} = 3.6 ms (typical) of the start-up, the latch-off feature is not enabled; however, the current is always limited to V_{LIM2} / R_{SEN}. This higher limit allows the part to start up normally. If the current limit is still tripped at the end of T_{LIM2} = 3.6 ms (typical), the T_{LIM1} = 900 µs (typical) timer is started. Once the T_{LIM1}= 900 µs time has expired, the pass FET(Q2) is latched off. This gives a total current-limited time of T_{LIM1}+ T_{LIM2} = 4.5 ms (typical), in cases where the LM3017 is started into a short circuit at the output.

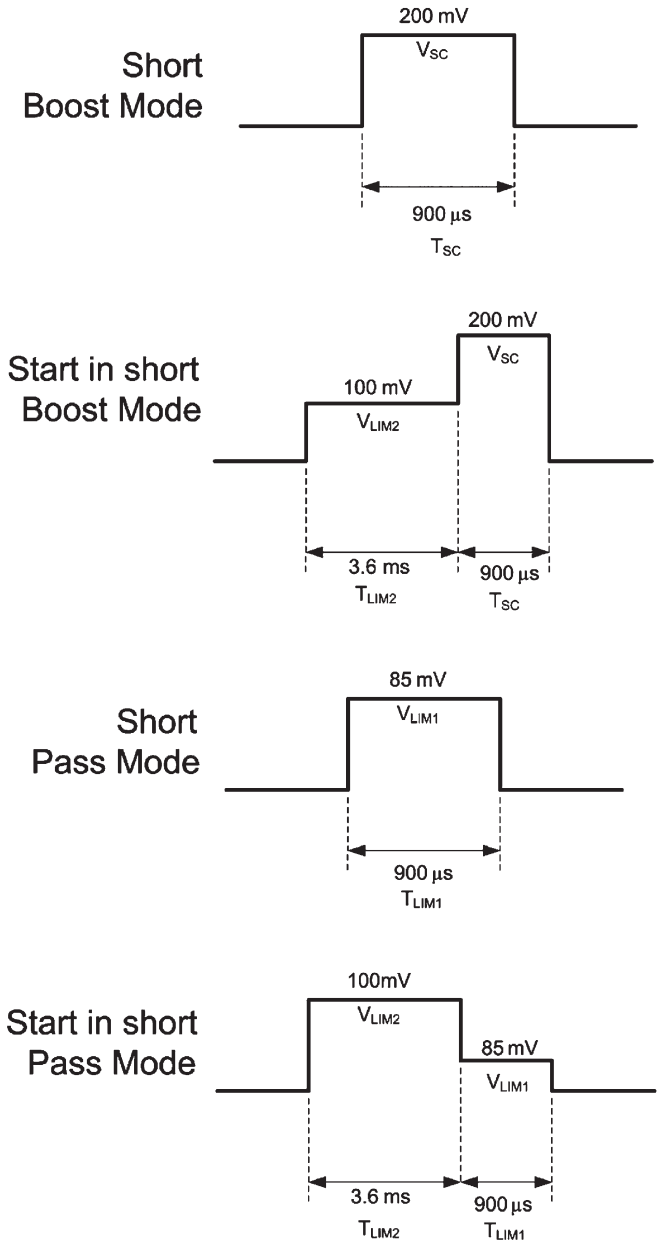


Figure 15. Current Limit and Short-Circuit Protection

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3017 may be operated in either continuous or discontinuous conduction mode. The following descriptions assume continuous conduction operation (CCM). This mode of operation has higher efficiency and lower EMI characteristics than the discontinuous mode.

8.2 Typical Application

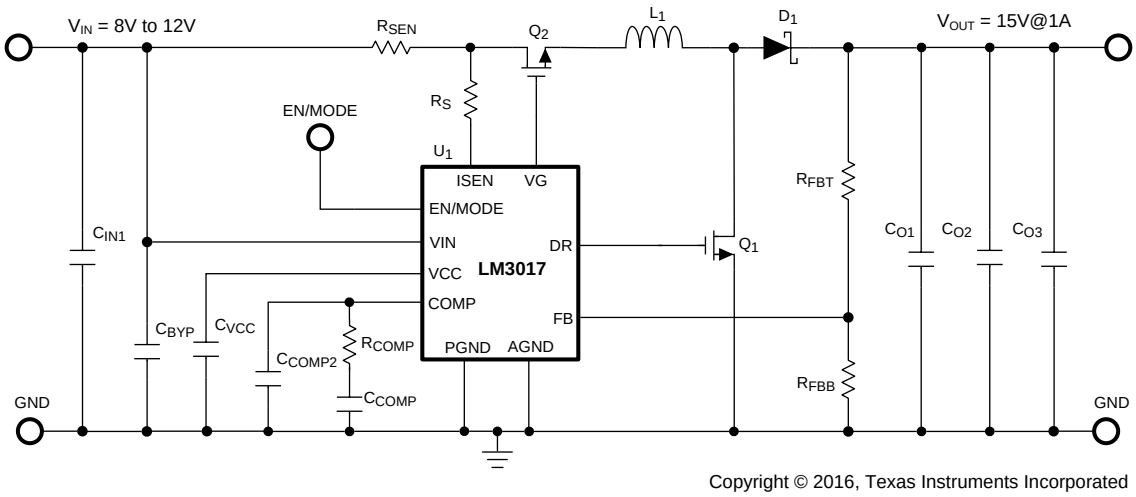


Figure 16. 1-A High Efficiency Step-Up (Boost) Converter

8.2.1 Design Requirements

To properly size the components for the application, the designer requires the following parameters: Input voltage range, output voltage, output current, and switching frequency. These four main parameters affect the choices of component available to achieve a proper system behavior.

Table 2 lists the design parameters for this application example.

Table 2. Design Parameters

PARAMETER	VALUE
Input voltage, V_{IN}	8 V to 12 V
Output voltage, V_{OUT}	15 V
Output current, I_{OUT}	1 A
Switching frequency, f_S	600 kHz

8.2.2 Detailed Design Procedure

The most common topology for the LM3017 is the boost or step-up topology. The boost converter converts a low input voltage into a higher output voltage. The basic configuration for a boost regulator is shown in Figure 17. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles. In the first cycle of operation, MOSFET Q is turned on and energy is stored in the inductor. During this cycle, diode D1 is reverse biased and load current is supplied by the output capacitor, COUT.

In the second cycle, MOSFET Q is off and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined with Equation 1.

$$V_{OUT} = \frac{V_{IN}}{1-D};\ D = 1 - \frac{V_{IN}}{V_{OUT}} \tag{1}$$

Including the voltage drop of the diode in Equation 2.

$$V_{OUT} + V_{D1} = \frac{V_{IN}}{1-D};\ D = \frac{V_{OUT} - V_{IN} + V_{D1}}{V_{OUT} + V_{D1}} \tag{2}$$

where

- D is the duty cycle of the switch
- V_{D1} is the forward voltage drop of the diode

The following sections describe selection of components for a boost converter.

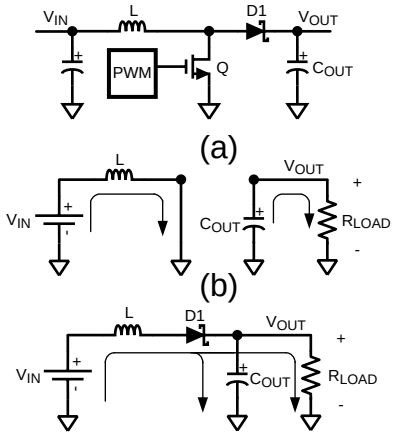


Figure 17. 4 Simplified Boost Converter Diagram
(a) First Cycle of Operation, (b) Second Cycle of Operation

8.2.2.1 Programming the Output Voltage

The output voltage can be programmed using a resistor divider between the output and the feedback pins, as shown in Figure 20. The resistors are selected such that the voltage at the feedback pin is equal to $_{VFB}$ (see *Electrical Characteristics*). R_{FBT} and R_{FBB} can be selected using Equation 3.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right) \tag{3}$$

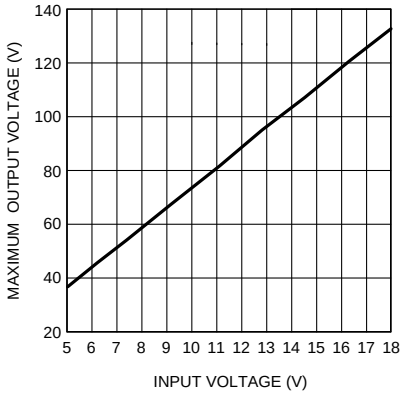


Figure 18. Maximum Output Voltage

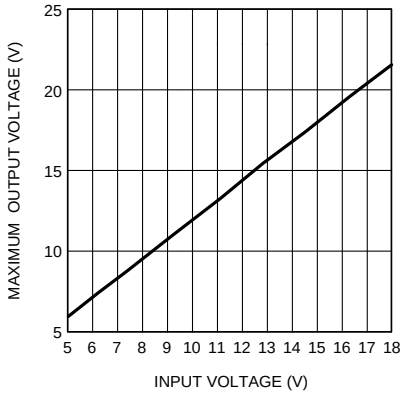


Figure 19. Minimum Output Voltage

Figure 18 shows maximum regulated output voltage based on maximum duty cycle value of 85% and by assuming a voltage drop on the output diode of 0.5 V and 90% efficiency. Figure 19 shows the minimum regulated output voltage, the calculation is based on minimum on time of 126 ns (typical) that generates a minimum duty cycle equal to Equation 4.

$$D_{MIN} = t_{ON(min)} \times f_S = 0.076 \quad (4)$$

where

- f_S is the switching frequency and it's equal to 600 kHz and by assuming 90% efficiency

8.2.2.2 Power Inductor Selection

The inductor is one of the two energy storage elements in a boost converter.

Choose the minimum I_{OUT} to determine the minimum inductance L. A common choice is to set (2 x Δi_L) from 30% to 50% of I_L. Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. In a boost converter the inductor current I_L, the peak of the inductor current and the inductor current ripple Δi_L are equal to Equation 5.

$$I_L = \frac{I_{OUT}}{1-D}$$

$$I_{Lpeak} = I_L(max) + \Delta i_L(max)$$

$$\Delta i_L = \frac{D \times V_{IN}}{2 \times L \times f_S} \quad (5)$$

The inductance used is a tradeoff between size and cost. Larger inductance means lower input ripple current; however, because the inductor is connected to the output during the off-time only, there is a limit to the reduction in output voltage ripple. Lower inductance results in smaller, less expensive magnetics.

All the analysis in this data sheet assumes operation in continuous conduction mode. To operate in continuous conduction mode, the conditions in Equation 6 must be met.

$$I_L = \Delta i_L$$

$$\frac{I_{OUT}}{1-D} = \frac{D \times V_{IN}}{2 \times f_S \times L}$$

$$L \geq \frac{(1-D) \times D \times V_{IN}}{2 \times f_S \times I_{OUT}} \quad (6)$$

A core size with ratings higher than these values must be chosen. If the core is not properly rated, saturation dramatically reduces overall efficiency or damage the power stage. Choose an inductor with a saturation current value higher than I_{Lpeak}. The LM3017 senses the peak current through the switch. The peak current through the switch is the same as the peak current calculated in the previous equation.

Losses due to DCR of the inductance can be easily calculated with Equation 7.

$$P_L = DCR \times \left[\left(\frac{I_{OUT}}{1-D} \right)^2 + \frac{\Delta i_L^2}{12} \right] \quad (7)$$

No core losses are considered.

8.2.2.3 Setting the Output Current

The maximum amount of current that can be delivered at the output can be controlled by the sense resistor, R_{SEN}. Current limit occurs when the voltage that is generated across the sense resistor equals the current sense threshold voltage, V_{SENSE}. Limits for V_{SENSE} are specified in *Electrical Characteristics*. This is expressed with Equation 8.

$$I_{sw(peak)} \times R_{SEN} = V_{SENSE} \tag{8}$$

The peak current through the switch is equal to the peak inductor current in Equation 9.

$$I_{sw(peak)} = I_L(max) + \Delta i_L \tag{9}$$

Therefore for a boost converter in Equation 10.

$$I_{SW_{peak}} = \frac{I_{OUT}}{1-D} + \frac{D \times V_{IN}}{2 \times f_S \times L} \tag{10}$$

Combining the two equations yields an expression for R_{SEN} and includes a 20% margin on the peak of the switching current with Equation 11.

$$R_{SEN} = \frac{V_{SENSE}}{1.2 \times \left(\frac{I_{OUT}}{1-D} + \frac{D \times V_{IN}}{2 \times f_S \times L} \right)} \tag{11}$$

Evaluate R_{SEN} at the maximum and minimum V_{IN} values and choose the smallest R_{SEN} calculated.

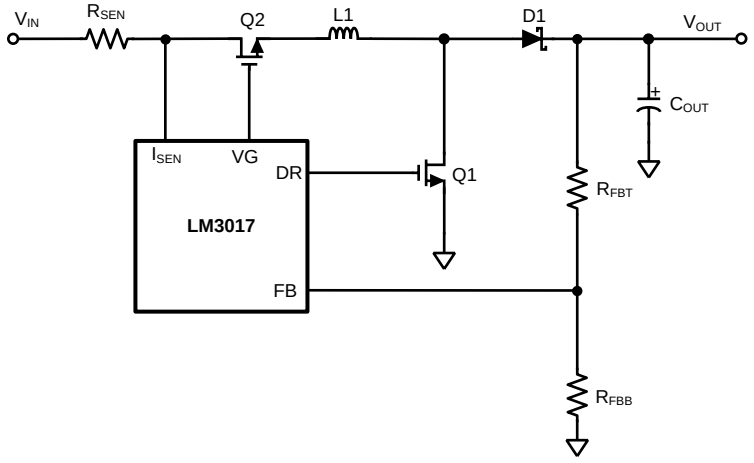


Figure 20. Adjusting the Output Voltage

8.2.2.4 Additional Slope Compensation

It is good design practice to only add as much slope compensation as required to avoid instability. Additional slope compensation (see Figure 24) minimizes the influence of the sensed current in the control loop. With very large slope compensation the control loop characteristics are similar to a voltage mode regulator which compares the error voltage to a saw tooth waveform rather than the inductor current. It is possible to calculate the minimum value of RS to meet Equation 12.

$$M_C > M_2/2 \tag{12}$$

Hence Equation 13,

$$R_S \geq \frac{1}{K} \times \left[\frac{R_{SEN} \times \left(V_{OUT} - V_{IN}(min) \right)}{2 \times L \times f_S} - V_{SL} \right]$$

where

- K = 40 µA (13)

If the result of the previous equation is negative, it means that no additional slope compensation is required. TI recommends a 100-Ω resistor.

8.2.2.5 Current Limit With Additional Slope Compensation

If an external slope compensation resistor is used, then the internal control signal is modified and this has an effect on the current limit.

If R_S is used, then this adds to the existing slope compensation. The command voltage, V_{CS}, is then given by Equation 14.

$$V_{CS} = V_{SL} + \Delta V_{SL}$$

where

- V_{SENSE} is a defined parameter in *Electrical Characteristics*
- V_{SL} is the amplitude of the internal compensation ramp
- $\Delta V_{SL} = R_S \times K$ is the additional slope compensation generated (14)

This changes the equation for R_{SEN} to Equation 15.

$$R_{SEN} = \frac{V_{SENSE} - D \times V_{CS}}{\left(\frac{I_{OUT}}{1-D} + \frac{D \times V_{IN}}{2 \times f_S \times L} \right)} \quad (15)$$

Because $\Delta V_{SL} = R_S \times K$ as defined earlier, R_S can be used to provide an additional method for setting the current limit. In some designs R_S can also be used to help filter noise to keep the I_{SEN} pin quiet. Dissipation due to R_{SEN} resistor is equal to Equation 16.

$$P_{SEN} = R_{SEN} \times \left[\left(\frac{I_{OUT}}{1-D} \right)^2 + \frac{\Delta i_{Lpp}^2}{12} \right] \quad (16)$$

8.2.2.6 Power Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average output current, and the peak current through the diode is the peak current through the inductor. The peak diode current can be calculated using Equation 17.

$$I_{D(Peak)} = [I_{OUT} / (1 - D)] + \Delta i_L \quad (17)$$

The peak reverse voltage for a boost converter is equal to the regulator output voltage. The diode must be capable of handling this peak reverse voltage as well as the output rms current. To improve efficiency, TI recommends a low forward drop Schottky diode due to low forward drop and near-zero reverse recovery time. The overall efficiency becomes more dependent on the selection of D at low duty cycles, where the boost diode carries the load current for an increasing percentage of the time. This power dissipation can be calculated by checking the typical diode forward voltage VD, from the I-V curve on the diode's datasheet and the multiplying it by IO. Diode data sheets also provides a typical junction-to-ambient thermal resistance, $R_{\theta JA}$, which can be used to estimate the operating die temperature of the Schottky. Multiplying the power dissipation ($P_D = I_O \times V_D$) by $R_{\theta JA}$ gives the temperature rise. The diode case size can then be selected to maintain the Schottky diode temperature below the operational maximum.

8.2.2.7 Low-Side MOSFET Selection (Switching MOSFET)

The drive pin, DR, of the LM3017 must be connected to the gate of an external MOSFET. In a boost topology, the drain of the external N-Channel MOSFET is connected to the inductor and the source is connected to the ground. The drive pin voltage, V_{DR}, depends on the input voltage (see *Typical Characteristics*).

The selected MOSFET directly affects the efficiency. The critical parameters for selection of a MOSFET are:

1. Minimum threshold voltage, $V_{TH(MIN)}$
2. On-resistance, $R_{DS(ON)}$
3. Total gate charge, Q_g
4. Reverse transfer capacitance, C_{RSS}
5. Maximum drain to source voltage, $V_{DS(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the output voltage. $V_{DS(MAX)}$ of the MOSFET must be greater than the output voltage plus the voltage drop across the output diode (20% margin recommended).

The power losses in the MOSFET can be categorized into conduction losses, gate charging losses and switching losses. $R_{DS(ON)}$ is required to estimate the conduction losses. The conduction loss, P_{COND}, is the I2R loss across the MOSFET. The maximum conduction loss is given by Equation 18 and Equation 19.

$$P_{COND} = \left(\frac{I_{OUT}}{1 - D_{MAX}}\right)^2 \times D_{MAX} \times R_{DS(on)}$$

where

- D_{MAX} is the maximum duty cycle (18)

$$D_{MAX} = 1 - \frac{V_{IN}(min)}{V_{OUT}} \quad (19)$$

To consider the increase in MOSFET on resistance due to heating, a factor of 1.3 is introduced, hence Equation 20.

$$P_{COND\_real} = P_{COND(max)} \times 1.3 \quad (20)$$

Gate charging loss, P_G, results from the current required to charge and discharge the gate capacitance of the power MOSFET and is approximated with Equation 21.

$$P_G = VCC \times Q_G f_S \quad (21)$$

Q_G is the total gate charge of the MOSFET. Gate charge loss differs from conduction and switching losses because the actual dissipation occurs in the LM3017 and not in the MOSFET itself. This loss, P_{VCC}, is estimated with Equation 22.

$$P_{VCC} = (V_{IN} - VCC) \times Q_G \times f_S \quad (22)$$

The switching losses are very difficult to calculate due to changing parasitics of a given MOSFET in operation. Often, the individual MOSFET datasheet does not give enough information to yield a useful result. The following formulas give a rough idea how the switching losses are calculated with Equation 23.

$$P_{SW} = \frac{I_L \times V_{OUT}}{2} \times f_S \times (t_{LH} + t_{HL})$$

where

- t_{LH} and t_{HL} are rise and fall times of the MOSFET (23)

8.2.2.8 Pass MOSFET Selection (High-Side MOSFET)

The VG pin drives the gate of the high side MOSFET (Pass FET Q2). This requires special considerations. When the output is shorted, this FET must sustain the full input voltage and the short-circuit current simultaneously. This is due to the fact that the controller regulates the short-circuit current in a quasi-linear manner, through Q2. This power pulse only lasts for T_{LIM2} or T_{SC}, depending on the operational mode. Therefore, the designer must carefully examine the SOA curve for the desired FET before committing to the design. Equation 24 and Equation 25 give the maximum energy pulses that Q2 is required to survive.

$$E_1 \geq (V_{in} + 2) \times \left(\frac{V_{LIM2}}{R_{sen}}\right) \times T_{LIM2} \quad (24)$$

$$E_2 \geq (V_{in} + 2) \times \left(\frac{V_{SC}}{R_{sen}}\right) \times T_{SC} \quad (25)$$

These two energy points must fall within the SOA of the selected FET. In addition, Q2 must have a low threshold voltage and low $R_{DS(on)}$ for high efficiency. Power dissipation during boost mode is given by Equation 26.

$$P_{Q2} = R_{DS(on)} \times \left[\left(\frac{I_{OUT}}{1 - D}\right)^2 + \frac{\Delta i_{Lpp}^2}{12}\right] \quad (26)$$

8.2.2.9 Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The rms current in the input capacitor is given by Equation 27.

$$I_{C_{IN}(rms)} = \frac{\Delta i_L}{\sqrt{3}} = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{\sqrt{12} \times V_{OUT} \times f_S} \quad (27)$$

The input capacitor must be capable of handling this rms current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore, a good quality capacitor must be chosen in the range of 10 µF to 20 µF. Furthermore, TI recommends a low-ESR, 0.1-µF ceramic bypass capacitor to avoid transients and ringing due to parasitics. Bypass capacitors must be placed as close as possible to the V_{IN} pin and grounded close to the GND pin on the IC to minimize additional ESR and ESL. Equation 28 can be used to define the input voltage ripple.

$$\Delta V_{ipp} = \Delta i_{LPP} \times \sqrt{ESR^2 + \left(\frac{1}{8 \times f_S \times C_i}\right)^2} \quad (28)$$

where

- $\Delta i_{Lpp} = 2 \times \Delta i_L$ is the peak-to-peak inductor current ripple
- ΔV_{ipp} is the peak-to-peak input voltage ripple

Many times it is necessary to use an electrolytic capacitor on the input in parallel with the ceramics. The ESR of this capacitor can help to damp any ringing on the input supply caused by long power leads.

8.2.2.10 Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the inductor is charging and it determines the steady state output voltage ripple ΔV_{Opp}. As a result it sees very large ripple currents. The output capacitor must be selected based on its capacitance C_O, its equivalent series resistance ESR and its RMS current rating. The rms current in the output capacitor is calculated with Equation 29.

$$I_{C_{OUT}(rms)} = \sqrt{(1-D) \times \left[I_{OUT}^2 \times \frac{D}{(1-D)^2} + \frac{\Delta i_L^2}{3}\right]} \quad (29)$$

where

- Δi_L is the inductor ripple current
- D is the duty cycle

The magnitude of the output voltage ripple during the on-time is equal to the ripple voltage during the off-time and it is composed of two parts. For simplicity, the analysis is performed for off-time only.

The first part of the ripple voltage is the surge created as the output diode D turns on. At this point inductor or diode current is at the peak value, and the ripple voltage increase can be calculated with Equation 30.

$$\Delta V_{O1} = I_{PK} \times ESR \quad (30)$$

where

- $I_{PK} = I_{OUT} / (1 - D)$

The second portion of the ripple voltage is the increase due to the charging of CO through the output diode. This portion can be approximated with Equation 31.

$$\Delta V_{O2} = (I_O / C_O) \times (D / f_S) \quad (31)$$

Equation 32 can be used to define the output voltage ripple.

$$\Delta V_{Opp} = ESR \times \left(\frac{I_{OUT}}{1-D} + \Delta i_L\right) + \frac{I_{OUT} \times D}{C_o \times f_S} \quad (32)$$

The ESR of the output capacitor(s) has a strong influence on the slope and direction of the output voltage ripple. Capacitors with high ESR such as tantalum and aluminum electrolytic create an output voltage ripple that is dominated by ΔV_{O1} with a shape shown in Figure 21. Ceramic capacitors, in contrast, have a very low ESR and lower capacitance, and the shape of the output voltage ripple is dominated by ΔV_{O2} with a shape shown in Figure 22.

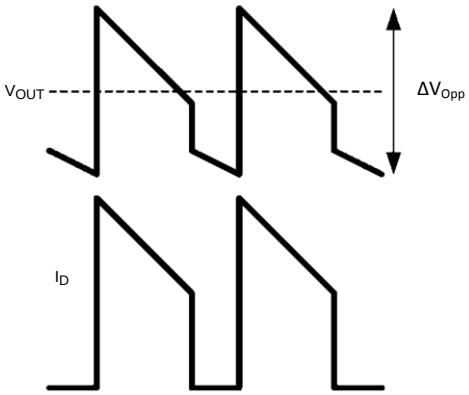


Figure 21. ΔV_{Opp} Using High ESR Capacitors

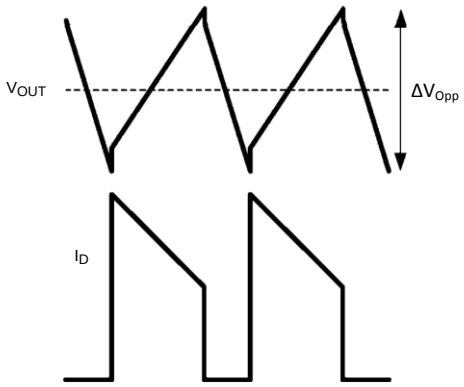


Figure 22. ΔV_{Opp} Using Low ESR Capacitors

Ceramic capacitors are recommended with a typical value from 10 µF to 100 µF. The minimum quality dielectric that is suitable for switching power supply output capacitors is X5R, while X7R (or better) is preferred. Careful attention must be paid to the DC voltage rating and case size, as ceramic capacitors can lose 60% or more of their rated capacitance at the maximum DC voltage. This is the reason that ceramic capacitors often derate to 50% of their capacitance at their working voltage.

8.2.2.11 VCC Decoupling Capacitor

The internal bias of the LM3017 comes from either the internal bias voltage generator as shown in the block diagram or directly from the voltage at the VIN pin. At input voltages lower than 6 V, the internal IC bias is the input voltage and at voltages above 6 V the internal bias voltage generator of the LM3017 provides the bias. A good quality ceramic bypass capacitor must be connected from the VCC pin to the PGND pin for proper operation. This capacitor supplies the transient current required by the internal MOSFET driver, as well as filtering the internal supply voltage for the controller. TI recommends a value of between 0.47 µF and 4.7 µF.

8.2.2.12 Slope Compensation Ramp

The LM3017 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch, simpler control loop characteristics and excellent line and load transient response. However, there is a natural instability due to subharmonic oscillations that occurs for duty cycles, D, greater than 50% if slope compensation is not addressed in Equation 33.

$$M_C > M_2 / 2 \quad (33)$$

For best input noise immunity, use Equation 34.

$$M_C = M_2 \quad (34)$$

For best sub-harmonic suppression, use Equation 35.

$$M_C = M_2 / 2$$

where

- M_C is the slope of the compensation ramp
- M_1 is the slope of the inductor current during the ON time
- M_2 is the slope of the inductor current during the OFF time
- R_{SEN} is the sensing resistor value
- V_{OUT} represents the output voltage
- V_{IN} represents the input voltage
- A is equal to 0.86 and it is the internal sensing amplification of the LM3017 (35)

In the case of the boost topology, use Equation 36 and Equation 37.

$$M_1 = [V_{IN} / L] \times R_{SEN} \times A \quad (36)$$

$$M_2 = [(V_{OUT} - V_{IN}) / L] \times R_{SEN} \times A \quad (37)$$

The compensation ramp is added internally in the LM3017. The slope of this compensation ramp is selected to satisfy most applications, and its value depends on the switching frequency. This slope can be calculated using Equation 38.

$$M_C = V_{SL} \times f_S \quad (38)$$

In the above equation, V_{SL} is the amplitude of the internal compensation ramp and f_S is the controller's switching frequency. Limits for V_{SL} are specified in *Electrical Characteristics*.

To provide the user additional flexibility, a patented scheme is implemented inside the IC to increase the slope of the compensation ramp externally, if the requirement arises. Adding a single external resistor, R_S (as shown in Figure 24) increases the amplitude of the compensation ramp as shown in Figure 23 where Equation 39.

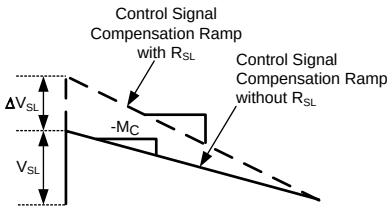


Figure 23. Additional Slope Compensation Added Using External Resistor R_S

$$\Delta V_{SL} = K \times R_s$$

where

- K = 40 µA typically and changes slightly as the switching frequency changes (39)

A more general equation for the slope compensation ramp, MC, is shown in Equation 40 to include ΔV_{SL} caused by the resistor, R_s.

$$M_C = (V_{SL} + \Delta V_{SL}) \times f_s \quad (40)$$

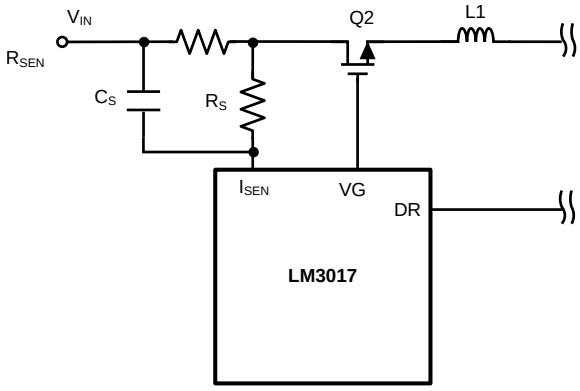


Figure 24. Increasing the Slope of the Compensation Ramp

An additional capacitor, C_S, could be added if the sensing signal generated by R_{SEN} is very noisy (parasitic circuit capacitance, inductance, and gate drive current create a spike in the current sense voltage at the point where Q1 turns on). The time constant R_{SEN} x C_S must be long enough to reduce the parasitics spike without significantly affecting the shape of the actual current sense voltage (a typical range is from 100 pF to 2.2 nF).

8.2.2.13 Control Loop Compensation

The LM3017 uses peak current-mode PWM control to correct changes in output voltage due to line and load transients. Peak current-mode provides inherent cycle-by-cycle current limiting, improved line transient response, and easier control loop compensation. The control loop is comprised of two parts. The first is the power stage, which consists of the pulse width modulator, output filter, and the load. The second part is the error amplifier. Figure 25 shows the regulator control loop components.

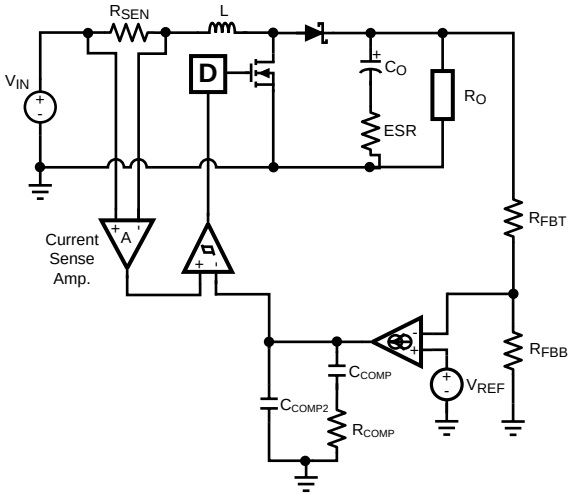


Figure 25. Power Stage and Error Amp

The power stage in a CCM peak current mode boost converter consists of the DC gain, G_{VC0}, a single low frequency pole, f_P, the ESR zero, f_Z, a right-half plane zero, f_R, and a double pole resulting from the sampling of the peak current. The power stage transfer function (also called the Control-to-Output transfer function) can be written with Equation 41.

$$G_{VC}(s) = G_{VC0} \times \frac{\left(1 - \frac{s}{\omega_R}\right)\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)\left(1 + \frac{s}{\omega_n} + \frac{s^2}{\omega_n^2}\right)} \quad (41)$$

The DC gain is defined with Equation 42.

$$G_{VC0} = \frac{R_O(1-D)}{2 \times A \times R_{SEN}}$$

where

- $R_O = V_{OUT} / I_{OUT}$ (42)

In the equation for G_{VC0}, DC gain is highest when input voltage and output current are at the maximum. The system ESR zero is defined with Equation 43.

$$f_Z = \frac{\omega_Z}{2\pi} = \frac{1}{2\pi \times C_O \times ESR} \quad (43)$$

The low frequency pole is Equation 44.

$$f_P = \frac{\omega_P}{2\pi} = \frac{2}{2\pi \times C_O \times (ESR + R_O)} \quad (44)$$

The right-half plane zero is Equation 45.

$$f_R = \frac{\omega_R}{2\pi} = \frac{R_O \times (1-D)^2}{2\pi \times L} \quad (45)$$

The sampling double pole quality factor is Equation 46.

$$Q_n = \frac{1}{\pi \times \left[(1-D) \times \left(1 + \frac{M_C}{M_1} \right) - 0.5 \right]} \quad (46)$$

The sampling double corner frequency is Equation 47.

$$\omega_n = \pi \times f_S \quad (47)$$

The natural inductor current slope is Equation 48.

$$M_1 = R_{SEN} \times V_{IN} / L \quad (48)$$

The external ramp slope is Equation 49.

$$M_C = (V_{SL} + \Delta V_{SL}) \times f_S \quad (49)$$

A step-up converter produces an undesirable right-half plane zero in the regulation feedback loop. This requires compensating the regulator such that the crossover frequency occurs well below the frequency of the right-half plane zero

8.2.2.13.1 Compensation Network Components Calculations

As shown in Figure 25, the LM3017 uses a compensation network base on a transconductance amplifier. The closed-loop transfer function is defined with Equation 50 through Equation 54.

$$T(s) = G_{VA}(s) \times G_{VC}(s)$$

where

- $G_{VA}(s)$ is the transfer function implemented by the compensation network

(50)

$$G_{VA}(s) = \frac{\omega_{P1}\left(1 + \frac{s}{\omega_{Z1}}\right)}{s\left(1 + \frac{s}{\omega_{P2}}\right)} \quad (51)$$

$$\omega_{Z1} = \frac{1}{C_{COMP} \times R_{COMP}} \quad (52)$$

$$\omega_{P1} = \frac{G_m \times \frac{R_{FBB}}{R_{FBB} + R_{FBT}}}{C_{COMP} + C_{COMP2}} \quad (53)$$

$$\omega_{P2} = \frac{C_{COMP} + C_{COMP2}}{C_{COMP} \times C_{COMP2} \times R_{COMP}} \quad (54)$$

To stabilize the regulator, ensure that the regulator crossover frequency is less than or equal to one-fifth of the right-half plane zero with Equation 55.

$$f_C \leq \frac{f_R}{5} \quad (55)$$

To determine the crossover frequency it is important to note that, at that frequency, the compensation impedance (Z_{COMP}) is dominated by a resistor, and the output impedance (Z_{OUT}) is dominated by the impedance of an output capacitor. Therefore, when solving for the crossover frequency, the equation (by definition of the crossover frequency) of the loop gain is simplified to Equation 56.

$$|T| = \frac{V_{FB}}{V_{OUT}} \times \frac{V_{IN}}{V_{OUT}} \times G_m \times \frac{1}{2\pi \times f_C \times C_O} \times R_{COMP} \times \frac{1}{A \times R_{SEN}} = 1 \quad (56)$$

where

- |T| is the loop gain magnitude
- V_{FB} is feedback voltage, 1.275 V
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

- G_m is the error amplifier transconductance
- Z_{COMP} is the impedance of the compensation network from the COMP pin to ground
- R_{SEN} is the current sensing resistor
- A is equal to 0.86 and it is the internal sensing amplification of the LM3017
- C_O is the output capacitor value (56)

Solve for R_{COMP} with Equation 57.

$$R_{COMP} = \frac{2\pi \times f_C \times C_O \times V_{OUT}^2}{V_{FB} \times V_{IN} \times G_m} \times A \times R_{SEN} \quad (57)$$

Once the compensation resistor is known, set the zero formed by the compensation capacitor and resistor to one-fourth of the crossover frequency in Equation 58.

$$C_{COMP} = \frac{2}{\pi \times f_C \times R_{COMP}}$$

where

- C_{COMP} is the compensation capacitor (58)

The high-frequency capacitor C_{COMP2}, is chosen to cancel the zero introduced by output capacitance ESR with Equation 59.

$$C_{COMP2} = \frac{ESR \times C_O}{R_{COMP}} \quad (59)$$

For optimal transient performance, R_{COMP} and C_{COMP} might require adjustment by observing the load transient response.

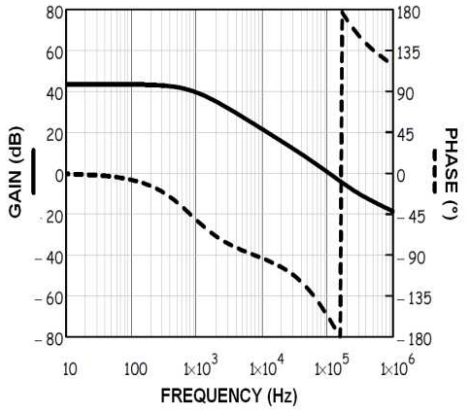
For detailed explanation on how to select the right compensation components for a boost topology, see *AN-1286 Compensation for the LM3478 Boost Controller* (SNVA067), and *AN-1994 Modeling and Design of Current Mode Control Boost Converters* (SNVA408).

8.2.2.13.2 Compensation Design Example

Table 3 lists the design parameters for this application example to calculate the compensation network.

Table 3. Design Parameters

PARAMETER	VALUE
Input voltage, V_{IN}	8 V to 12 V
Output voltage, V_{OUT}	15 V
Output current, I_{OUT}	1 A
Switching frequency, f_S	600 kHz
Duty cycle, D (considering losses)	0.482 with V_{IN} = 8 V
	0.223 with V_{IN} = 12 V
Right-half plane zero, f_R	136.187 kHz when V_{IN} = 8 V
	206.421 kHz when V_{IN} = 12 V
Inductor, L	4.7 µH
Output capacitance, C_O (considering derating due to applied voltage)	33 µF



V_{IN} = 8 V, V_{OUT} = 15 V, I_{OUT} = 1 A

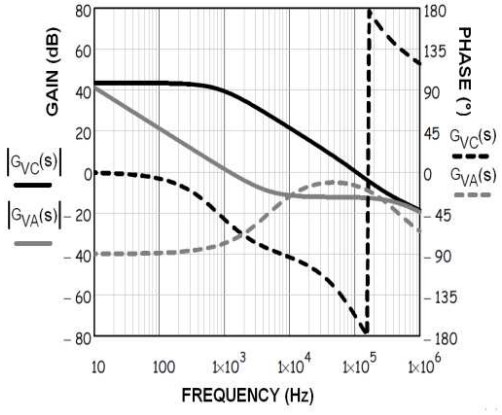
Figure 26. Control-to-Output Transfer Function $G_{VC}(s)$ Bode Plot

Choose the crossover frequency with Equation 60.

$$f_C = 20 \text{ kHz} = f_S / 20\ f_R / 5 \quad (60)$$

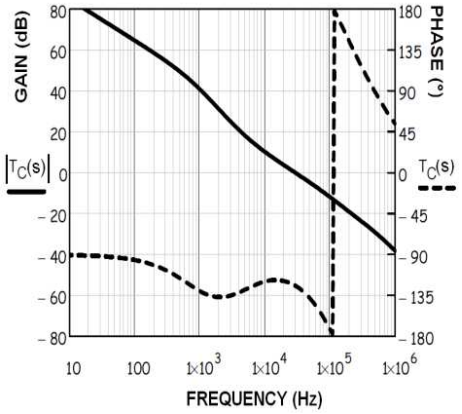
Table 4. Calculated Compensation Network Components

PARAMETER	CALCULATED VALUE	ACTUAL VALUE
R_{COMP}	3.42 kΩ	3.4 kΩ
C_{COMP}	9.306 nF	10 nF
C_{COMP2}	96.48 pF	100 pF



V_{IN} = 8 V, V_{OUT} = 15 V, I_{OUT} = 1 A

Figure 27. $G_{VC}(s)$ and Compensation Network $G_{VA}(s)$ Bode Plots



V_{IN} = 8 V, V_{OUT} = 15 V, I_{OUT} = 1 A

Figure 28. Closed-Loop Bode Plot T(s)

Table 5. Bill of Materials (BOM) for LM3017

DESIGNATION	DESCRIPTION	SIZE	MANUFACTURER PART #	VENDOR
C_{IN1}	Cap 22 µF, 25 V X5R	1206	GRM31CR61E226KE15L	Murata
C_{O1},C_{O2}, C_{O3}	Cap 22 µF, 25 V X5R	1206	GRM31CR61E226KE15L	Murata
C_{COMP}	Cap 0.022 µF	0603	C0603C103J1RACTU	Kemet
C_{COMP2}	Cap 1000 pF	0603	C1608C0G1H101J	TDK
C_{BYP}	Cap 0.1 µF, 25 V X7R	0603	06033C104KAT2A	AVX
C_{VCC}	Cap 0.47 µF, 16 V X7R	0805	C2012X7R1C474K	TDK
R_{COMP}	RES, 3.4 kΩ, 1%, 0.1W	0603	CRCW06033K40FKEA	Vishay

Table 5. Bill of Materials (BOM) for LM3017 (continued)

DESIGNATION	DESCRIPTION	SIZE	MANUFACTURER PART #	VENDOR
R_{FBT}	RES, 21.5 kΩ, 1%, 0.1W	0603	CRCW060321K5FKEA	Vishay
R_{FBB}	RES, 2 kΩ, 1%, 0.1W	0603	CRCW06032K00FKEA	Vishay
R_S	RES, 100 Ω, 1%, 0.1W	0603	CRCW0603100RFKEA	Vishay
R_{SEN}	RES, 0.03 Ω, 1%, 1W	1206	WSLP1206R0300FEA	Vishay
Q_1	NexFET™ N-CH, 25 V, 60 A, $R_{DS(on)}$= 4.4 mΩ	8-SON	CSD16323Q3	TI
Q_2	NexFET™ N-CH, 25 V, 60 A, $R_{DS(on)}$= 4.3 mΩ	8-SON	CSD16340Q3	TI
D_1	Diode Schottky, 30 V, 2 A	SMB	20BQ030TRPBF	Vishay
L_1	Shielded Inductor, 4.7 µH, 2.3 A	4 mm L × 4 mm W × 1.85 mm H	MPI4040R3-4R7-R	Cooper
U_1	LM3017	—	—	TI

8.2.3 Application Curve

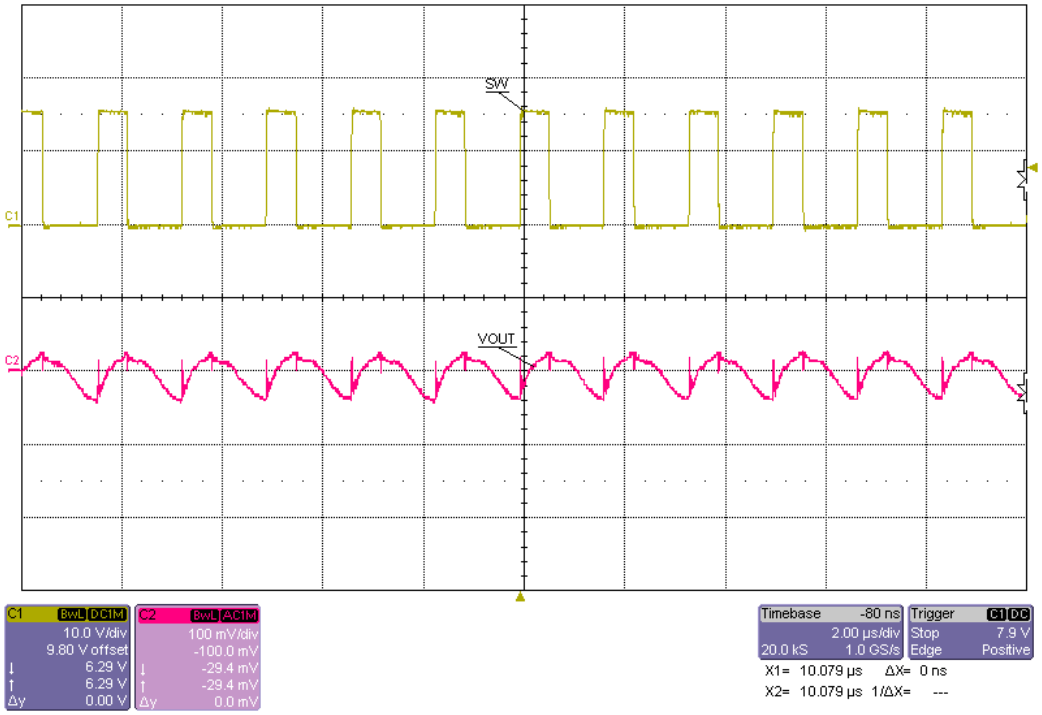


Figure 29. Switch Node and Output Voltage Ripple With 5.5 V_{IN} and 15 V at 1-A Output

9 Power Supply Recommendations

The LM3017 is designed to operate from an input voltage supply range from 5 V to 18 V. This input supply must be able to withstand the maximum input current and maintain a voltage above 5 V. In cases where input supply is placed farther away (more than a few inches) from LM3017, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

Good board layout is critical for switching controllers such as the LM3017. First the ground plane area must be sufficient for thermal dissipation purposes and second, appropriate guidelines must be followed to reduce the effects of switching noise. Switch mode converters are very fast switching devices. In such devices, the rapid increase of input current combined with the parasitic trace inductance generates unwanted voltage noise spikes. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may create electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, take care in layout to minimize the effect of this switching noise.

10.1.1 Filter Capacitors

Ceramic filter capacitors are most effective when the inductance of the current loops that they filter is minimized. Place C_{BYP} as close as possible to the VIN and GND pins of the LM3017. Place C_{VCC} next to the VCC and GND pins of the LM3017 (see Figure 16 for designators).

10.1.2 Sense Lines

The current sensing circuit in current mode devices can be easily effected by switching noise. This noise can cause duty cycle jitter which leads to increased spectral noise. R_{SEN} must be connected to the ISEN pin with a separate trace made as short as possible, TI also recommends to route the trace that connects the VIN pin to the input voltage as close as possible to R_{SEN}. Route this trace away from the inductor and the switch node (where D1, Q1, and L1 connect). For the voltage loop, keep $R_{FBB/T}$ close to the LM3017 and run a trace as close as possible to the positive side of C_O. As with the ISEN line, the FB line must be routed away from the inductor and the switch node. These measures minimize the length of high impedance lines and reduce noise pickup.

10.1.3 Compact Layout

The most important layout rule is to keep the AC current loops as small as possible. Figure 30 shows the current flow of a boost converter. The top schematic shows a dotted line which represents the current flow during on-state and the middle schematic shows the current flow during off-state. The bottom schematic shows the currents referred to as AC currents. They are the most critical ones because current is changing in very short time periods. The dotted line traces of the bottom schematic are the ones to make as short as possible. In a boost regulator the primary switching loop consists of the output capacitor, diode and MOSFET. Minimizing the area of this loop reduces the stray inductances and minimizes noise and possible erratic operation (see *Layout Examples*). The output capacitor(s) must be placed as close as possible to the diode cathode and MOSFET GND.

Layout Guidelines (continued)

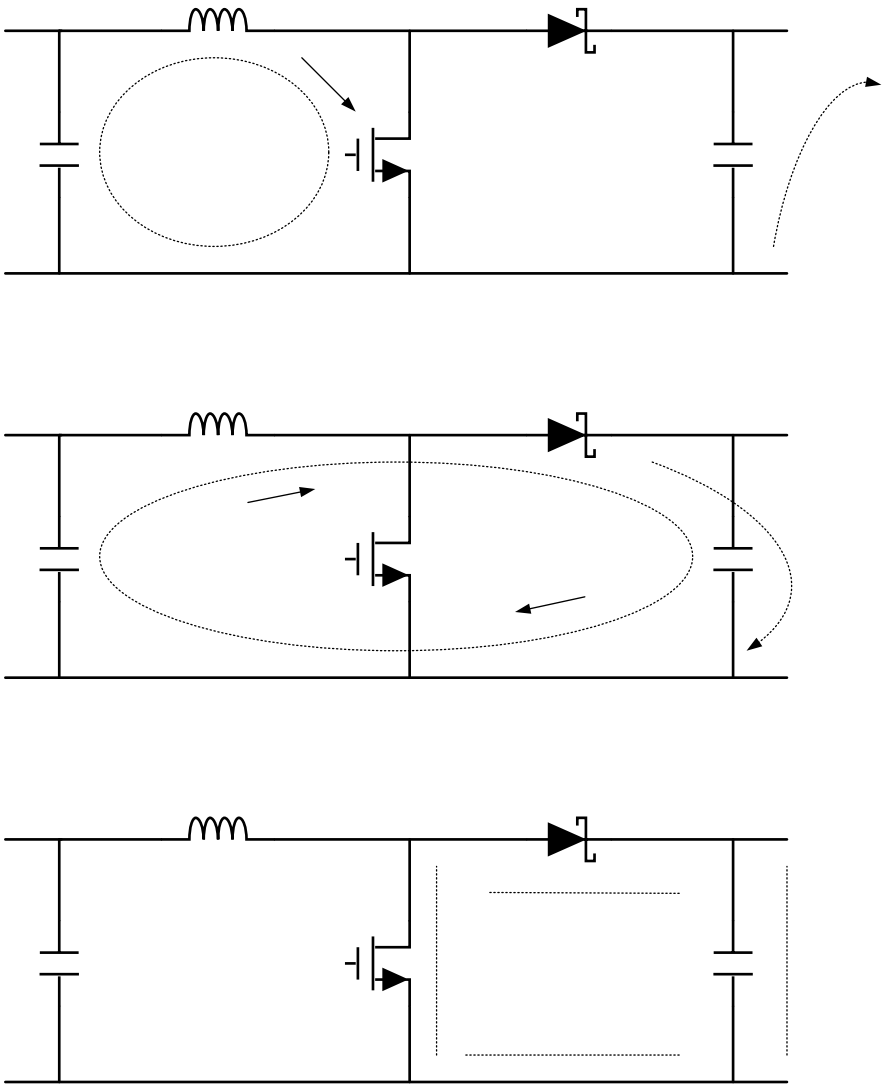


Figure 30. Current Flow in a Boost Application

10.1.4 Ground Plane and Vias

A ground plane in the printed-circuit board is recommended as a means to connect the quiet end (input voltage ground side) of the input filter capacitor to the output filter capacitors and the PGND pin of the controller. Connect all the low power ground connections directly to the regulator AGND. Connect the AGND and PGND pins together through a copper area covering the entire underside of the device. Place several vias in this underside copper area to ground plane. If a via is required to connect the sensing resistor to the ISEN pin, then place that via in the inner side of the sensing resistor such that no current flow occurs. Place several vias from the ground side of the output capacitor(s) to ground place, that minimizes the path for AC current. The PGND and AGND pins have to be connected to the same ground very close to the IC. To avoid ground loop currents attach all the grounds of the system only at one point.

10.2 Layout Examples

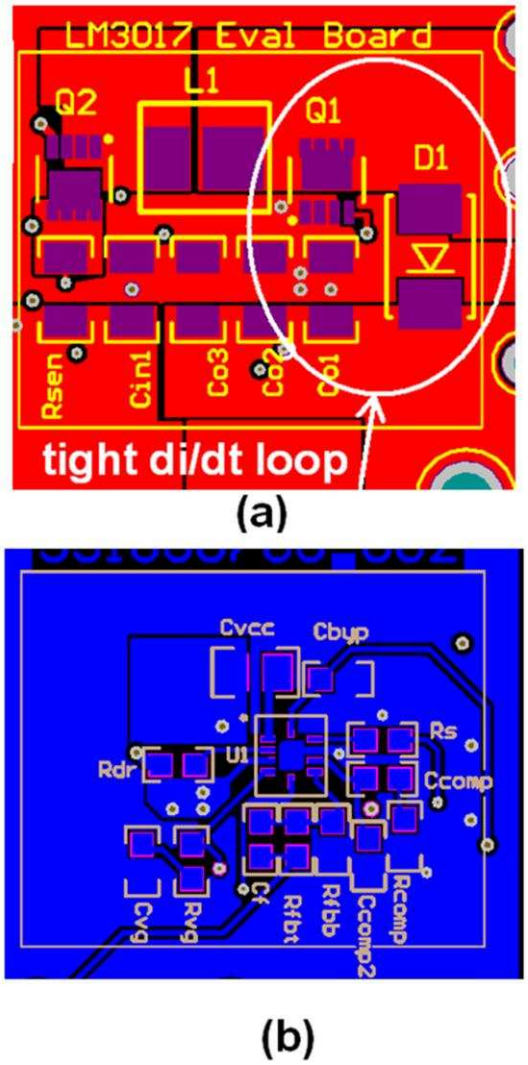


Figure 31. Layout Example (a) Top Layer, (b) Bottom Layer

10.3 Thermal Considerations

The majority of power dissipation and heat generation comes from FETs and diode. Selecting MOSFETs with exposed pads aids the power dissipation of these devices. Careful attention to RDS(on) at high temperature must be observed. Diode data sheets provide a typical junction-to-ambient thermal resistance $R_{\theta JA}$, which can be used to estimate the operating die temperature of the Schottky. Multiplying the power dissipation by $R_{\theta JA}$ gives the temperature rise. The diode case size can then be selected to maintain the Schottky diode temperature below the operational maximum. Larger case sizes generally have lower $R_{\theta JA}$ and lower forward voltage drop.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *AN-1286 Compensation for the LM3478 Boost Controller* (SNVA067)
- *AN-1994 Modeling and Design of Current Mode Control Boost Converters* (SNVA408)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
Thunderbolt is a trademark of Intel Corporation.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3017LE/NOPB	Active	Production	WQFN (NKL) | 10	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	SK6B
LM3017LE/NOPB.A	Active	Production	WQFN (NKL) | 10	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	SK6B
LM3017LEX/NOPB	Active	Production	WQFN (NKL) | 10	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	SK6B
LM3017LEX/NOPB.A	Active	Production	WQFN (NKL) | 10	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	SK6B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

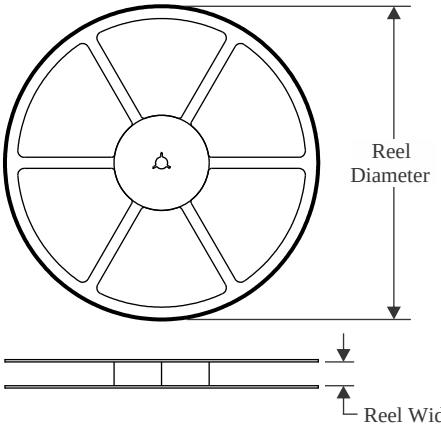
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

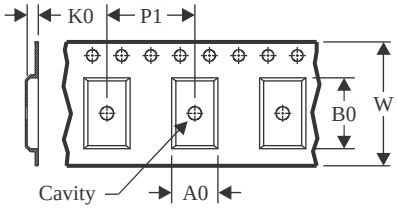
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

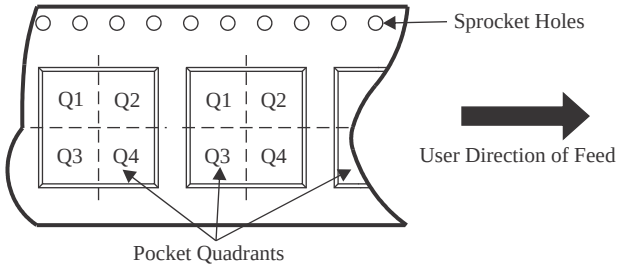


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

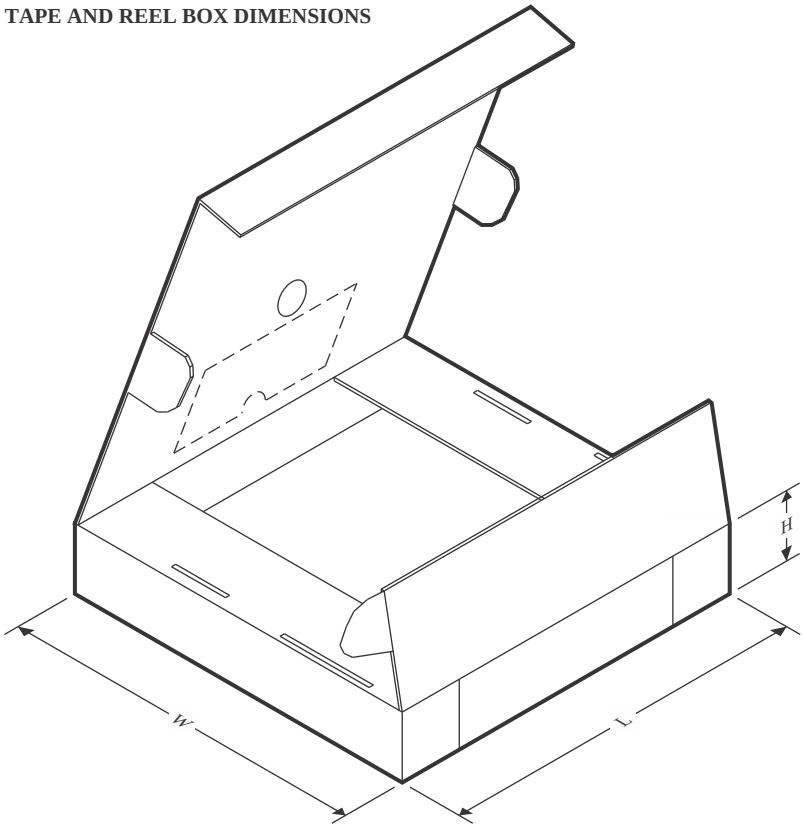
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3017LE/NOPB	WQFN	NKL	10	1000	177.8	12.4	2.7	3.0	1.0	8.0	12.0	Q1
LM3017LEX/NOPB	WQFN	NKL	10	4500	330.0	12.4	2.7	3.0	1.0	8.0	12.0	Q1

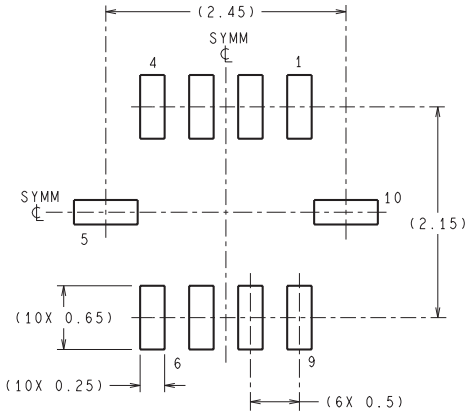
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

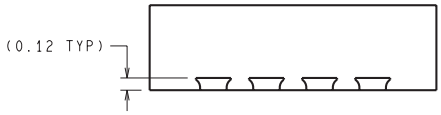
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3017LE/NOPB	WQFN	NKL	10	1000	208.0	191.0	35.0
LM3017LEX/NOPB	WQFN	NKL	10	4500	356.0	356.0	36.0

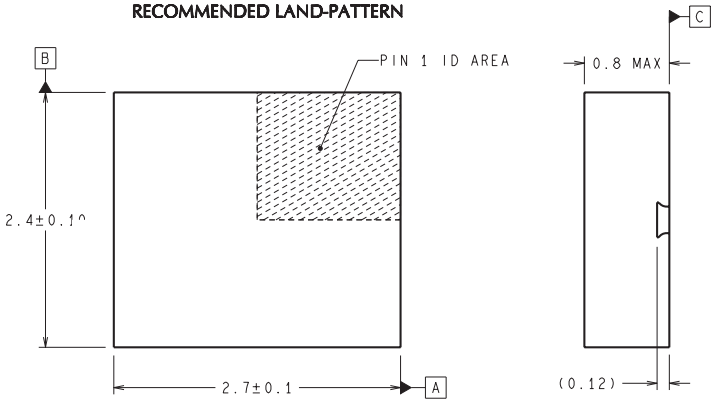
NKL0010A



RECOMMENDED LAND-PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN ( ) FOR REFERENCE ONLY





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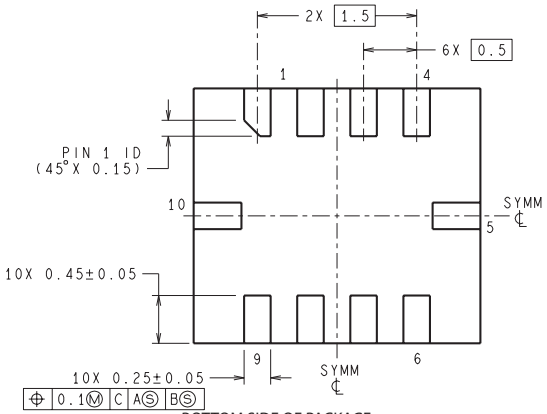

BOTTOM SIDE OF PACKAGE

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