INA20x Unidirectional Measurement Current-Shunt Monitor With Dual Comparators

1 Features

- Complete Current Sense Solution
- Three Gain Options Available:
  - INA206 = 20 V/V
  - INA207 = 50 V/V
  - INA208 = 100 V/V
- Dual Comparators:
  - Comparator 1 With Latch
  - Comparator 2 With Optional Delay
- Common-mode Range: –16 V to 80 V
- High Accuracy: 3.5% (Maximum) Over Temperature
- Bandwidth: 500 kHz
- Quiescent Current: 1.8 mA
- Packages: SO-14, TSSOP-14, VSSOP-10

2 Applications

- Notebook Computers
- Cell Phones
- Telecom Equipment
- Automotive
- Power Management
- Battery Chargers
- Welding Equipment

3 Description

The INA206, INA207, and INA208 are a family of undirectional current-shunt monitors with voltage output, dual comparators, and voltage reference. The INA206, INA207, and INA208 can sense drops across shunts at a common-mode voltages from –16 V to 80 V. The INA206, INA207, and INA208 are available with three output voltage scales: 20 V/V, 50 V/V, and 100 V/V, with up to 500-kHz bandwidth.

The INA206, INA207, and INA208 also incorporates two open-drain comparators with internal 0.6-V references. On 14-pin versions, the comparator references can be overridden by external inputs. Comparator 1 includes a latching capability, and Comparator 2 has a user-programmable delay on 14-pin versions. The 14-pin versions also provide a 1.2 V reference output.

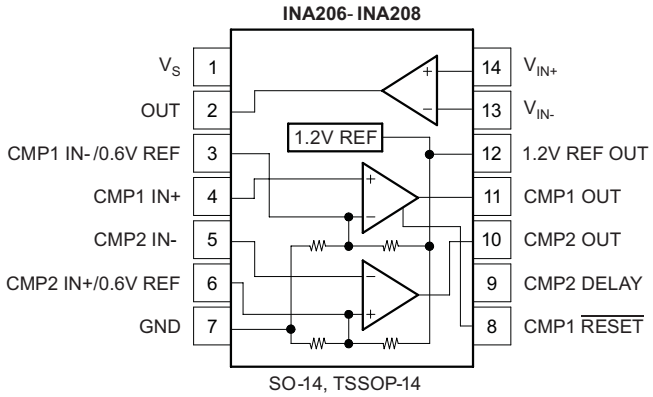
The INA206, INA207, and INA208 operate from a single 2.7-V to 18-V supply. They are specified over the extended operating temperature range of –40°C to 125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA206 INA207 INA208	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



SO-14, TSSOP-14

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2007) to Revision F **Page**

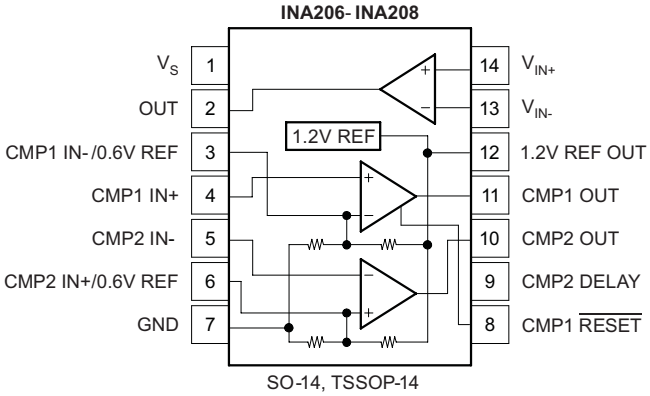
- *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Device Comparison Table

DEVICE	GAIN
INA206	20 V/V
INA207	50 V/V
INA208	100 V/V

6 Pin Configuration and Functions

D or PW Packages
14-Pin SOIC OR TSSOP
Top View

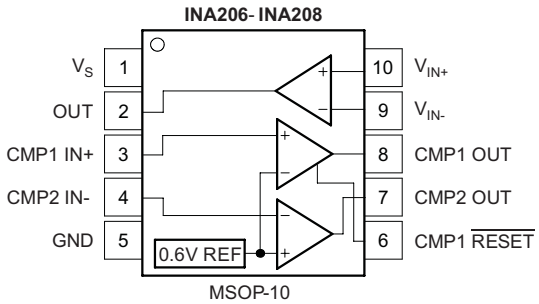


SO-14, TSSOP-14

Pin Functions: SOIC and TSSOP

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Vs	I	Power Supply
2	OUT	O	Output voltage
3	CMP1 IN- /0.6V Ref	I	Comparator 1 negative input, can be used to override the internal 0.6-V reference
4	CMP1 IN+	I	Comparator 1 positive input
5	CMP2 IN-	I	Comparator 2 negative input
6	CMP2 IN+/0.6V Ref	I	Comparator 2 positive input, can be used to override the internal 0.6-V reference
7	GND	I	Ground
8	CMP1 $\overline{\text{RESET}}$	I	Comparator 1 ouput reset, active low
9	CMP2 DELAY	I	Connect an optional capacitor to adjust comparator 2 delay
10	CMP2 OUT	O	Comparator 2 output
11	CMP1 OUT	O	Comparator 1 output
12	1.2V REF OUT	O	1.2-V reference output
13	VIN-	I	Connect to shunt low side
14	VIN+	I	Connect to shunt high side

DGS Package
10-Pin VSSOP
Top View



Pin Functions: VSSOP

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_S	I	Power Supply
2	OUT	O	Output voltage
3	CMP1 IN+	I	Comparator 1 positive input
4	CMP2 IN-	I	Comparator 2 negative input
5	GND	I	Ground
6	$\frac{\text{CMP1}}{\text{RESET}}$	I	Comparator 1 ouput reset, active low
7	CMP2 OUT	O	Comparator 2 output
8	CMP1 OUT	O	Comparator 1 output
9	VIN-	I	Connect to shunt low side
10	VIN+	I	Connect to shunt high side

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S			18	V
Current-shunt monitor analog inputs, V_{IN+} and V_{IN-}	Differential (V_{IN+}) – (V_{IN-})	–18	18	V
	Common-Mode	–16	80	V
Comparator analog input and reset pins		GND – 0.3	(V_S) + 0.3	V
Analog output, out pin		GND – 0.3	(V_S) + 0.3	V
Comparator output, out pin		GND – 0.3	18	V
V_{REF} and CMP2 delay pin		GND – 0.3	10	V
Input current into any pin			5	mA
Operating temperature		–55	150	°C
Junction temperature		–65	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Vcm Common-mode input voltage	–16	12	80	V
Vs Operating supply voltage	2.7	12	18	V
T_A Operating free-air temperature	–40	25	125	ºC

7.4 Thermal Information

THERMAL METRIC (1)		INA20x			UNIT
		D (SOIC)	DGS (VSSOP)	PW (TSSOP)	
		14 PINS	10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.9	161.3	112.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44	36.8	37.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.4	82.3	55.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.3	1.3	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.1	80.8	54.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	150	200	150	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: Current-Shunt Monitor

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, and CMP1 IN+ = 1 V and CMP2 IN– = GND, unless otherwise noted.

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{SENSE}	Full-scale sense input voltage	$V_{SENSE} = V_{IN+} - V_{IN-}$			0.15	$(V_S$ –0.25)/Gain	V
V_{CM}	Common-mode input range	T_A = –40°C to 125°C		–16		80	V
CMRR	Common-mode rejection ratio	V_{IN+} = –16 V to 80 V		80	100		dB
	Common-mode rejection ratio over temperature	V_{IN+} = 12 V to 80 V, T_A = –40°C to 125°C		100		123	dB
V_{OS}	Offset voltage RTI (1)	T_A = 25°C			±0.5	±2.5	mV
		T_A = 25°C to 125°C				±3	
		T_A = –40°C to 25°C				±3.5	
dV_{OS}/dT	Offset voltage RTI vs temperature	T_A = –40°C to 125°C			5		µV/°C
PSR	Offset voltage RTI vs power supply	V_{OUT} = 2 V, V_{IN+} = 18 V, 2.7 V, T_A = –40°C to 125°C			2.5	100	µV/V
I_B	Input bias current, V_{IN-} Pin	T_A = –40°C to 125°C			±9	±16	µA
OUTPUT (V_{SENSE} ≥ 20 mV)							
G	Gain	INA206			20		V/V
		INA207			50		
		INA208			100		
	Gain error	V_{SENSE} = 20 mV to 100 mV			±0.2%	±1%	
	Gain error over temperature	V_{SENSE} = 20 mV to 100 mV, T_A = –40°C to 125°C				±2%	
	Total output error (2)	V_{SENSE} = 120 mV, V_S = 16 V			±0.75%	±2.2%	
	Total output error over temperature	V_{SENSE} = 120 mV, V_S = 16 V, T_A = –40°C to 125°C				±3.5%	
	Nonlinearity error (3)	V_{SENSE} = 20 mV to 100 mV			±0.002%		
R_O	Output impedance				1.5		Ω
	Maximum capacitive load	No Sustained Oscillation			10		nF
OUTPUT (VSENSE < 20 mV) (4)							
	Output voltage	INA206	–16 V ≤ V_{CM} < 0 V		300		mV
		INA207			300		
		INA208			300		
		INA206	0 V ≤ V_{CM} ≤ V_S, V_S = 5 V			0.4	V
		INA207				1	
		INA208				2	
		INA206	V_S < V_{CM} ≤ 80 V		300		mV
		INA207			300		
		INA208			300		
VOLTAGE OUTPUT							
	Output swing to the positive rail	V_{IN-} = 11 V, V_{IN+} = 12 V, T_A = –40°C to 125°C			(V_s) – 0.15	(V_s) – 0.25	V
	Output swing to GND (5)	V_{IN-} = 0 V, V_{IN+} = –0.5 V, T_A = –40°C to 125°C			(V_{GND}) + 0.004	(V_{GND}) + 0.05	V

(1) Offset is extrapolated from measurements of the output at 20 mV and 100 mV V_{SENSE}.
(2) Total output error includes effects of gain error and V_{OS}.
(3) Linearity is best fit to a straight line.
(4) For details on this region of operation, see the *Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage* section.
(5) Specified by design.

Electrical Characteristics: Current-Shunt Monitor (continued)

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, and CMP1 IN+ = 1 V and CMP2 IN– = GND, unless otherwise noted.

PARAMETERS	TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
Bandwidth	INA206	C_{LOAD} = 5 pF		500		kHz
	INA207			300		
	INA208			200		
Phase margin	C_{LOAD} < 10 pF			40		°
Slew rate				1		V/µs
Settling time (1%)	V_{SENSE} = 10 mV_{PP} to 100 mV_{PP}, C_{LOAD} = 5 pF			2		µs
NOISE, RTI						
Output voltage noise density				40		nV/√Hz

7.6 Electrical Characteristics: Comparator

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, unless otherwise noted.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
Offset Voltage	Comparator Common-Mode Voltage = Threshold Voltage, Figure 1		2		mV
Offset Voltage Drift, Comparator 1	T_A = –40°C to 125°C		±2		µV/°C
Offset Voltage Drift, Comparator 2	T_A = –40°C to 125°C		5.4		µV/°C
Threshold	T_A = 25°C	590	608	620	mV
Threshold over Temperature	T_A = –40°C to 125°C	586		625	mV
Hysteresis (1), CMP1	T_A = –40°C to 85C		–8		mV
Hysteresis (1), CMP2	T_A = –40°C to 85°C		8		mV
INPUT BIAS CURRENT (2)					
CMP1 IN+, CMP2 IN–			0.005	10	nA
CMP1 IN+, CMP2 IN– vs Temperature	T_A = –40°C to 125°C			15	nA
INPUT IMPEDANCE					
Pins 3 and 6 (14-pin packages only)			10		kΩ
INPUT RANGE					
CMP1 IN+ and CMP2 IN–			0 V to V_S – 1.5V		V
Pins 3 and 6 (14-pin packages only) (3)			0 V to V_S – 1.5V		V
OUTPUT					
Large-signal differential voltage gain	CMP V_{OUT} 1 V to 4 V, R_L ≥ 15 kΩ connected to 5 V		200		V/mV
High-level output current	V_{ID} = 0.4 V, V_{OH} = V_S		0.0001	1	µA
Low-level output voltage	V_{ID} = –0.6 V, I_{OL} = 2.35 mA		220	300	mV
RESPONSE TIME (3)					
Comparator 1	R_L to 5 V, C_L = 15 pF, 100-mV Input Step with 5-mV Overdrive		1.3		µs
Comparator 2	R_L to 5 V, C_L = 15 pF, 100-mV Input Step with 5-mV Overdrive, C_{DELAY} Pin Open		1.3		µs
RESET					
RESET Threshold (4)			1.1		V
Logic Input Impedance			2		mΩ
Minimum RESET Pulse Width			1.5		µs
RESET Propagation Delay			3		µs

(1) Hysteresis refers to the threshold (the threshold specification applies to a rising edge of a noninverting input) of a falling edge on the noninverting input of the comparator. See Figure 1.
(2) Specified by design.
(3) The comparator response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.
(4) $\overline{\text{RESET}}$ input has an internal 2 MΩ (typical) pull-down. Leaving $\overline{\text{RESET}}$ open results in a LOW state, with transparent comparator operation.

Electrical Characteristics: Comparator (continued)

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, unless otherwise noted.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator 2 Delay Equation (5)			$C_{DELAY} = t_D/5$		µF
Comparator 2 Delay, t_D	C_{DELAY} = 0.1 µF		0.5		s

(5) The Comparator 2 delay applies to both rising and falling edges of the comparator output.

7.7 Electrical Characteristics: Reference

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, unless otherwise noted.

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE VOLTAGE						
	$1.2V_{REFOUT}$ Output Voltage		1.188	1.2	1.212	V
dV_{OUT}/dT	Reference Drift	T_A = –40°C to 85°C		40	100	ppm/°C
	0.6VREF Output Voltage (Pins 3 and 6 of 14-pin packages only)			0.6		V
dV_{OUT}/dT	Reference Drift	T_A = –40°C to 85°C		40	100	ppm/°C
dV_{OUT}/dI_{LOAD}	LOAD REGULATION					
	Sourcing	0 mA < I_{SOURCE} < 0.5 mA		0.4	2	mV/mA
	Sinking	0 mA < I_{SINK} < 0.5 mA		0.4		mV/mA
I_{LOAD}	LOAD CURRENT	T_A = –40°C to 125°C		1		mA
dV_{OUT}/dV_S	LINE REGULATION	2.7 V < V_S < 18 V, T_A = –40°C to 125°C		30		µV/V
	CAPACITIVE LOAD					
	Reference Output Maximum Capacitive Load	No Sustained Oscillations		10		nF
	OUTPUT IMPEDANCE					
	Pins 3 and 6 of 14-Pin Packages Only			10		kΩ

7.8 Electrical Characteristics: General

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, and CMP1 IN+ = 1 V and CMP2 IN– = GND, unless otherwise noted.

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Operating Power Supply	T_A = –40°C to 125°C	2.7		18	V
I_Q	Quiescent Current	V_{OUT} = 2 V		1.8	2.2	mA
	Quiescent Current over Temperature	V_{SENSE} = 0 mV, T_A = –40°C to 125°C			2.8	mA
	Comparator Power-On Reset Threshold (1)			1.5		V
TEMPERATURE						
	Specified Temperature Range		–40		125	°C
	Operating Temperature Range		–55		150	°C
	Storage Temperature Range		–65		150	°C
θ_{JA}	Thermal Resistance	MSOP-10 Surface-Mount		200		°C/W
		SO-14, TSSOP-14 Surface-Mount		150		°C/W

(1) The INA206, INA207, and INA208 are designed to power-up with the comparator in a defined reset state as long as CMP1 $\overline{\text{RESET}}$ is open or grounded. The comparator will be in reset as long as the power supply is below the voltage shown here. The comparator will assume a state based on the comparator input above this supply voltage. If CMP1 $\overline{\text{RESET}}$ is high at power-up, the comparator output comes up high and requires a reset to assume a low state, if appropriate.

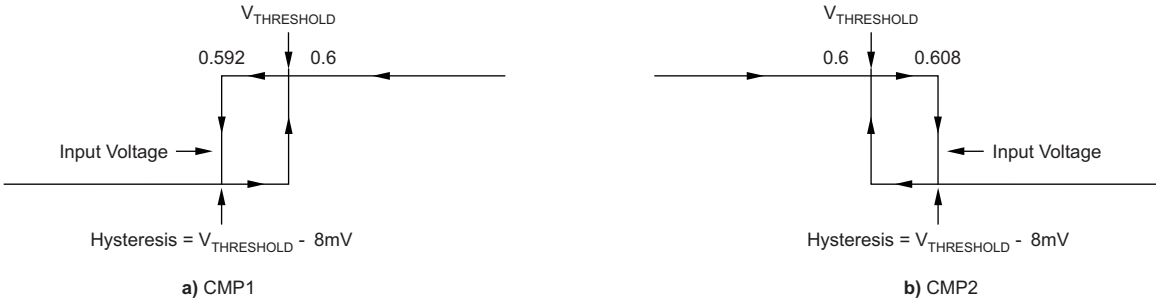


Figure 1. Comparator Hysteresis

7.9 Typical Characteristics

All specifications at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

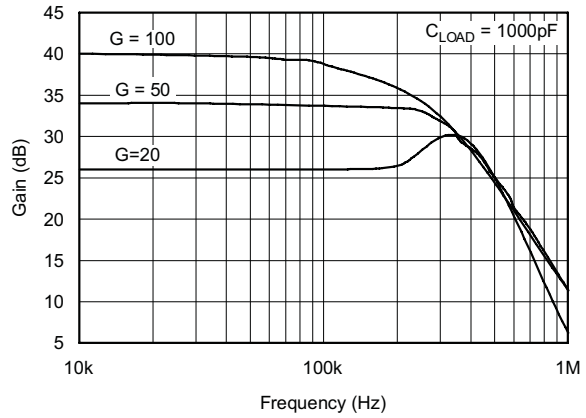


Figure 2. Gain vs Frequency

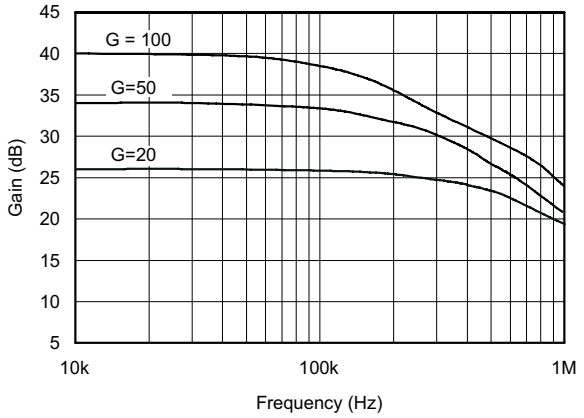


Figure 3. Gain vs Frequency

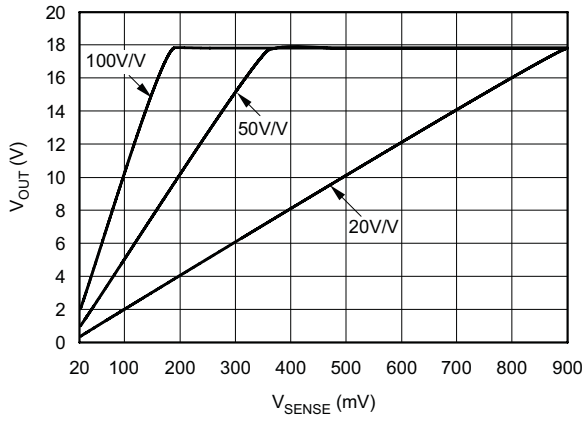


Figure 4. Gain Plot

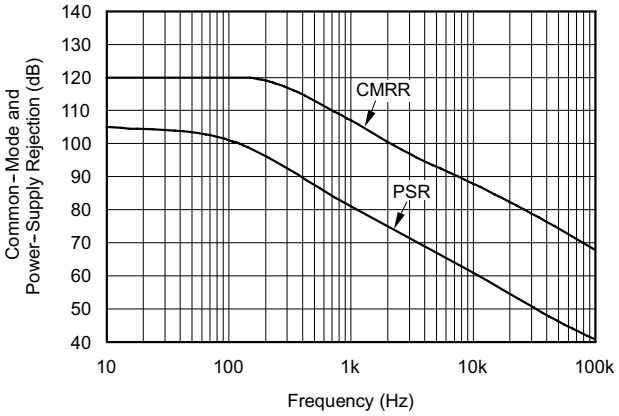


Figure 5. Common-Mode and Power-Supply Rejection vs Frequency

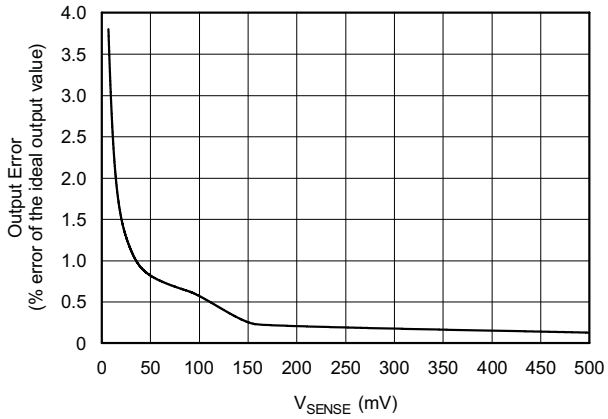


Figure 6. Output Error vs V_{SENSE}

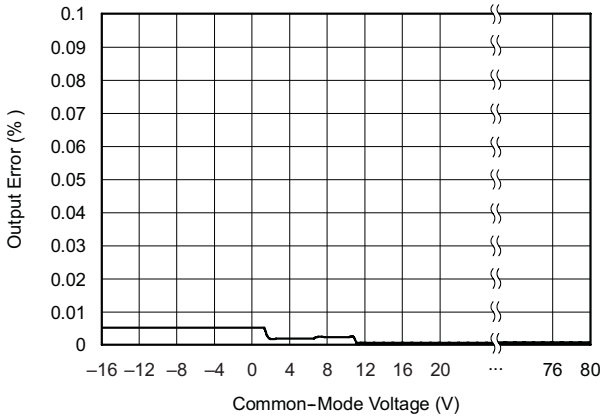


Figure 7. Output Error vs Common-Mode Voltage

Typical Characteristics (continued)

All specifications at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

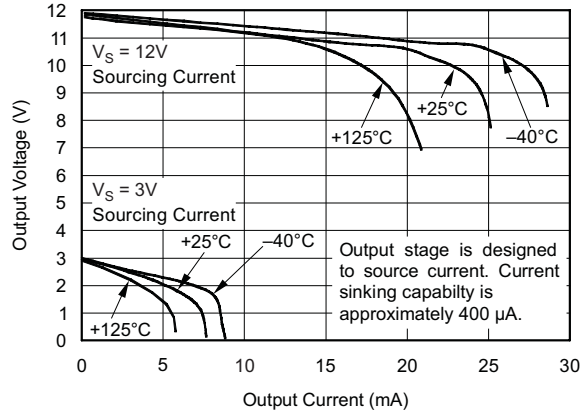


Figure 8. Positive Output Voltage Swing vs Output Current

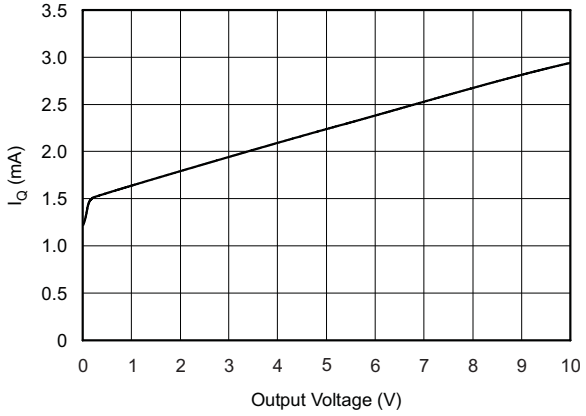


Figure 9. Quiescent Current vs Output Voltage

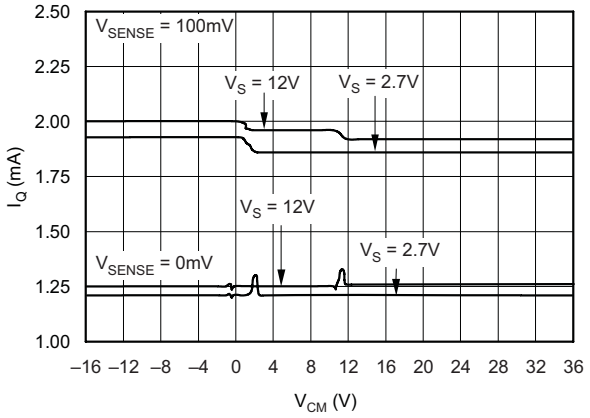


Figure 10. Quiescent Current vs Common-Mode Voltage

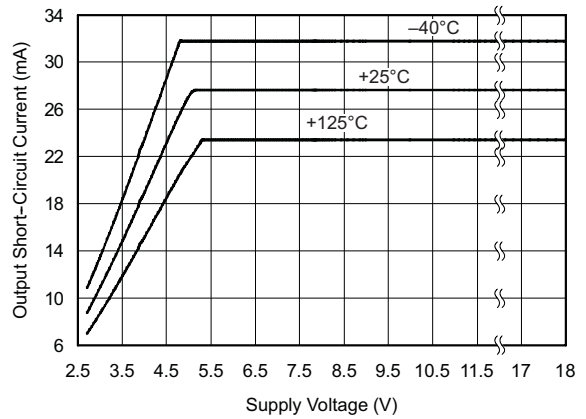


Figure 11. Output Short-Circuit Current vs Supply Voltage

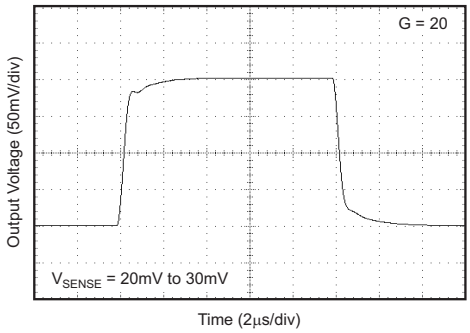


Figure 12. Step Response

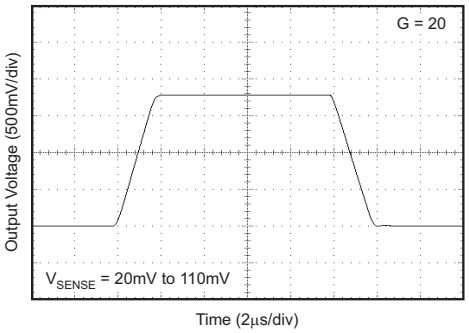


Figure 13. Step Response

Typical Characteristics (continued)

All specifications at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

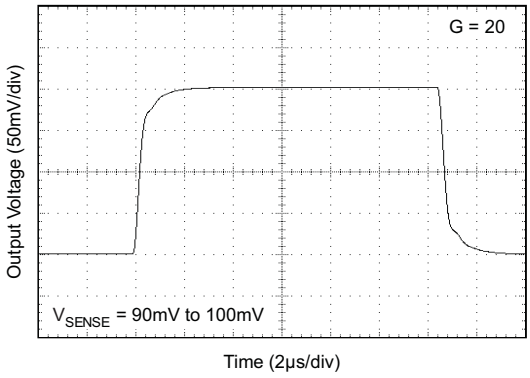


Figure 14. Step Response

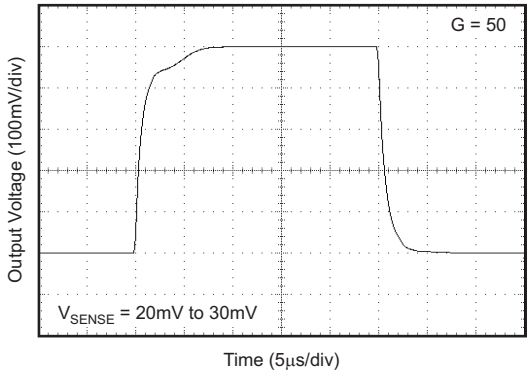


Figure 15. Step Response

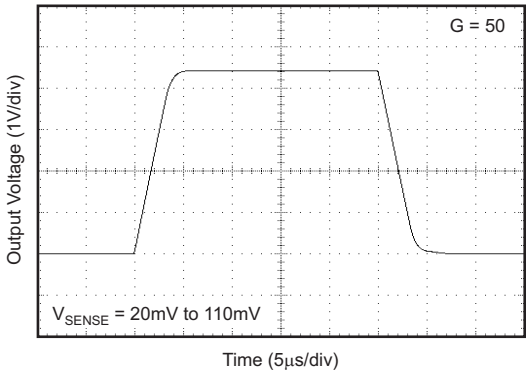


Figure 16. Step Response

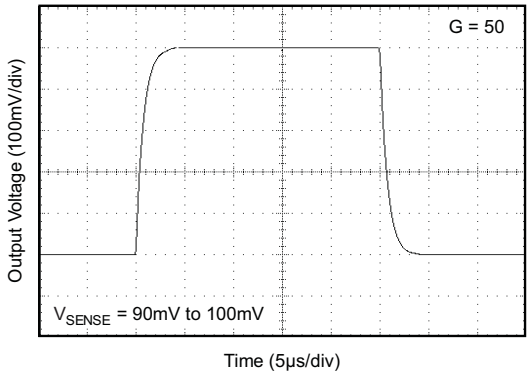


Figure 17. Step Response

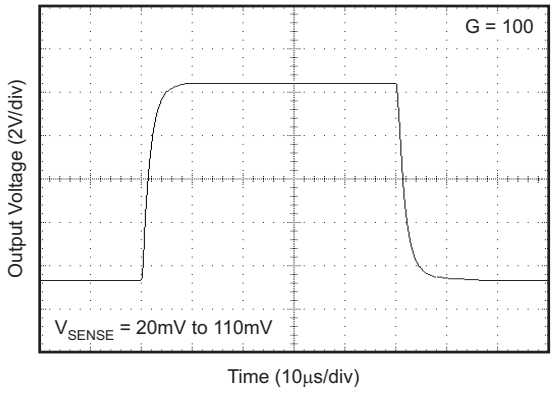


Figure 18. Step Response

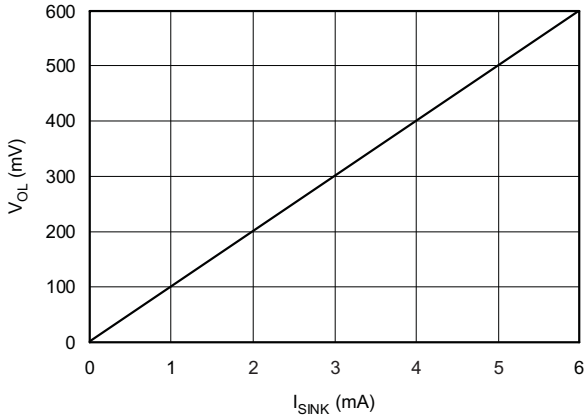


Figure 19. Comparator V_{OL} vs I_{SINK}

Typical Characteristics (continued)

All specifications at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

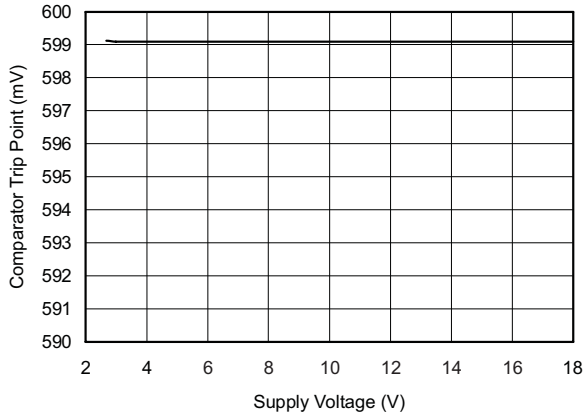


Figure 20. Comparator Trip Point vs Supply Voltage

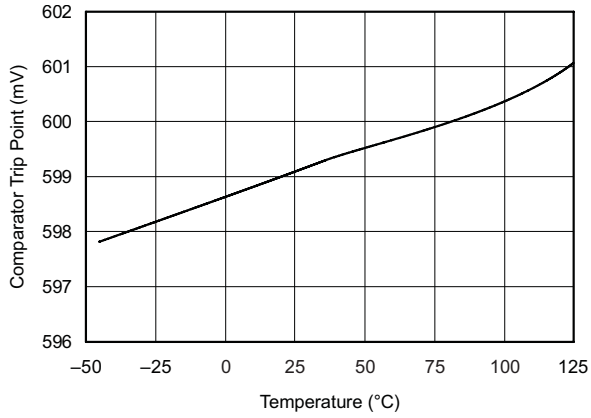


Figure 21. Comparator Trip Point vs Temperature

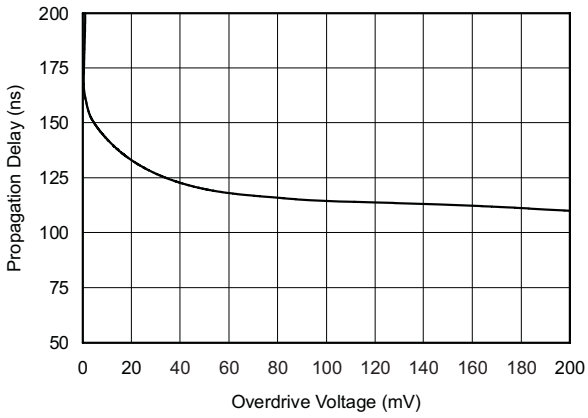


Figure 22. Comparator 1 Propagation Delay vs Overdrive Voltage

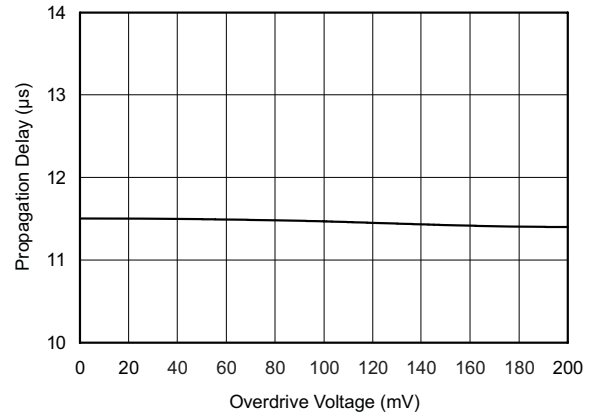


Figure 23. Comparator 2 Propagation Delay vs Overdrive Voltage

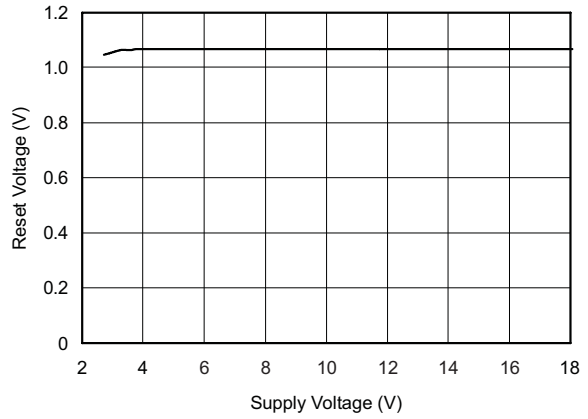


Figure 24. Comparator Reset Voltage vs Supply Voltage

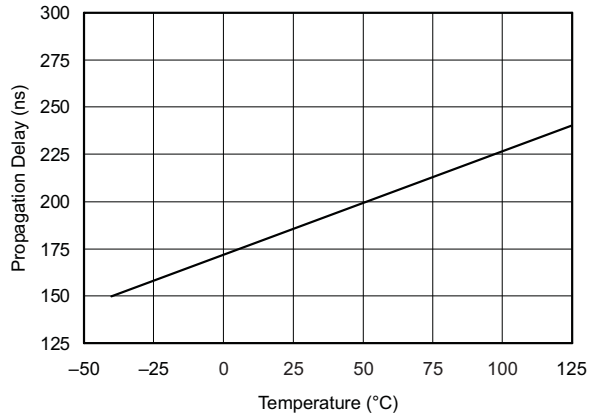


Figure 25. Comparator 1 Propagation Delay vs Temperature

Typical Characteristics (continued)

All specifications at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

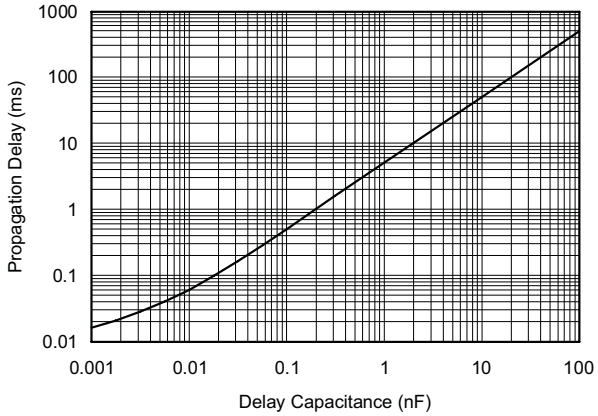


Figure 26. Comparator 2 Propagation Delay vs Capacitance

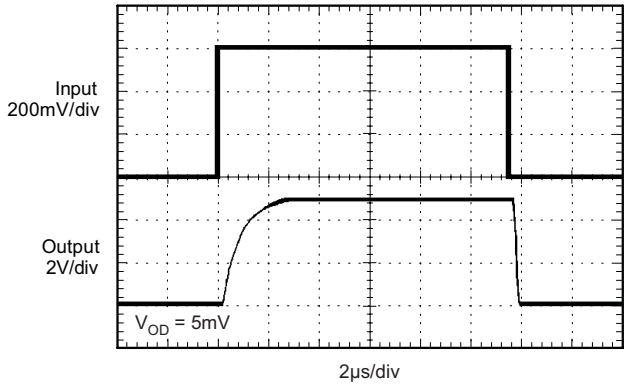


Figure 27. Comparator 1 Propagation Delay

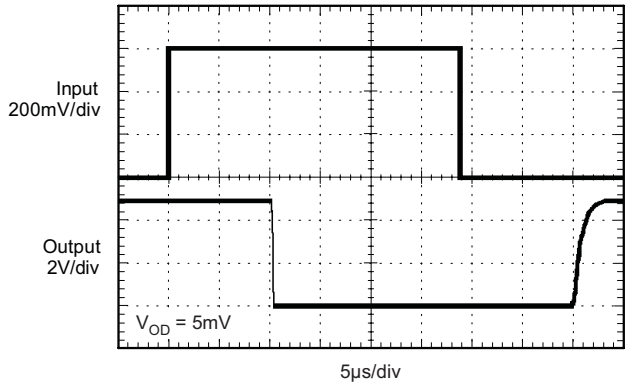


Figure 28. Comparator 2 Propagation Delay

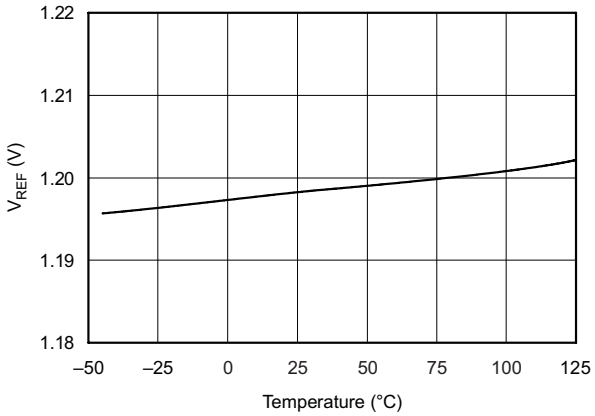


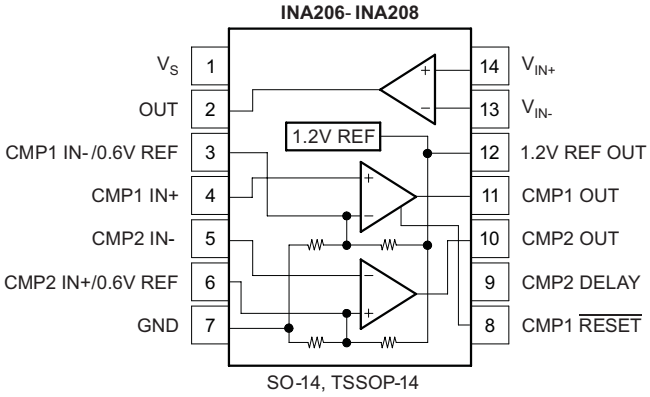
Figure 29. Reference Voltage vs Temperature

8 Detailed Description

8.1 Overview

The INA206, INA207, and INA208 are a family of unidirectional current-shunt monitors with voltage output, dual comparators, and voltage reference. The INA206, INA207, and INA208 can sense drops across shunts at common-mode voltages from –16 V to 80 V. The INA206, INA207, and INA208 are available with three output voltage scales: 20 V/V, 50 V/V, and 100 V/V, with up to 500-kHz bandwidth. The INA206, INA207, and INA208 also incorporate two open-drain comparators with internal 0.6-V references. On 14-pin versions, the comparator references can be overridden by external inputs. Comparator 1 includes a latching capability, and Comparator 2 has a user-programmable delay. 14-pin versions also provide a 1.2-V reference output. The INA206, INA207, and INA208 operate from a single 2.7-V to 18-V supply. They are specified over the extended operating temperature range of –40°C to 125°C

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Voltage Range

The output of the INA206, INA207, and INA208 is accurate within the output voltage swing range set by the power supply pin, V_S. This performance is best illustrated when using the INA208 (a gain of 100 version), where a 100-mV full-scale input from the shunt resistor requires an output voltage swing of 10 V, and a power-supply voltage sufficient to achieve 10 V on the output.

8.3.2 Reference

The INA206, INA207, and INA208 include an internal voltage reference that has a load regulation of 0.4 mV/mA (typical), and not more than 100 ppm/°C of drift. Only the 14-pin package allows external access to reference voltages, where voltages of 1.2 V and 0.6 V are both available. Output current versus output voltage is illustrated in *Typical Characteristics*.

8.3.3 Comparator

The INA206, INA207, and INA208 devices incorporate two open-drain comparators. These comparators typically have 2 mV of offset and a 1.3-µs (typical) response time. The output of Comparator 1 latches and is reset through the CMP1 $\overline{\text{RESET}}$ pin, as shown in Figure 31. This configuration applies to both the 10- and 14-pin versions. Figure 30 illustrates the comparator delay.

The 14-pin versions of the INA206, INA207, and INA208 include additional features for comparator functions. The comparator reference voltage of both Comparator 1 and Comparator 2 can be overridden by external inputs for increased design flexibility. Comparator 2 has a programmable delay.

Feature Description (continued)

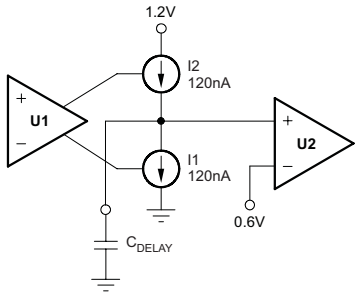


Figure 30. Simplified Model of the Comparator 2 Delay Circuit

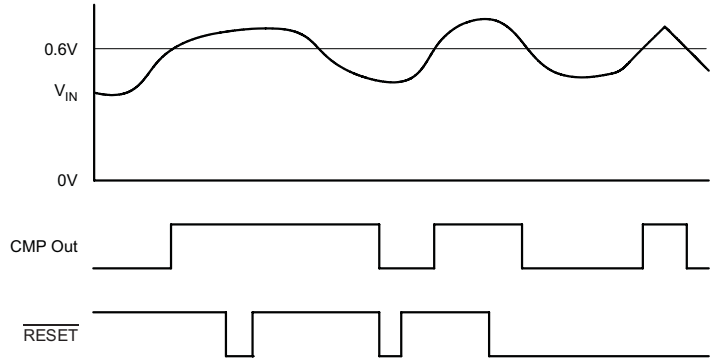


Figure 31. Comparator 1 Latching Capability

8.3.4 Comparator Delay (14-Pin Version Only)

The Comparator 2 programmable delay is controlled by a capacitor connected to the CMP2 Delay Pin; see Figure 40. The capacitor value (in µF) is selected by using Equation 1.

$$C_{DELAY}(\text{in } \mu F) = \frac{t_D}{5} \quad (1)$$

A simplified version of the delay circuit for Comparator 2 is shown in Figure 30. The delay comparator consists of two comparator stages with the delay between them. Note that I1 and I2 cannot be turned on simultaneously; I1 corresponds to a U1 low output and I2 corresponds to a U1 high output. Using an initial assumption that the U1 output is low, I1 is on, then U2 +IN is zero. If U1 goes high, I2 supplies 120 nA to C_{DELAY}. The voltage at U2 +IN begins to ramp toward a 0.6-V threshold. When the voltage crosses this threshold, the U2 output goes high while the voltage at U2 +IN continues to ramp up to a maximum of 1.2 V when given sufficient time (twice the value of the delay specified for C_{DELAY}). This entire sequence is reversed when the comparator outputs go low, so that returning to low exhibits the same delay.

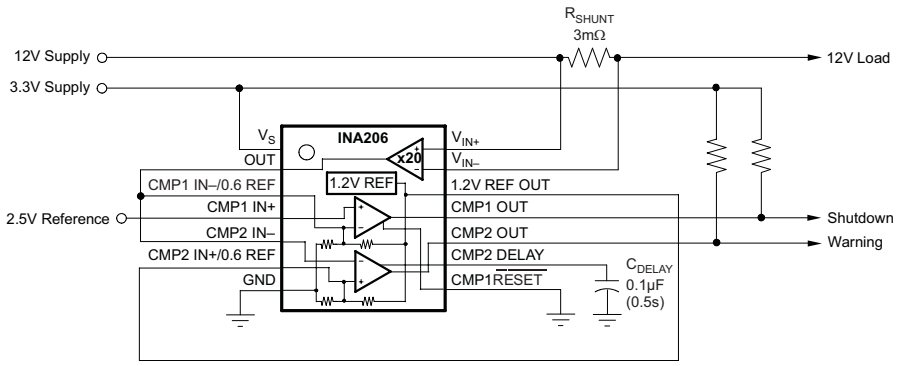


Figure 32. Server 12-V Supply Current Monitor

Feature Description (continued)

It is important to note what will happen if events occur more rapidly than the delay timeout; for example, when the U1 output goes high (turning on I2), but returns low (turning I1 back on) prior to reaching the 0.6-V transition for U2. The voltage at U2 +IN ramps back down at a rate determined by the value of C_{DELAY}, and only returns to zero if given sufficient time.

In essence, when analyzing Comparator 2 for behavior with events more rapid than its delay setting, use the model shown in Figure 30.

8.3.5 Comparator Maximum Input Voltage Range

The maximum voltage at the comparator input for normal operation is up to (V_S) – 1.5 V. There are special considerations when overdriving the reference inputs (pins 3 and 6). Driving either or both inputs high enough to drive 1 mA back into the reference introduces errors into the reference. Figure 33 shows the basic input structure. A general guideline is to limit the voltage on both inputs to a total of 20 V. The exact limit depends on the available voltage and whether either or both inputs are subject to the large voltage. When making this determination, consider the 20 kΩ from each input back to the comparator. Figure 34 shows the maximum input voltage that avoids creating a reference error when driving both inputs (an equivalent resistance back into the reference of 10 kΩ.

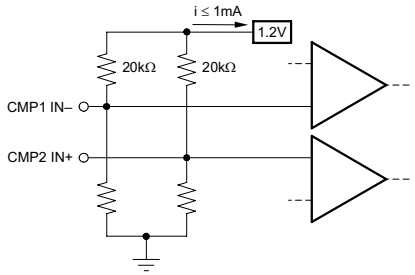


Figure 33. Limit Current Into Reference ≤ 1 mA

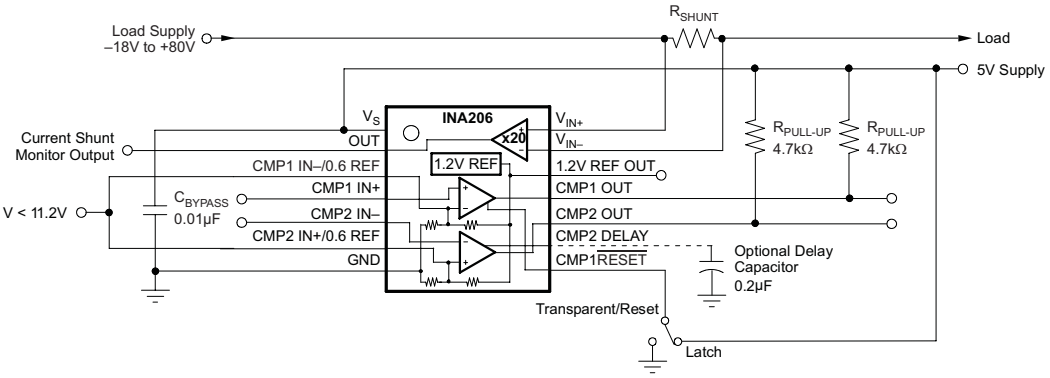


Figure 34. Overdriving Comparator Inputs Without Generating a Reference Error

Feature Description (continued)

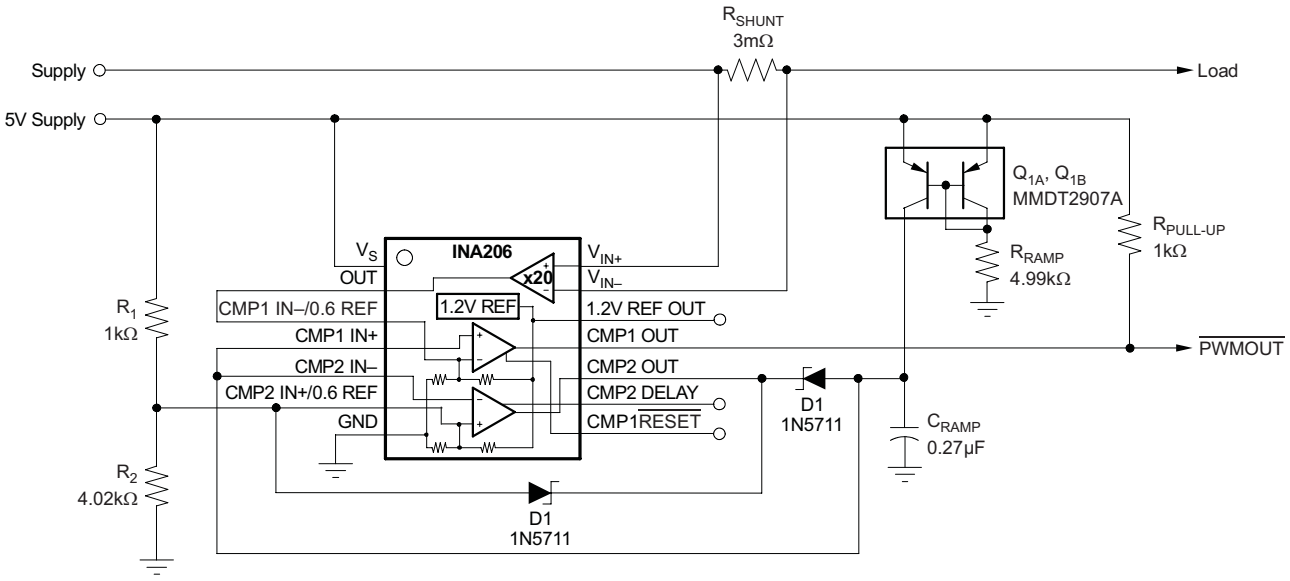


Figure 35. PWM Output Current-Shunt Monitor

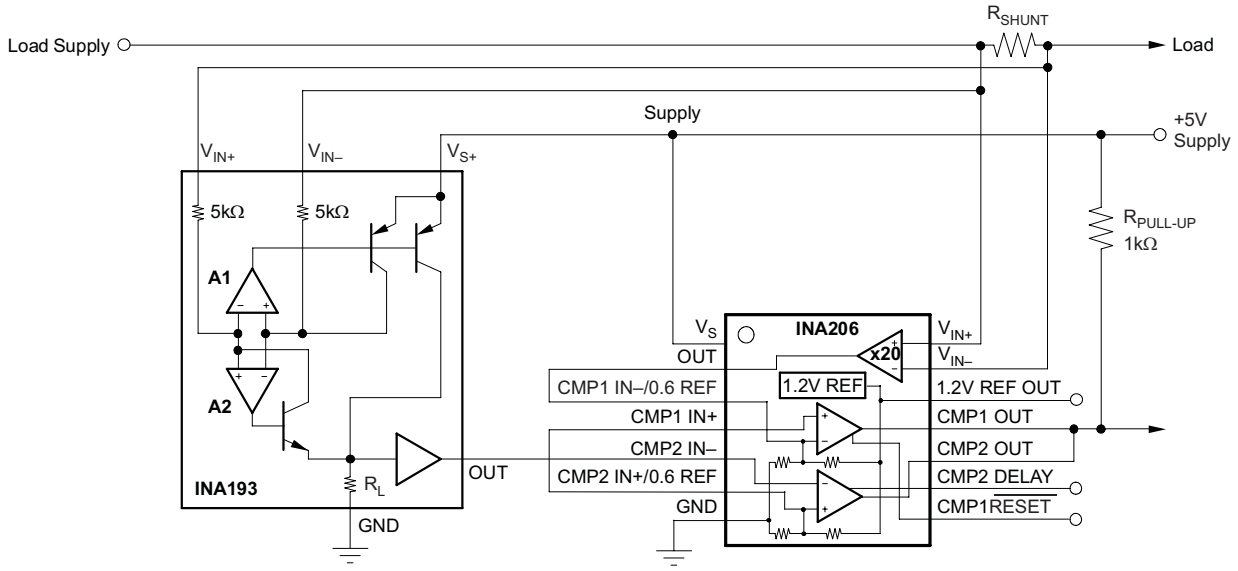


Figure 36. Bi-Directional Current Comparator

Feature Description (continued)

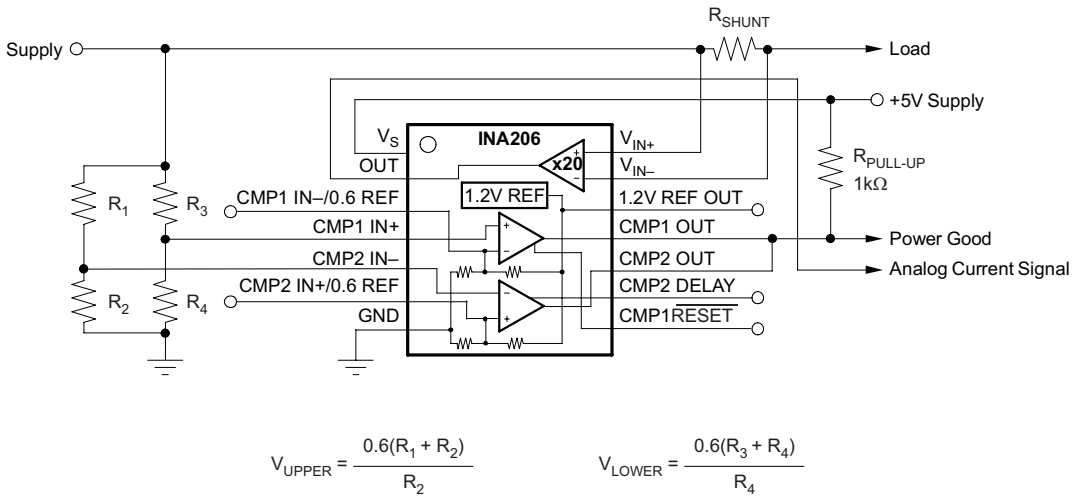


Figure 37. Analog Output Current-Shunt Monitor With Comparators Used as Power-Supply Under-Limit or Over-Limit or Power-Good Detector

8.4 Device Functional Modes

8.4.1 Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA206, INA207, and INA208 current-shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} – V_{IN–}$) and common-mode voltage, V_{CM}, relative to the supply voltage, V_S. V_{CM} is expressed as $(V_{IN+} + V_{IN–})/2$; however, in practice, V_{CM} is seen as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

- Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$
- Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$
- Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $–16\ V \leq V_{CM} < 0$
- Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, $0\ V \leq V_{CM} \leq V_S$
- Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

8.4.1.1 Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 2.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100\ mV - 20\ mV}$$

where

- V_{OUT1} = Output Voltage with V_{SENSE} = 100 mV
- V_{OUT2} = Output Voltage with V_{SENSE} = 20 mV (2)

Then the offset voltage is measured at V_{SENSE} = 100 mV and referred to the input (RTI) of the current-shunt monitor, as shown in Equation 3

$$V_{OS}RTI\ (Referred - To - Input) = \left(\frac{V_{OUT1}}{G}\right) - 100\ mV \quad (3)$$

In the Typical Characteristics, the *Output Error vs Common-Mode Voltage* curve shows the highest accuracy for this region of operation. In this plot, V_S = 12 V; for $V_{CM} \geq 12$ V, the output error is at its minimum. This case is also used to create the $V_{SENSE} \geq$ 20-mV output specifications in *Electrical Characteristics: Current-Shunt Monitor* through *Electrical Characteristics: General*.

Device Functional Modes (continued)

8.4.1.2 Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the part functions, as seen in the *Output Error vs Common-mode Voltage* curve. As noted, for this graph V_S = 12 V; for V_{CM} < 12 V, the Output Error increases as V_{CM} becomes less than 12 V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16 V.

Low V_{SENSE} Case 1: V_{SENSE} < 20 mV, –16 V ≤ V_{CM} < 0; and

Low V_{SENSE} Case 3: V_{SENSE} < 20 mV, V_S < V_{CM} ≤ 80 V

Although the INA206 family of devices are not designed for accurate operation in either of these regions, some applications are exposed to these conditions; for example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA206, INA207, or INA208. It is important to know what the behavior of the devices will be in these regions.

As V_{SENSE} approaches 0 mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the currenrt-shunt monitor output with a typical maximum value of V_{OUT} = 300 mV for V_{SENSE} = 0 mV. As V_{SENSE} approaches 20 mV, V_{OUT} Returns to the expected output value with accuracy as specified in *Electrical Characteristics: Current-Shunt Monitor* through *Electrical Characteristics: General*. Figure 38 illustrates this effect using the INA208 (Gain = 100).

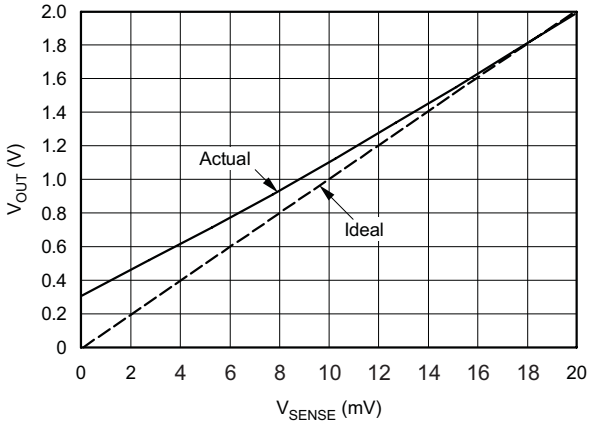
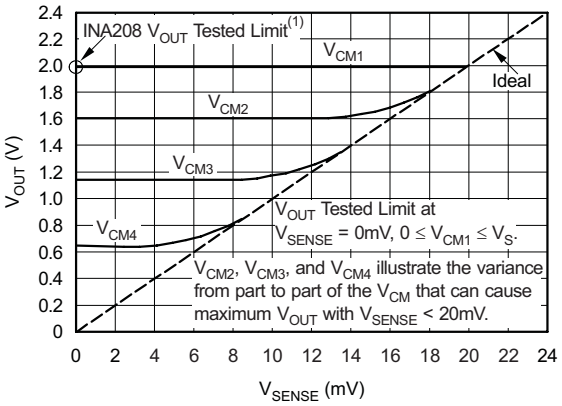


Figure 38. Example for Low V_{SENSE} Cases 1 and 3 (INA208, Gain = 100)

8.4.1.3 Low V_{SENSE} Case 2: $V_{SENSE} < 20$mV, 0V ≤ $V_{CM} \leq V_S$

This region of operation is the least accurate for the INA206 family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for Normal Case 2. This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, as V_{SENSE} approaches 20 mV, device operation is closer o that described by Normal Case 2. Figure 39 illustrates this behavior for the INA208. The V_{OUT} maximum peak for this case is tested by maintaining a constant VS, setting V_{SENSE} = 0 mV and sweeping V_{CM} from 0 V to VS. The exact V_{CM} at which V_{OUT} peaks during this test varies from part to part, but the V_{OUT} maximum peak is tested to be less than the specified V_{OUT} Tested Limit.

Device Functional Modes (continued)



NOTE: (1) INA206 V_{OUT} Tested Limit = 0.4V. INA207 V_{OUT} Tested Limit = 1V.

Figure 39. Example for Low V_{SENSE} Case 2 (INA208, Gain = 100)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Basic Connection

Figure 40 shows the basic connection of the INA206, INA207, and INA208. The input pins, VIN+ and VIN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

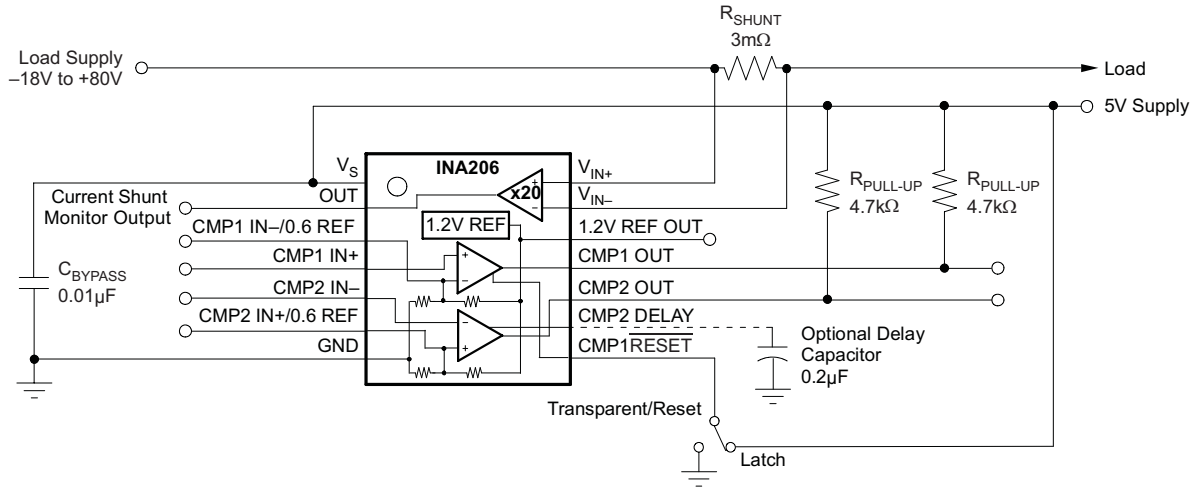


Figure 40. INA20x Basic Connection

9.2 Typical Application

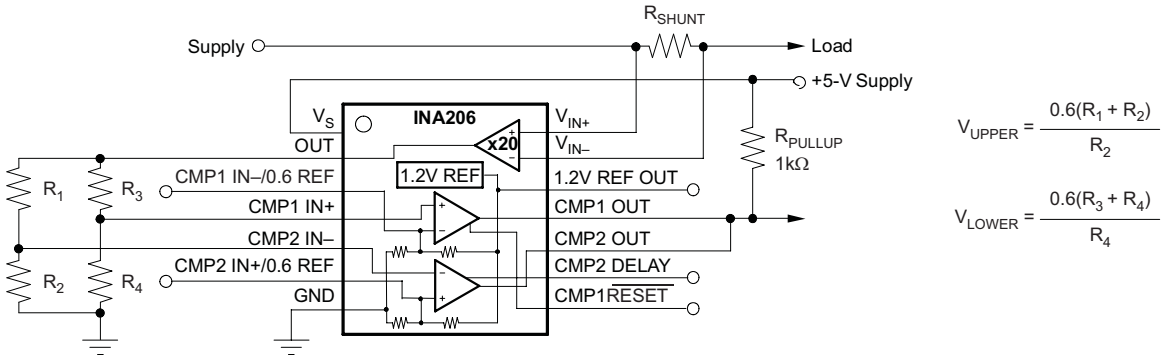


Figure 41. Using the INA206, INA207, and INA208 as Window Comparators

Typical Application (continued)

9.2.1 Design Requirements

The device measures current through a resistive shunt with current flowing in one direction. The outputs of the two comparators are in logic AND connection thus enabling the window comparison. When the INA output voltage is within the upper and lower limits, the composite comparator output is high. When the INA output voltage is above the upper limit or below the lower limit, the composite comparator output remains low.

9.2.2 Detailed Design Procedure

9.2.2.1 Selecting R_S

The value chosen for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_S minimize voltage loss in the supply line. For most applications, best performance is attained with an R_S value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is (V_S – 0.2) / Gain.

9.2.2.2 Transient Protection

The –16-V to 80-V common-mode range of the INA206, INA207, and INA208 is ideal for withstanding automotive fault conditions ranging from 12-V battery reversal up to 80-V transients, since no additional protective components are needed up to those levels. In the event that the INA206, INA207, and INA208 are exposed to transients on the inputs in excess of their ratings, then external transient absorption with semiconductor transient absorbers (Zeners or *Transzorbs*) will be necessary. Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it will never allow the INA206, INA207, and INA208 to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage due to transient absorber dynamic impedance). Despite the use of internal Zener-type ESD protection, the INA206, INA207, and INA208 do not lend themselves to using external resistors in series with the inputs since the internal gain resistors can vary up to ±30% but are closely matched. (If gain accuracy is not important, then resistors can be added in series with the INA206, INA207, and INA208 inputs with two equal resistors on each input.)

9.2.2.3 Input Filtering

An obvious and straightforward location for filtering is at the output of the INA206, INA207, and INA208 series; however, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA206, INA207, and INA208, which is complicated by the internal 5 kΩ + 30% input impedance; this is shown in Figure 42. Using the lowest possible resistor values minimizes both the initial shift in gain and effects of tolerance. The effect on initial gain is given by Equation 4.

$$\text{Gain Error\%} = 100 - \left(100 \times \frac{5\ \text{k}\Omega}{5\ \text{k}\Omega + R_{FILT}}\right) \tag{4}$$

Total effect on gain error can be calculated by replacing the 5-kΩ term with 5 kΩ – 30%, (or 3.5 kΩ) or 5 kΩ + 30%, (or 6.5 kΩ). The tolerance extremes of R_{FILT} can also be inserted into the equation. If a pair of 100 Ω 1% resistors are used on the inputs, the initial gain error will be 1.96%. Worst-case tolerance conditions will always occur at the lower excursion of the internal 5-kΩ resistor (3.5 kΩ), and the higher excursion of R_{FILT}– 2.8% in this case.

Typical Application (continued)

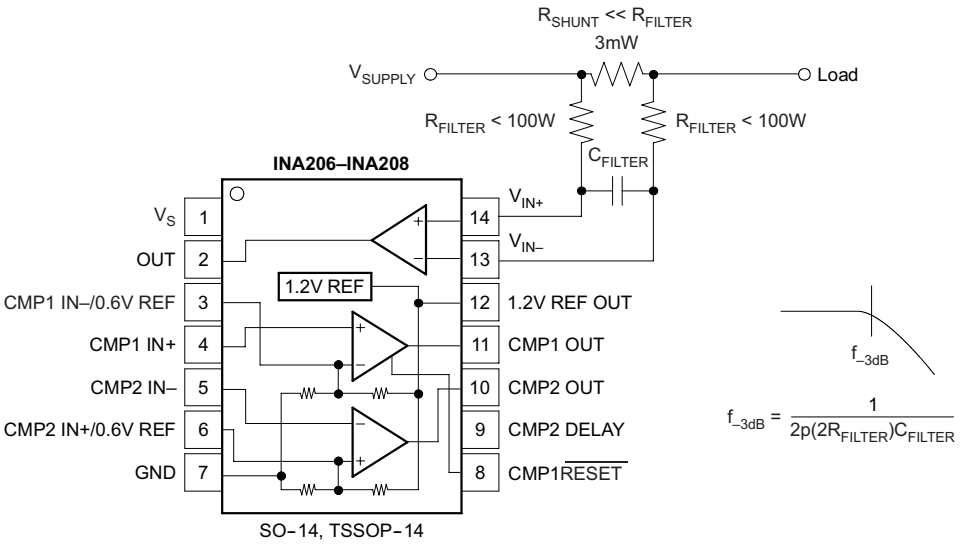


Figure 42. Input Filter (Gain Error 1.5% to 2.8%)

Note that the specified accuracy of the INA26, INA207, and INA208 must then be combined in addition to these tolerances. While this discussion treated accuracy worst-case conditions by combining the extremes of the resistor values, it is appropriate to use geometric mean or root sum square calculations to total the effects of accuracy variations.

Typical Application (continued)

9.2.3 Application Curve

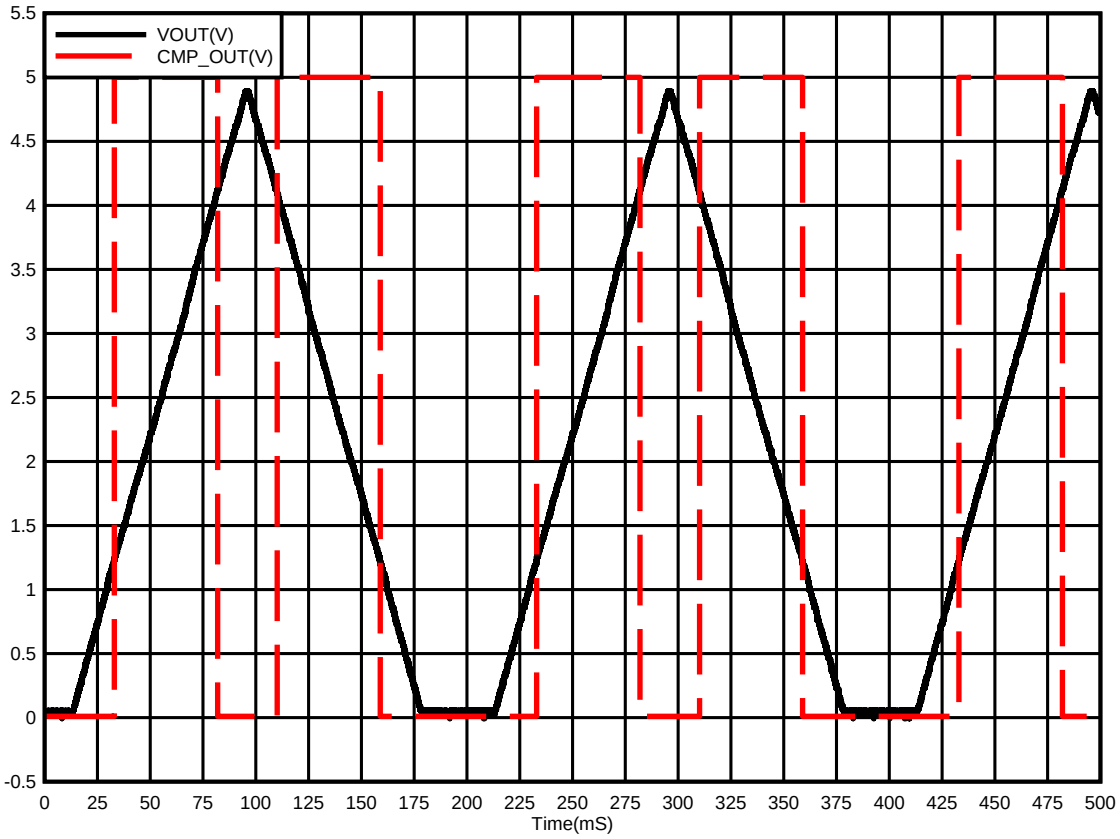


Figure 43. Window Comparator Circuit Response

10 Power Supply Recommendations

The input circuitry of the INA206, INA207, and INA208 can accurately measure beyond the power-supply voltage, V_S. For example, the V_S power supply can be 5 V, whereas the load power-supply voltage is up to 80 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- The power-supply bypass capacitor must be placed as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.2 Layout Example

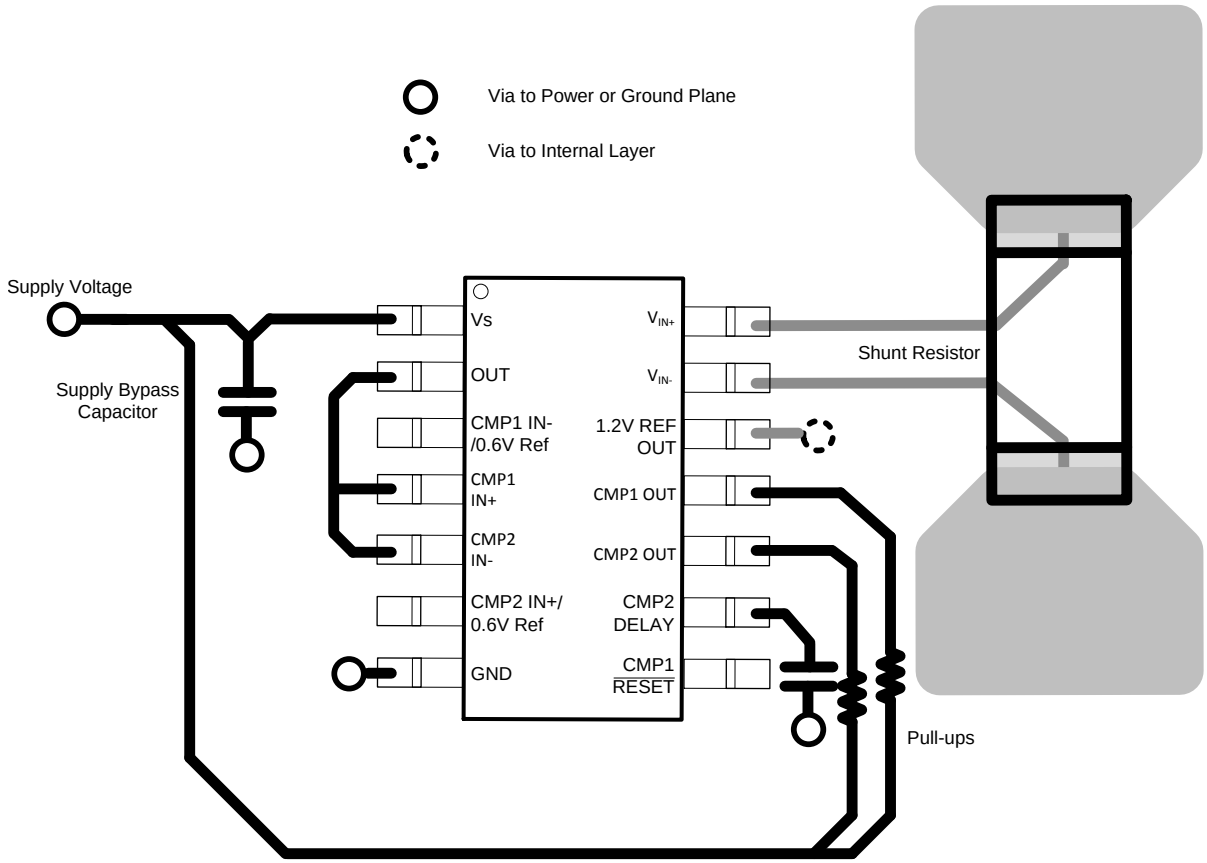


Figure 44. Layout Recommendation

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA206	Click here	Click here	Click here	Click here	Click here
INA207	Click here	Click here	Click here	Click here	Click here
INA208	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA206AID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	INA206A
INA206AIDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQQ
INA206AIDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQQ
INA206AIDGST	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 125	BQQ
INA206AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A
INA206AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A
INA206AIPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	INA206A
INA206AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A
INA206AIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A
INA206AIPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A
INA206AIPWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A
INA207AID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA207A
INA207AID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA207A
INA207AIDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQR
INA207AIDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQR
INA207AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA207A
INA207AIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA207A
INA208AID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	INA208A
INA208AIDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQS
INA208AIDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQS
INA208AIDGST	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 125	BQS
INA208AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA208A
INA208AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA208A
INA208AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA208A
INA208AIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA208A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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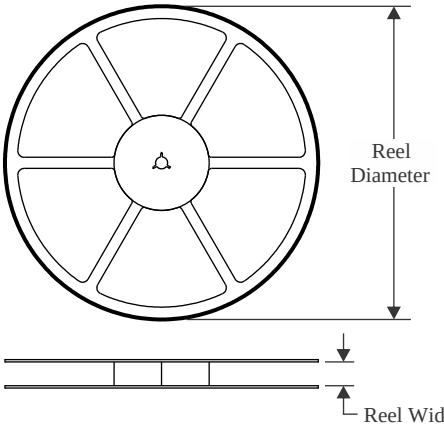
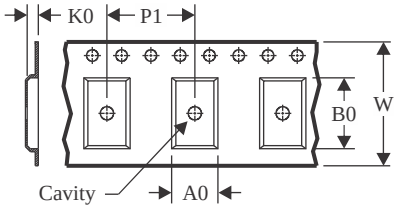
TAPE AND REEL INFORMATION

REEL DIMENSIONS

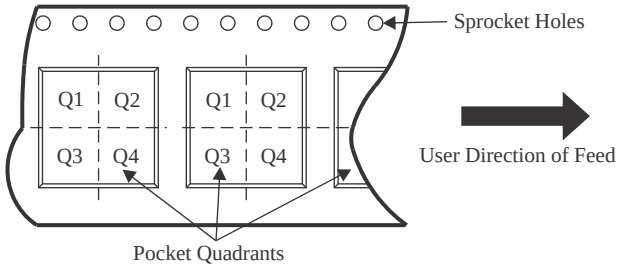


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

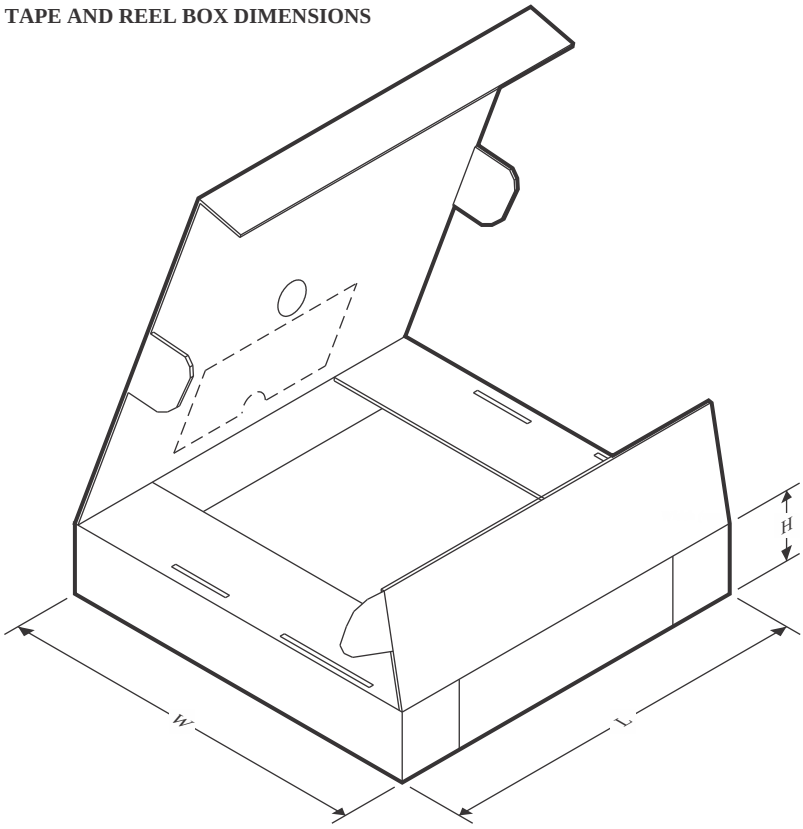
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA206AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA206AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
INA206AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA206AIPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA207AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA207AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA208AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
INA208AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

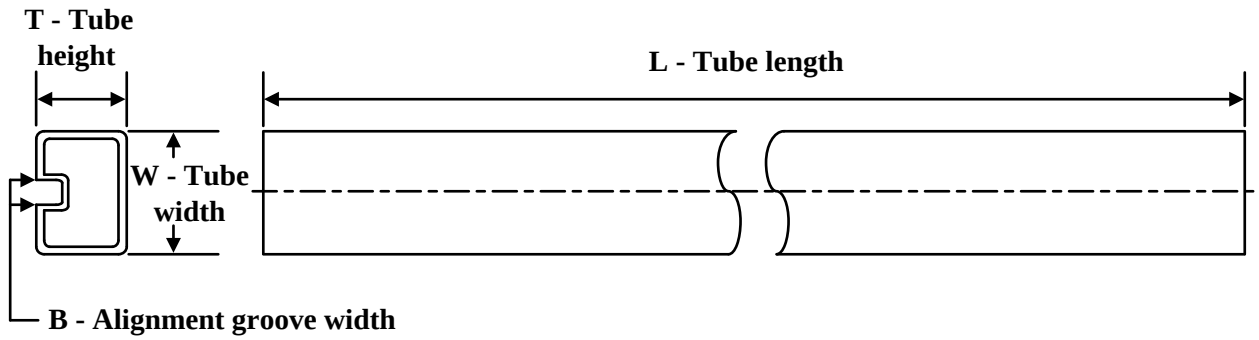
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA206AIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA206AIDR	SOIC	D	14	2500	353.0	353.0	32.0
INA206AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
INA206AIPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
INA207AIDGSR	VSSOP	DGS	10	2500	353.0	353.0	32.0
INA207AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
INA208AIDR	SOIC	D	14	2500	353.0	353.0	32.0
INA208AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

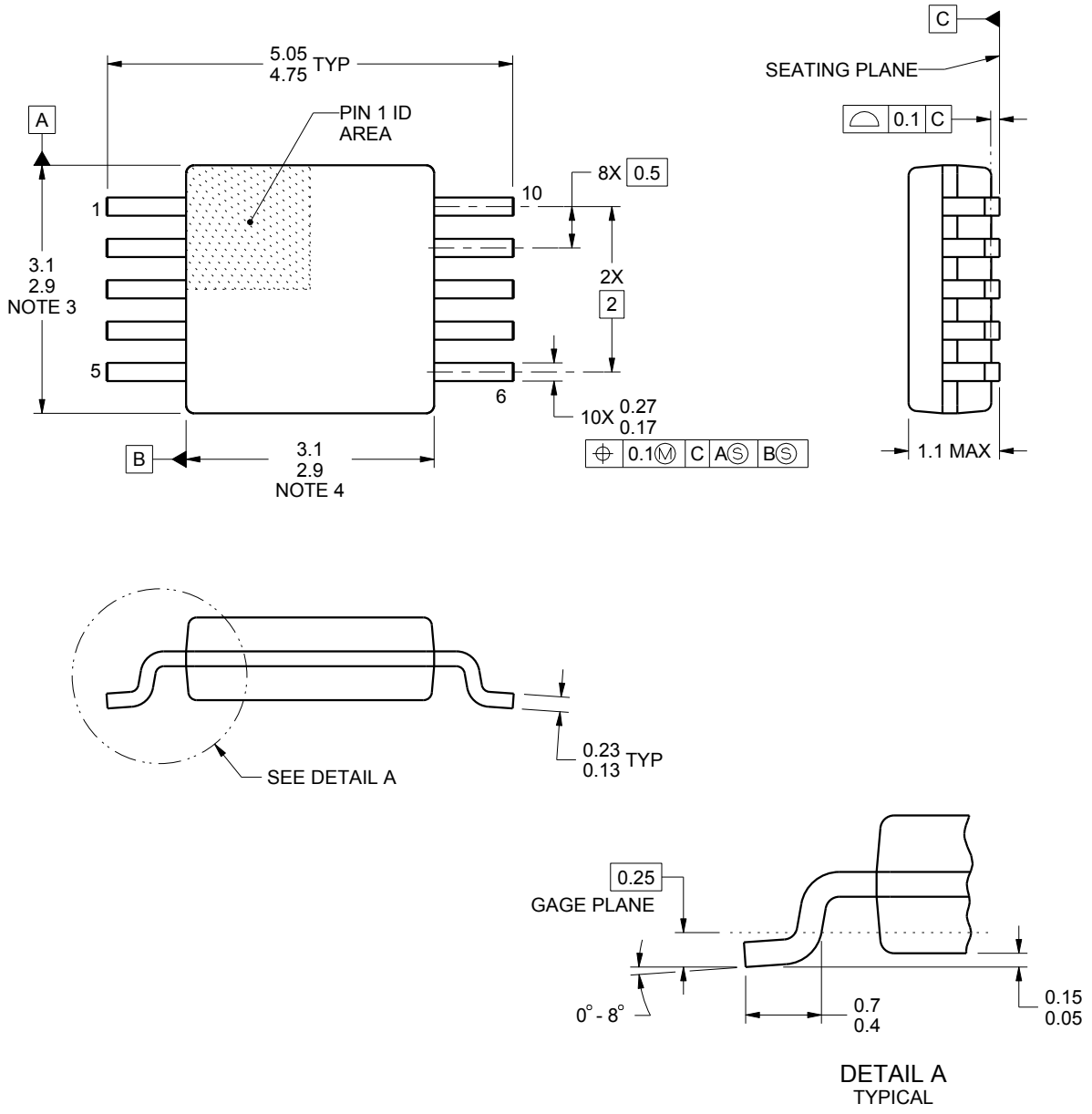
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA207AID	D	SOIC	14	50	506.6	8	3940	4.32
INA207AID.A	D	SOIC	14	50	506.6	8	3940	4.32
INA207AIDGSR	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA207AIDGSR.A	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA208AIDGSR	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA208AIDGSR.A	DGS	VSSOP	10	2500	274	6.55	500	2.88

PACKAGE OUTLINE

DGS0010A

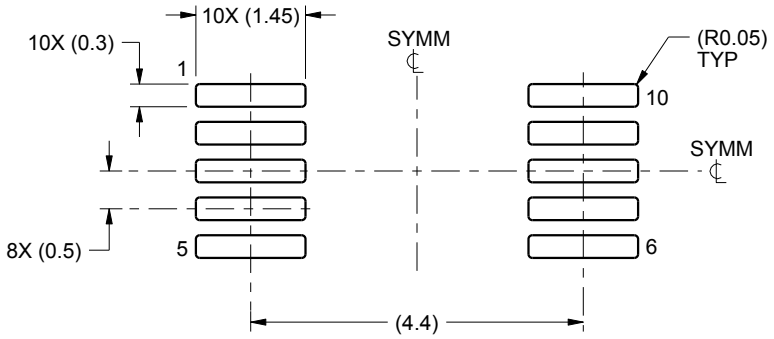
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

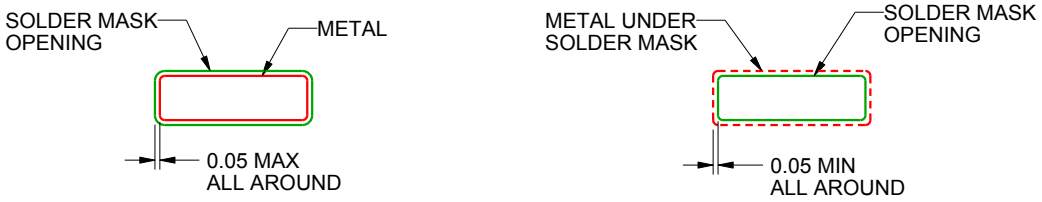


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

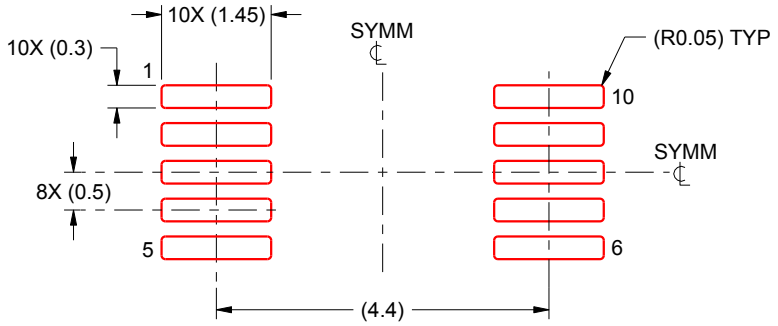


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

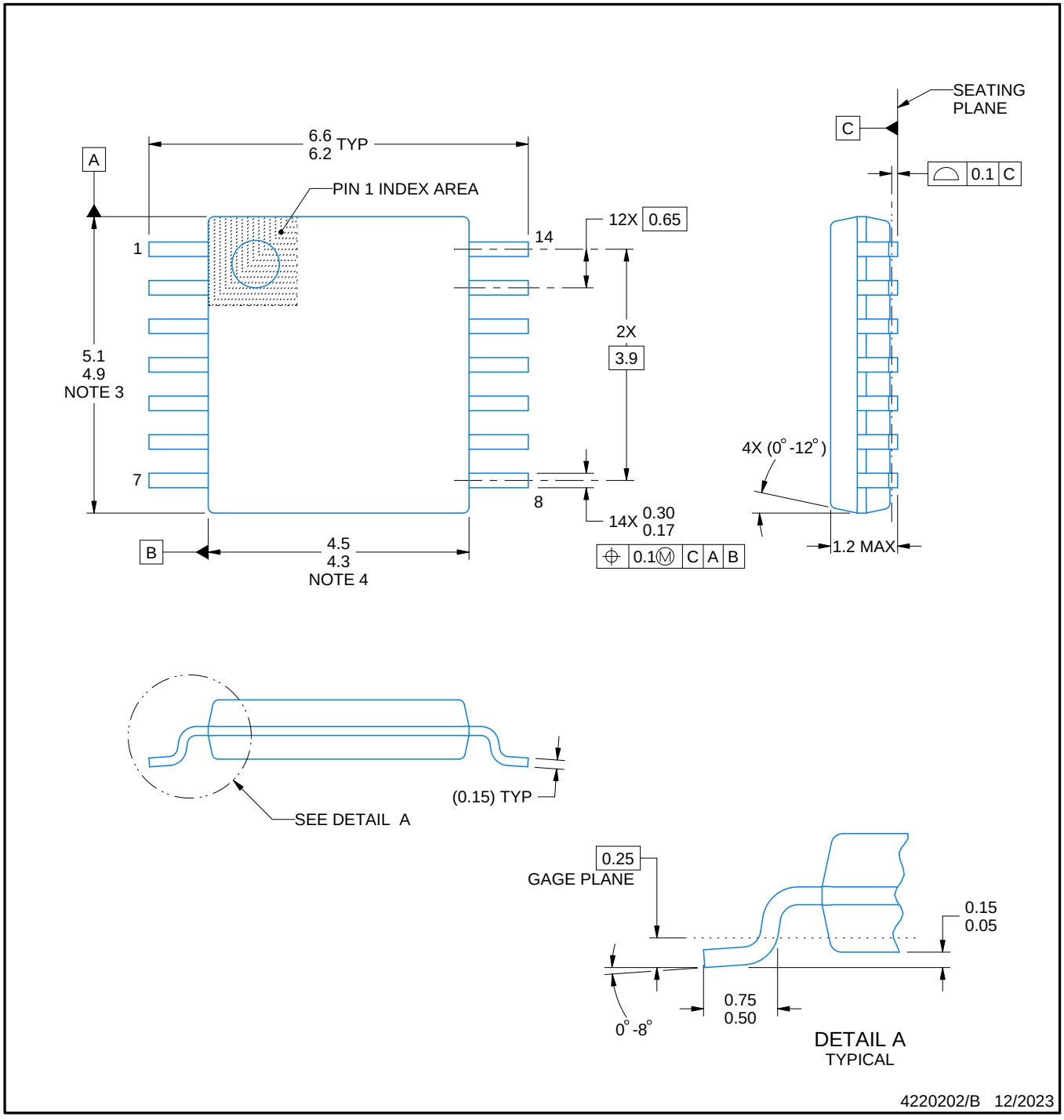
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

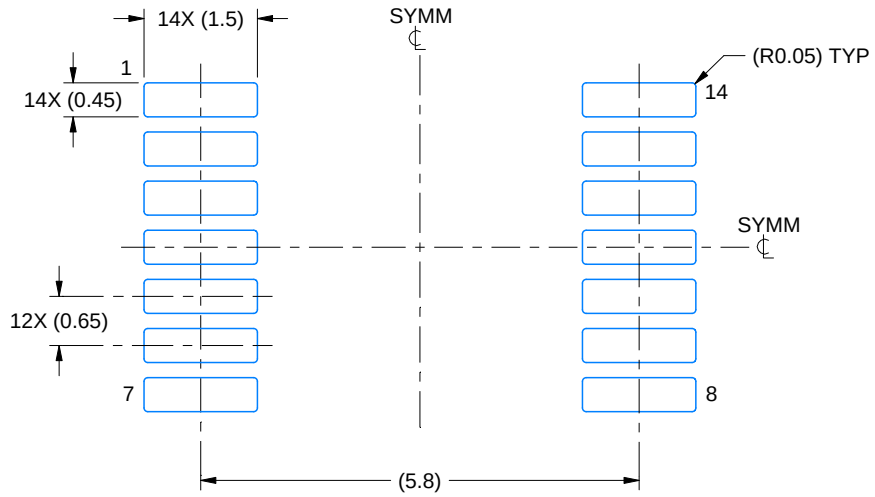
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

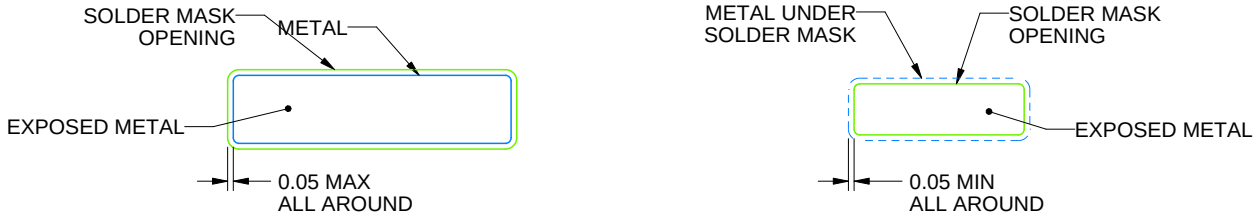


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

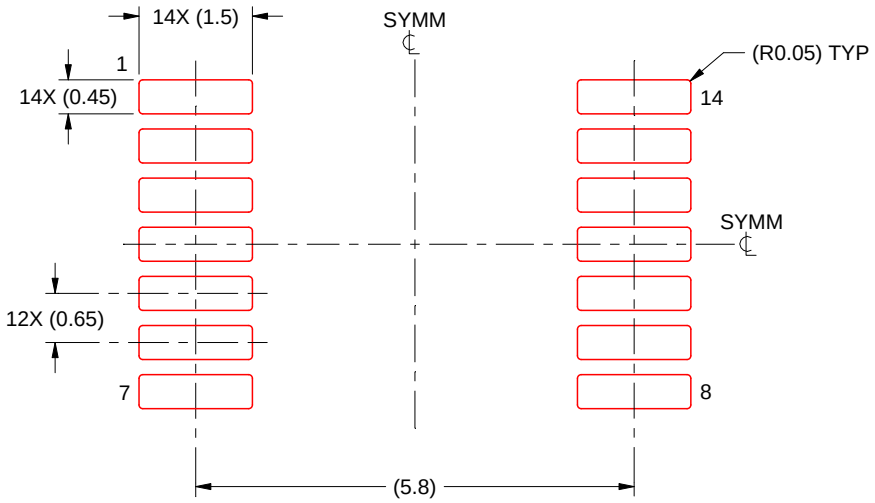


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

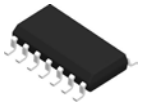


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

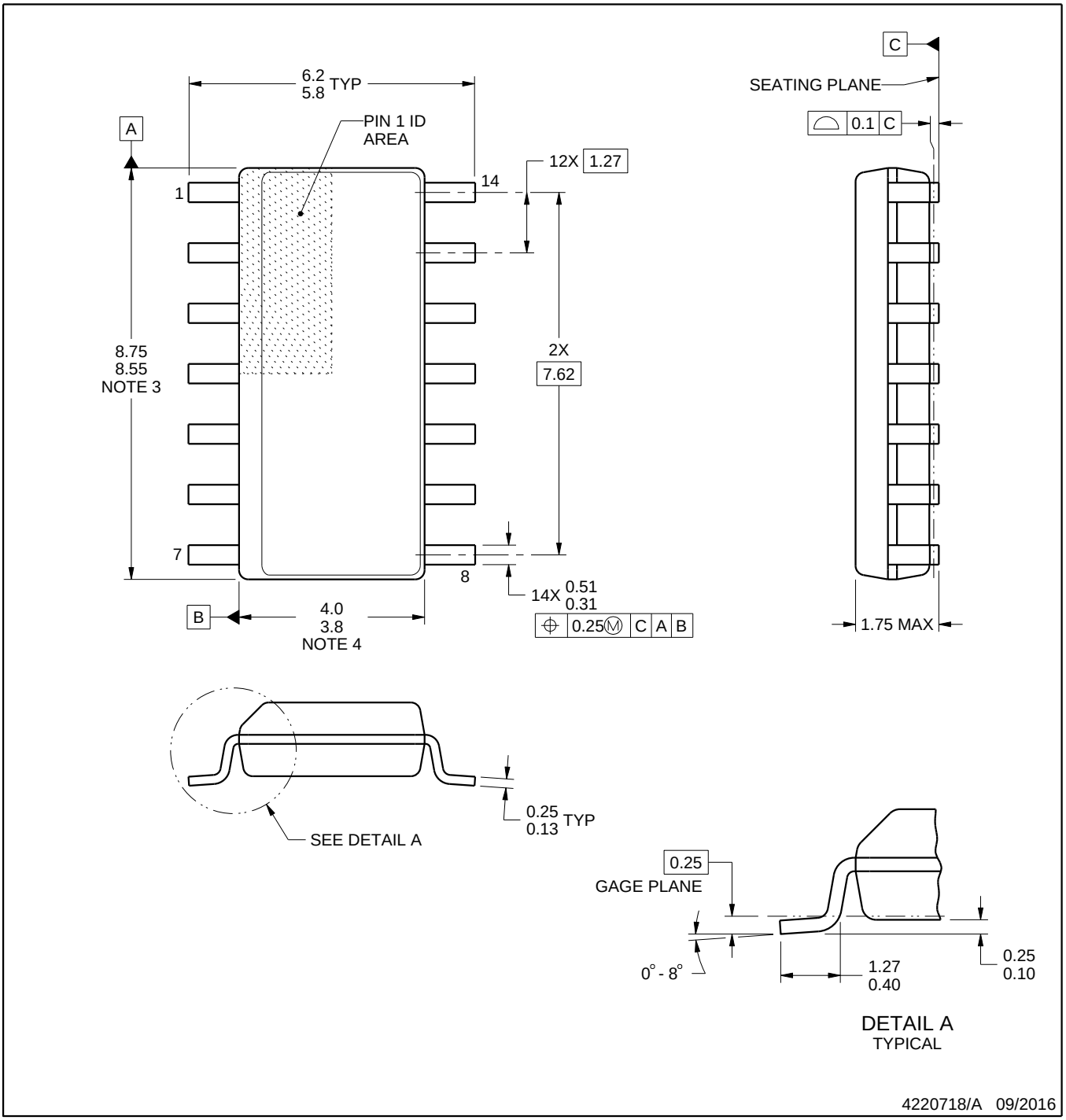


PACKAGE OUTLINE

D0014A

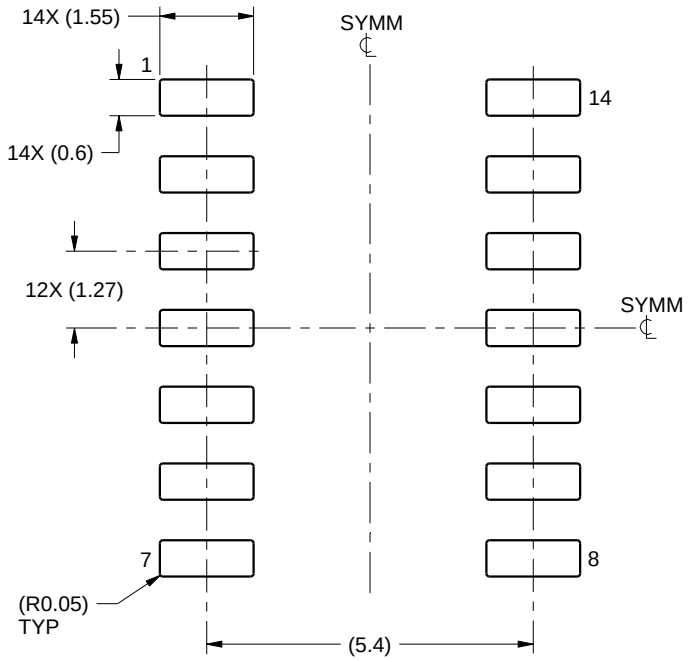
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

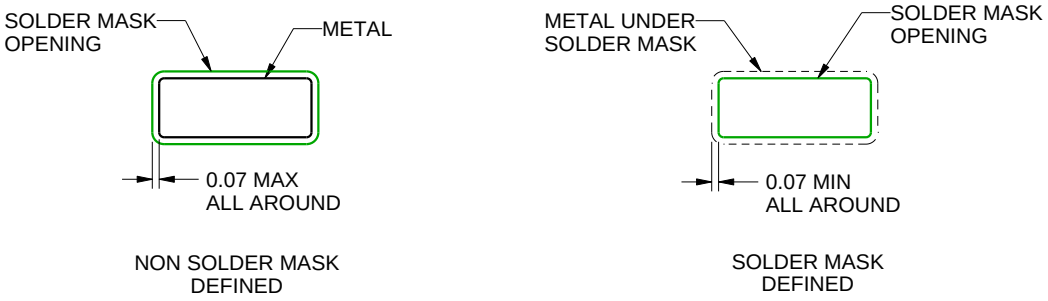


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

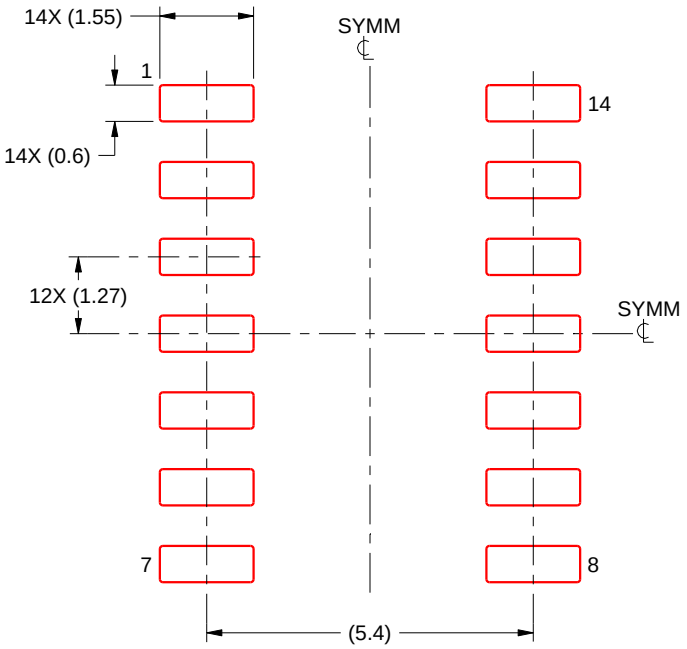
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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