INA1H182-SEP Low Offset, $7nV/\sqrt{Hz}$ Noise, Low-Power, Radiation-Tolerant, Precision Instrumentation Amplifier in Space-Enhanced Plastic

1 Features

- Radiation tolerant
  - Total ionizing dose (TID) RLAT for every wafer up to 30krad(Si)
  - ELDRS-free up to TID = 30krad(Si)
  - Single event latch-up (SEL) immune to 43MeV×cm^2 /mg
  - Single event effect (SEE) characterized to 43MeV×cm^2 /mg
- Space enhanced plastic
  - Supports defense and aerospace applications
  - Controlled baseline
  - One assembly and test site
  - One Fabrication site
  - Extended product life cycle
  - Product traceability
  - Outgassing test performed per ASTM E595
  - Au bondwire and NiPdAu lead finish
- Low offset voltage: 10μV (typical)
- Input stage voltage noise: $7nV/\sqrt{Hz}$
- Bandwidth: 2MHz at G = 1, 190kHz at G = 100
- Inputs protected up to ±40V
- Common-mode rejection: 110dB, G = 10 (min)
- Power supply rejection: 110dB, G = 1 (min)
- Supply current: 650μA (max)
- Supply range:
  - Single-supply: 4.5V to 18V
  - Dual-supply: ±2.25V to ±9V
- Packages: 8-pin VSSOP

2 Applications

- Space Sensor and control (telemetry)
- Satellite command & data handling
- Flight Control
- Satellite Payloads

3 Description

The INA1H182-SEP is a radiation-tolerant, high-precision instrumentation amplifier that offers low power consumption and operates over a wide single-supply or dual-supply range. A single external resistor sets any gain from 1 to 10,000. The device has high precision as a result of super-beta input transistors, which provide low input offset voltage, offset voltage drift, input bias current, and input voltage and current noise. Additional circuitry protects the inputs against overvoltage up to ±40V.

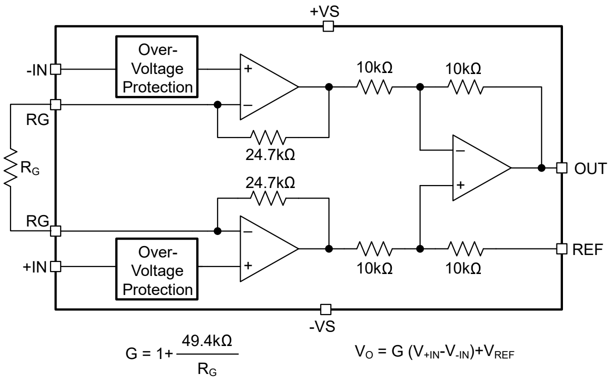
The INA1H182-SEP is optimized to provide a high common-mode rejection ratio. At gain (G) = 1, the common-mode rejection ratio exceeds 90dB across the full input common-mode range. The device is designed for low-voltage operation from a 4.5V single supply, and dual supplies up to ±9V.

The INA1H182-SEP is available in an 8-pin VSSOP package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA1H182-SEP	DGK (VSSOP, 8)	3mm × 3mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



INA1H182-SEP Simplified Internal Schematic

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4 Pin Configuration and Functions

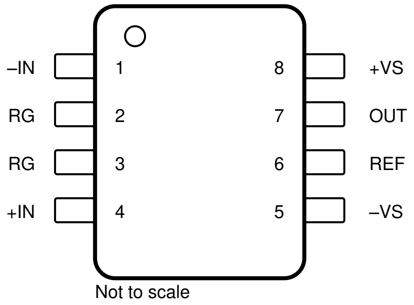


Figure 4-1. DGK Package, 8-Pin VSSOP (Top View)

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN	1	Input	Negative (inverting) input
+IN	4	Input	Positive (noninverting) input
OUT	7	Output	Output
RG	2, 3	Input	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
REF	6	Input	Reference input. This pin must be driven by a low impedance source.
–VS	5	—	Negative supply
+VS	8	—	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	V_S = (+VS) – (–VS)		20	V
Signal input pins	Voltage	–40	+40	V
	REF pin	–VS	+VS	
Output short-circuit[2]		Continuous		
Ambient Temperature, T_A		–55	150	°C
Junction Temperature, T_J			175	°C
Storage Temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22C101[2]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_S = (+VS) – (–VS)	Single-supply	4.5	18	V
	Dual-supply	±2.25	±9	
Ambient temperature, T_A	Specified temperature	–55	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		INA1H182-SEP	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	82.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at T_A = 25°C, V_S = ±9 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{OSI}	Input stage offset voltage(1) (2)			10	55	μV
		T_A = –55°C to +125°C			100	
	Input stage offset drift	T_A = –55°C to +125°C		0.1		μV/°C
V_{OSO}	Output stage offset voltage(1) (2)			50	500	μV
		Post NDD exposure(6)			800	
		T_A = –55°C to +125°C			900	
	Output stage offset drift	T_A = –55°C to +125°C		1		μV/°C
PSRR	Power-supply rejection ratio	G = 1, RTI	110	120		dB
		G = 10, RTI	114	130		
		G = 100, RTI		135		
		G = 1000, RTI		140		
z_{id}	Differential impedance			100 || 1		GΩ || pF
z_{ic}	Common-mode impedance			100 || 7		GΩ || pF
	RFI filter, –3-dB frequency			45		MHz
V_{CM}	Operating input range(3)		(–VS) + 2		(+VS) – 2	V
		V_S = ±2.25 V to ±9 V, T_A = –55°C to +125°C	See *Typical Characteristics*			
	Input overvoltage range	T_A = –55°C to +125°C	–40		40	V
CMRR	Common-mode rejection ratio	At DC to 60 Hz, RTI V_{CM} = (–VS) + 2 V to (+VS) – 2 V G = 1	90	103		dB
		At DC to 60 Hz, RTI V_{CM} = (–VS) + 2 V to (+VS) – 2 V G = 1, T_A = –55°C to +125°C	88			
		At DC to 60 Hz, RTI V_{CM} = (–VS) + 2 V to (+VS) – 2 V G = 10	110	122		
		At DC to 60 Hz, RTI V_{CM} = (–VS) + 2 V to (+VS) – 2 V G = 10, T_A = –55°C to +125°C	108			
		At DC to 60 Hz, RTI V_{CM} = (–VS) + 2 V to (+VS) – 2 V G = 100		145		
		At DC to 60 Hz, RTI V_{CM} = (–VS) + 2 V to (+VS) – 2 V G = 1000		150		
BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		0.15	0.5	nA
		T_A = –55°C to +125°C, V_{CM} = V_S / 2			1	
		Post NDD exposure(6), V_{CM} = V_S / 2			5	
I_{OS}	Input offset current	V_{CM} = V_S / 2		0.15	0.5	nA
		T_A = –55°C to +125°C, V_{CM} = V_S / 2			1	
		Post NDD exposure(6), V_{CM} = V_S / 2			5	
NOISE VOLTAGE						
e_{NI}	Input stage voltage noise(5)	f = 1 kHz, G = 100, R_S = 0 Ω		7.2		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω		0.14		μV_{PP}
e_{NO}	Output stage voltage noise(5)	f = 1 kHz, R_S = 0 Ω		70.5		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, R_S = 0 Ω		2.5		μV_{PP}
I_n	Noise current	f = 1 kHz		130		fA/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100		4.7		pA_{PP}

at T_A = 25°C, V_S = ±9 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAIN						
G	Gain equation			1 + (49.4 kΩ / R_G)		V/V
	Range of gain		1		10000	V/V
GE	Gain error	G = 1, V_O = ±5 V		±0.007	±0.035	%
		G = 10, V_O = ±5 V		±0.032	±0.22	
		G = 100, V_O = ±5 V		±0.032		
		G = 1000, V_O = ±5 V		±0.05		
	Gain vs temperature(4)	G = 1, T_A = –55°C to +125°C		±1		ppm/°C
		G > 1, T_A = –55°C to +125°C		±5.5		
	Gain nonlinearity	G = 1 to 10, V_O = –5 V to +5 V, R_L = 10 kΩ		±1		ppm
		G = 10, V_O = –5 V to +5 V, R_L = 10 kΩ		±2		
		G = 1000, V_O = –5 V to +5 V, R_L = 10 kΩ		±10		
		G = 1 to 100, V_O = –5 V to +5 V, R_L = 2 kΩ		±30		
OUTPUT						
	Voltage swing		(–VS) + 0.15		(+VS) – 0.15	V
	Load capacitance stability			1000		pF
Z_O	Closed-loop output impedance	f = 10 kHz		1.3		Ω
I_{SC}	Short-circuit current	Continuous to V_S / 2		±20		mA
FREQUENCY RESPONSE						
BW	Bandwidth, –3 dB	G = 1		2		MHz
		G = 10		750		kHz
		G = 100		190		
		G = 1000		30		
SR	Slew rate	G = 1, V_O = ±5 V		2.0		V/µs
t_S	Settling time	0.01%, G = 1 to 100, V_{STEP} = 5 V		6		µs
		0.01%, G = 1000, V_{STEP} = 5 V		40		
		0.001%, G = 1 to 100, V_{STEP} = 5 V		10		
		0.001%, G = 1000, V_{STEP} = 5 V		50		
REFERENCE INPUT						
R_{IN}	Input impedance			10		kΩ
	Voltage range		(–VS)		(+VS)	V
	Gain to output			1		V/V
	Reference gain error			0.01%		
POWER SUPPLY						
I_Q	Quiescent current	V_{IN} = 0 V		600	650	µA
		vs temperature, T_A = –55°C to +125°C			870	

(1) Total offset, referred-to-input (RTI): $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$.
(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}{}^2 + (\Delta V_{OSO} / G)^2]}$.
(3) Input voltage range of the Instrumentation Amplifier input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves for more information.
(4) The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.
(5) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}{}^2 + (e_{NO} / G)^2]}$.
(6) For more information, see the INA1H182-SEP Neutron Displacement Damage (NDD) radiation report.

5.6 Typical Characteristics

at T_A = 25°C, V_S = ±9V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)

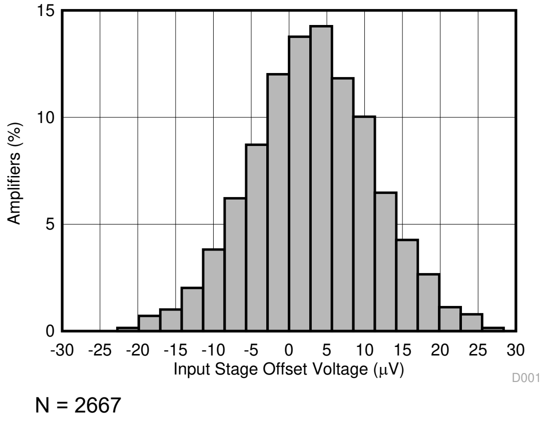


Figure 5-1. Typical Distribution of Input Stage Offset Voltage

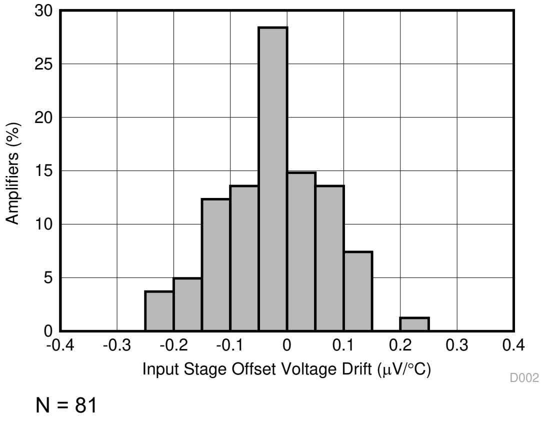


Figure 5-2. Typical Distribution of Input Stage Offset Voltage Drift

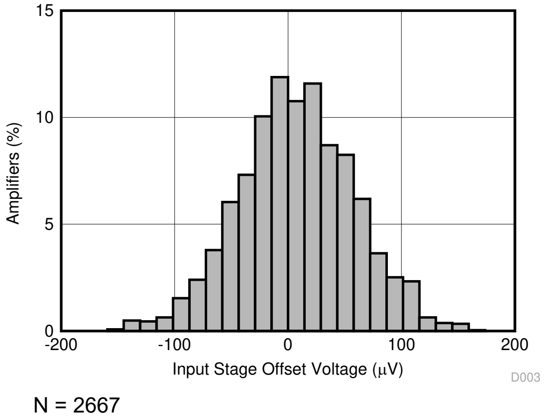


Figure 5-3. Typical Distribution of Output Stage Offset Voltage

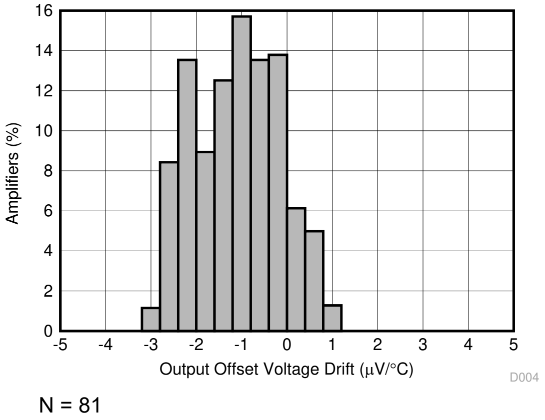


Figure 5-4. Typical Distribution of Output Stage Offset Voltage Drift

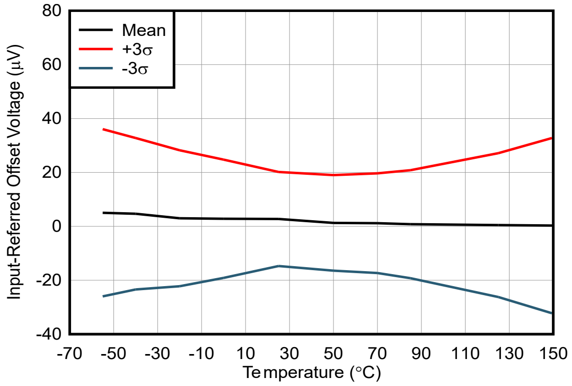


Figure 5-5. Input Stage Offset Voltage vs Temperature

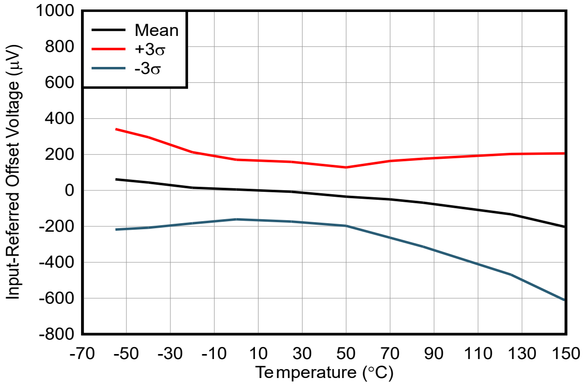
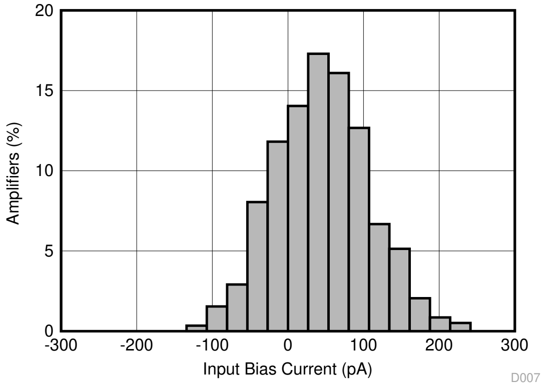


Figure 5-6. Output Stage Offset Voltage vs Temperature

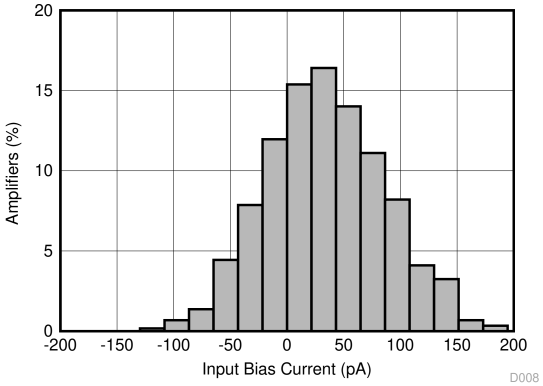
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)



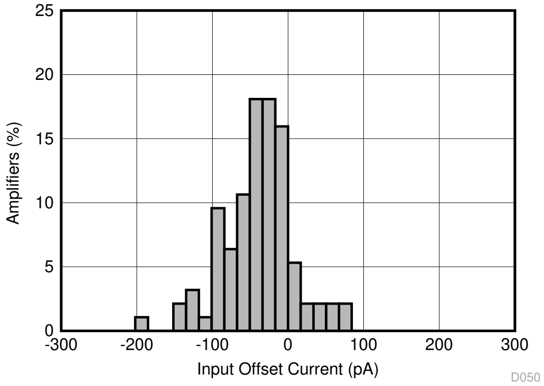
N = 292

Figure 5-7. Typical Distribution of Input Bias Current, T_A = 25°C



N = 292

Figure 5-8. Typical Distribution of Input Bias Current, T_A = 90°C



N = 94

Figure 5-9. Typical Distribution of Input Offset Current

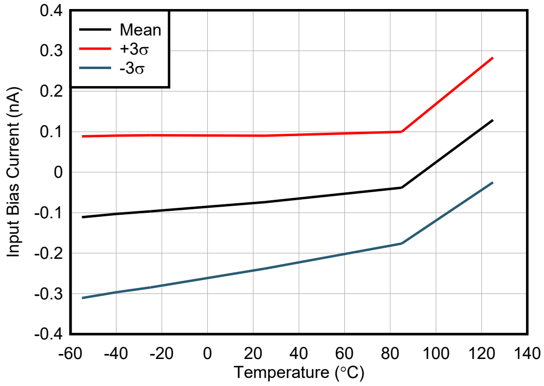


Figure 5-10. Input Bias Current Vs Temperature

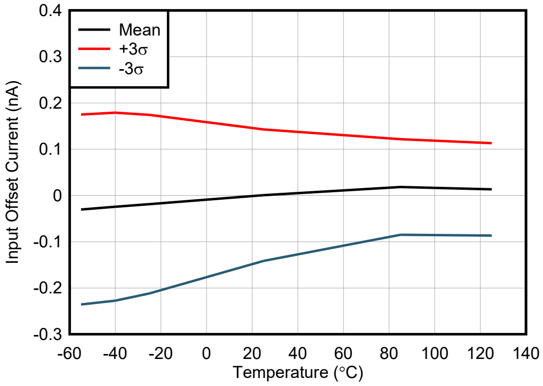
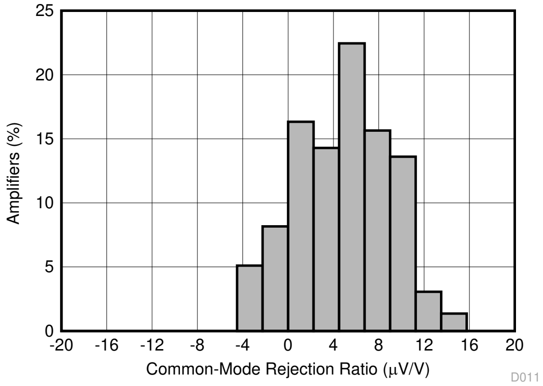


Figure 5-11. Input Offset Current vs Temperature

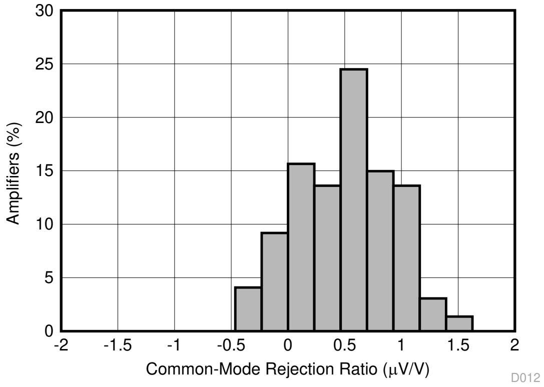


N = 294

Figure 5-12. Typical CMRR Distribution, G = 1

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)



N = 294

Figure 5-13. Typical CMRR Distribution, G = 10

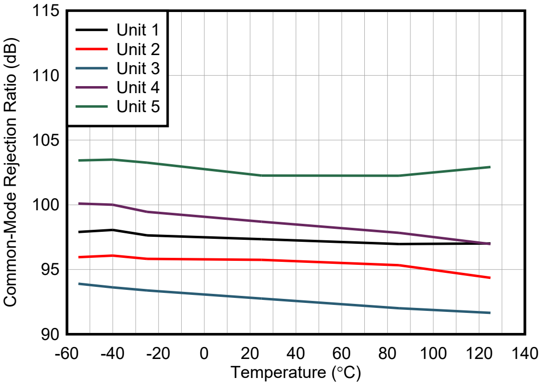


Figure 5-14. CMRR vs Temperature, G = 1

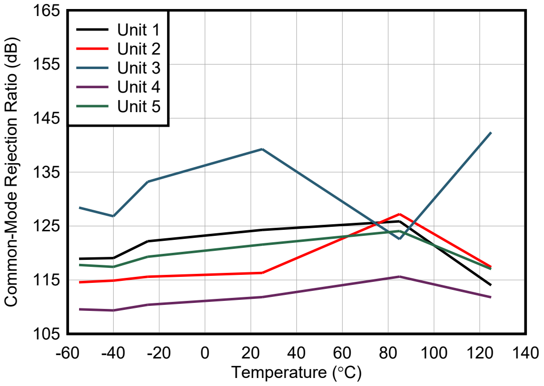


Figure 5-15. CMRR vs Temperature, G = 10

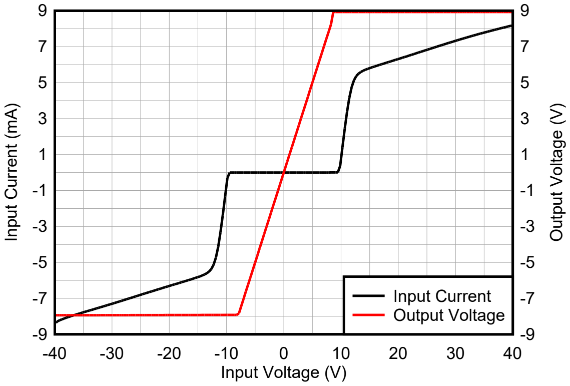


Figure 5-16. Input Current vs Input Overvoltage

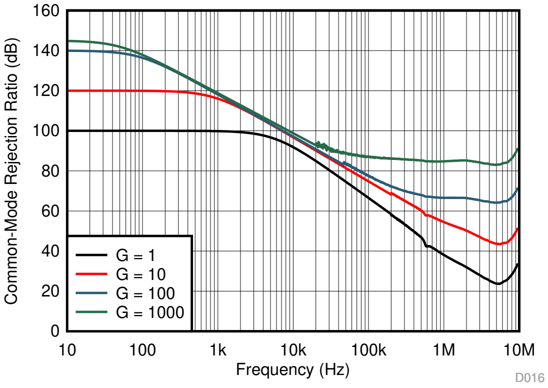


Figure 5-17. CMRR vs Frequency (RTI)

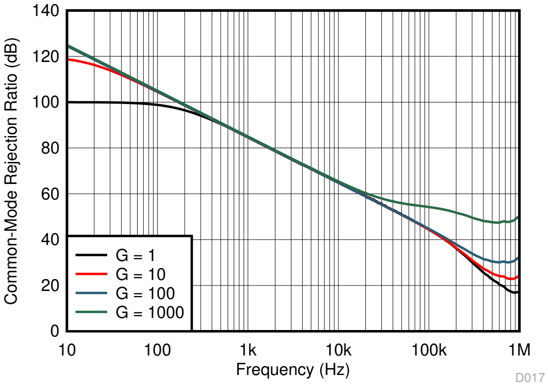


Figure 5-18. CMRR vs Frequency (RTI, 1kΩ source imbalance)

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)

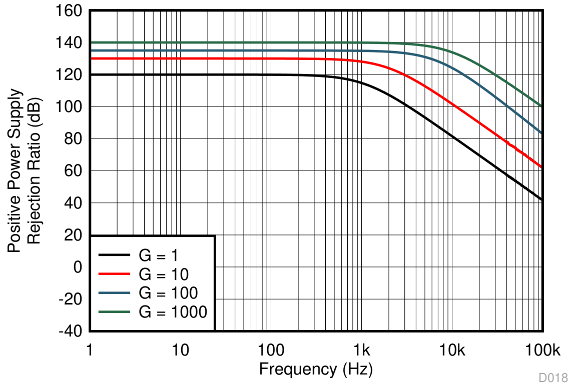


Figure 5-19. Positive PSRR vs Frequency (RTI)

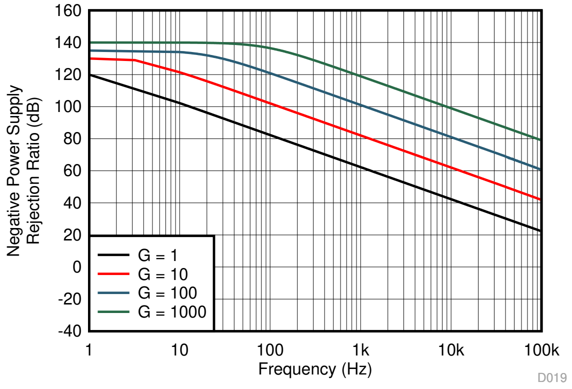


Figure 5-20. Negative PSRR vs Frequency (RTI)

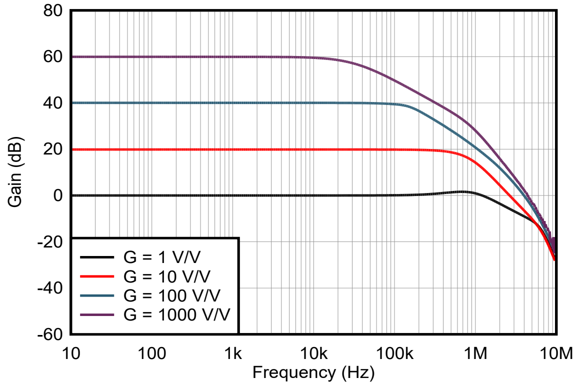


Figure 5-21. Gain vs Frequency

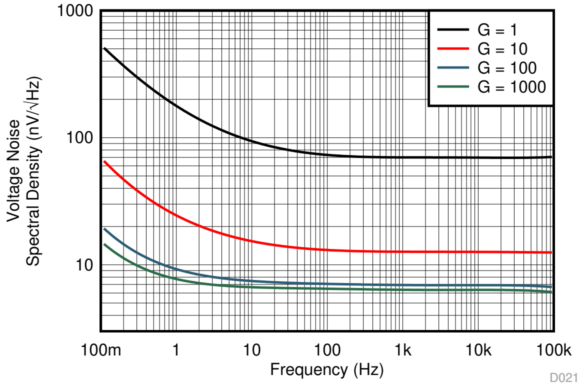


Figure 5-22. Voltage Noise Spectral Density vs Frequency (RTI)

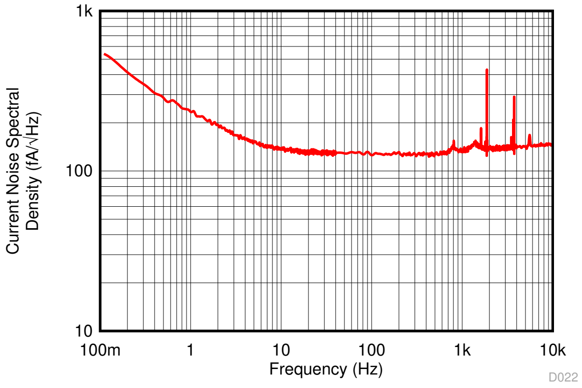
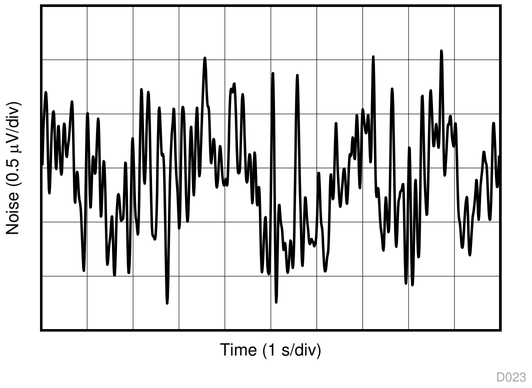


Figure 5-23. Current Noise Spectral Density vs Frequency (RTI)

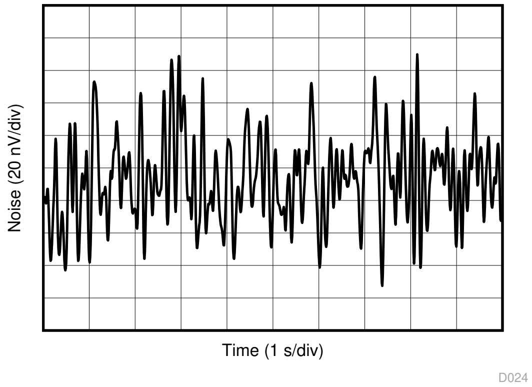


G = 1

Figure 5-24. 0.1Hz to 10Hz RTI Voltage Noise, G = 1

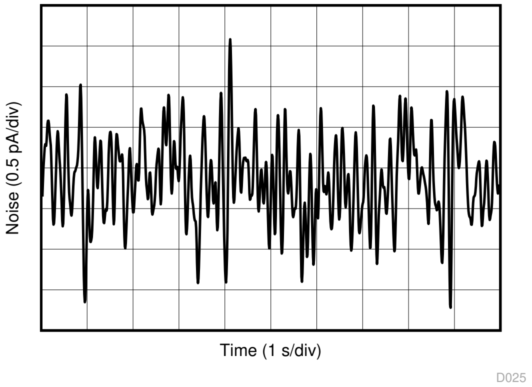
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)



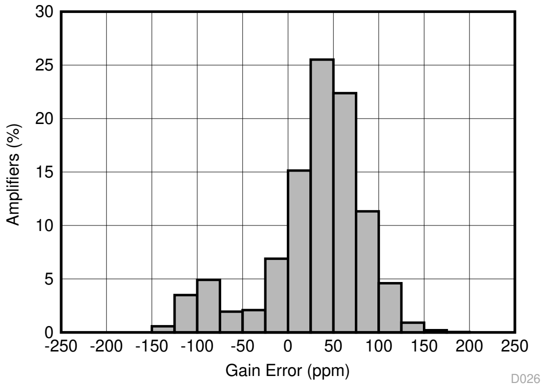
G = 1000

Figure 5-25. 0.1Hz to 10Hz RTI Voltage Noise, G = 1000



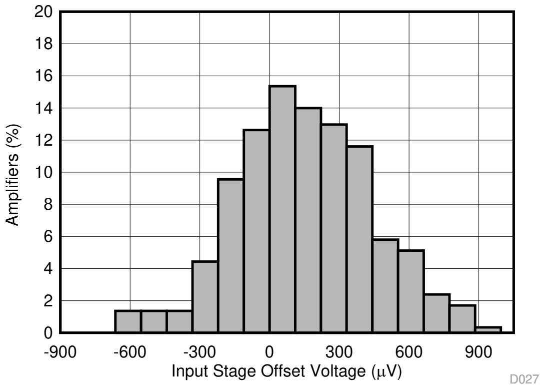
G = 1

Figure 5-26. 0.1Hz to 10Hz RTI Current Noise



N = 5412

Figure 5-27. Typical Distribution of Gain Error, G = 1



N = 293

Figure 5-28. Typical Distribution of Gain Error, G = 10

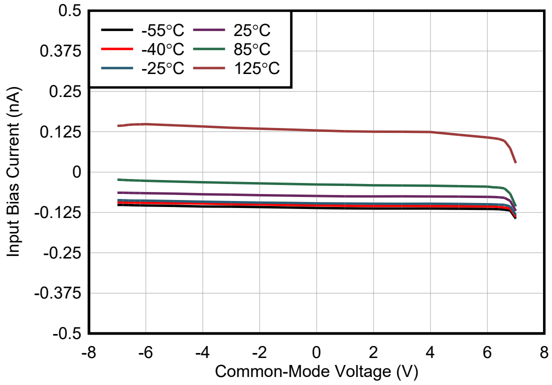
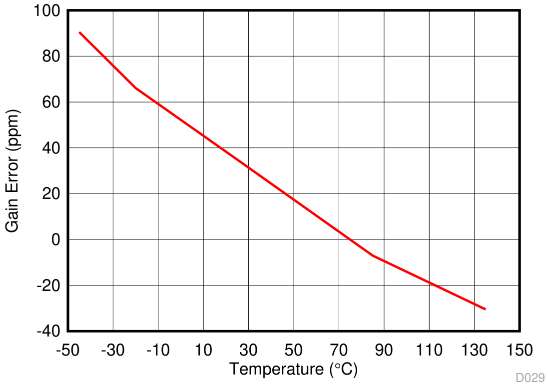


Figure 5-29. Input Bias Current vs Common-Mode Voltage

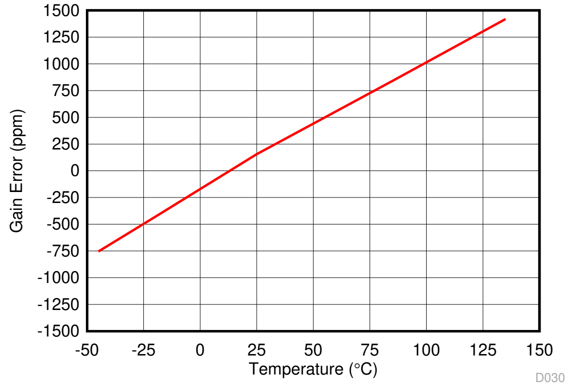


Average of 294 units

Figure 5-30. Gain Error vs Temperature, G = 1

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)



Average of 294 units G = 10

Figure 5-31. Gain Error vs Temperature, G = 10

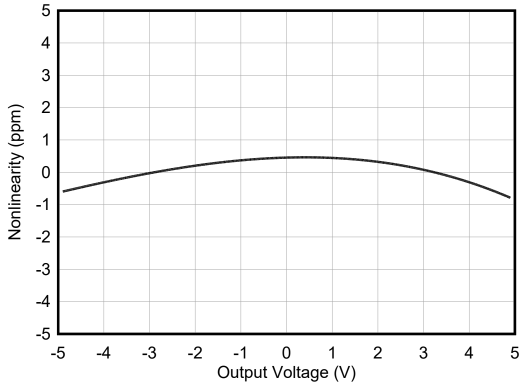


Figure 5-32. Gain nonlinearity, G = 1

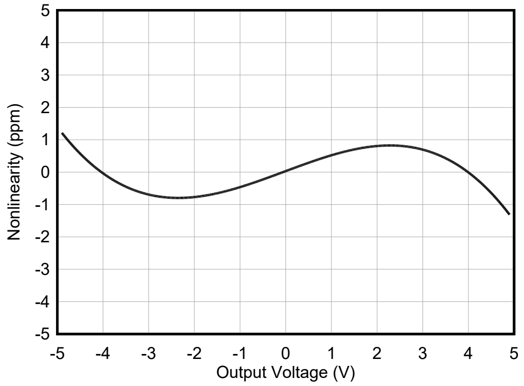


Figure 5-33. Gain Nonlinearity, G = 10

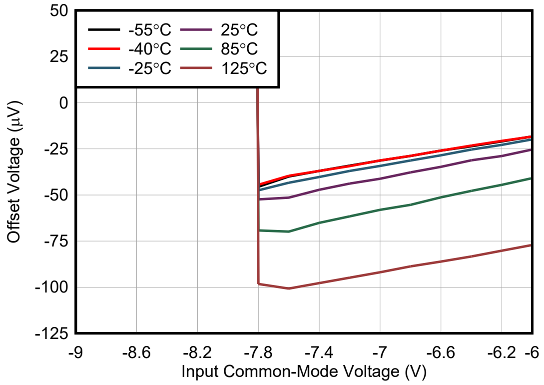


Figure 5-34. Offset Voltage vs Negative Common-Mode Voltage

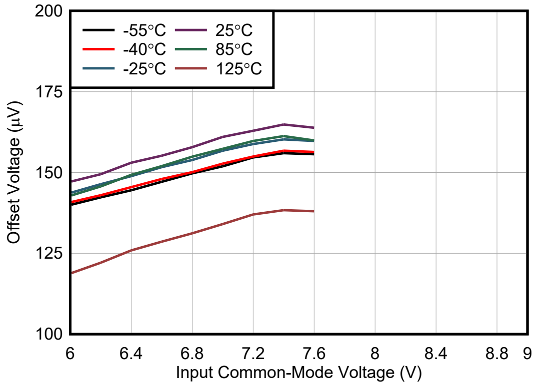


Figure 5-35. Offset Voltage vs Positive Common-Mode Voltage

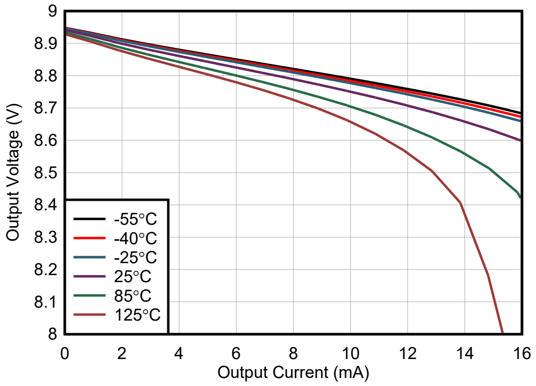


Figure 5-36. Positive Output Voltage Swing vs Output Current

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)

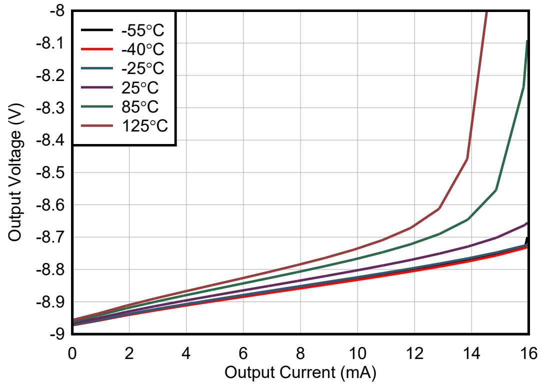


Figure 5-37. Negative Output Voltage Swing vs Output Current

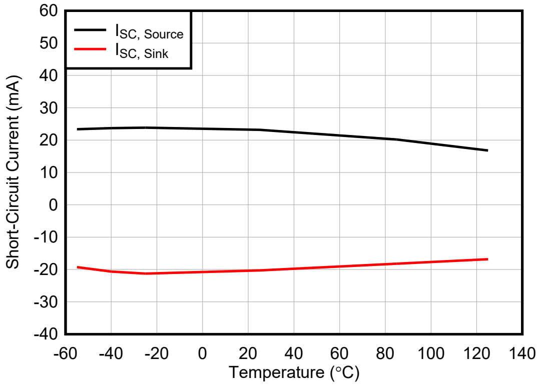
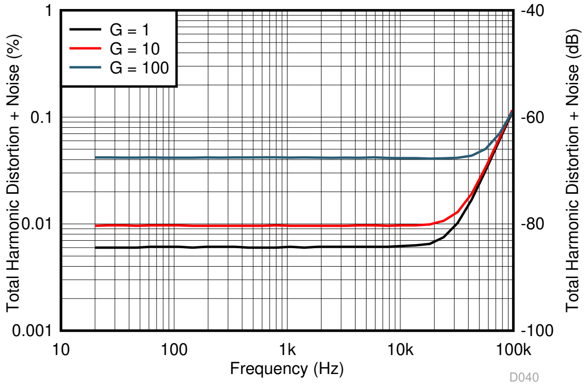


Figure 5-38. Short-Circuit Current vs Temperature



500kHz measurement bandwidth

$1V_{RMS}$ output voltage 100kΩ load

Figure 5-39. THD+N vs Frequency

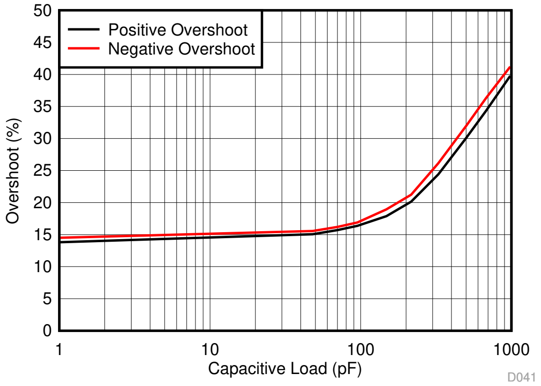
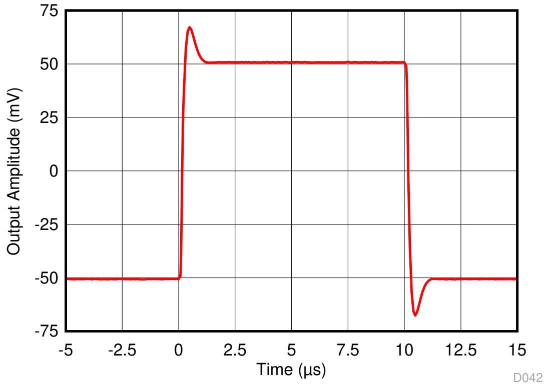
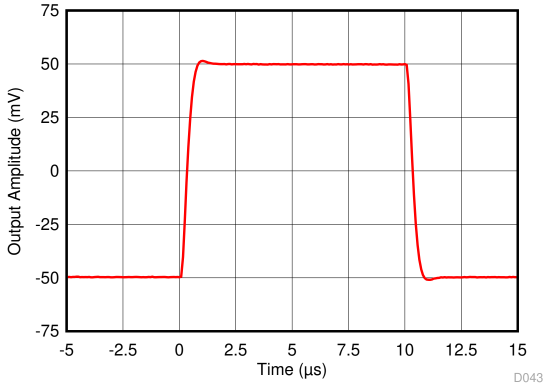


Figure 5-40. Overshoot vs Capacitive Loads



G = 1 R_L = 10kΩ C_L = 100pF

Figure 5-41. Small-Signal Response

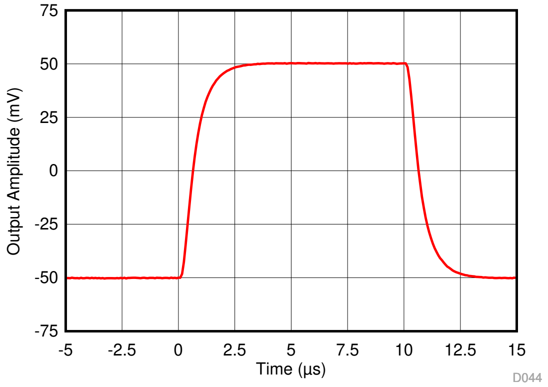


G = 10 R_L = 10kΩ C_L = 100pF

Figure 5-42. Small-Signal Response

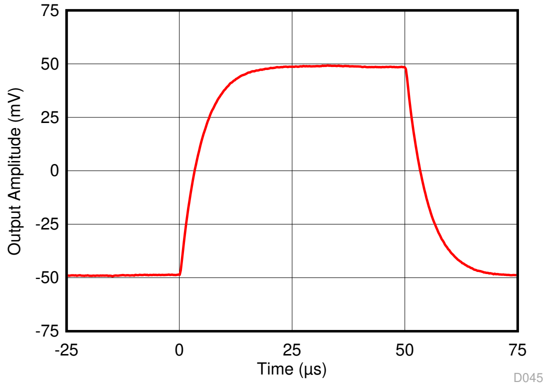
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)



G = 100 R_L = 10kΩ C_L = 100pF

Figure 5-43. Small-Signal Response



G = 1000 R_L = 10kΩ C_L = 100pF

Figure 5-44. Small-Signal Response

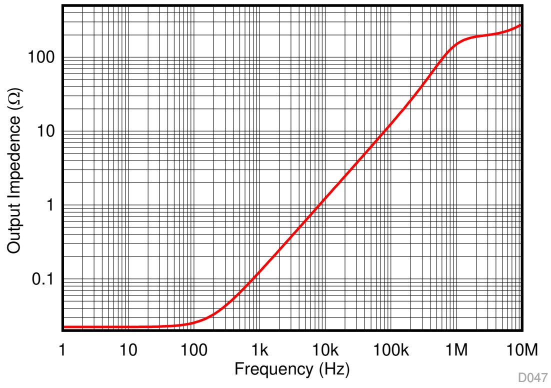


Figure 5-45. Closed-Loop Output Impedance

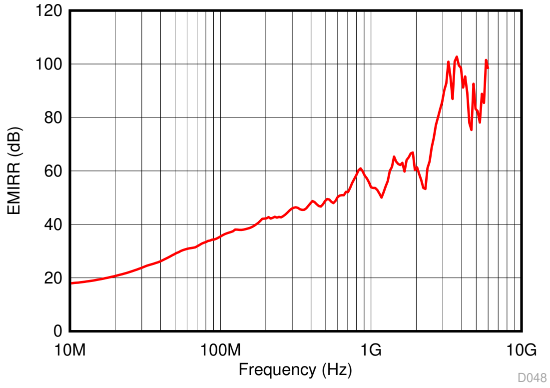


Figure 5-46. Differential-Mode EMI Rejection Ratio

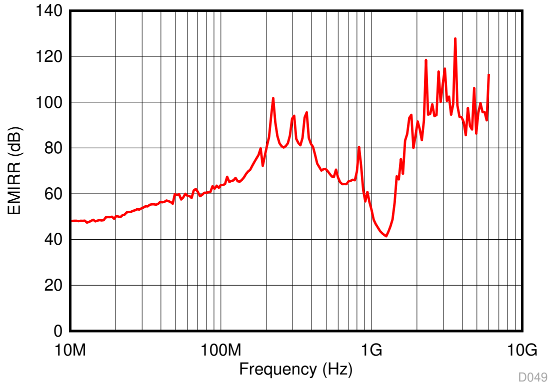
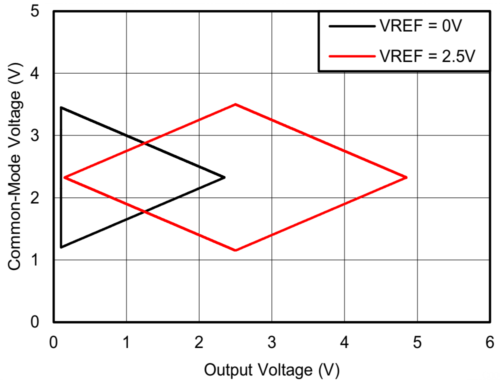


Figure 5-47. Common-Mode EMI Rejection Ratio

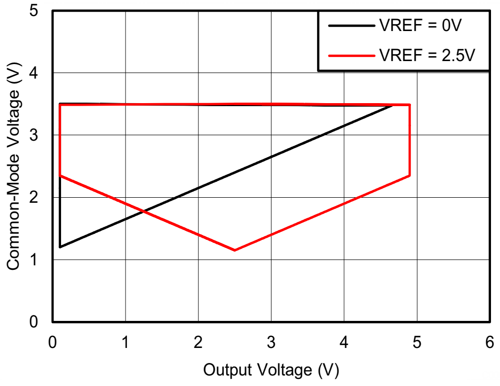


V_S = 5V G = 1

Figure 5-48. Input Common-Mode Voltage vs Output Voltage

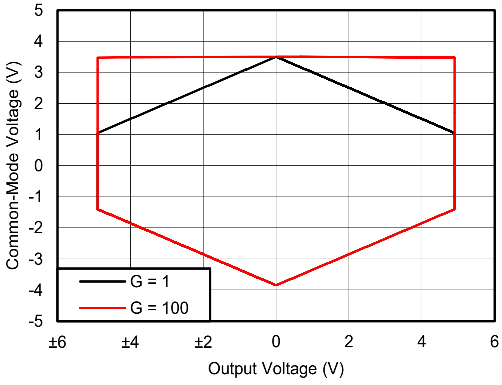
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)



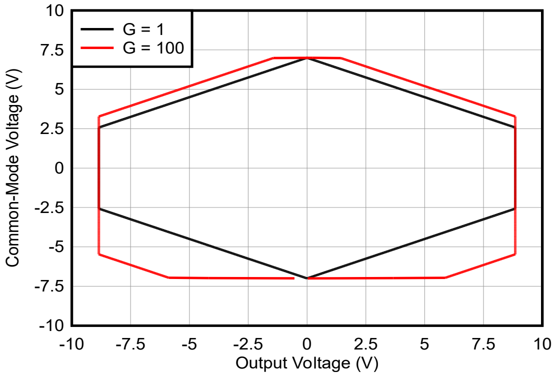
V_S = 5V G = 100

Figure 5-49. Input Common-Mode Voltage vs Output Voltage



V_S = ±5V V_{REF} = 0V

Figure 5-50. Input Common-Mode Voltage vs Output Voltage



V_S = ±9V, V_{REF} = 0V

Figure 5-51. Input Common-Mode Voltage vs Output Voltage

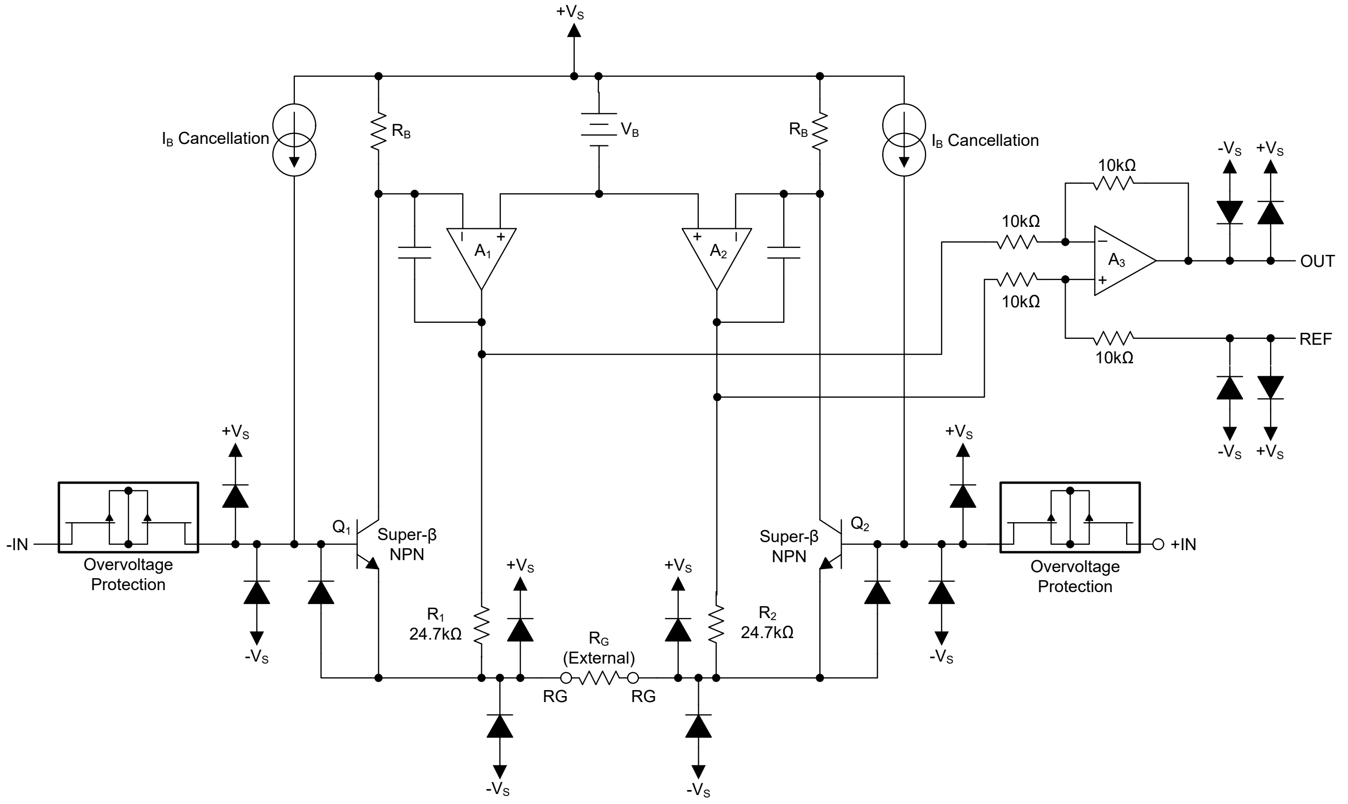
6 Detailed Description

6.1 Overview

The INA1H182-SEP is a monolithic precision instrumentation amplifier that incorporates a current-feedback input stage and a four-resistor difference amplifier output stage. The functional block diagram in the next section shows how the differential input voltage is buffered by Q_1 and Q_2 and is forced across R_G, which causes a signal current to flow through R_G, R_1, and R_2. The output difference amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the REF pin. The V_{BE} and voltage drop across R_1 and R_2 produces output voltages on A_1 and A_2 that are approximately 0.8V lower than the input voltages.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8mA.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Setting the Gain

Figure 6-1 shows that the gain of the INA1H182-SEP is set by a single external resistor (R_G) connected between the RG pins (pins 1 and 8).

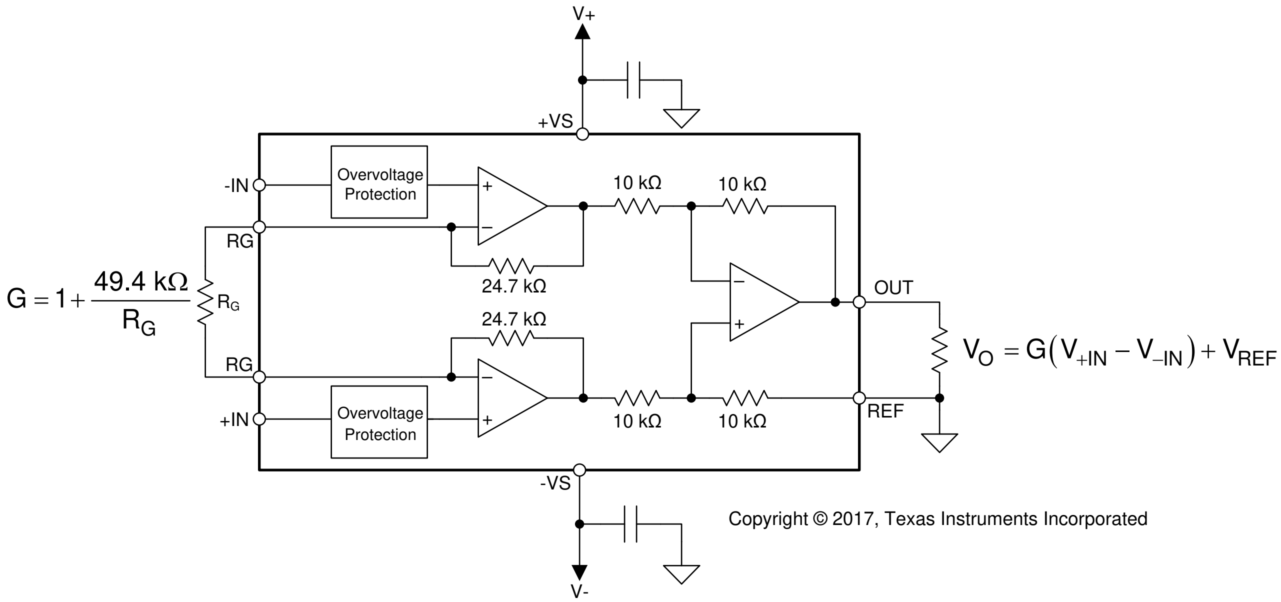


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Figure 6-1. Simplified Diagram of the INA1H182-SEP With Gain and Output Equations

The value of R_G is selected according to:

$$G = 1 + \frac{49.4k\Omega}{R_G} \quad (1)$$

Table 6-1 lists several commonly used gains and resistor values. The 49.4kΩ term in Equation 1 is a result of the sum of the two internal 24.7kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA1H182-SEP. As shown in Figure 6-1 and explained in more details in *Section 7.4*, make sure to connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, and place as close to the device as possible.

Table 6-1. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	49.4k	49.9k
5	12.35k	12.4k
10	5.489k	5.49k
20	2.600k	2.61k
50	1.008k	1k
100	499	499
200	248	249
500	99	100
1000	49.4	49.9

6.3.1.1 Gain Drift

The stability and temperature drift of the external gain setting resistor (R_G) also affects gain. The contribution of R_G to gain accuracy and drift is determined from Equation 1.

The best gain drift of 5ppm/°C (maximum) is achieved when the INA1H182-SEP uses G = 1 without R_G connected. In this case, gain drift is limited by the slight mismatch of the temperature coefficient of the integrated 10kΩ resistors in the differential amplifier (A_3). At gains greater than 1, gain drift increases as a result of the individual drift of the 24.7kΩ resistors in the feedback of A_1 and A_2 relative to the drift of the external gain resistor (R_G.) The low temperature coefficient of the internal feedback resistors significantly improves the overall temperature stability of applications using gains greater than 1V/V over alternate options.

Low resistor values required for high gain make wiring resistance an important consideration. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To maintain stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on the R_G pins maintains the best CMRR over frequency; see Figure 5-17.

6.3.2 EMI Rejection

Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA1H182-SEP to reject EMI. The offset resulting from an input EMI signal is calculated using Equation 2:

$$\Delta V_{OS} = \left(\frac{V_{RF\_PEAK}^{2}}{100mV_P}\right) \times 10^{-\left(\frac{EMIRR(dB)}{20}\right)} \tag{2}$$

where

- V_{RF_PEAK} is the peak amplitude of the input EMI signal.

Figure 6-2 and Figure 6-3 show the INA1H182-SEP EMIRR graph for differential and common-mode EMI rejection across this frequency range. Table 6-2 lists the EMIRR values for the INA1H182-SEP at frequencies commonly encountered in real-world applications. Applications listed in Table 6-2 are centered on or operated near the particular frequency shown. Depending on the end-system requirements, additional EMI filters can be required near the signal inputs of the system. Incorporate known good practices, such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing.

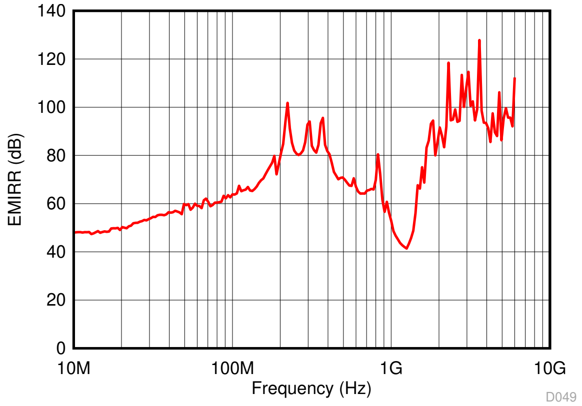


Figure 6-2. Common-Mode EMIRR Testing

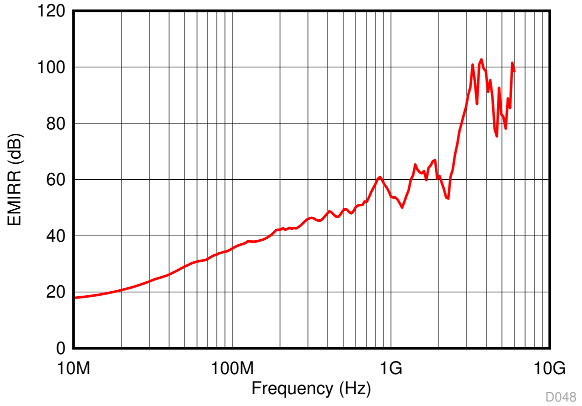


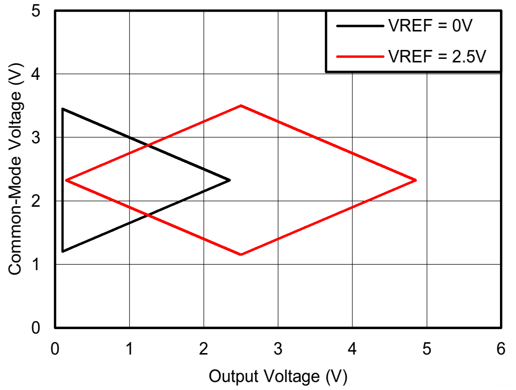
Figure 6-3. Differential-Mode EMIRR Testing

Table 6-2. INA1H182-SEP EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL EMIRR	COMMON-MODE EMIRR
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	60dB	88dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6GHz), GSM, aeronautical mobile, UHF applications	58dB	60dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	66dB	89dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	73dB	98dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	99dB	111dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	83dB	91dB

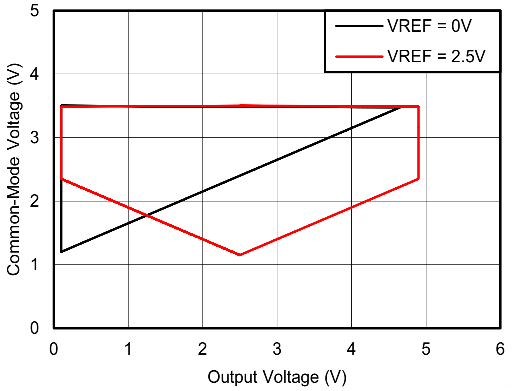
6.3.3 Input Common-Mode Range

The linear input voltage range of the INA1H182-SEP input circuitry extends within 2V of power supplies and maintains excellent common-mode rejection throughout this range. The common-mode ranges for some common operating conditions are shown in Figure 6-4 to Figure 6-7.



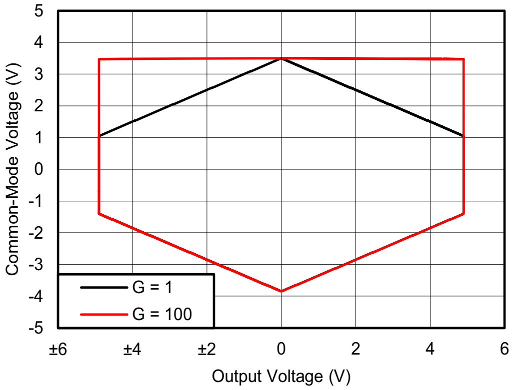
V_S = 5V, G = 1

Figure 6-4. Input Common-Mode Voltage vs Output Voltage



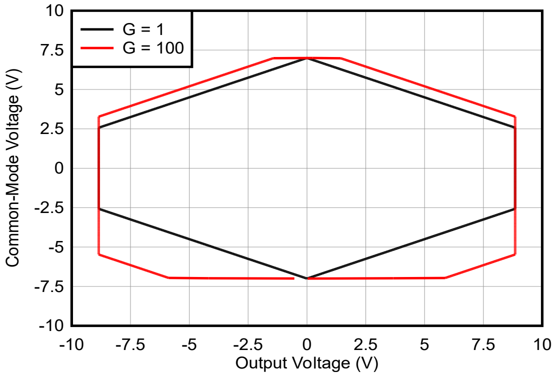
V_S = 5V, G = 100

Figure 6-5. Input Common-Mode Voltage vs Output Voltage



V_S = ±5V, V_{REF} = 0V

Figure 6-6. Input Common-Mode Voltage vs Output Voltage



V_S = ±9V, V_{REF} = 0V

Figure 6-7. Input Common-Mode Voltage vs Output Voltage

6.3.4 Input Protection

The inputs of the INA1H182-SEP device are individually protected for voltages up to ±20V beyond the supply rails. For example, a condition of –20V on one input and +20V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe level.

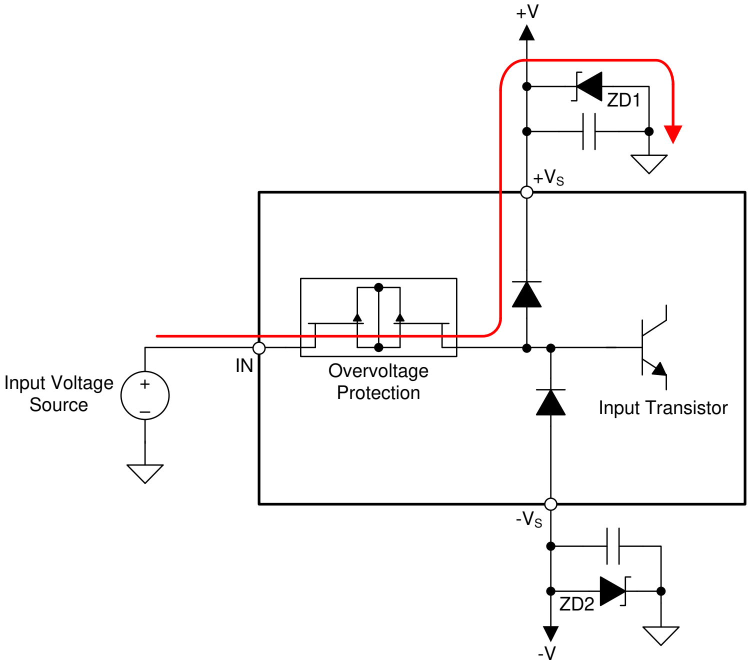


Figure 6-8. Input Current Path During an Overvoltage Condition

During an input overvoltage condition, current flows through the input protection diodes into the power supplies, as shown in Figure 6-8. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in Figure 6-8) must be placed on the power supplies to provide a current pathway to ground. Figure 6-9 shows the input current for input voltages from –40V to +40V when the INA1H182-SEP is powered by ±9V supplies.

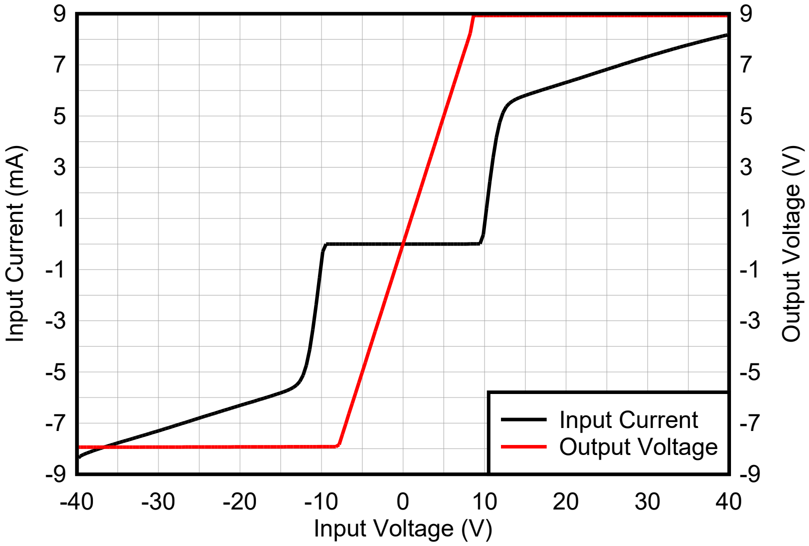


Figure 6-9. Input Current vs Input Overvoltage

6.4 Device Functional Modes

The INA1H182-SEP has a single functional mode and is operational when the power supply voltage is greater than 4.5V (±2.25V). The maximum power-supply voltage for the INA1H182-SEP is 18V (±9V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Reference Pin

The output voltage of the INA1H182-SEP is developed with respect to the voltage on the reference pin (REF). In dual-supply operation, REF (pin 6) often connects to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5V in a 5V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA1H182-SEP drives a single-supply analog-to-digital converter (ADC).

The voltage source applied to the reference pin must have a low output impedance. As shown in Figure 7-1, any resistance at the reference pin (R_{REF} in Figure 7-1) is in series with one of the internal 10kΩ resistors.

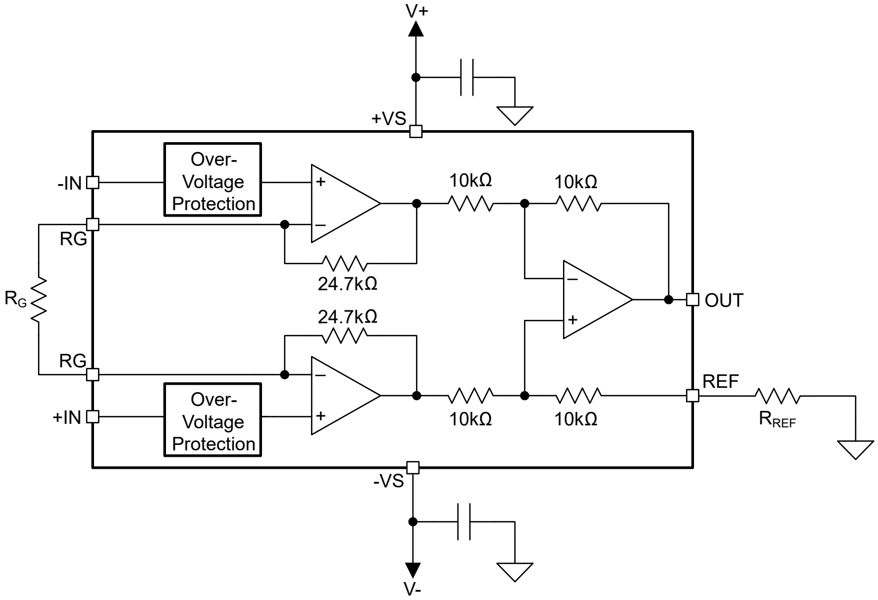


Figure 7-1. Parasitic Resistance Shown at the Reference Pin

The parasitic resistance at the reference pin (R_{REF}) creates an imbalance in the four resistors of the internal difference amplifier that results in a degraded common-mode rejection ratio (CMRR). Figure 7-2 shows the degradation in CMRR of the INA1H182-SEP as a result of the increased resistance at the reference pin. For the best performance, keep the source impedance to the REF pin (R_{REF}) less than 5Ω.

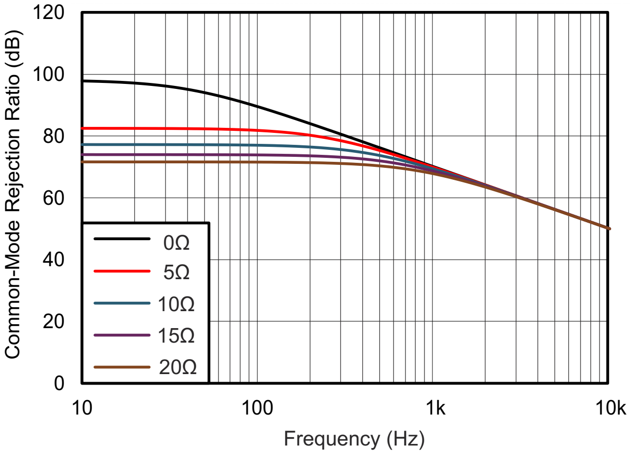


Figure 7-2. The Effect of Increasing Resistance at the Reference Pin

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, buffer the divider by an op amp, as shown in Figure 7-3, to avoid CMRR degradation.

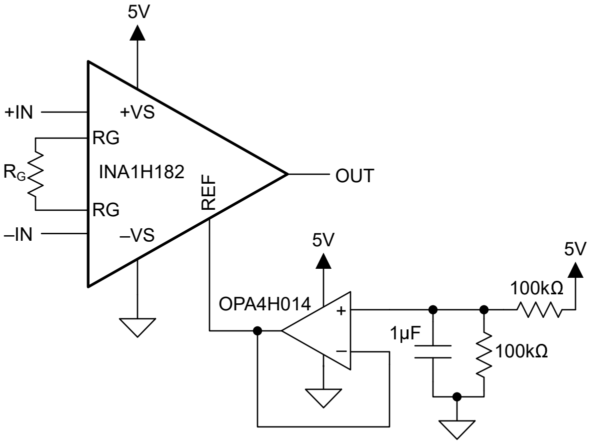


Figure 7-3. Use an Op Amp to Buffer Reference Voltages

7.1.2 Input Bias Current Return Path

The input impedance of the INA1H182-SEP is extremely high (approximately 100GΩ.) However, a path must be provided for the input bias current of both inputs. This input bias current is typically 150pA. High input impedance means that this input bias current changes little with varying input voltage.

For proper operation, Input circuitry must provide a path for this input bias current. Figure 7-4 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA1H182-SEP and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example in Figure 7-4). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

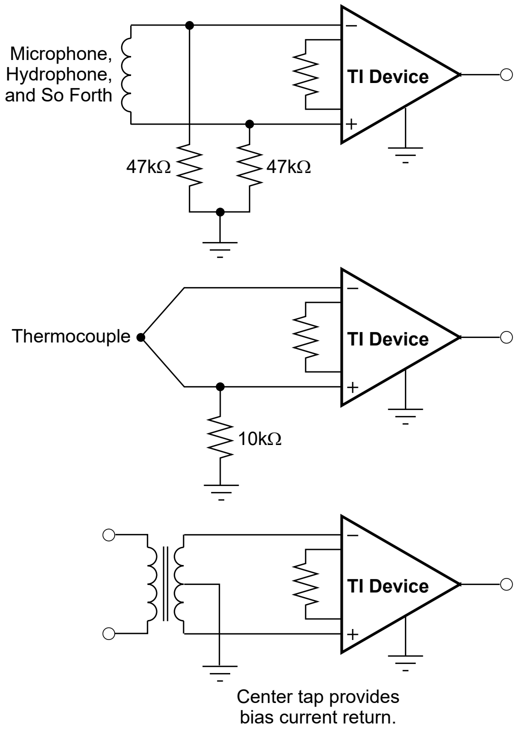


Figure 7-4. Providing an Input Common-Mode Current Path

7.2 Typical Applications

7.2.1 Resistor Temperature Detector Signal Conditioning Circuit

Figure 7-5 illustrates a 4-wire interface circuit for resistance temperature detectors (RTDs). The circuit is implemented using the OPA4H838-SEP and the ADS1278-SP. The ADS1278-SP is a radiation hardened, precision 24B, 8ch simultaneous sampling delta-sigma ADC and the OPA4H838-SEP is a radiation tolerant, precision, zero-drift operational amplifier.

The circuit is powered with a unipolar 5V supply and supports an RTD temperature measurement in the range of -100°C to 250°C, where the RTD sensor resistance varies in a range of 60.26Ω to 194.1Ω. The OPA4H838 op-amp circuit biases RTD with 1mA constant excitation current. The same excitation current is used to generate aratio-metric ADC voltage reference of +2.5V through a 2.5kΩ resistor, producing low noise, accurate RTD measurements. The INA1H182-SEP is able to drive the ADS1278-SP directly in the low speed mode, supporting data rates up to 10kSPS.

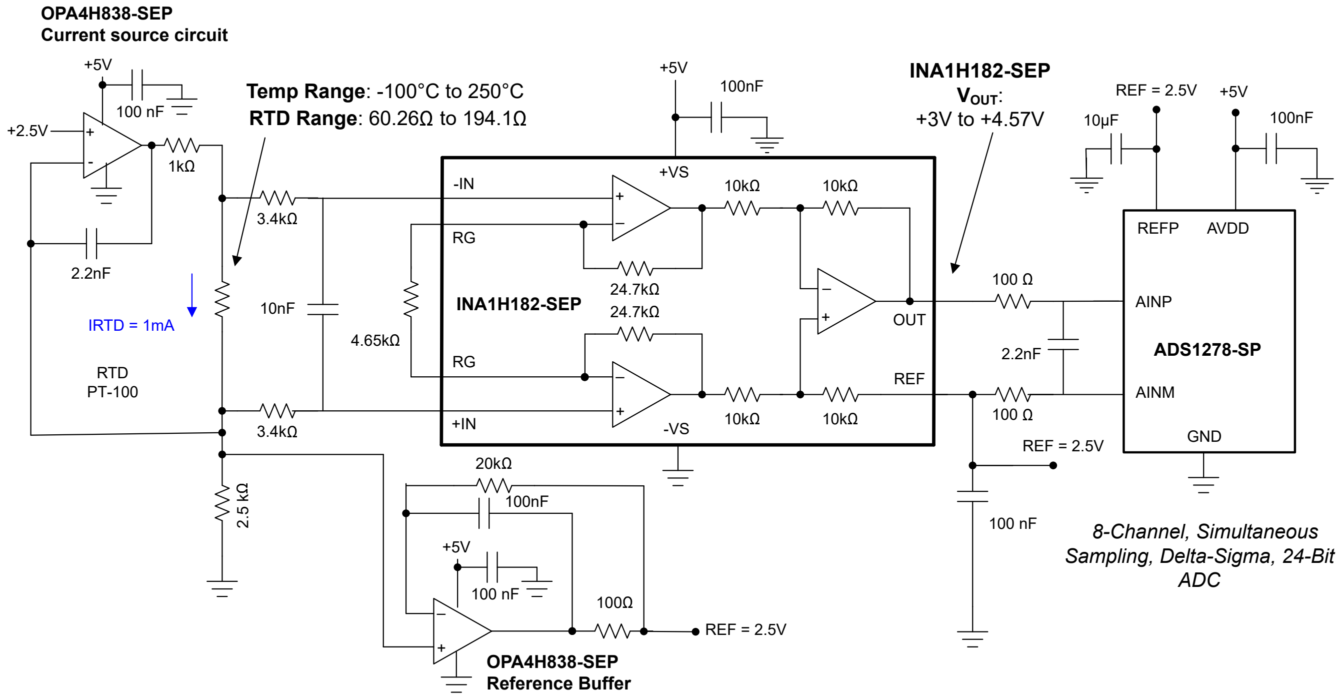


Figure 7-5. INA1H182-SEP RTD Sensor Measurement Circuit

7.2.1.1 Design Requirements

The design requirements for the RTD sensor measurement circuit are listed on .Design Requirements.

Table 7-1. Design Requirements

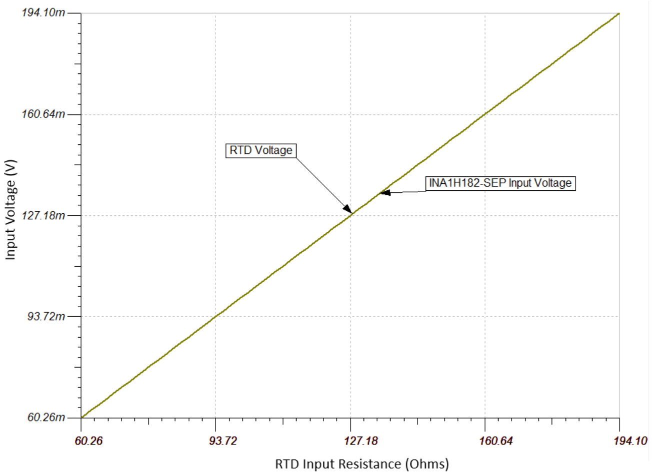
PARAMETER	VALUE
Supply voltage (unipolar supply circuit)	VS+ = 5V, VS– = GND, ADC REF =+2.5V)
RTD Temperature Measurement Range	-100°C to 250°C
RTD Resistance Range	60.26Ω to 194.1Ω
Full-scale range of ADC	FSR =±2.5V
INA Output Range	3V to 4.57V (1.57V range)
Maximum data rate supported	10kSPS (ADC in low-speed mode)

7.2.1.2 Detailed Procedure

1. High-grade C0G (NP0) are used everywhere in the filters on signal path for high-linearity and low settling times. Among ceramic surface-mount capacitors, C0G (NP0) ceramic capacitors provide the best capacitance accuracy. The type of dielectric used in C0G (NP0) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
2. The R-C-R filter at the ADS1278-SEP inputs works as a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand on the instrumentation amplifier, maintaining high linearity and low gain error that otherwise can degrade because of incomplete amplifier settling. The ADC input filter values are R = 100Ω and C = 2.2nF.
3. Use a 4.65kΩ precision, low drift R_G resistor with 0.1% tolerance to set the instrumentation amplifier gain and minimize gain and drift errors.
4. Use a precision ±0.1% tolerance, 2.5kΩ resistor to generate the reference of the ADC. The current source circuit takes advantage of the OPA4H838 feedback to force 2.5V across the 2.5kΩ resistor, generating a 1mA RTD constant current excitation.
5. The OPA4H838 amplifier reference buffer is configured in a dual-feedback configuration to provide stability while driving the REFP ADC input pin and 10µF bypass capacitor. RISO is a 100Ω isolation resistor that provides separation of two feedback paths for optimized stability. Feedback path number one is through feedback resistor, RF = 20kΩ, connected directly to the REF pin. Feedback path number two is through feedback capacitor CF = 100nF connected to the output of the op amp. The circuit provides a loop gain phase margin of 95°.

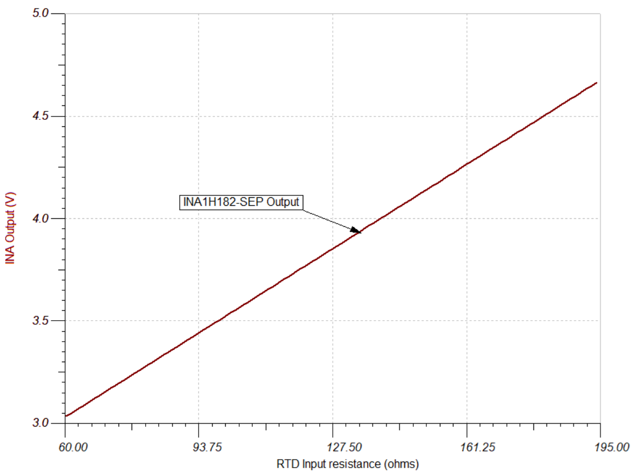
7.2.1.3 Application Curves

Figure 7-6 and Figure 7-7 show typical characteristic curves for the circuit.



RTD PT-100, I_{RTD} = 1mA

Figure 7-6. RTD Measurement: Circuit Simulation, INA Input Voltage



VS+ = 5V, VS– = GND, R_G = 4.65kΩ, INA_{REF} = 2.5V

Figure 7-7. RTD Measurement: Circuit Simulation, INA Output Voltage

7.3 Power Supply Recommendations

The nominal performance of the INA1H182-SEP is specified with a supply voltage of ±9V and midsupply reference voltage. The device also operates using power supplies from ±2.25V (4.5V) to ±9V (18V) and non-midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in *Section 5.6*.

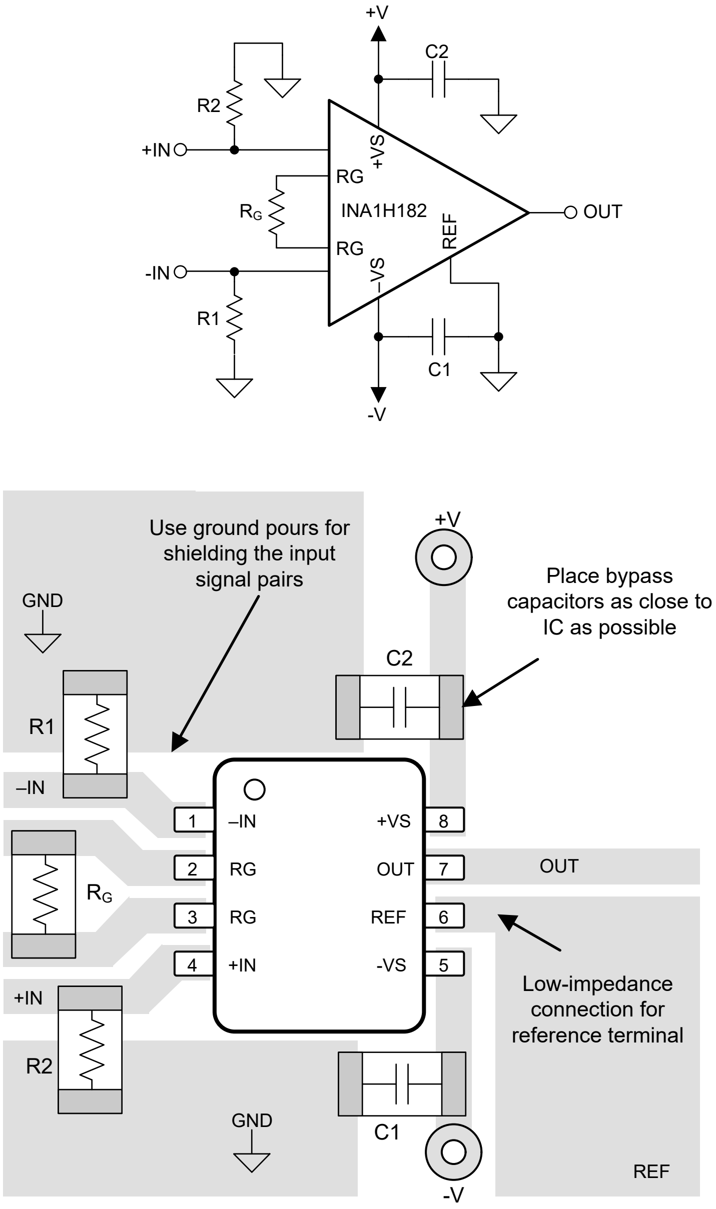
7.4 Layout

7.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. Even slight mismatch in parasitic capacitance at the gain setting pins can degrade CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible and most importantly so that capacitance mismatch between the RG pins is minimized.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
    - Connect low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from +V to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 7-8, keep R_G close to the pins to minimize parasitic capacitance.
- Keep the traces as short as possible.

7.4.2 Layout Example



Use ground pours for shielding the input signal pairs

Place bypass capacitors as close to IC as possible

Low-impedance connection for reference terminal

Figure 7-8. Example Schematic and Associated PCB Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

- *SPICE-based analog simulation program — TINA-TI software folder*
- *Common-Mode Input Range Calculator for Instrumentation Amplifiers*

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA1H182-SEP Single Effects (SEE) Radiation Report*
- Texas Instruments, *INA1H182-SEP Radiation-Tolerant, Low offset, Low Noise, Precision Instrumentation Amplifier TID Report*
- *Texas Instruments, INA1H182-SEP Neutron Displacement Damage (NDD) Characterization*
- Texas Instruments, *INA1H182-SEP Production Flow and Reliability Report*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA1H182DGKTSEP	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	821S
V62/25653-01XE	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	-	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	821S

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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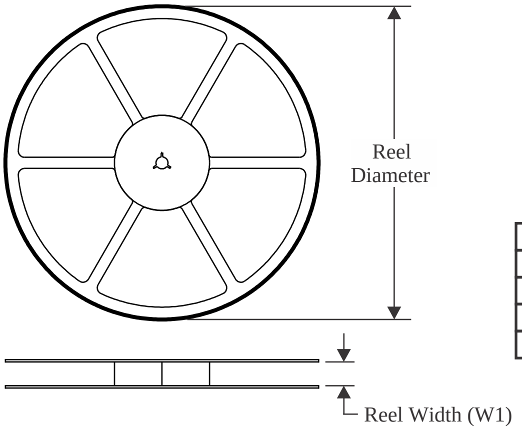
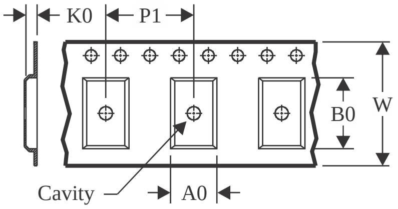
TAPE AND REEL INFORMATION

REEL DIMENSIONS

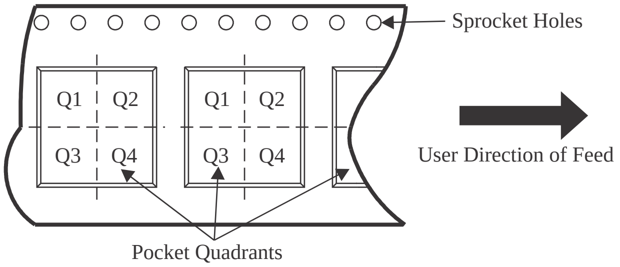


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

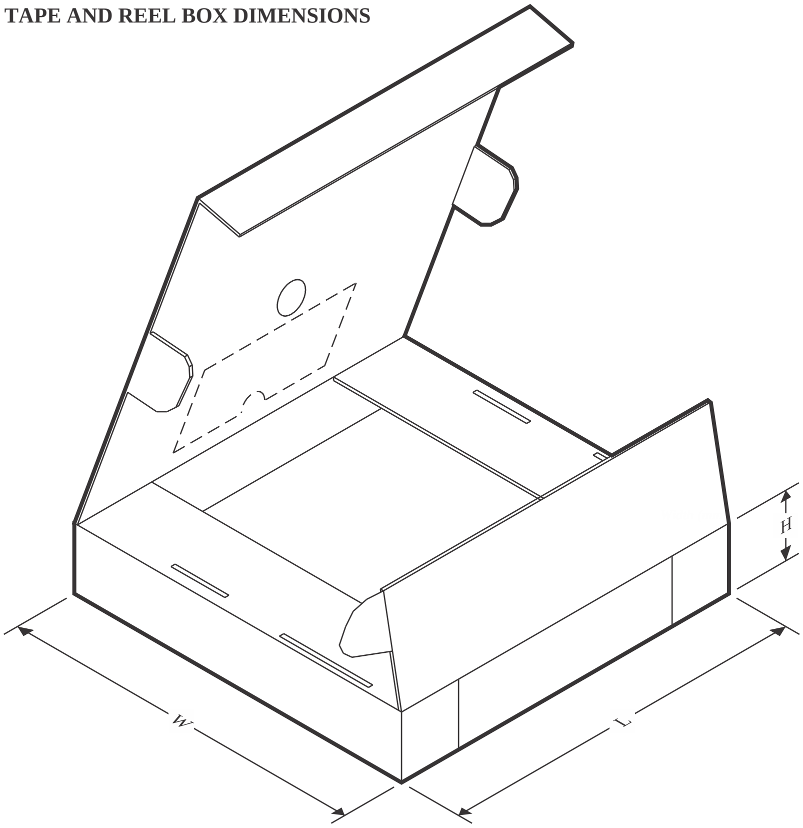
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA1H182DGKTSEP	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

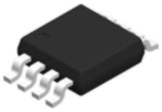
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA1H182DGKTSEP	VSSOP	DGK	8	250	353.0	353.0	32.0

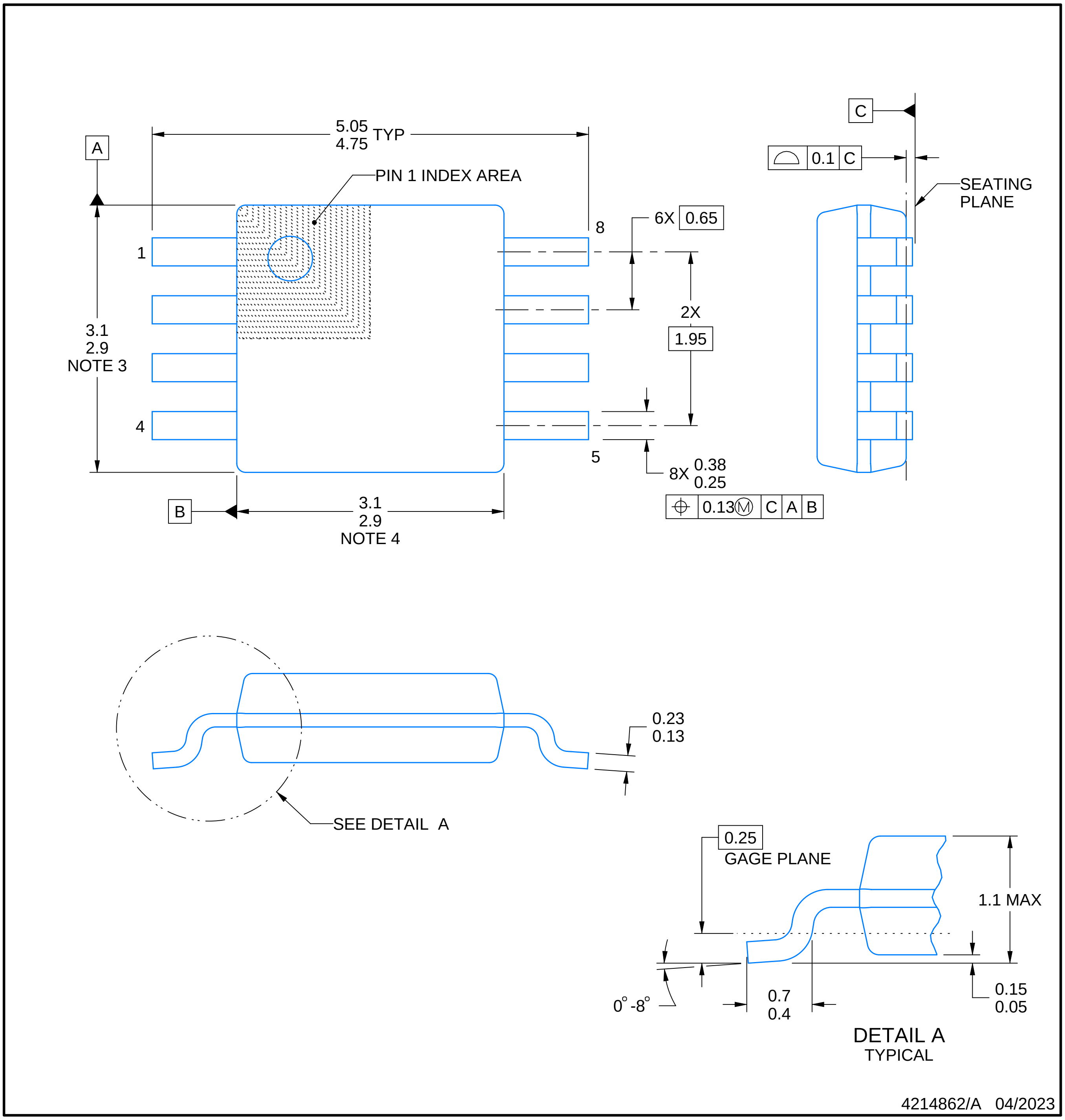
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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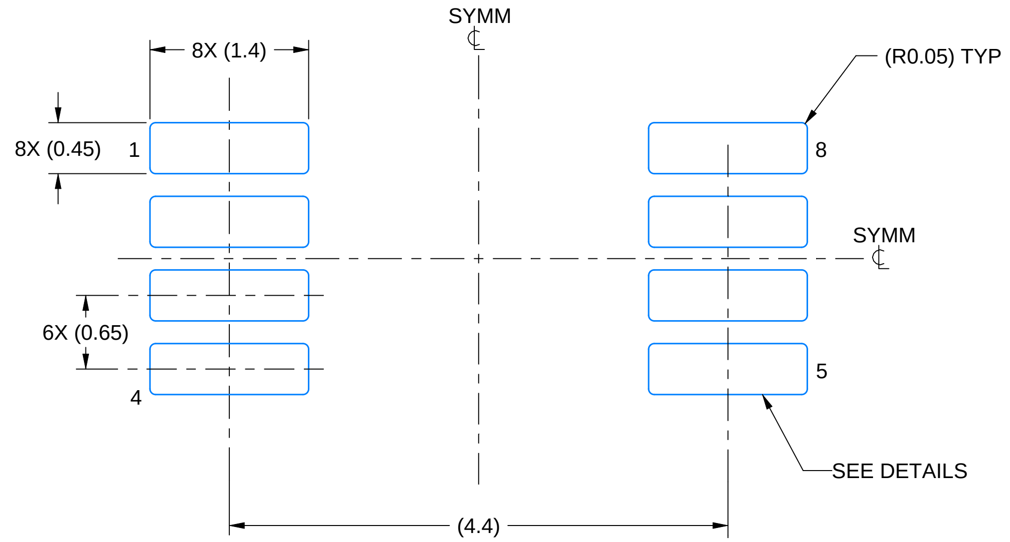
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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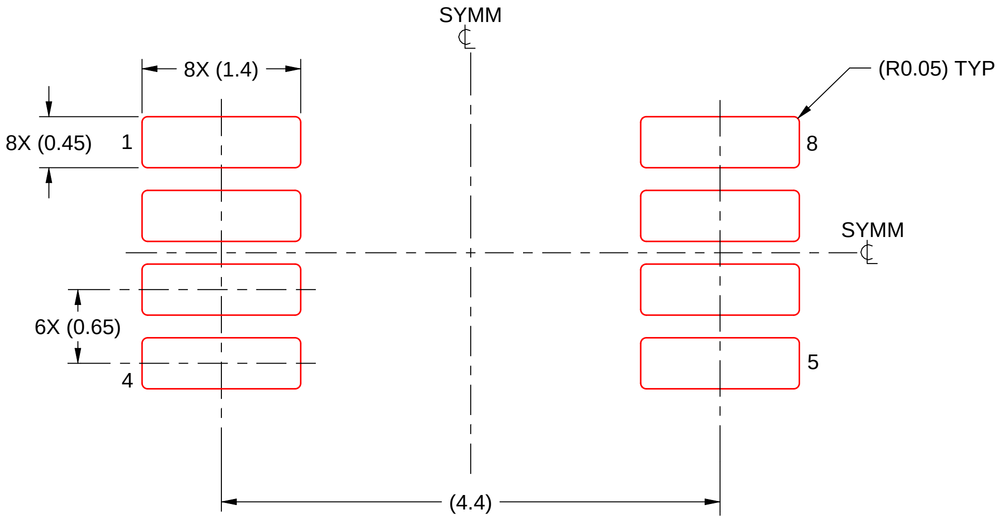
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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