INA148 ±200V Common-mode Voltage Difference Amplifier

1 Features

- High common-mode voltage:
  - +75V at V_S = +5V
  - ±200V at V_S = ±15V
- Fixed differential gain = 1V/V
- Low quiescent current: 260µA
- Wide supply range:
  - Single supply: 2.7V to 36V
  - Dual supplies: ±1.35V to ±18V
- Low gain error: 0.075% maximum
- Low non-linearity: 0.002% maximum
- High CMRR: 86dB
- SOIC-8 Package

2 Applications

- Battery cell formation and test equipment
- Battery management systems
- Analog input module
- Mixed module (AI, AO, DI, DO)
- DC fast charging power module
- String inverter

3 Description

The INA148 is a precision, low-power, unity-gain difference amplifier with a high common-mode input voltage range. The device consists of a monolithic precision bipolar op amp with a thin-film resistor network.

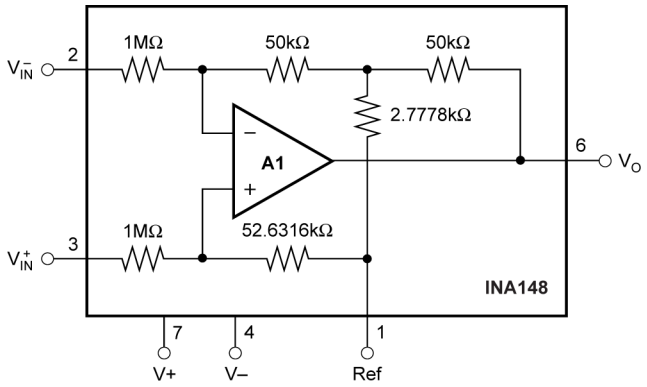
The on-chip resistors are laser trimmed for an accurate 1V/V differential gain and high common-mode rejection. Excellent temperature tracking of the resistor network maintains high gain accuracy and common-mode rejection over temperature. The INA148 operates on single or dual supplies.

The INA148 is available in SOIC-8 surface-mount package and is specified for the –40°C to +85°C industrial temperature range.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA148	D (SOIC, 8)	4.9mm × 6mm

(1) For more information, see Section 9.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

TOP VIEW SO-8

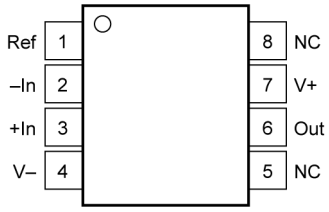


Figure 4-1. D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
-IN	2	I	Negative (inverting) input
+IN	3	I	Positive (non-inverting) input
NC	5, 8	NC	No connect.
Out	6	O	Output
Ref	1	I	Reference input
V-	4	–	Negative power supply
V+	7	–	Positive power supply

(1) I=Input; O=Output; NC = No Connect.

5 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see Section 7.1.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply, V_S = (V+) – (V–)		±18	V
		Single supply, V_S = (V+) – 0V		36	
	Signal input pins	Continuous		±200	V
		Peak (0.1s)		±500	V
	Output short-circuit(2)		Continuous		
T_A	Operating temperature		–55	125	°C
T_{stg}	Storage temperature		–55	125	°C
	Junction temperature			150	°C
	Lead temperature (soldering, 10s)			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	2.7	30	36	V
		Dual-supply	±1.35	±15	±18	
T_A	Specified temperature		–40		85	°C

5.3 Thermal Information

THERMAL METRIC(1)		INA148 D (SOIC) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	150	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.4 Electrical Characteristics

at T_A = 25°C, V_S = ±5V to ±15V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = V_S / 2, and all chip site origins (CSO), (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V_{OS}	Offset voltage (RTI) (1) (4)	V_S = ±15V				±1	±5	mV
		V_S = ±5V				±1	±5	
	Offset voltage drift (RTI)(1)	T_A = –40°C to 85°C				±10		µV/°C
PSRR	Power-supply rejection ratio (RTI)(1)	V_S = ±1.35V to ±18V		CSO: SHE		±50	±400	µV/V
				CSO: TID		±3.5	±80	
V_{CM}	Common-mode voltage (2)	V_O = 0V	V_S = ±15V		–200		200	V
			V_S = ±5V		–100		100	
			V_S = +5V(3), V_{REF} = V_S / 2		–47.5		32.5	
			V_S = +5V(3), V_{REF} = 0.25V		–4		75	
CMRR	Common-mode voltage rejection	V_S = ±15V, V_{CM} = –200V to 200V, R_S = 0Ω			70	86		dB
		V_S = ±5V, V_{CM} = –100V to 80V, R_S = 0Ω			70	86		
		V_S = +5V(3), V_{CM} = –47.5V to 32.5V, R_S = 0Ω			70	86		
	Differential input impedance					2		MΩ
	Common-mode input impedance					1		
e_N	Voltage noise (RTI)(1) (5)	f_B = 0.1Hz to 10Hz				17		$µV_{PP}$
		f = 1kHz				880		nV/√Hz
GAIN								
	Initial					1		V/V
GE	Gain error	V_O = (V–) + 0.5V to (V+) – 1.5V				±0.01	±0.075	%
	Gain error drift	T_A = –40°C to +85°C				±3	±10	ppm/°C
	Gain nonlinearity	V_O = (V–) + 0.5V to (V+) – 1.5V		V_S = ±15V		±0.001	±0.002	% of FSR
				V_S = ±5V		±0.001		
		V_S = +5V(3), V_O = 0.5V to 3.5V				±0.001		
OUTPUT								
	Output voltage	R_L = 100kΩ			(V–) + 0.25		(V+) – 1	V
		R_L = 10kΩ			(V–) + 0.5		(V+) – 1.5	
C_L	Load capacitance	Stable operation				10		nF
I_{SC}	Short-circuit current	Continuous to V_S / 2	CSO: SHE			±13		mA
				V_S = +5V(3)		±8		
			CSO: TID			±20		

5.4 Electrical Characteristics (continued)

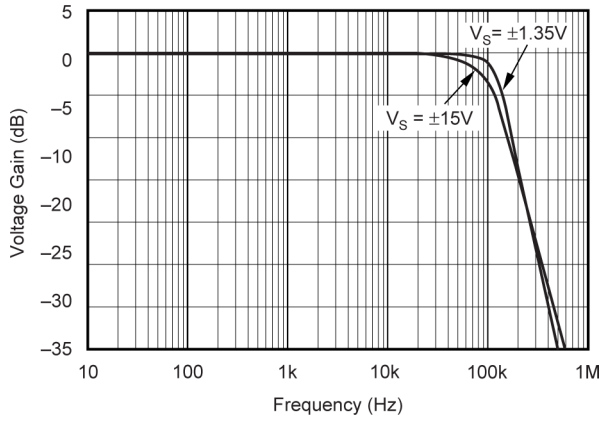
at T_A = 25°C, V_S = ±5V to ±15V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = V_S / 2, and all chip site origins (CSO), (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE								
BW	Bandwidth, –3dB	CSO: SHE				100		kHz
		CSO: TID				155		
SR	Slew rate					1		V/µs
t_S	Settling time	To 0.1%	V_S = ±15V, V_O = 10V step	CSO: SHE		21		µs
				CSO: TID		15		
			V_S = ±5V, V_O = 6V step	CSO: SHE		21		
				CSO: TID		15		
			V_S = +5V(3), V_O = 3V step			21		
		To 0.01%	V_S = ±15V, V_O = 10V step	CSO: SHE		25		
				CSO: TID		23		
			V_S = ±5V, V_O = 6V step	CSO: SHE		25		
				CSO: TID		23		
			V_S = +5V(3), V_O = 3V step			25		
	Overload recovery	50% input overload	CSO: SHE			4		µs
			CSO: TID			1.2		
			V_S = +5V(3)			3		
POWER SUPPLY								
I_Q	Quiescent current	V_{IN} = 0V				±260	±300	µA

(1) RTI stands for Referred to Input
(2) Input common-mode voltage varies with output voltage; see Section 5.5.
(3) V_S = +5V single supply means V_{S+} = +5V and V_{S-} = GND
(4) Input offset voltage specification includes effects of input bias current and offset current of amplifier
(5) Includes effects of input current noise and thermal noise contributor of resistor network

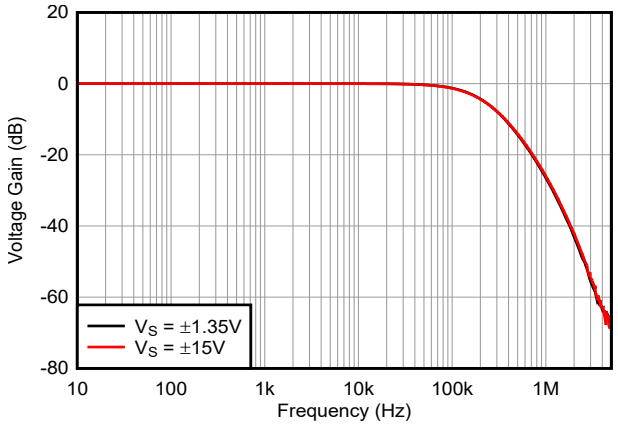
5.5 Typical Characteristics

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ to common, and V_{REF} = 0V, and all chip site origin (CSO), (unless otherwise noted)



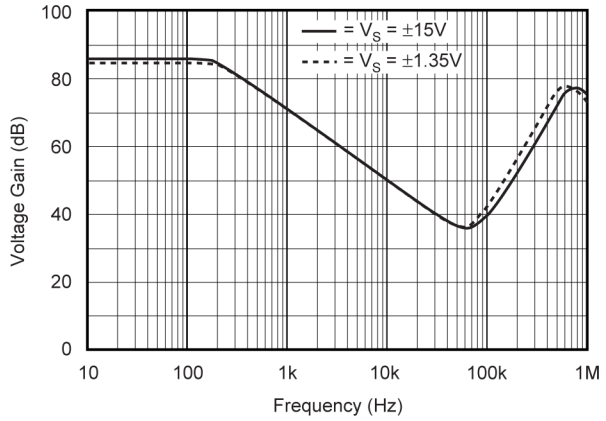
CSO: SHE

Figure 5-1. Gain vs Frequency



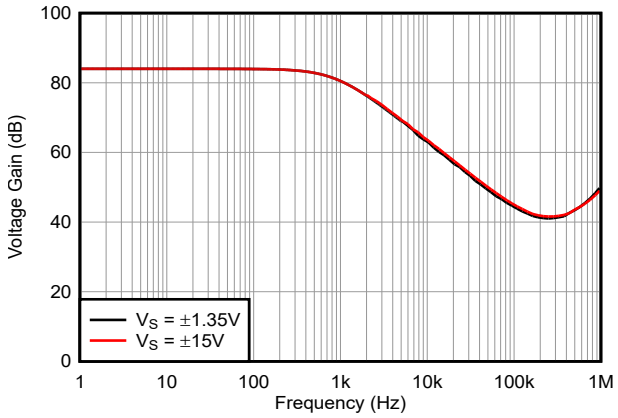
CSO: TID

Figure 5-2. Gain vs Frequency



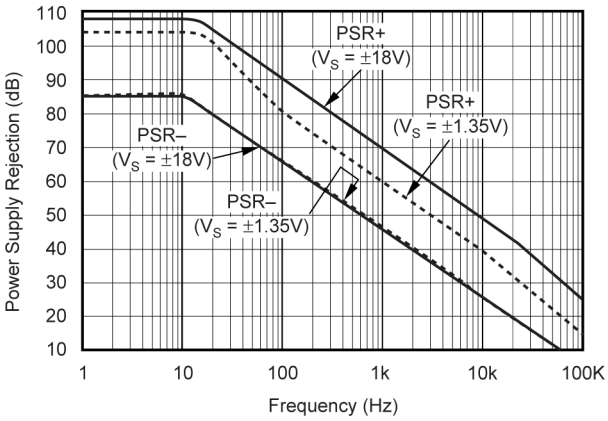
CSO: SHE

Figure 5-3. Common-mode Rejection vs Frequency



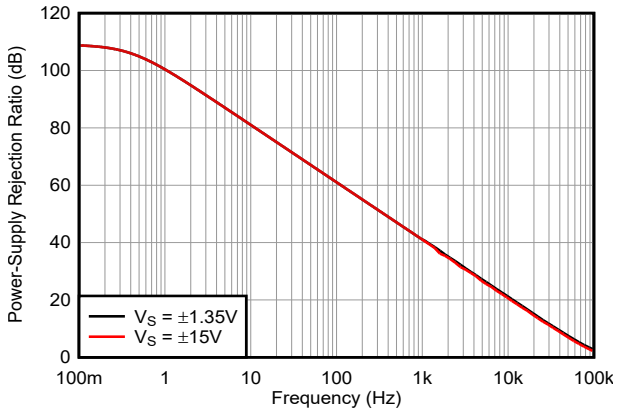
CSO: TID

Figure 5-4. Common-mode Rejection vs Frequency



CSO: SHE

Figure 5-5. Power Supply Rejection vs Frequency

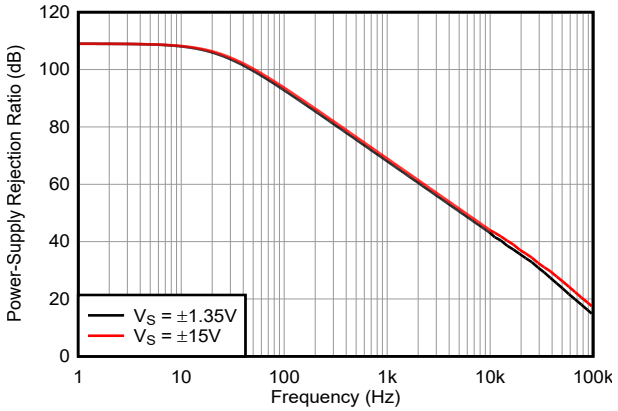


CSO: TID

Figure 5-6. Power Supply Rejection (PSRR+) vs Frequency

5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ to common, and V_{REF} = 0V, and all chip site origin (CSO), (unless otherwise noted)



CSO: TID

Figure 5-7. Power Supply Rejection (PSRR-) vs Frequency

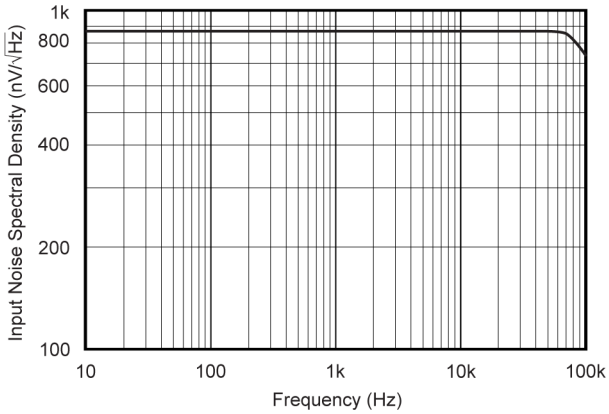


Figure 5-8. Input Voltage Noise Spectral Density

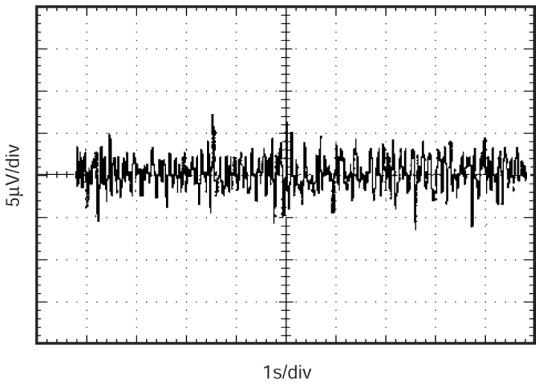


Figure 5-9. Voltage Noise (RTI) 0.1Hz to 10Hz

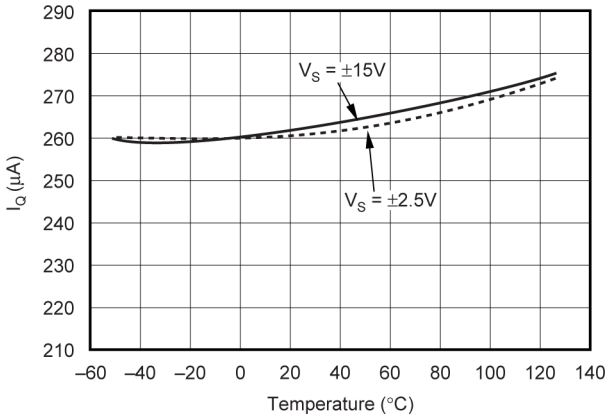
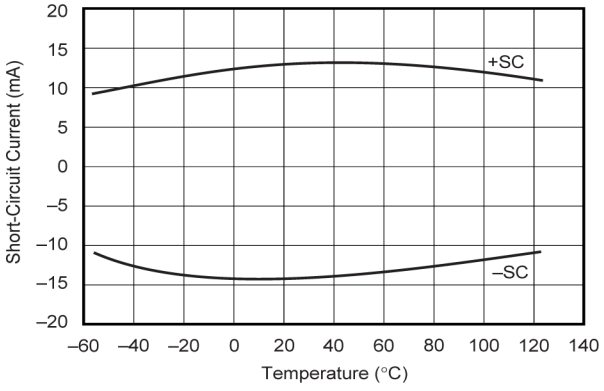
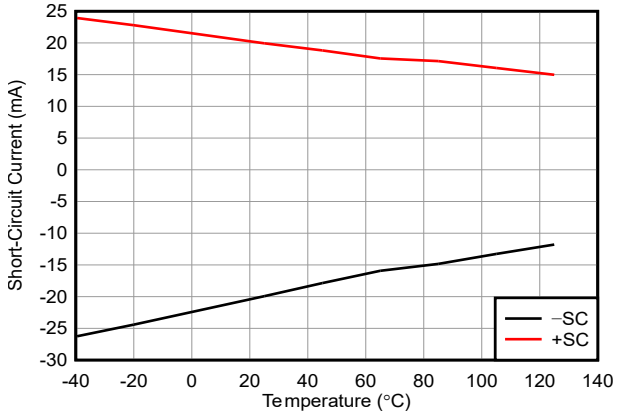


Figure 5-10. Quiescent Current vs Temperature



CSO: SHE

Figure 5-11. Short-Circuit Current vs Temperature



CSO: TID

Figure 5-12. Short-Circuit Current vs Temperature

5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ to common, and V_{REF} = 0V, and all chip site origin (CSO), (unless otherwise noted)

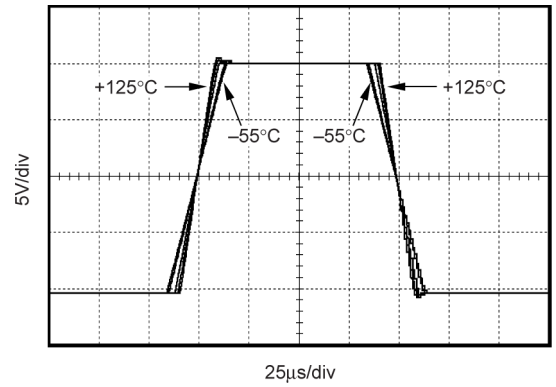
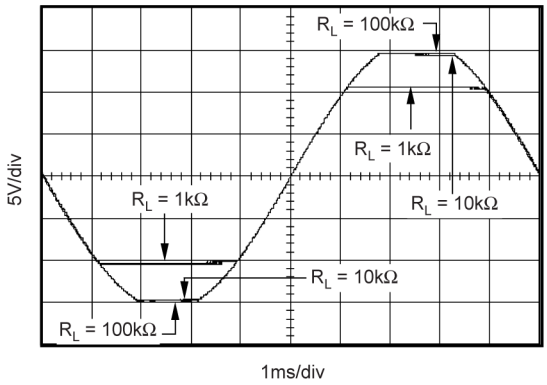
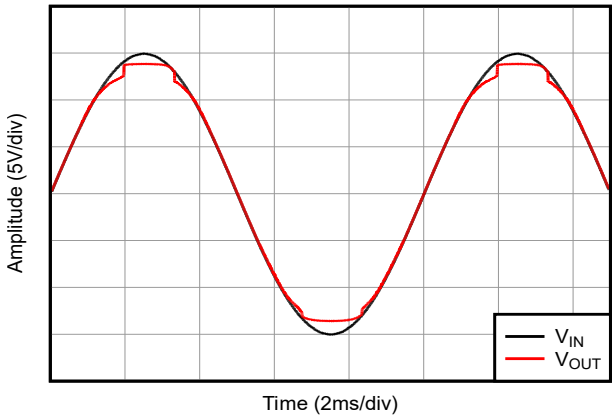


Figure 5-13. Large-Signal Step Response vs Temperature



CSO: SHE

Figure 5-14. Output Voltage Swing vs R_L



CSO: TID

Figure 5-15. Output Voltage Swing (R_L = 1kΩ)

CSO: TID

Figure 5-16. Output Voltage Swing (R_L = 10kΩ, 100kΩ)

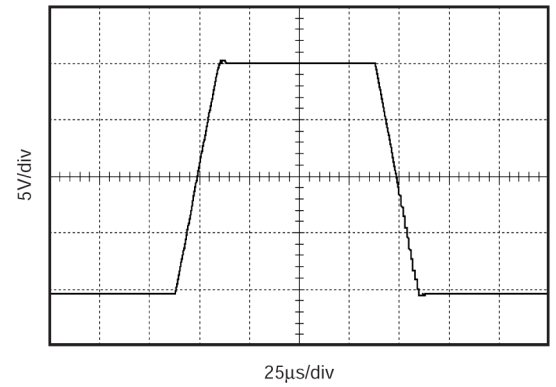
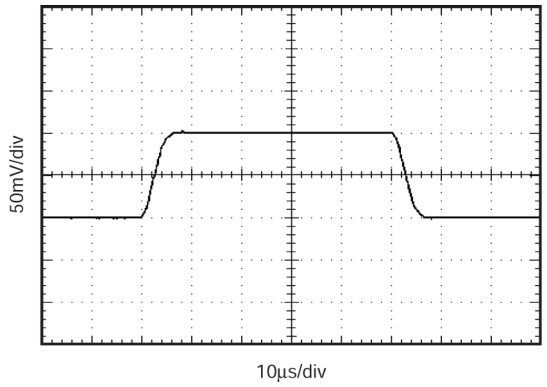


Figure 5-17. Large-Signal Step Response (R_L = 10kΩ, C_L = 10pF)

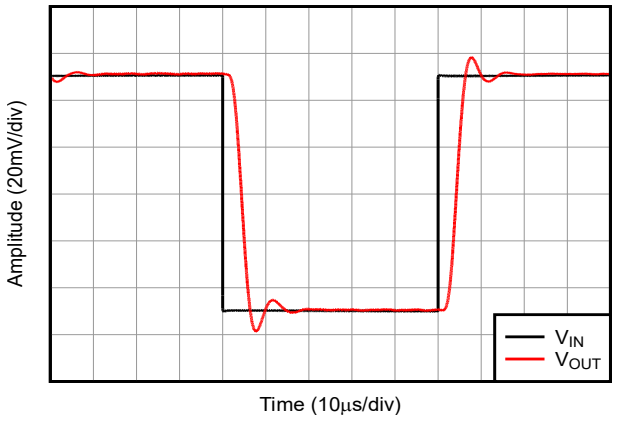


CSO: SHE

Figure 5-18. Small-Signal Step Response (R_L = 10kΩ, C_L = 10pF)

5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ to common, and V_{REF} = 0V, and all chip site origin (CSO), (unless otherwise noted)

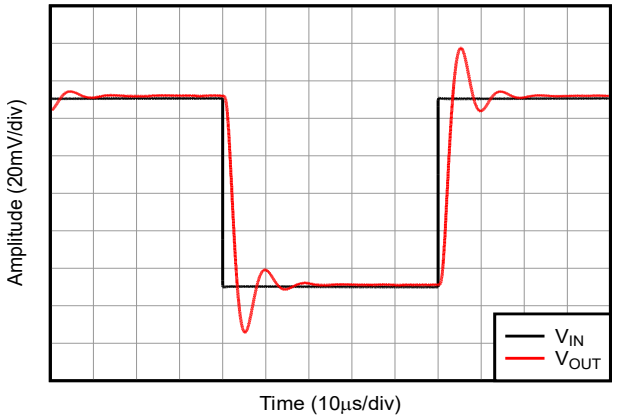


CSO: SHE

Figure 5-19. Small-Signal Step Response (R_L = 10kΩ, C_L = 1nF)

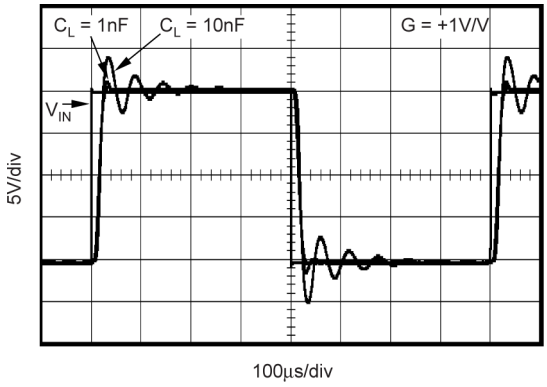
CSO: TID

Figure 5-20. Small-Signal Step Response (R_L = 10kΩ, C_L = 10pF)



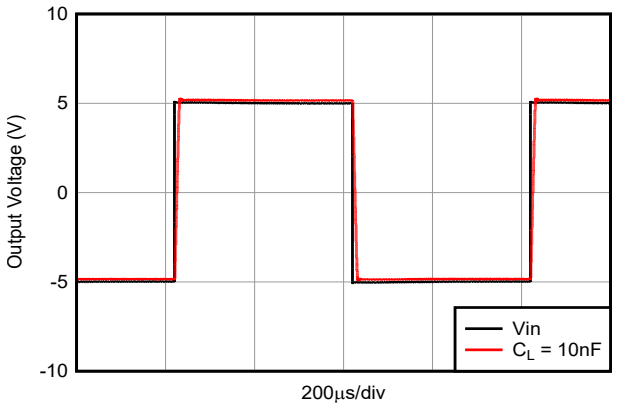
CSO: TID

Figure 5-21. Small-Signal Step Response (R_L = 10kΩ, C_L = 10nF)



CSO: SHE

Figure 5-22. Large-Signal Capacitive Load Response (C_L = 1nF and 10nF)



CSO: TID

Figure 5-23. Large-Signal Capacitive Load Response (C_L = 10nF)

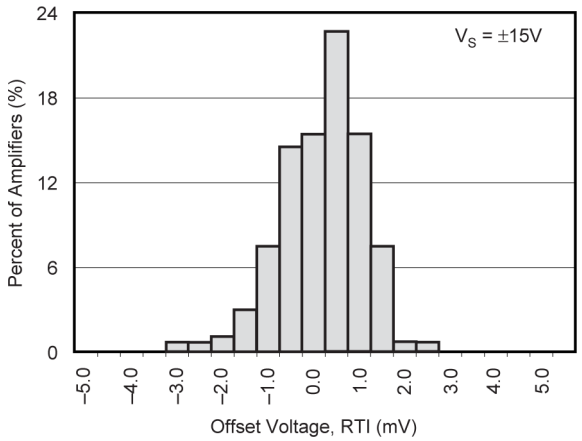


Figure 5-24. Offset Voltage Production Distribution

5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ to common, and V_{REF} = 0V, and all chip site origin (CSO), (unless otherwise noted)

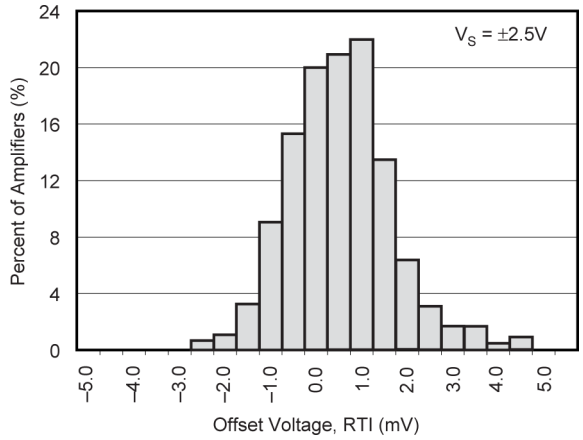


Figure 5-25. Offset Voltage Production Distribution

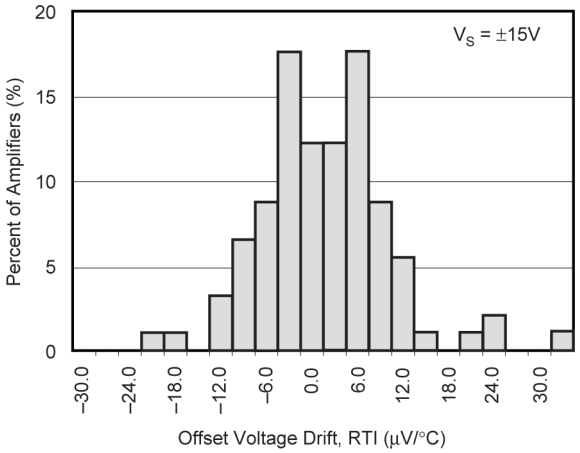


Figure 5-26. Offset Voltage Drift Production Distribution

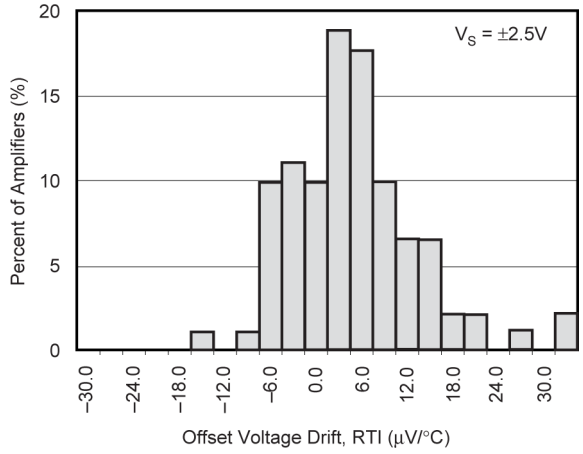


Figure 5-27. Offset Voltage Drift Production Distribution

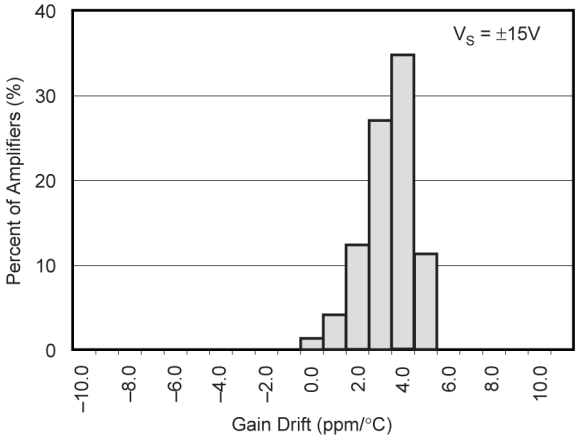


Figure 5-28. Gain Drift Production Distribution

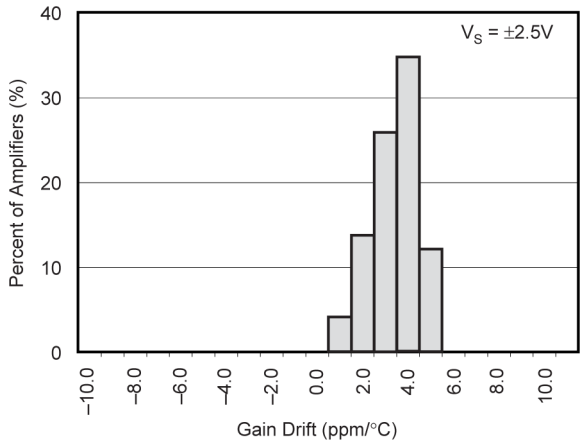
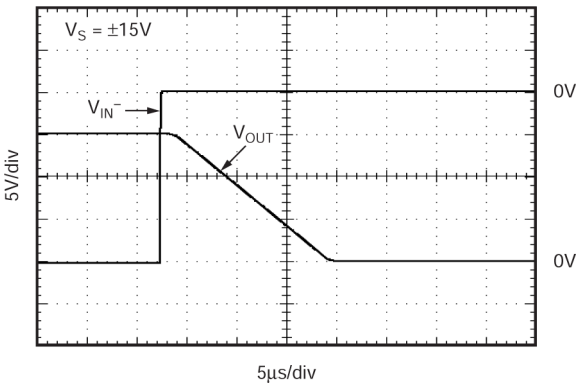


Figure 5-29. Gain Drift Production Distribution

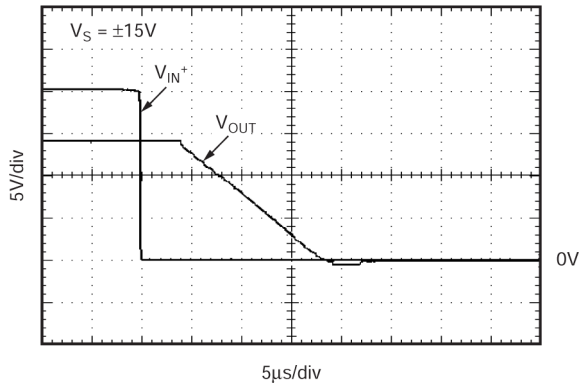


CSO: SHE

Figure 5-30. Inverting Input 50% Overload Recovery Time

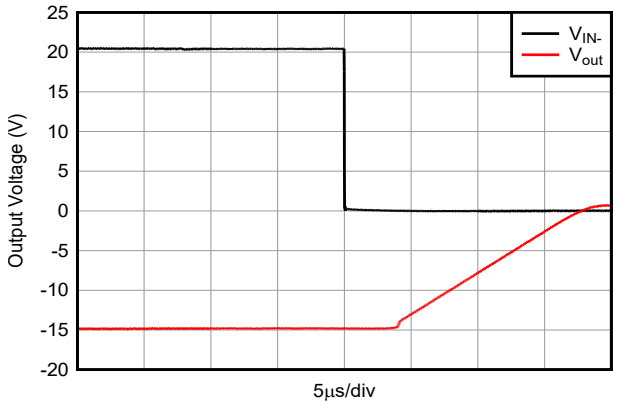
5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ to common, and V_{REF} = 0V, and all chip site origin (CSO), (unless otherwise noted)



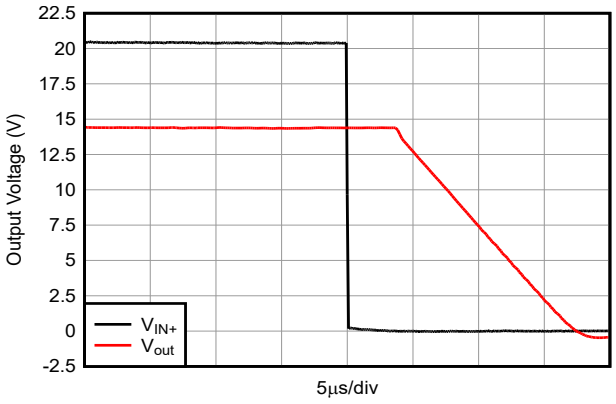
CSO: SHE

Figure 5-31. Noninverting Input 50% Overload Recovery Time



CSO: TID

Figure 5-32. Inverting Input 50% Overload Recovery Time



CSO: TID

Figure 5-33. Noninverting Input 50% Overload Recovery Time

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The INA148 is a unity gain difference amplifier with a high common-mode input voltage range. A basic diagram of the circuit and pin connections is shown in Figure 6-1.

To achieve the high common-mode voltage range, the INA148 features a precision laser-trimmed thin-film resistor network with a 20:1 input voltage divider ratio. High input voltages are thereby reduced in amplitude to bring both positive and negative inputs of the internal operational amplifier within linear operating range. A "Tee" network in the operational amplifier feedback network places the amplifier in a gain of 20V/V, thus restoring the overall gain to unity (1V/V) of the circuit.

External voltages can be summed into the output of the amplifier by using the Ref pin, making the differential amplifier a highly versatile design tool. Voltages on the Ref pin also influence the common-mode voltage range of the INA148.

Use low ESR, power supply bypass capacitors and connect as close to pins 4 and 7 as practicable. Bypass capacitors reduce coupled noise by providing low impedance power sources local to analog circuitry. Ceramic or tantalum types are recommended for use as bypass capacitors.

The input impedance of the INA148 must be considered when routing input signal traces on a PCB board. Avoid placing digital signal traces near the input traces of the difference amplifier to minimize noise pickup.

6.1.1 Operating Voltage

The INA148 is specified for ±15V and ±5V dual supplies and +5V single supplies. The INA148 can be operated with single or dual supplies with excellent performance.

The INA148 is fully characterized for supply voltages from ±1.35V to ±18V and over temperatures of –40°C to +125°C. Parameters that vary with operating voltage, load conditions, or temperature are shown in the Typical Performance section.

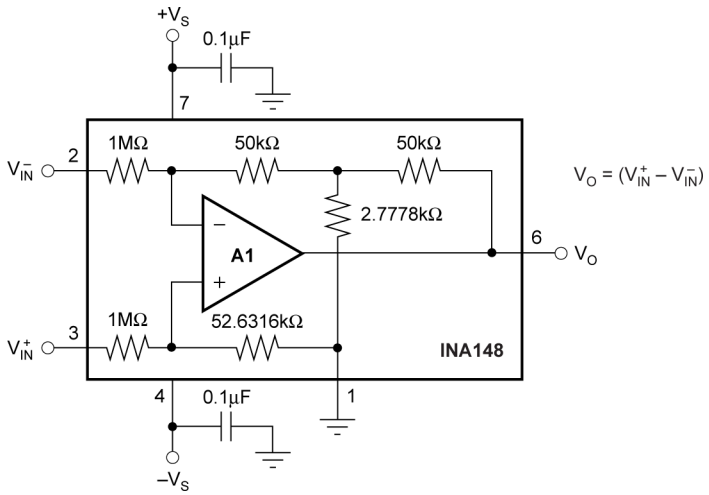


Figure 6-1. Basic Circuit Connections.

6.1.2 Gain Equation

An internal on-chip resistor network sets the overall differential gain of the INA148 to precisely 1V/V. The output is accordance with the equation:

$$V_{OUT} = \left(V^{+}_{IN} - V^{-}_{IN}\right) + V_{REF} \quad (1)$$

6.1.3 Common-Mode Range

The 20:1 input resistor ratio of the INA148 provides an input common-mode range that extends well beyond the power supply rails.

The exact input voltage range depends on the amplifier power supply voltage and the voltage applied to the Ref terminal (pin 1). Typical input voltage ranges at different power supply voltages can be found in the *Section 6.2* section.

Do not attempt to extend the INA148 input voltage range further by adding external resistors as this degrades CMRR.

6.1.4 Offset Trim

The INA148 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment.

A voltage applied to the reference pin (Ref, pin 1) is summed directly into the amplifier output signal. Therefore, this technique can be used to null the amplifier input offset voltage. Figure 6-2 shows an optional circuit for trimming the offset voltage.

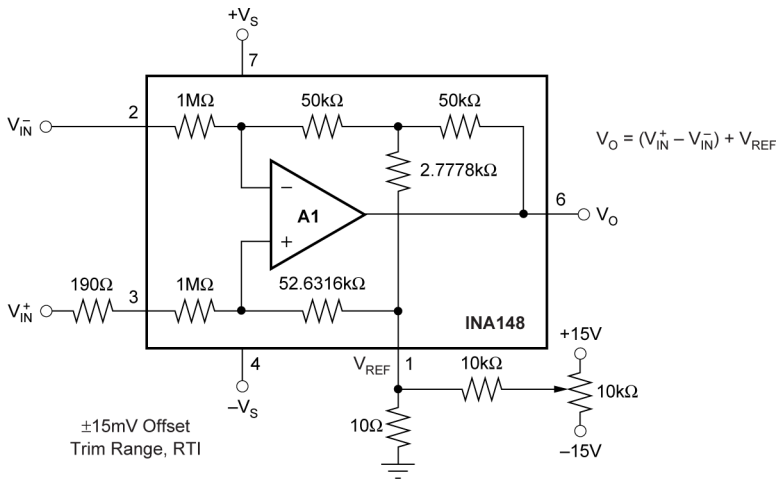


Figure 6-2. Optional Offset Trim Voltage.

To maintain high common-mode rejection (CMRR), verify that the source impedance of any signal applied to the Ref pin is very low (≤ 5Ω).

A source impedance of only 10Ω at the Ref pin reduces the INA148 CMRR to approximately 74dB. High CMRR can be restored if a resistor is added in series with the amplifier positive input (pin 3). Use a resistor that is 19 times the source impedance that drives the Ref pin. For example, if the Ref pin has a source impedance of 10Ω, add a resistor of 190Ω in series with pin 3.

Preferably, buffer the offset trim voltage applied to the Ref pin with an amplifier such as an OPA237 (see Figure 6-3). In this case, the operational amplifier output impedance is low enough that no external resistor is needed to maintain the INA148 excellent CMRR.

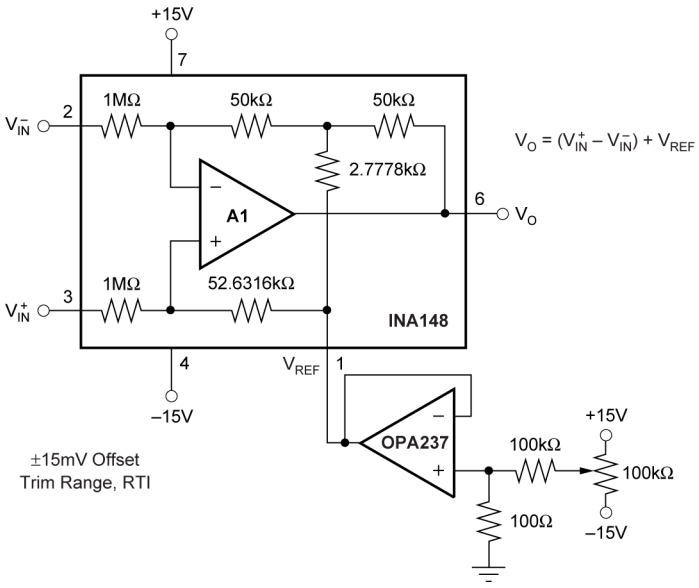


Figure 6-3. Preferred Offset Trim Circuit.

6.1.5 Input Impedance

The input resistor network determines the impedance of each of the INA148 inputs; approximately 1MΩ. Unlike an instrumentation amplifier, signal source impedance at the two input terminals must be nearly equal to maintain good common-mode rejection.

A mismatch between the two inputs source impedance causes a differential amplifier common-mode rejection to be degraded. With a source impedance imbalance of only 500Ω, CMRR can fall to approximately 66dB.

Figure 6-4 shows a common application: measuring power supply current through a shunt resistor (R_S). A shunt resistor creates an unbalanced source resistance condition that can degrade a differential amplifier common-mode rejection.

Unless the shunt resistor is less than approximately 100Ω, use an additional equal compensating resistor (R_C) to maintain input balance and high CMRR.

Source impedances (or shunts) greater than 5kΩ are not recommended, even if well compensated. The internal resistor network is laser-trimmed for accurate voltage divider ratios, but not necessarily to absolute values. Input resistors are shown as 1MΩ; however, this value is only nominal.

In practice, the input resistors absolute values can vary by as much as 30 percent. The two input resistors match to about 5 percent. Therefore, adding compensating resistors greater than 5kΩ can cause a serious mismatch in the resulting resistor network voltage divider ratios, thus degrading CMR.

6.2 Typical Applications

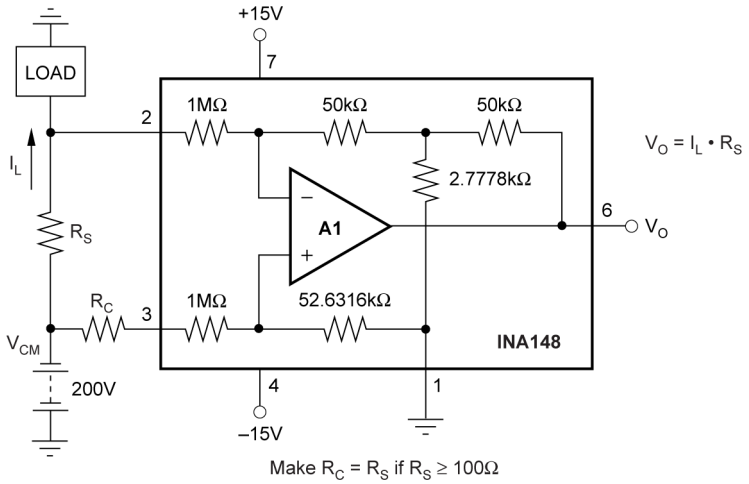
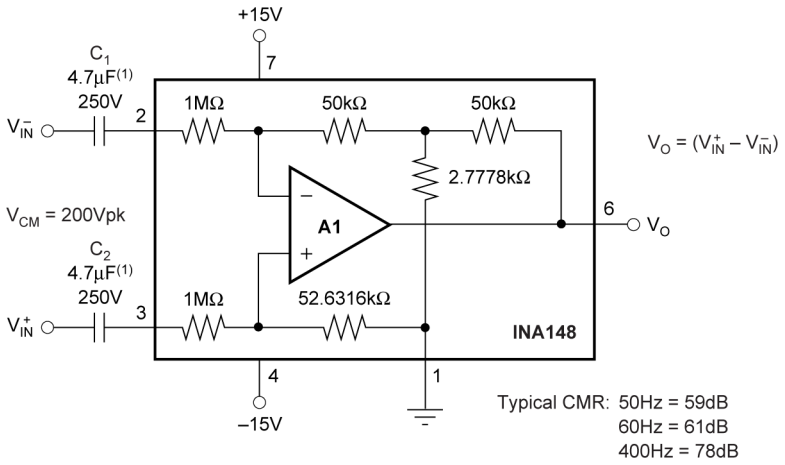


Figure 6-4. Shunt-Resistor Current Measurement Circuit



1. Metallized polypropylene, ±5% tolerance.

Figure 6-5. AC-Coupled Difference Amplifier

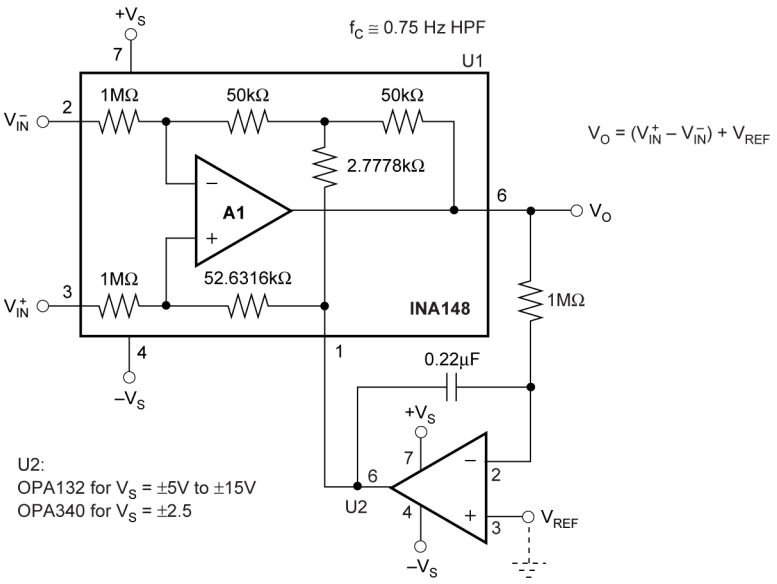


Figure 6-6. Quasi-AC-Coupled Differential Amplifier

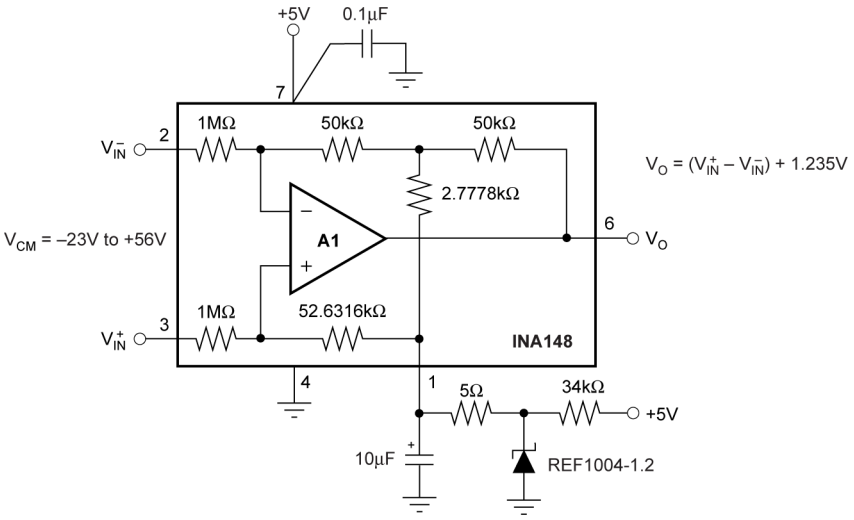


Figure 6-7. Single-Supply Differential Amplifier

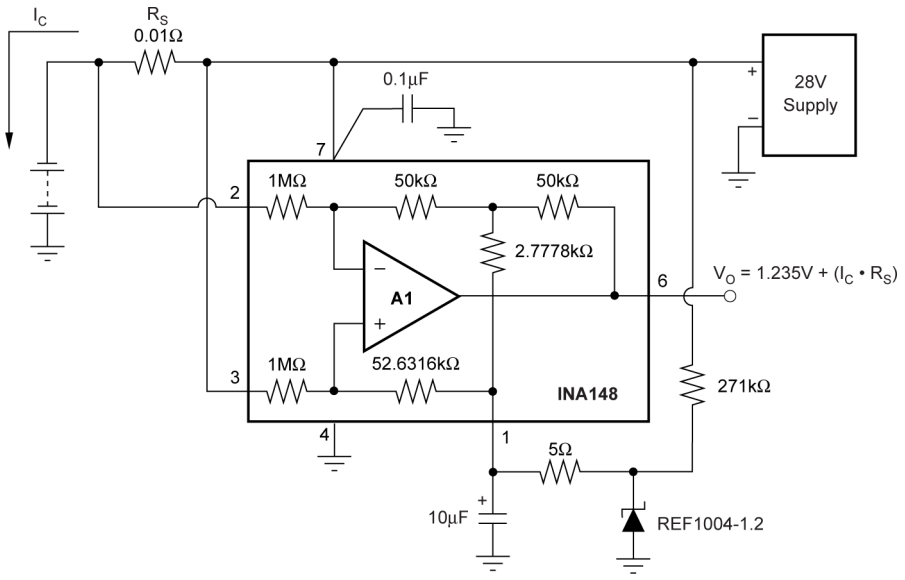


Figure 6-8. Battery Monitor Circuit

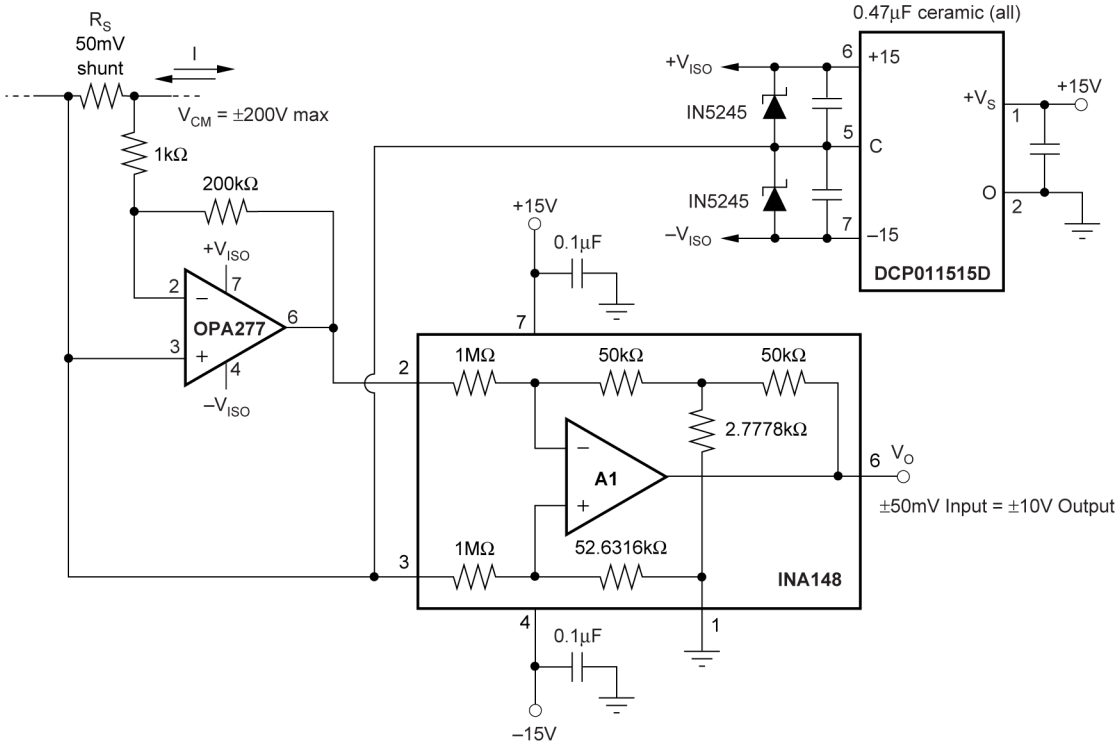


Figure 6-9. 50mV Current Shunt Amplifier With ±200V Common-Mode Voltage Range

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Device Support

7.1.1 Device Nomenclature

Table 7-1. Device Nomenclature

Part Number	Definition
INA148UA INA148UA/2K5	The die is manufactured in CSO: SHE or CSO: TID.

7.1.2 Development Support

7.1.2.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

7.1.2.2 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2000) to Revision A (December 2025)	Page
• Updated *Applications* links	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added Pin Configuration and Functions section	2
• Added chip site origin (CSO) note to *Specification* section for clarity	3
• Removed separate Electrical Characteristics Table for Single Supply +5V Supply Range. Added relevant single supply parameters to the combined table	4
• Added additional test conditions on header and throughout table in *Electrical Characteristics* and *Typical Characteristics* for clarity	4
• Changed from *Offset Voltage vs Power Supply* to *Power-supply rejection ratio* for more clarity	4
• Added additional fabrication process specification for Power-Supply Rejection Ratio in *Electrical Characteristics* table	4
• Added test condition "T_A = –40°C to +85°C" for "Gain error vs temperature" in *Electrical Characteristics* and renamed to "Gain error drift" for clarity	4
• Added test condition "Continuous to VS / 2" to short-circuit current specification in *Electrical Characteristics* for clarity	4
• Added additional fabrication process specification for Short Circuit current in *Electrical Characteristics* table	4
• Added additional fabrication process specification for Bandwidth in *Electrical Characteristics* table	4
• Added additional fabrication process specification for 0.1% and 0.01% Settling Time in *Electrical Characteristics* table	4
• Changed overload recovery dual supply CSO:SHE specification from 21µs to 4µs to accurately reflect the specification in the *Electrical Characteristics* table	4
• Added additional fabrication process specification for Overload Recovery in *Electrical Characteristics* table	4
• Changed overload recovery for single supply from 13µs to 3µs to accurately reflect the specification in *Electrical Characteristics* table	4
• Moved power supply, operating and specification temperature range specifications from *Electrical Characteristics* to *Recommended Operating Conditions* table	4
• Added all chip site origin (CSO) to typical test conditions in *Typical Characteristics* section	6
• Added chip site origin (CSO) note to Gain vs Frequency, Common-Mode Rejection vs Frequency, Power-Supply Rejection vs Frequency, Short-Circuit Current vs Temperature, Output Voltage Swing vs R_L, Large-Signal Capacitive Load Response, and Overload Recovery Time in *Typical Characteristics* section	6
• Added additional fabrication process curve for Gain vs Frequency, Common-Mode Rejection vs Frequency, Power-Supply Rejection vs Frequency, Short-Circuit Current vs Temperature, Output Voltage Swing vs R_L, Large-Signal Capacitive Load Response, and Overload Recovery Time in *Typical Characteristics* section	6
• Updated *Application Information* verbiage for more clarity	12
• Added device nomenclature for chip site origin in *Device Support*	18

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA148UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA 148UA
INA148UA.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA 148UA
INA148UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA 148UA
INA148UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA 148UA
INA148UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA 148UA
INA148UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA 148UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF INA148 :

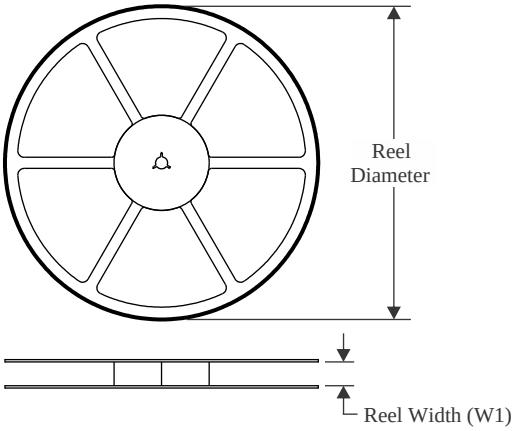
- Automotive : INA148-Q1

NOTE: Qualified Version Definitions:

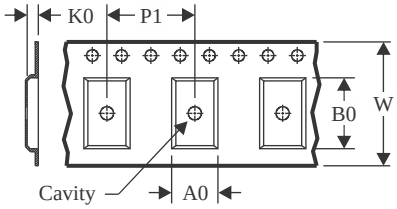
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

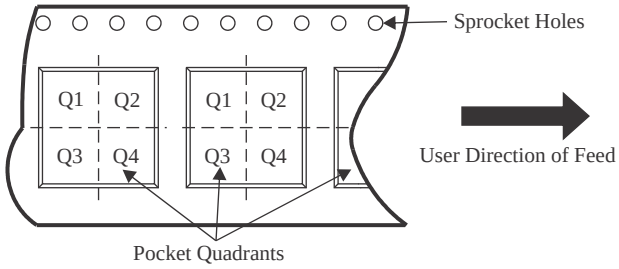


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

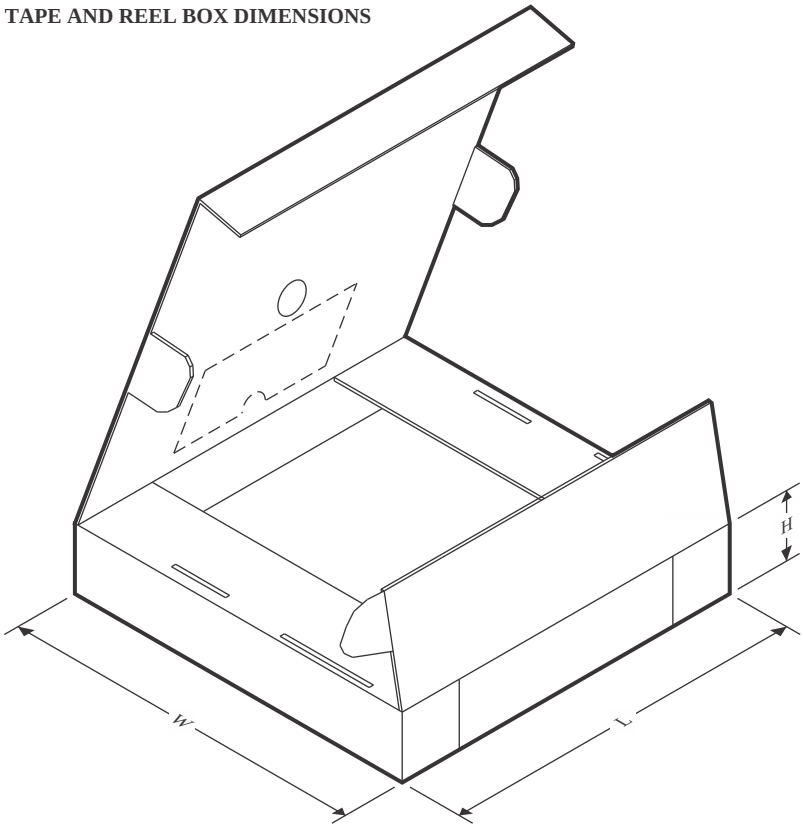
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA148UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

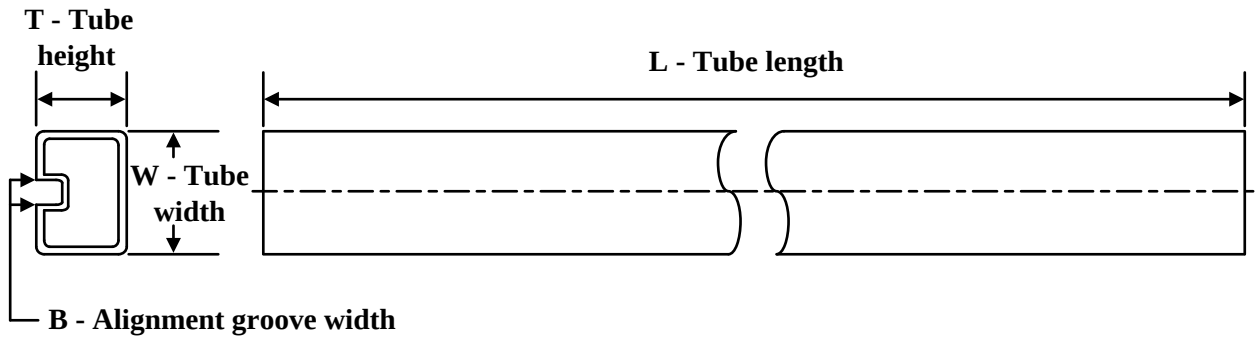
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA148UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA148UA	D	SOIC	8	75	506.6	8	3940	4.32
INA148UA.A	D	SOIC	8	75	506.6	8	3940	4.32
INA148UA.B	D	SOIC	8	75	506.6	8	3940	4.32

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