16-BIT, QUAD VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Low Power: 10 mW**
- **Unipolar or Bipolar Operation**
- **Settling Time: 10 µs to 0.003%**
- **15-Bit Linearity and Monotonicity: –40°C to 85°C**
- **Programmable Reset to Mid-Scale or Zero-Scale**
- **Double-Buffered Data Inputs**

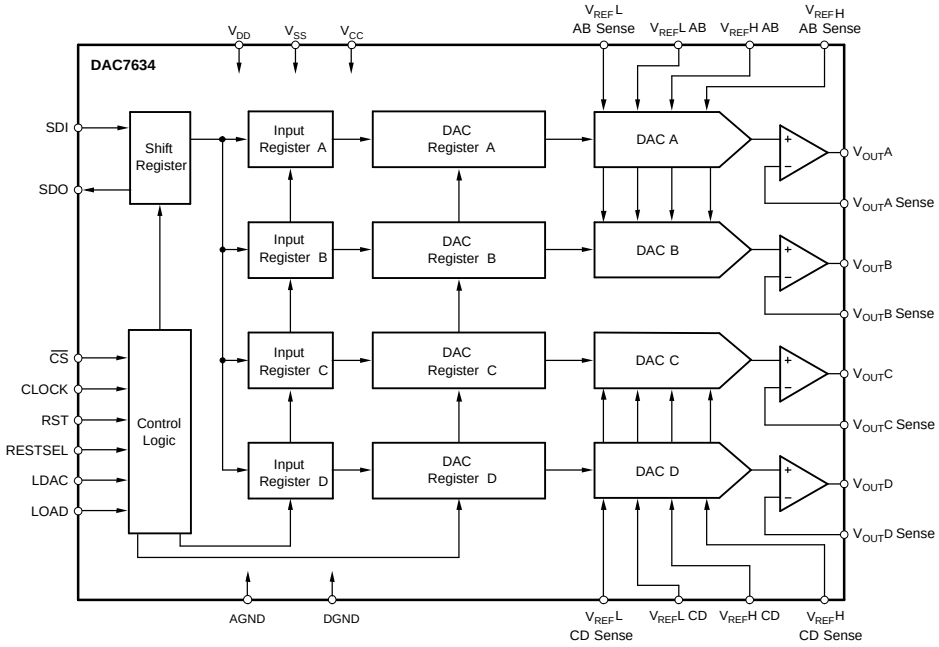
APPLICATIONS

- **Process Control**
- **Closed-Loop Servo-Control**
- **Motor Control**
- **Data Acquisition Systems**
- **DAC-Per-Pin Programmers**

DESCRIPTION

The DAC7634 is a 16-bit, quad voltage output, digital-to-analog converter with specified 15-bit monotonic performance over the specified temperature range. It accepts 24-bit serial input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a serial data output for daisy-chaining multiple DACs. Programmable asynchronous reset clears all registers to a mid-scale code of 8000_H or to a zero-scale of 0000_H. The DAC7634 can operate from a single 5-V supply or from 5-V and –5 V supplies.

Low power and small size per DAC make the DAC7634 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7634 is available in a 48-lead SSOP package and offers specifications over the –40°C to 85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

		UNIT
	V_{CC} and V_{DD} to V_{SS}	–0.3 V to 11 V
	V_{CC} and V_{DD} to GND	–0.3 V to 5.5 V
	$V_{REF}L$ to V_{SS}	–0.3 V to (V_{CC} - V_{SS})
	V_{CC} to $V_{REF}H$	–0.3 V to (V_{CC} - V_{SS})
	$V_{REF}H$ to $V_{REF}L$	–0.3 V to (V_{CC} - V_{SS})
	Digital input voltage to GND	–0.3 V to V_{DD} + 0.3 V
	Digital output voltage to GND	–0.3 V to V_{DD} + 0.3 V
T_J	Maximum junction temperature	150°C
T_A	Operating temperature range	–40°C to 85°C
T_{stg}	Storage temperature range	–65°C to 125°C
	Lead temperature (solder, 10s)	300°C

(1) Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

SPECIFICATIONS

At T_A = T_{MIN} to T_{MAX}, V_{DD} = V_{CC} = 5 V, V_{SS} = –5 V, $V_{REF}H$ = 2.5 V, and $V_{REF}L$ = –2.5 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	DAC7634E			DAC7634EB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity error			±3	±4		±2	±3	LSB
Linearity match			±4			±2		LSB
Differential linearity error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Bipolar zero error			±1	±2		±1	±2	mV
Bipolar zero error drift			5	10		5	10	ppm/°C
Full-scale error			±1	±2		±1	±2	mV
Full-scale error drift			5	10		5	10	ppm/°C
Bipolar zero matching	Channel-to-channel matching		±1	±2		±1	±2	mV
Full-scale matching	Channel-to-channel matching		±1	±2		±1	±2	mV
Power supply rejection ratio (PSRR)	At full scale		10	100		10	100	ppm/V

SPECIFICATIONS (continued)

At $T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = V_{CC} = 5$ V, $V_{SS} = -5$ V, $V_{REF}H = 2.5$ V, and $V_{REF}L = -2.5$ V, unless otherwise noted

PARAMETER	TEST CONDITIONS	DAC7634E			DAC7634EB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Voltage output	$V_{REF} = -2.5$ V, $R_L = 10$ kΩ, $V_{SS} = -5$ V	$V_{REF}L$		$V_{REF}H$	$V_{REF}L$		$V_{REF}H$	V
Output current		– 1.25		1.25	1.25		1.25	mA
Maximum load capacitance	No oscillation		500			500		pF
Short-circuit current			–10, 30			–10, +30		mA
Short-circuit duration	GND or V_{CC} or V_{SS}		Indefinite			Indefinite		
REFERENCE INPUT								
Ref high input voltage range		$V_{REF}L$ +1.25		2.5	$V_{REF}L$ +1.25		2.5	V
Ref low input voltage range		–2.5		$V_{REF}H$ – 1.25	–2.5		$V_{REF}H$ – 1.25	V
Ref high input current			500			500		µA
Ref low input current			–500			–500		µA
DYNAMIC PERFORMANCE								
Settling time	To ±0.003%, 5-V output step		8	10		8	10	µs
Channel-to-channel crosstalk	See Figure 5		0.5			0.5		LSB
Digital feedthrough			2			2		nV-s
Output noise voltage	f = 10 kHz		60			60		nV/√Hz
DAC glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			40		nV-s
DIGITAL INPUT								
V_{IH}		0.7 × V_{DD}			0.7 × V_{DD}			V
V_{IL}				0.3 × V_{DD}			0.3 × V_{DD}	V
I_{IH}				±10			±10	µA
I_{IL}				±10			±10	µA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = -0.8$ mA	3.6	4.5		3.6	4.5		V
V_{OL}	$I_{OL} = 1.6$ mA		0.3	0.4		0.3	0.4	V
POWER SUPPLY								
V_{DD}		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{CC}		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{SS}		–5.25	–5.0	–4.75	–5.25	–5.0	–4.75	V
I_{CC}			1.5	2		1.5	2	mA
I_{DD}			50			50		µA
I_{SS}		–2.3	–1.5		–2.3	–1.5		mA
Power			15	20		15	20	mW

SPECIFICATIONS

At $T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = V_{CC} = 5$ V, $V_{SS} = 0$ V, $V_{REF}H = 2.5$ V, and $V_{REF}L = 0$ V, unless otherwise noted

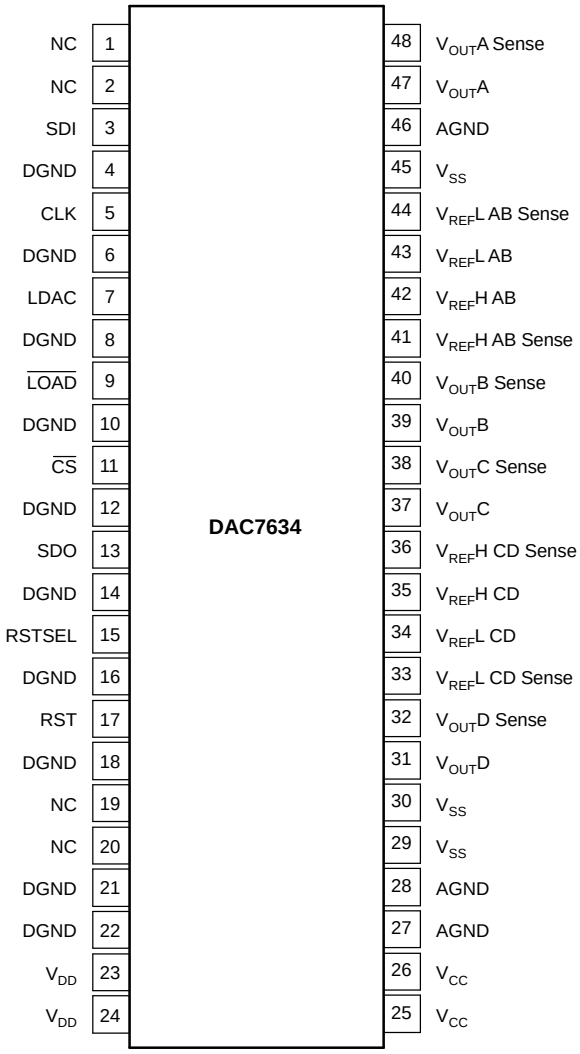
PARAMETER	TEST CONDITIONS	DAC7634E			DAC7634EB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity error(1)			±3	±4		±2	±3	LSB
Linearity match			±4			±2		LSB
Differential linearity error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Zero-scale error			±1	±2		±1	±2	mV
Zero-scale error drift			5	10		5	10	ppm/°C
Full-scale error			±1	±2		±1	±2	mV
Full-scale error drift			5	10		5	10	ppm/°C
Zero-scale matching	Channel-to-channel matching		±1	±2		±1	±2	mV
Full-scale matching	Channel-to-channel matching		±1	±2		±1	±2	mV
Power supply rejection ratio (PSRR)	At full scale		10	100		10	100	ppm/V
ANALOG INPUT								
Voltage output	$V_{REF}L$ = 0 V, V_{SS} = 0 V, R_L = 10 kΩ	0		$V_{REF}H$	0		$V_{REF}H$	V
Output current		– 1.25		1.25	–1.25		1.25	mA
Maximum load capacitance	No oscillation		500			500		pF
Short-circuit current			±30			±30		mA
Short-circuit duration	GND or V_{CC}		Indefinite			Indefinite		
REFERENCE INPUT								
Ref high input voltage range		$V_{REF}L$ +1.25		2.5	$V_{REF}L$ +1.25		2.5	V
Ref low input voltage range		0		$V_{REF}H$ –1.25	0		$V_{REF}H$ –1.25	V
Ref high input current			250			250		µA
Ref low input current			–250			–250		µA
DYNAMIC PERFORMANCE								
Settling time	To ±0.003%, 2.5-V output step		8	10		8	10	µs
Channel-to-channel crosstalk	See Figure 6		0.5			0.5		LSB
Digital feedthrough			2			2		nV-s
Output noise voltage	f = 10 kHz		60			60		nV/√Hz
DAC glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			40		nV-s
DIGITAL INPUT								
V_{IH}		0.7 × V_{DD}			0.7 × V_{DD}			V
V_{IL}				0.3 × V_{DD}			0.3 × V_{DD}	V
I_{IH}				±10			±10	µA
I_{IL}				±10			±10	µA
DIGITAL OUTPUT								
V_{OH}	I_{OH} = –0.8 mA	3.6	4.5		3.6	4.5		V
V_{OL}	I_{OL} = 1.6 mA		0.3	0.4		0.3	0.4	V
POWER SUPPLY								
V_{DD}		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{CC}		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{SS}		0	0	0	0	0	0	V
I_{CC}			1.5	2		1.5	2	mA
I_{DD}			50			50		µA
Power			7.5	10		7.5	10	mW

(1) If V_{SS} = 0 V specification applies at Code 0040_H and above due to possible negative zero-scale error.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	NC	No connection	25	V_{CC}	Analog +5-V power supply
2	NC	No connection	26	V_{CC}	Analog +5-V power supply
3	SDI	Serial data input	27	AGND	Analog ground
4	DGND	Digital ground	28	AGND	Analog ground
5	CLK	Data clock input	29	V_{SS}	Analog +5-V power supply or 0-V single supply
6	DGND	Digital ground	30	V_{SS}	Analog +5-V power supply or 0-V single supply
7	LDAC	DAC register load control, rising edge triggered	31	$V_{OUT}D$	DAC D output voltage
8	DGND	Digital ground	32	$V_{OUT}D$ Sense	DAC D's output amplifier inverting input. Used to close feedback loop at load.
9	$\overline{LOAD}$	DAC input register load control, active low	33	$V_{REF}L$ CD Sense	DAC C and D reference low sense input
10	DGND	Digital ground	34	$V_{REF}L$ CD	DAC C and D reference low input
11	$\overline{CS}$	Chip select, active low	35	$V_{REF}H$ CD	DAC C and D reference high input
12	DGND	Digital ground	36	$V_{REF}H$ CD Sense	DAC C and D reference high sense input
13	SDO	Serial data output	37	$V_{OUT}C$	DAC C output voltage
14	DGND	Digital ground	38	$V_{OUT}C$ Sense	DAC C's output amplifier inverting input. Used to close the feedback loop at the load.
15	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST common sets the DAC registers to mid-scale (8000_H). If LOW, a RST command sets the DAC registers to zero (0000_H).	39	$V_{OUT}B$	DAC B output voltage
16	DGND	Digital ground	40	$V_{OUT}B$ Sense	DAC B's output amplifier inverting input. Used to close the feedback loop at the load.
17	RST	Reset, rising edge triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.	41	$V_{REF}H$ AB Sense	DAC A and B reference high sense input
18	DGND	Digital ground	42	$V_{REF}H$ AB	DAC A and B reference high input
19	NC	No connection	43	$V_{REF}L$ AB	DAC A and B reference low input
20	NC	No connection	44	$V_{REF}L$ AB Sense	DAC A and B reference low sense input
21	DGND	Digital ground	45	V_{SS}	Analog –5-V power supply or 0-V single supply
22	DGND	Digital ground	46	AGND	Analog ground
23	V_{DD}	Digital 5-V power supply	47	$V_{OUT}A$	DAC A output voltage
24	V_{DD}	Digital 5-V power supply	48	$V_{OUT}A$ Sense	DAC A's output amplifier inverting input. Used to close the feedback loop at the load.

PIN CONFIGURATION



TYPICAL PERFORMANCE CURVES: V_{SS} = 0 V

At T_A = 25°C, V_{DD} = V_{CC} = 5 V, V_{REFH} = 2.5 V, V_{REFL} = 0 V, representative unit, unless otherwise specified.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC A, 25°C)

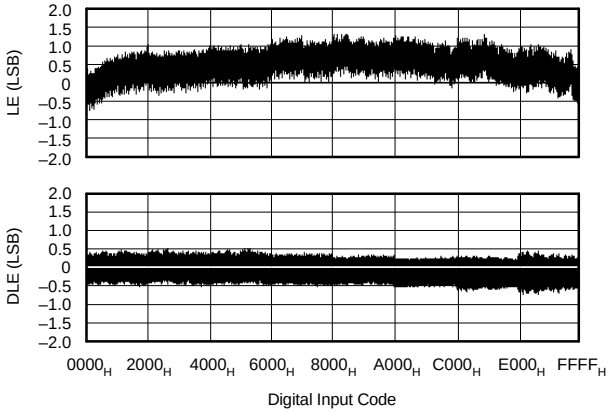


Figure 1.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC B, 25°C)

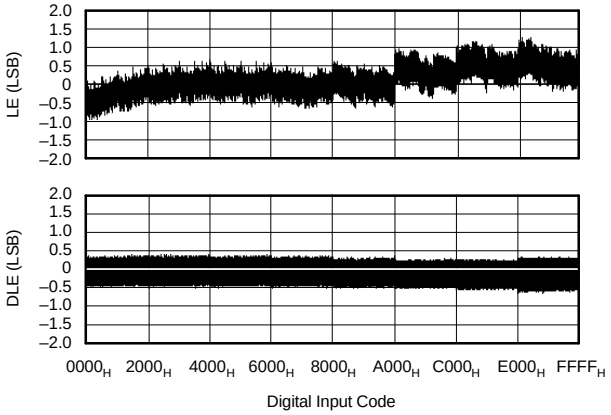


Figure 2.

LINEARY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC C, 25°C)

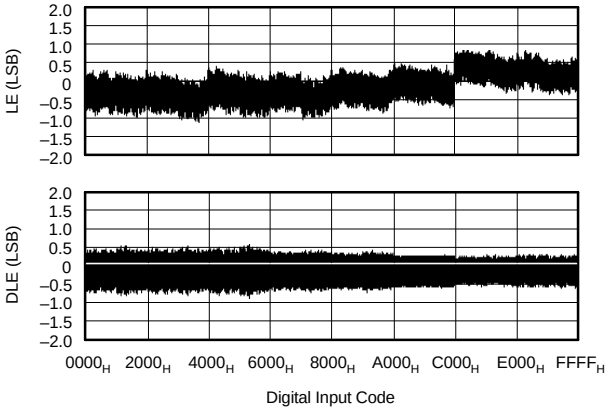


Figure 3.

LINEARY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, 25°C)

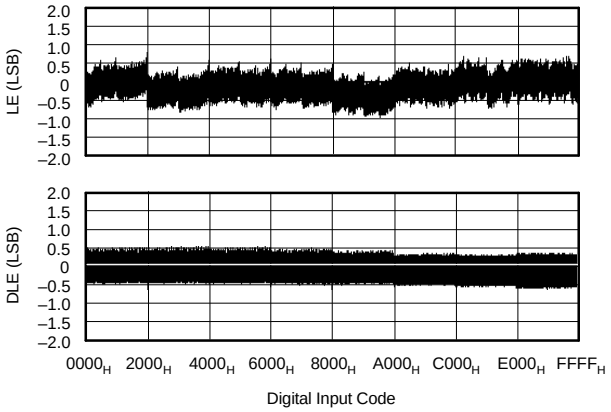


Figure 4.

TYPICAL PERFORMANCE CURVES: V_{SS} = 0 V (continued)

At T_A = 25°C, V_{DD} = V_{CC} = 5 V, V_{REFH} = 2.5 V, V_{REFL} = 0 V, representative unit, unless otherwise specified.

LINEARY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC A, 85°C)

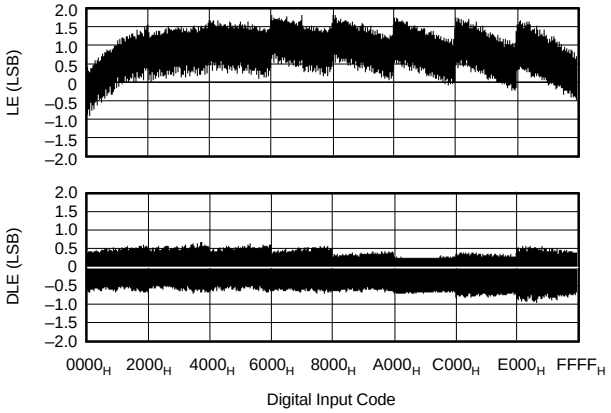


Figure 5.

LINEARY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC B, 85°C)

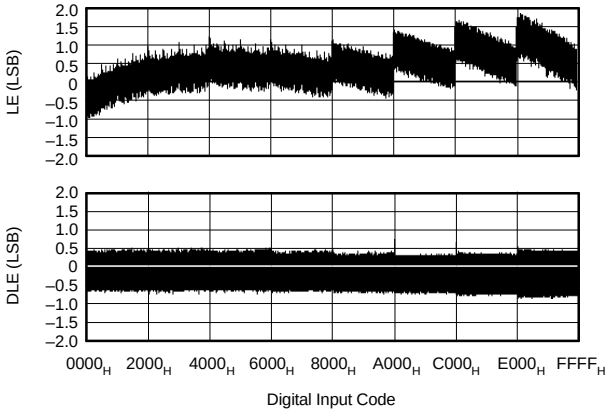


Figure 6.

LINEARY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC C, 85°C)

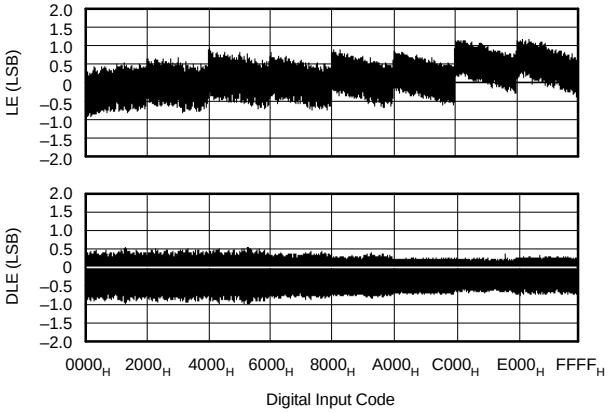


Figure 7.

LINEARY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, 85°C)

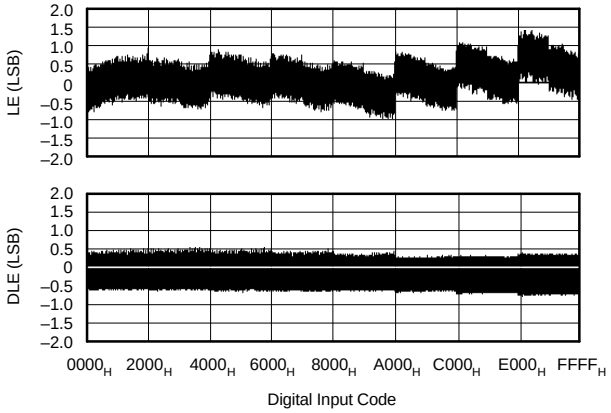


Figure 8.

TYPICAL PERFORMANCE CURVES: V_{SS} = 0 V (continued)

At T_A = 25°C, V_{DD} = V_{CC} = 5 V, V_{REFH} = 2.5 V, V_{REFL} = 0 V, representative unit, unless otherwise specified.

LINEARY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC A, –40°C)

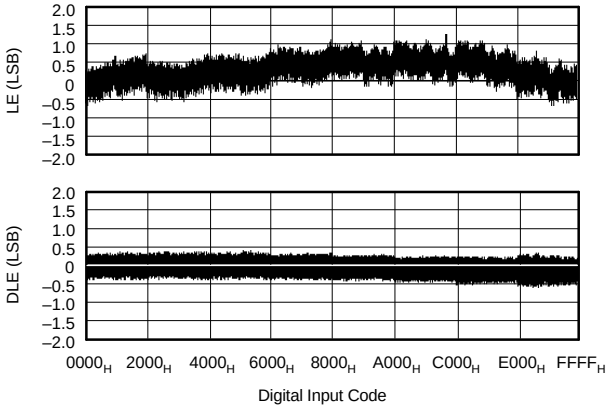


Figure 9.

LINEARY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC B, –40°C)

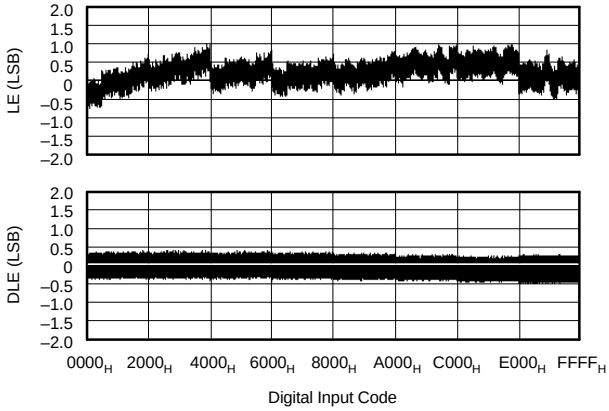


Figure 10.

LINEARY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC C, –40°C)

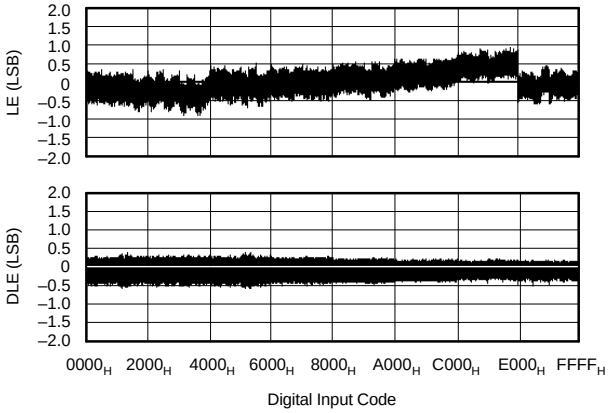


Figure 11.

LINEARY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, –40°C)

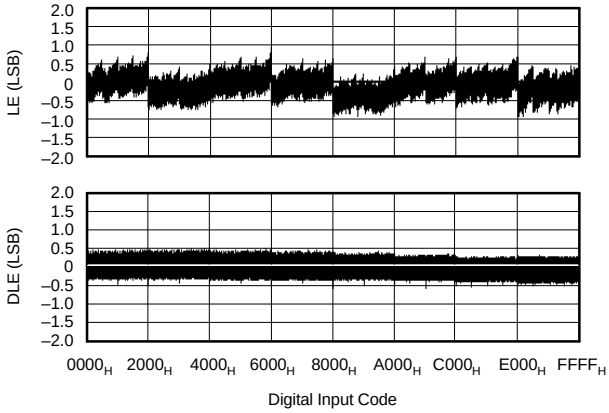


Figure 12.

ZERO-SCALE ERROR vs TEMPERATURE

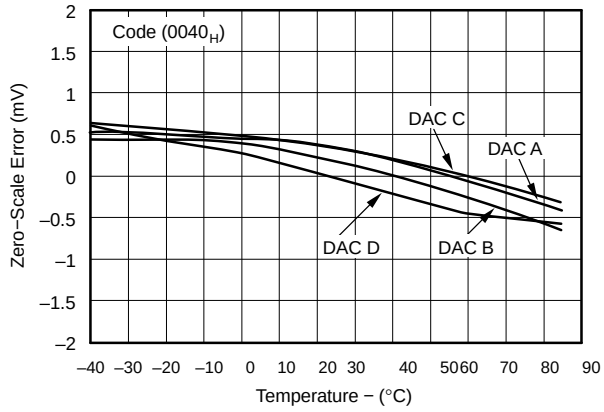


Figure 13.

FULL-SCALE ERROR vs TEMPERATURE

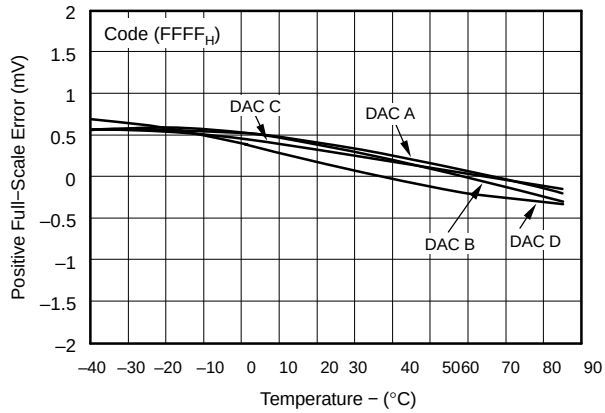


Figure 14.

TYPICAL PERFORMANCE CURVES: V_{SS} = 0 V (continued)

At T_A = 25°C, V_{DD} = V_{CC} = 5 V, V_{REFH} = 2.5 V, V_{REFL} = 0 V, representative unit, unless otherwise specified.

V_{REFH} CURRENT vs CODE (ALL DACs SENT TO INDICATED CODE)

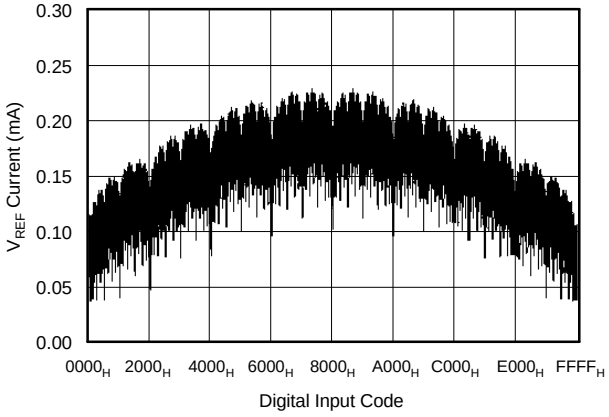


Figure 15.

V_{REFL} CURRENT vs CODE (ALL DACs SENT TO INDICATED CODE)

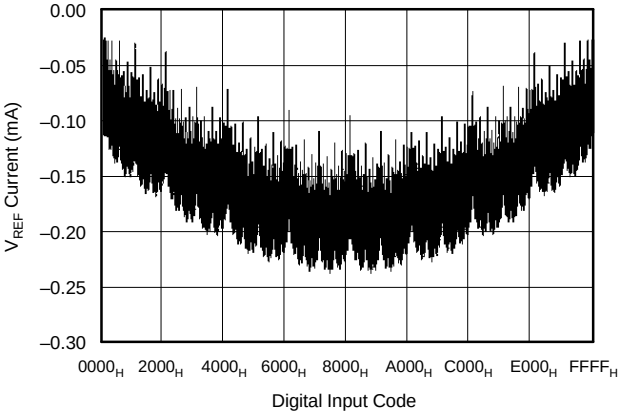


Figure 16.

POWER SUPPLY CURRENT vs TEMPERATURE

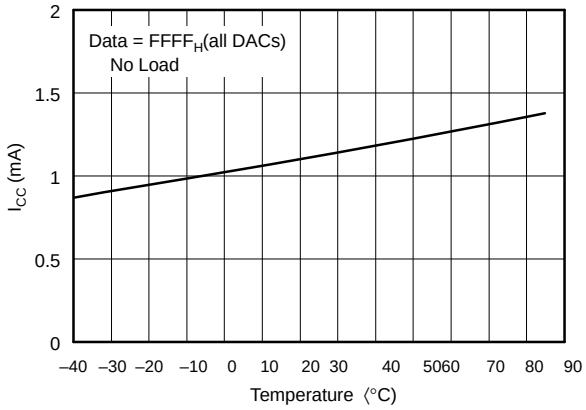


Figure 17.

POSITIVE SUPPLY CURRENT vs DIGITAL INPUT CODE

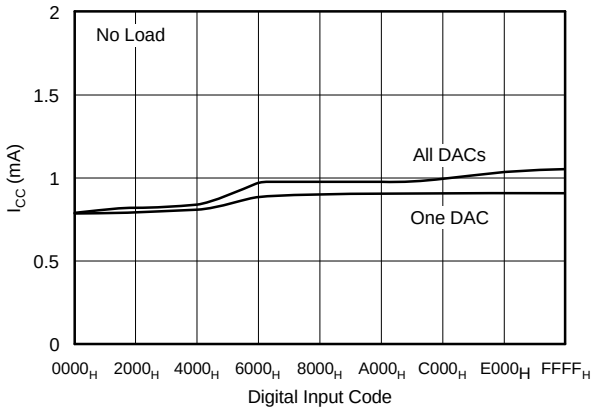


Figure 18.

OUTPUT VOLTAGE vs SETTLING TIME (0 V TO 2.5 V)

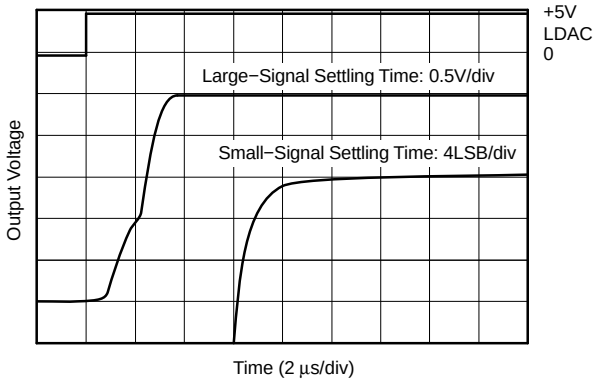


Figure 19.

OUTPUT VOLTAGE vs SETTLING TIME (2.5 V TO 2 mV)

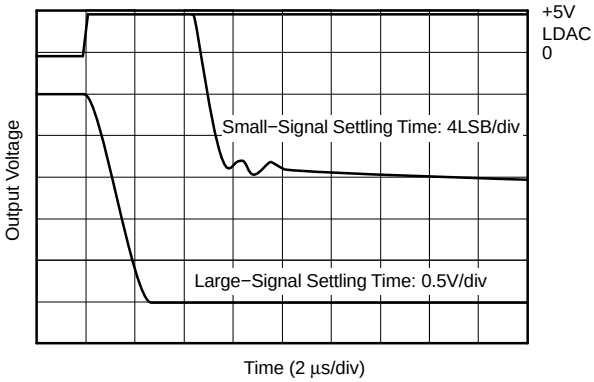


Figure 20.

TYPICAL PERFORMANCE CURVES: V_{SS} = 0 V (continued)

At T_A = 25°C, V_{DD} = V_{CC} = 5 V, V_{REFH} = 2.5 V, V_{REFL} = 0 V, representative unit, unless otherwise specified.

OUTPUT VOLTAGE vs MIDSCALE GLITCH PERFORMANCE

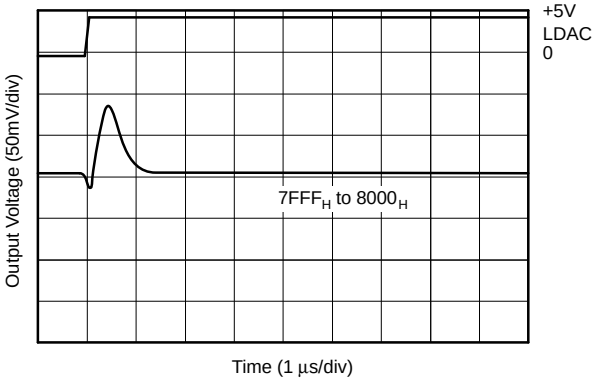


Figure 21.

OUTPUT VOLTAGE vs MIDSCALE GLITCH PERFORMANCE

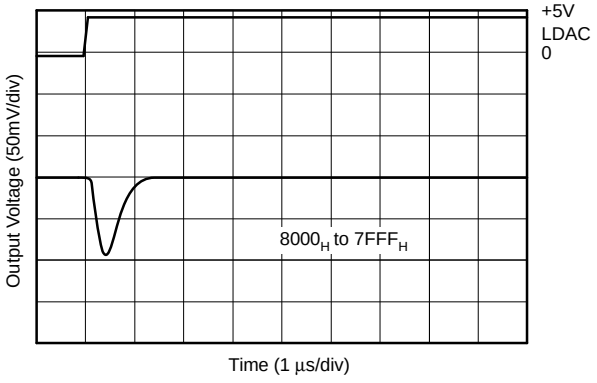


Figure 22.

BROADBAND NOISE

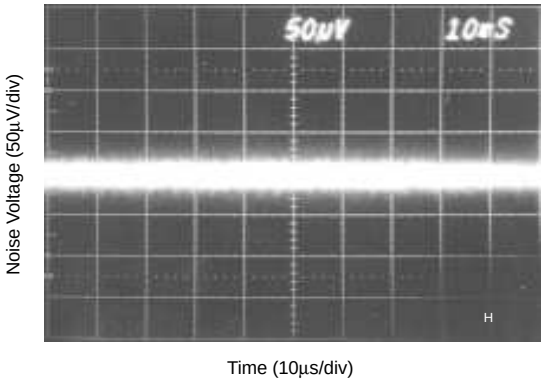


Figure 23.

OUTPUT NOISE VOLTAGE vs FREQUENCY

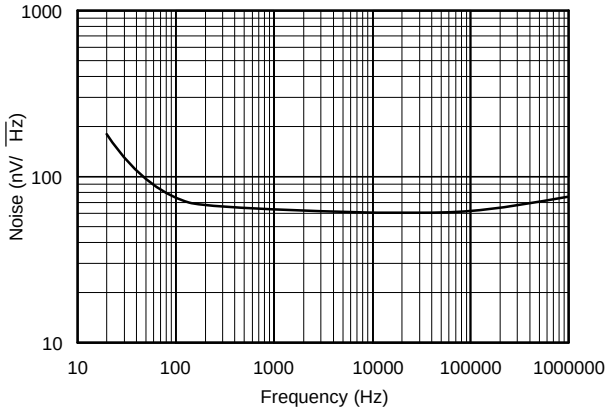


Figure 24.

V_{OUT} vs R_{LOAD}

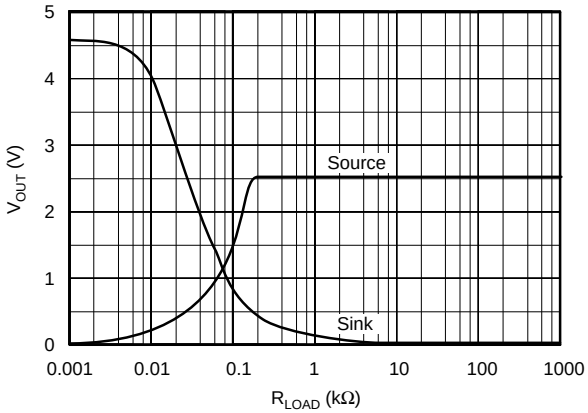


Figure 25.

TYPICAL PERFORMANCE CURVES: V_{SS} = –5 V

At T_A = 25°C, V_{DD} = V_{CC} = 5 V, V_{REFH} = 2.5 V, V_{REFL} = 0 V, representative unit, unless otherwise specified.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC A, 25°C)

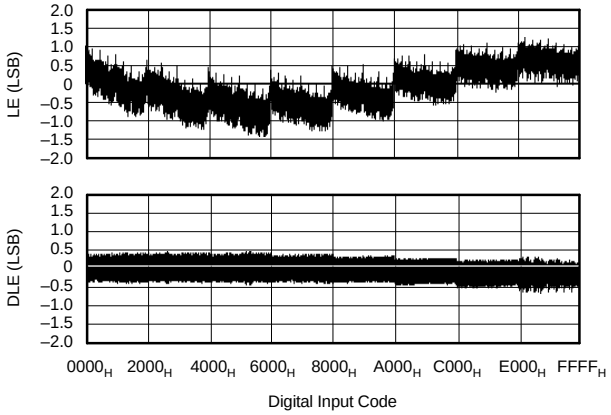


Figure 26.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC B, 25°C)

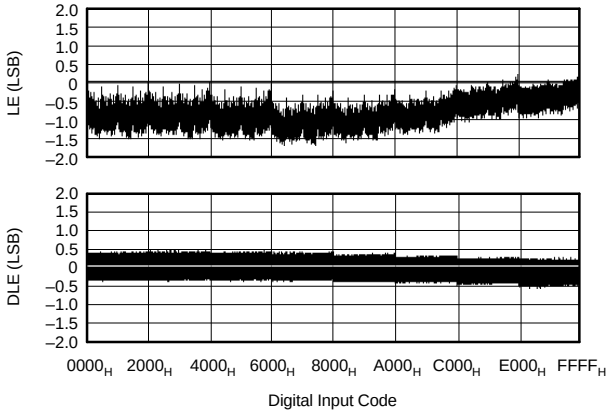


Figure 27.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC C, 25°C)

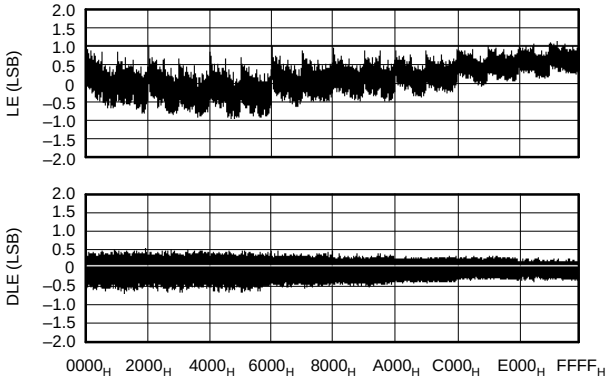


Figure 28.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, 25°C)

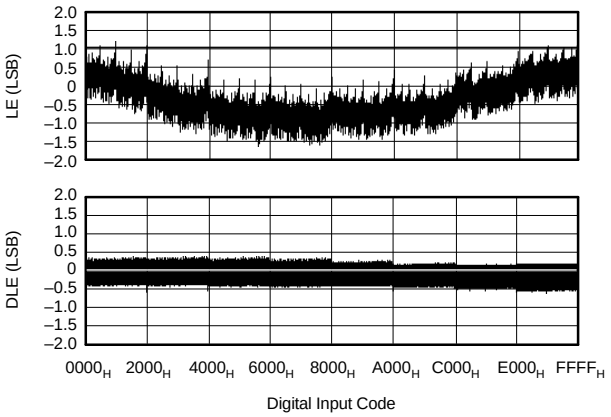


Figure 29.

TYPICAL PERFORMANCE CURVES: V_{SS} = –5 V (continued)

At T_A = 25°C, V_{DD} = V_{CC} = 5 V, V_{REFH} = 2.5 V, V_{REFL} = 0 V, representative unit, unless otherwise specified.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC A, 85°C)

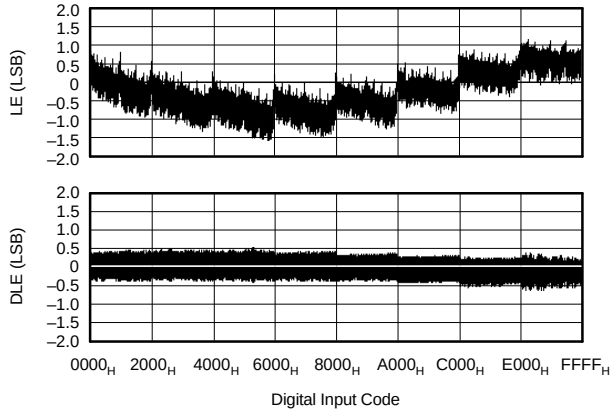


Figure 30.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC B, 85°C)

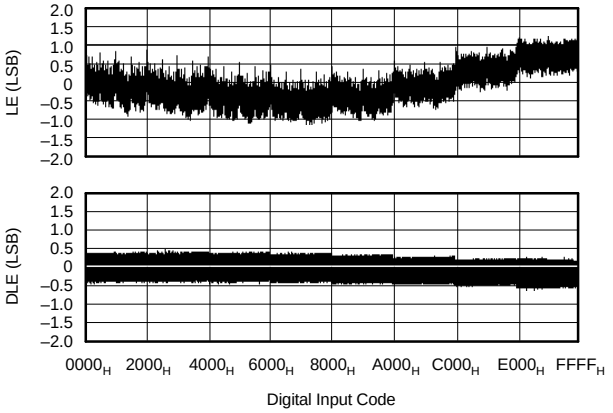


Figure 31.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC C, 85°C)

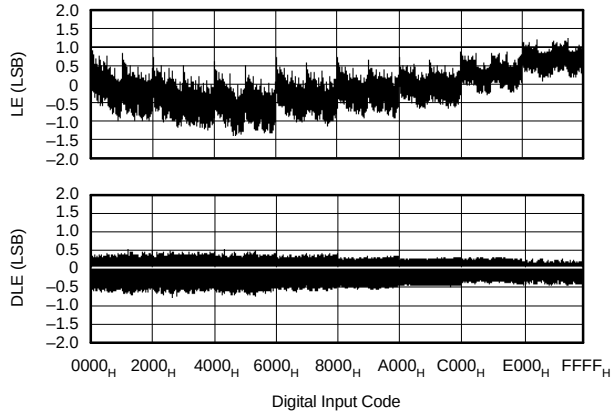


Figure 32.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, 85°C)

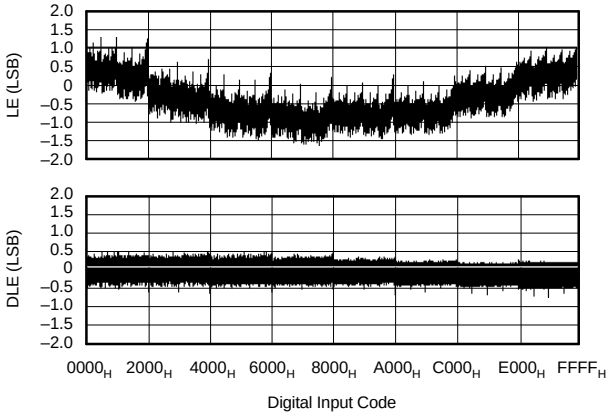


Figure 33.

TYPICAL PERFORMANCE CURVES: V_{SS} = –5 V (continued)

At T_A = 25°C, V_{DD} = V_{CC} = 5 V, V_{REFH} = 2.5 V, V_{REFL} = 0 V, representative unit, unless otherwise specified.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC A, –40°C)

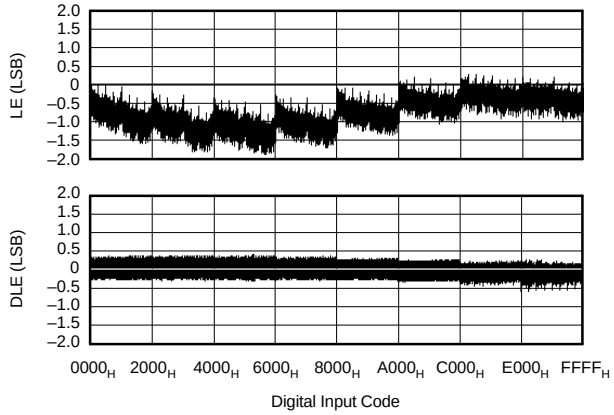


Figure 34.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC B, –40°C)

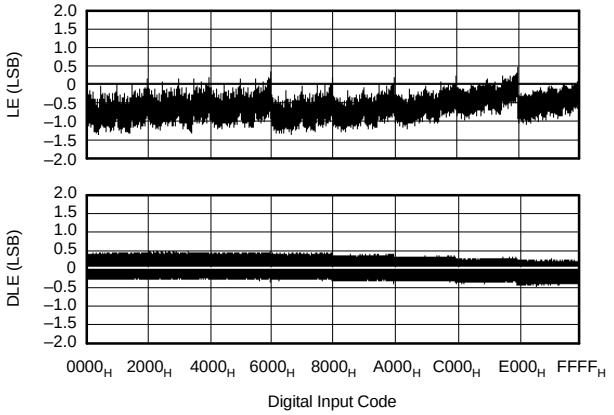


Figure 35.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC C, –40°C)

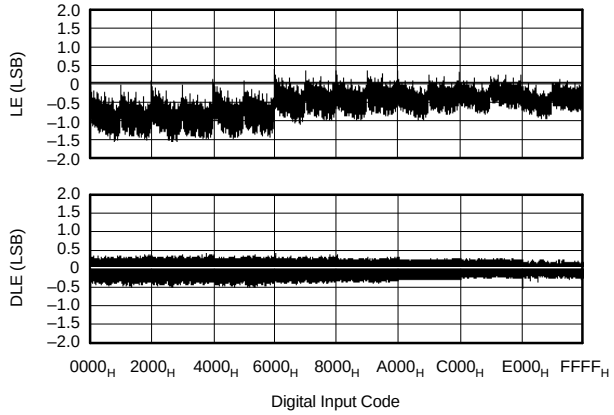


Figure 36.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, –40°C)

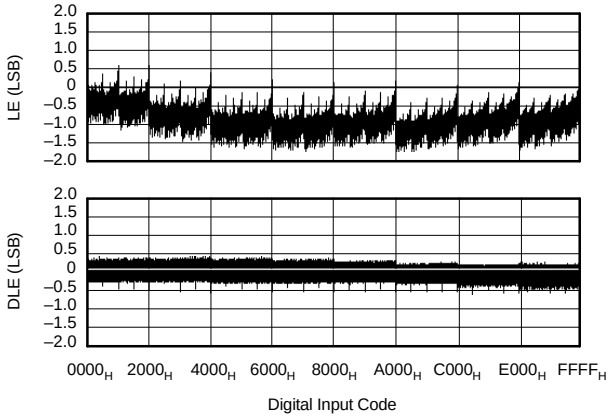


Figure 37.

TYPICAL PERFORMANCE CURVES: V_{SS} = –5 V (continued)

At T_A = 25°C, V_{DD} = V_{CC} = 5 V, V_{REFH} = 2.5 V, V_{REFL} = 0 V, representative unit, unless otherwise specified.

V_{REFH} CURRENT vs CODE (ALL DACs SENT TO INDICATED CODE)

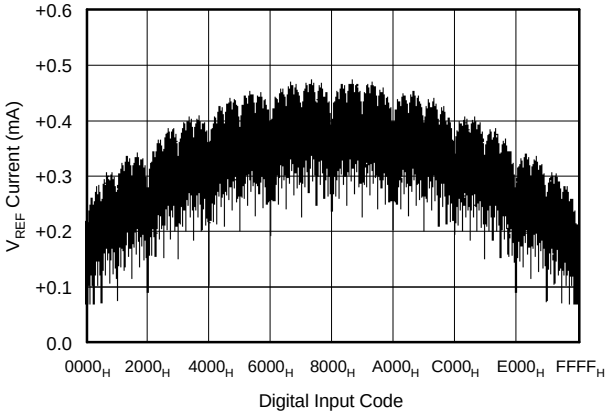


Figure 38.

V_{REFl} CURRENT vs CODE (ALL DACs SENT TO INDICATED CODE)

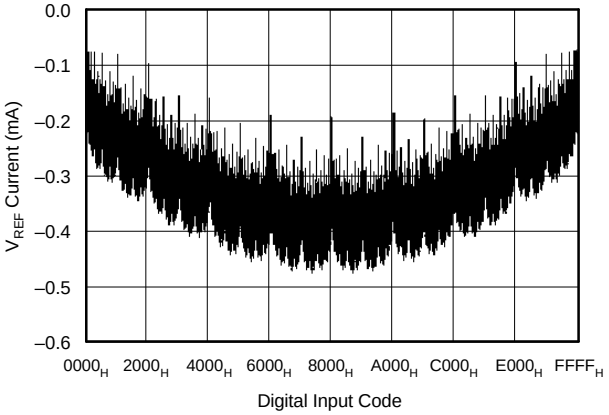


Figure 39.

ZERO-SCALE ERROR vs TEMPERATURE (Code 8000_H)

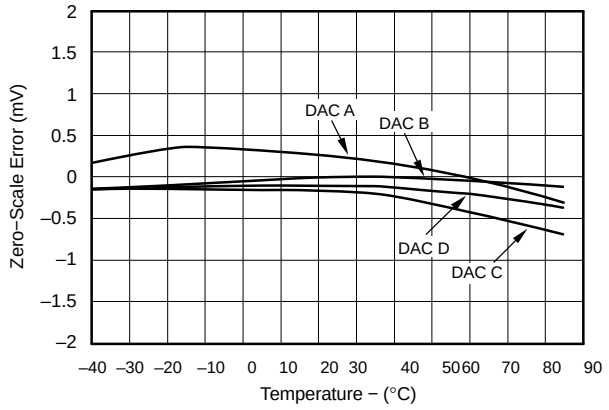


Figure 40.

POSITIVE FULL-SCALE ERROR vs TEMPERATURE (Code $FFFF_H$)

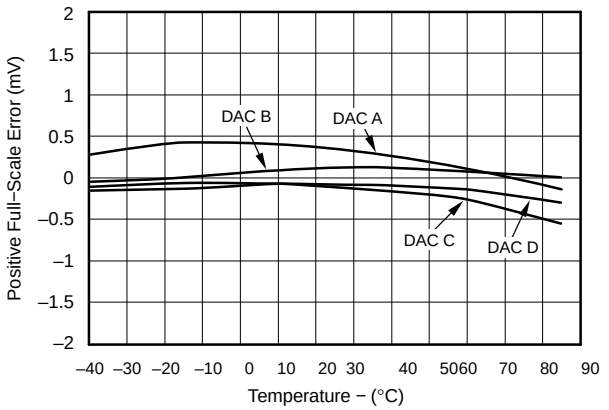


Figure 41.

NEGATIVE FULL-SCALE ERROR vs TEMPERATURE (Code 0000_H)

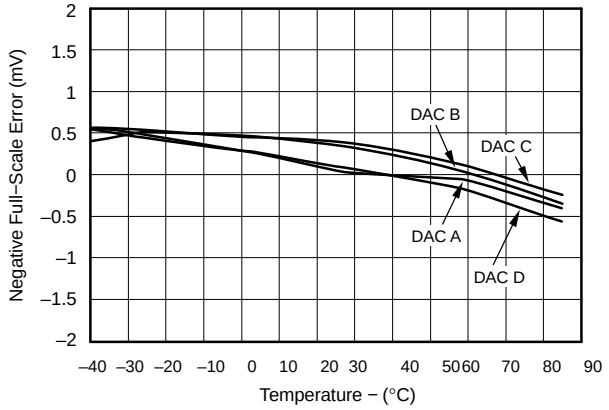


Figure 42.

POWER SUPPLY CURRENT vs TEMPERATURE

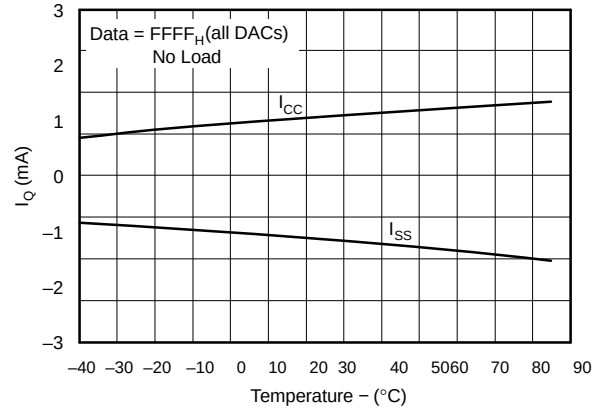


Figure 43.

TYPICAL PERFORMANCE CURVES: V_{SS} = –5 V (continued)

At T_A = 25°C, V_{DD} = V_{CC} = 5 V, V_{REFH} = 2.5 V, V_{REFL} = 0 V, representative unit, unless otherwise specified.

V_{OUT} vs R_{LOAD}

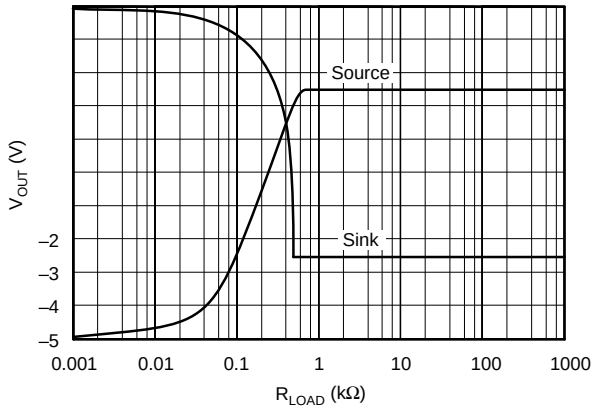


Figure 44.

POSITIVE SUPPLY CURRENT vs DIGITAL INPUT CODE

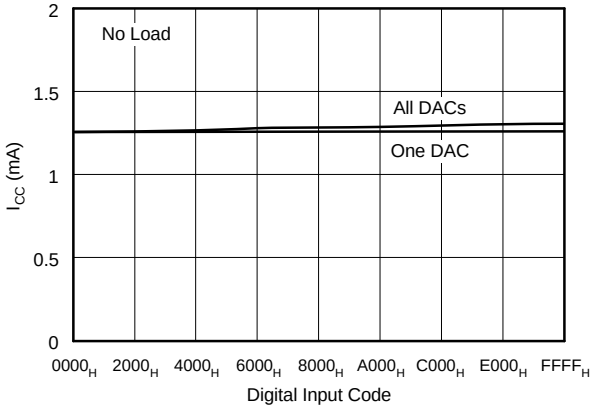


Figure 45.

OUTPUT VOLTAGE vs SETTLING TIME (–2.5 V TO 2.5 V)

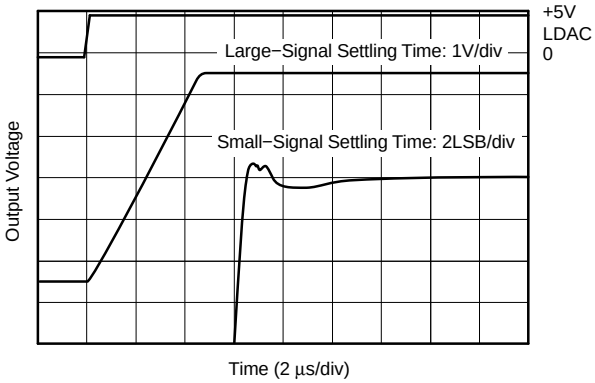


Figure 46.

OUTPUT VOLTAGE vs SETTLING TIME (2.5 V TO –2.5 V)

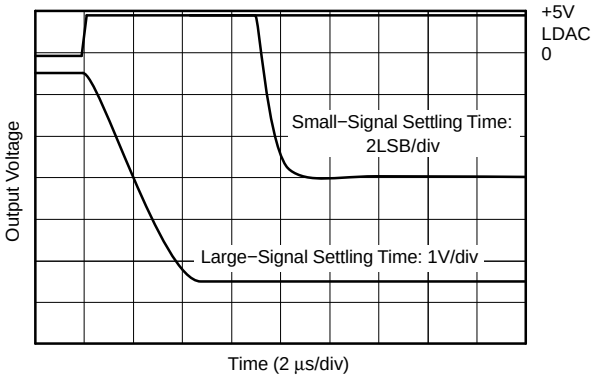


Figure 47.

THEORY OF OPERATION

The DAC7634 is a quad voltage output, 16-bit digital-to-analog converter (DAC). The architecture is an R-2R ladder configuration with the three MSBs segmented, followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs, and output operational amplifier, as shown in Figure 48. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the external voltage references (V_{REF}L and V_{REF}H, respectively).

The digital input is a 24-bit serial word that contains a 2-bit address code for selecting one of four DACs, a quick load bit, five unused bits, and the 16-bit DAC code (MSB first). The converters can be powered from either a single 5-V supply or a dual ±5-V supply. The device offers a reset function which immediately sets all DAC output voltages and DAC registers to mid-scale code 8000_H or to zero-scale, code 0000_H. See Figure 49 and Figure 50 for the basic operation of the DAC7634.

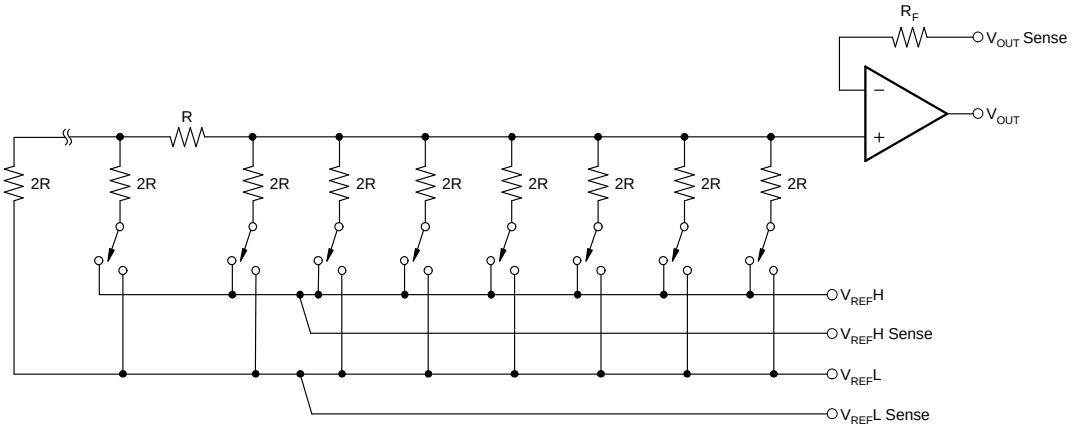


Figure 48. DAC7634 Architecture

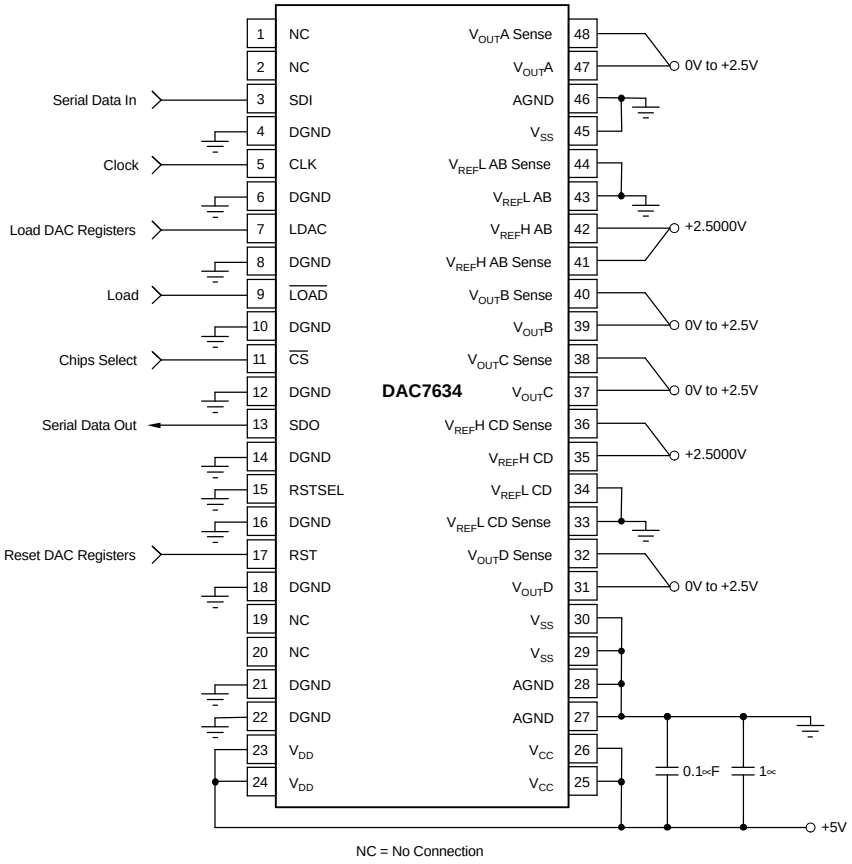


Figure 49. Basic Single-Supply Operation of the DAC7634

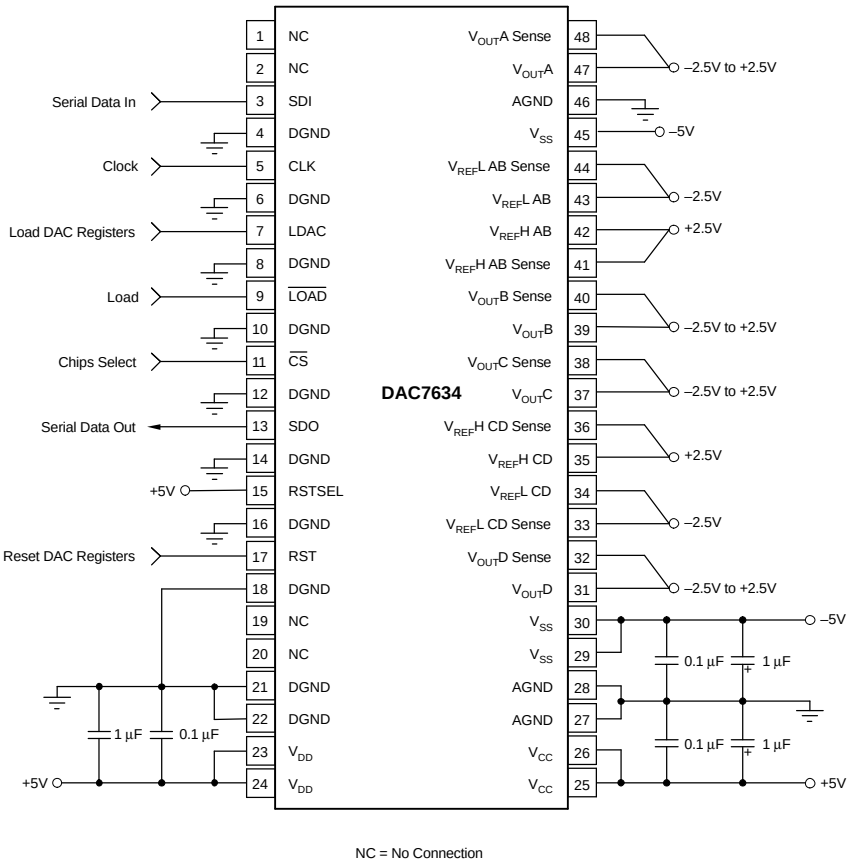


Figure 50. Basic Dual-Supply Operation of the DAC7634

ANALOG OUTPUTS

When V_{SS} = –5V (dual supply operation), the output amplifier can swing to within 2.25 V of the supply rails, specified over the –40°C to 85°C temperature range. When V_{SS} = 0 V (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when V_{SS} = 0 V. Because the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H, 0001_H, 0002_H, etc.) if the output amplifier has a negative offset. At the negative limit of –2 mV, the first specified output starts at code 0040_H.

Due to the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become important. A 16-bit converter with a 2.5 V full-scale range has a 1-LSB value of 38 µV. With a load current of 1 mA, series wiring and connector resistance of only 40 mΩ (R_{W2}) causes a voltage drop of 40 µV, as shown in Figure 51. To understand what this means in terms of a system layout, the resistivity of a typical 1-ounce copper-clad printed-circuit board is 1.2 mΩ per square. For a 1-mA load, a 10-mil wide printed-circuit conductor 600 mil long results in a voltage drop of 30 µV.

The DAC7634 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 51), thus ensuring an accurate output voltage.

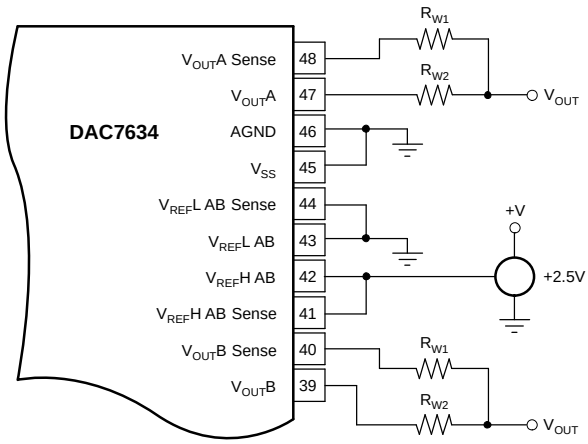


Figure 51. Analog Output Closed-Loop Configuration(1/2 DAC7634) (R_W Represents Wiring Resistances)

REFERENCE INPUTS

The reference inputs, $V_{REF}L$ and $V_{REF}H$, can be any voltage between VSS + 2.5 V and VCC – 2.5 V, provided that $V_{REF}H$ is at least 1.25 V greater than $V_{REF}L$. The minimum output of each DAC is equal to $V_{REF}L$ plus a small offset voltage (essentially, the offset of the output operational amp). The maximum output is equal to $V_{REF}H$ plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –4.75 V to –5.25 V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not specified.

The current into the $V_{REF}H$ input and out of $V_{REF}L$ depends on the DAC output voltages, and can vary from a few microamps to approximately 0.5 mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC7634 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figure 52 through Figure 60 show different reference configurations, and the effect on the linearity and differential linearity.

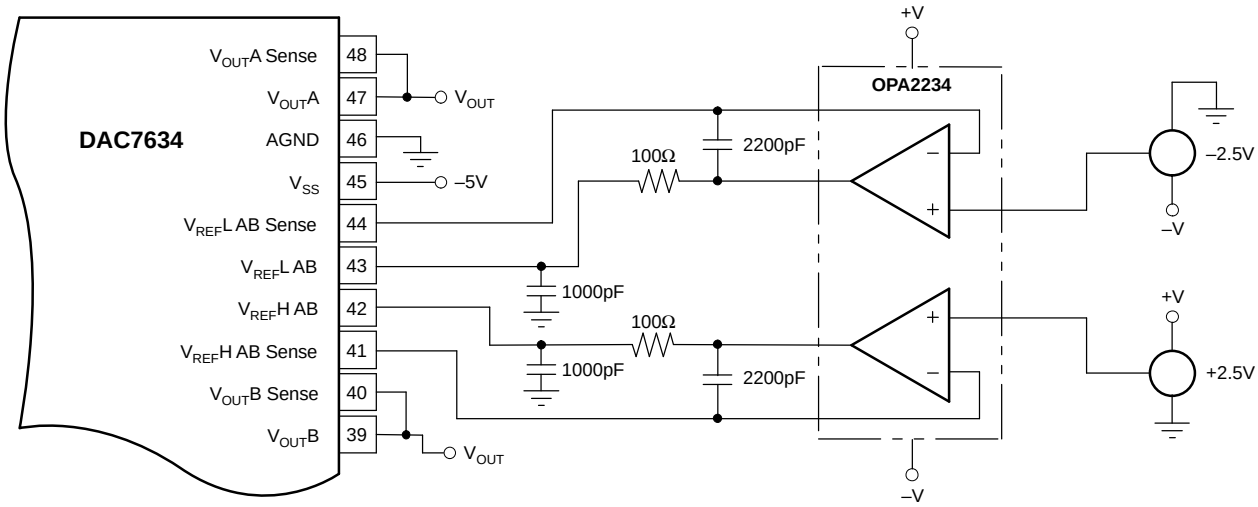
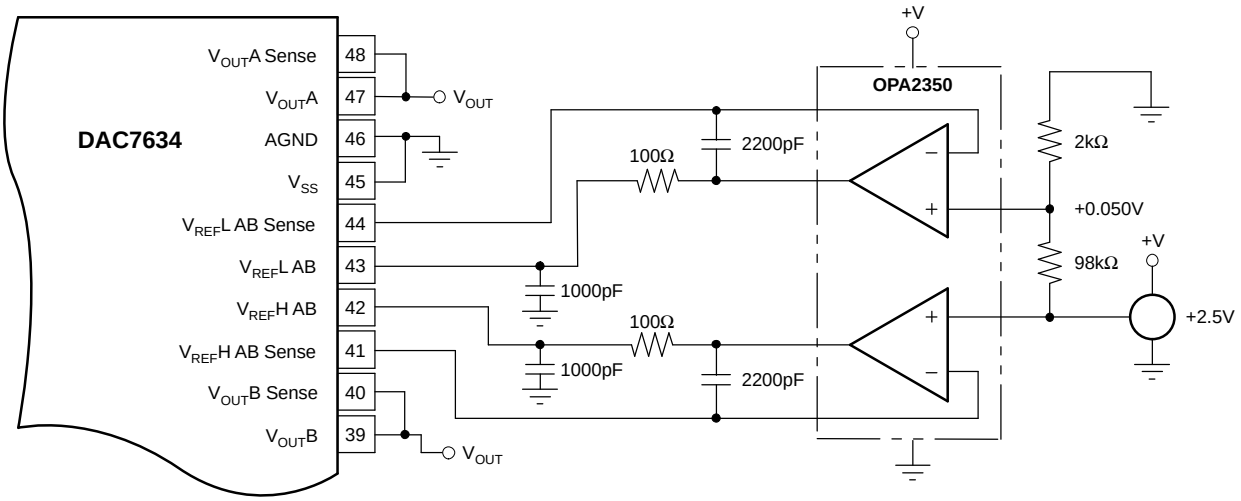


Figure 52. Dual Supply Configuration-Buffered References, Used for Dual Supply Performance



NOTE: $V_{REF}L$ has been chosen to be 50 mV to allow for current sinking voltage drops across the 100-Ω resistor and the output stage of the buffer operational amplifier.

Figure 53. Single-Supply Buffered Reference With a Reference Low of 50 mV (1/2 DAC7634)

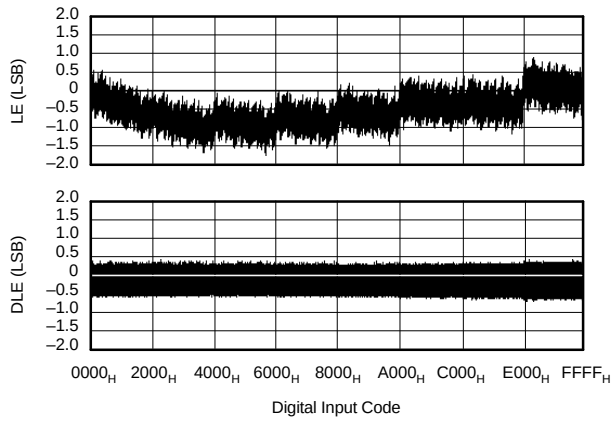


Figure 54. Integral Linearity and Differential Linearity Error Curves for Figure 53

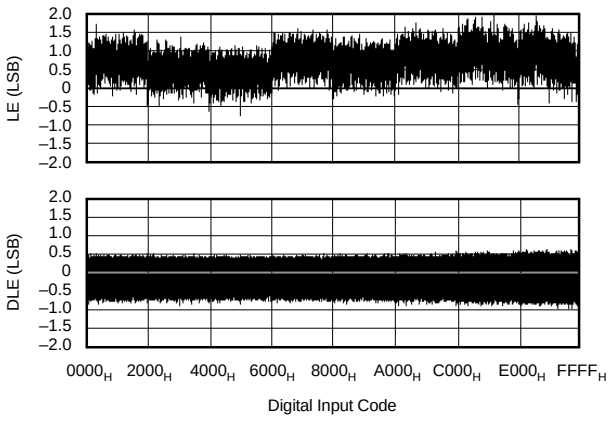


Figure 55. Integral Linearity and Differential Linearity Error Curves for Figure 56

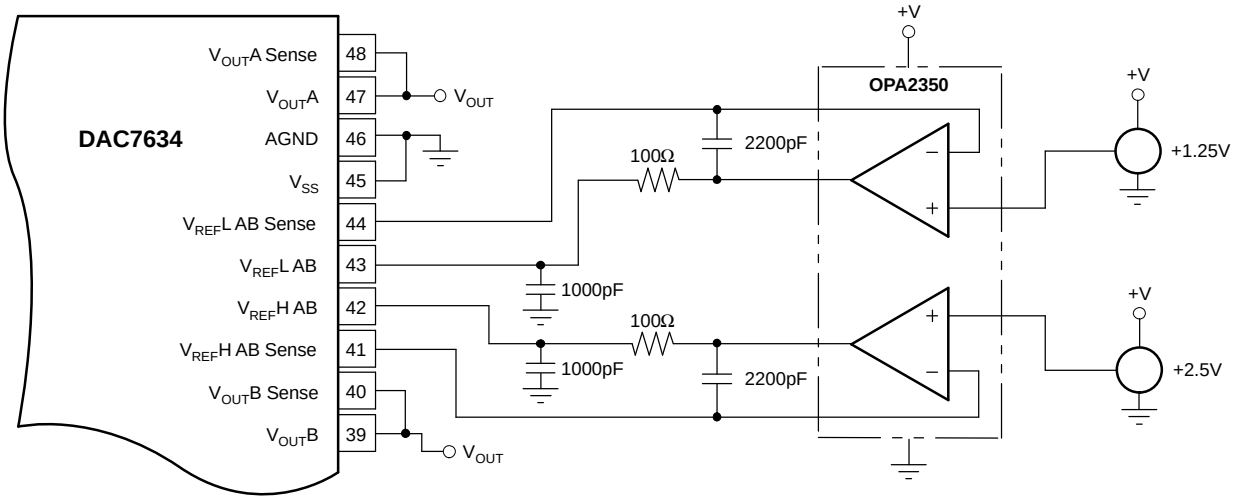


Figure 56. Single-Supply Buffered Reference With $V_{REF}L$ = 1.25 V and $V_{REF}H$ = 2.5 V (1/2 DAC7634)

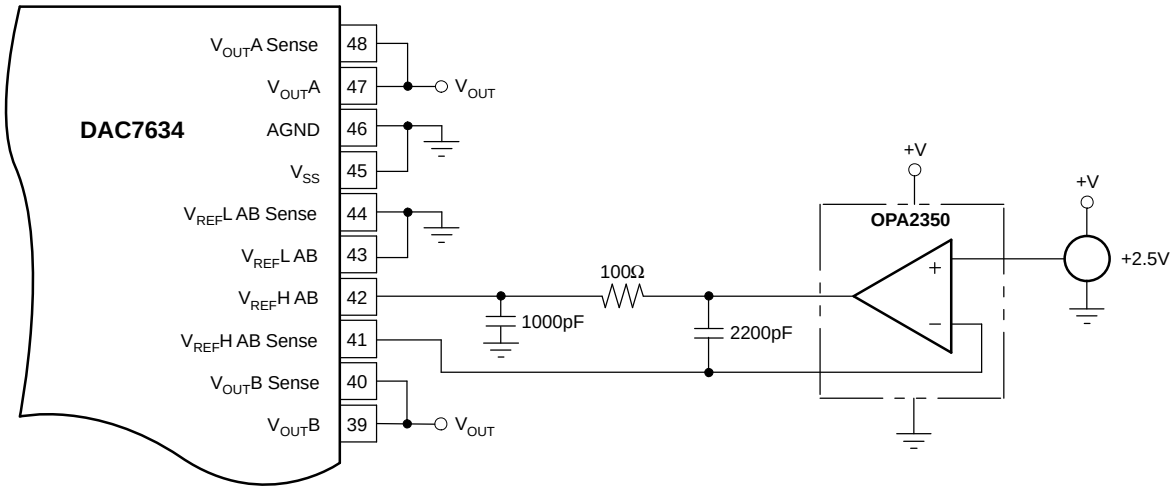


Figure 57. Single-Supply Buffered $V_{REF}H$ (1/2 DAC7634)

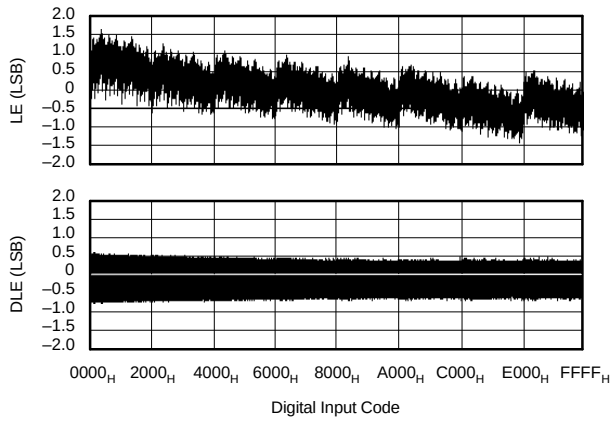


Figure 58. Linearity and Differential Linearity Error Curves for Figure 57

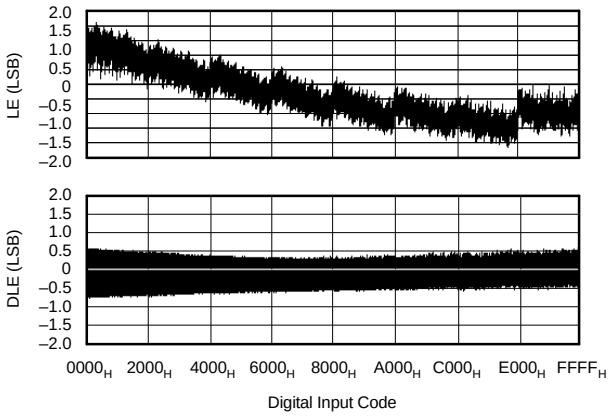


Figure 59. Linearity and Differential Linearity Error Curves for Figure 60

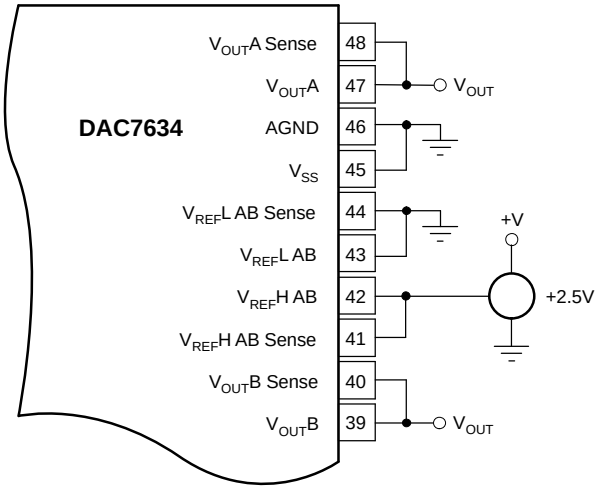


Figure 60. Low Cost Single-Supply Configuration

DIGITAL INTERFACE

Table 1 shows the basic control logic for the DAC7634. The interface consists of a signal data clock (CLK) input, serial data (SDI), DAC input register load control signal ($\overline{LOAD}$), and DAC register load control signal (LDAC). In addition, a chip select ($\overline{CS}$) input is available to enable serial communication when there are multiple serial devices. An asynchronous reset (RST) input, by the rising edge, is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state, depending on the status of the reset select (RSTSEL) signal.

The DAC code, quick load control, and address are provided via a 24-bit serial interface (see Figure 15). The first two bits select the input register that is updated when $\overline{LOAD}$ goes LOW. The third bit is a *Quick Load* bit such that if HIGH, the code in the shift register is loaded into ALL DAC's input register when $\overline{LOAD}$ signal goes LOW. If the *Quick Load* bit is LOW, the content of shift register is loaded only to the DAC input register that is addressed. The *Quick Load* bit is followed by five unused bits. The last sixteen bits (MSB first) are the DAC code.

SERIAL DATA INPUT

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	QUICK LOAD	X	X	X	X	X	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 1. DAC7634 Logic Truth Table(1)

A1	A0	$\overline{CS}$	RST	RSTSEL	LDAC	$\overline{LOAD}$	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	H	X	X	L	Write	Hold	Write Input	A
L	H	L	H	X	X	L	Write	Hold	Write Input	B
H	L	L	H	X	X	L	Write	Hold	Write Input	C
H	H	L	H	X	X	L	Write	Hold	Write Input	D
X	X	H	H	X	↑	H	Hold	Write	Update	All
X	X	H	H	X	H	H	Hold	Hold	Hold	All
X	X	X	↑	L	X	X	Reset to Zero	Reset to Zero	Reset to Zero	All
X	X	X	↑	H	X	X	Reset to Midscale	Reset to Midscale	Reset to Midscale	All

(1) If the DAC7634 is the only device on the serial bus, the $\overline{CS}$ pin can be connected to DGND permanently, which enables the shift register all the time. In this case, only the CLK operates the serial shift register and all other functions listed in Table 1 should be followed as shown. The DAC updates on the rising edge of LDAC.

The internal DAC register is edge-triggered and not level-triggered. When the LDAC signal is transitioned from LOW to HIGH, the digital word currently in the DAC input register is latched. The first set of registers (the DAC input registers) are level-triggered via the $\overline{LOAD}$ signal. This double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. When the new data has been entered into the device, all of the DAC outputs can be updated simultaneously by the rising edge of LDAC. Additionally, it allows the DAC input registers to be written to at any point, then the DAC output voltages can be synchronously changed via a trigger signal (LDAC).

Note that $\overline{CS}$ and CLK are combined with an OR gate, which controls the serial-to-parallel shift register. These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when $\overline{CS}$ rises at the end of a serial transfer. If CLK is LOW when $\overline{CS}$ rises, the OR gate provides a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register(s). If both $\overline{CS}$ and CLK are used, $\overline{CS}$ should rise only when CLK is HIGH. If not, then either $\overline{CS}$ or CLK can be used to operate the shift register. See Table 2 for more information.

SERIAL-DATA OUTPUT

Table 2. Serial Shift Register Truth Table

$\overline{CS}$ (1)	CLK(1)	$\overline{LOAD}$	RST	SERIAL SHIFT REGISTER
H(2)	X(3)	H	H	No Change
L(4)	L	H	H	No Change
L	↑(5)	H	H	Advanced One Bit
↑	L	H	H	Advanced One Bit
H(6)	X	L(7)	H	No Change
H(6)	X	H	↑(8)	No Change

(1) $\overline{CS}$ and CLK are interchangeable.
(2) H = Logic HIGH
(3) X = Don't Care
(4) L = Logic LOW
(5) Positive logic transition
(6) A HIGH value is suggested in order to avoid a *false clock* from advancing the shift register and changing the shift register.
(7) If data is clocked into the serial register while $\overline{LOAD}$ is LOW, the selected DAC register changes as the shift register bits *flow* through A1 and A0. This corrupts the data in each DAC register that has been erroneously selected.
(8) Rising edge of RST causes no change in the contents of the serial shift register.

The Serial-Data Output (SDO) is the internal shift register's output. For DAC7634, the SDO is a driven output and does not require an external pull-up. Any number of DAC7634s can be daisy-chained by connecting the SDO pin of one device to the SDI pin of the following device in the chain, as shown in Figure 61.

DIGITAL TIMING

Figure 62 and Table 3 provide detailed timing for the digital interface of the DAC7634.

DIGITAL INPUT CODING

The DAC7634 input data is in straight binary format. The output voltage is given by Equation 1.

Where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

$$V_{OUT} = V_{REF}L + \frac{\left(V_{REF}H - V_{REF}L\right) \times N}{65,536} \quad (1)$$

DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7634 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7634 offers both a differential reference input, as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows a transistor to be placed within the loop to implement a digitally- programmable, unidirectional current source. The availability of a differential reference allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left[\left(\frac{V_{REF}H - V_{REF}L}{R_{SENSE}}\right) \times \left(\frac{N}{65,536}\right)\right] + \left(V_{REF}L/R_{SENSE}\right) \quad (2)$$

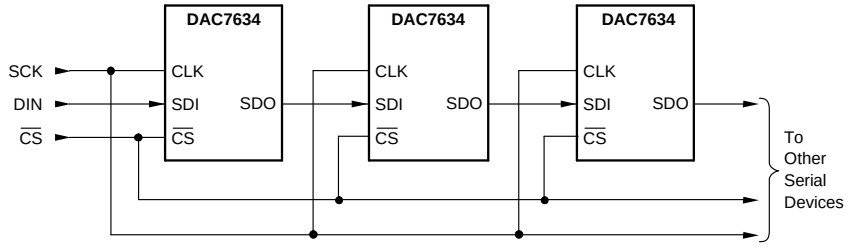


Figure 61. Daisy-Chaining DAC7634

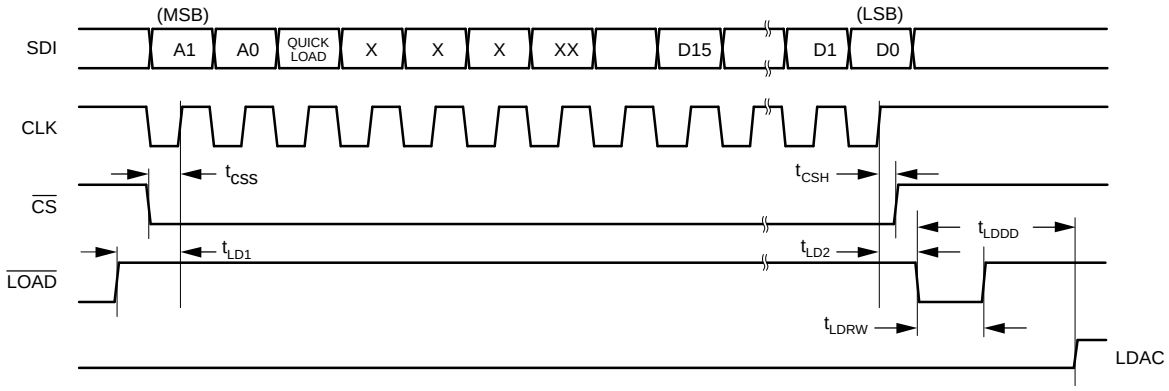


Figure 62. Serial Interface Timing

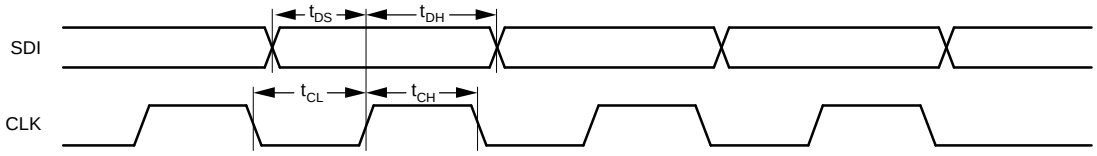


Figure 63. Data and Clock Timing

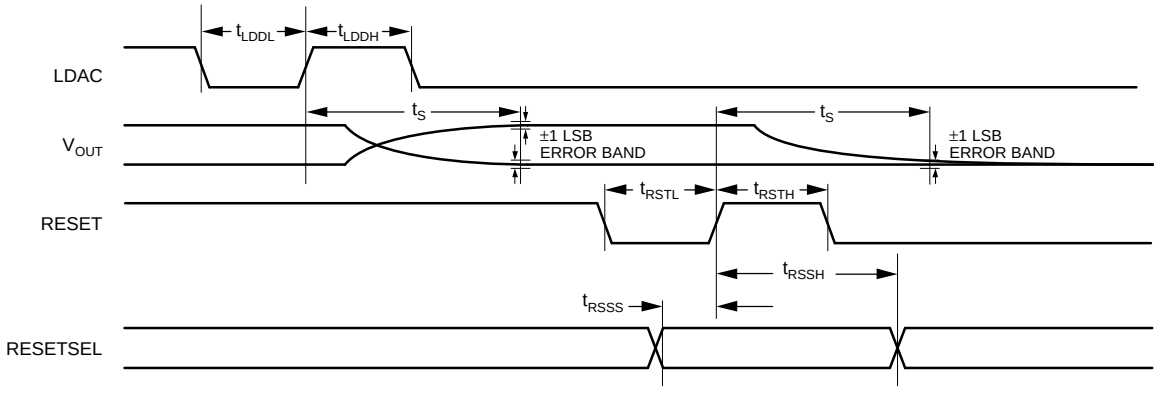


Figure 64. Reset and Output Timing

Table 3. Timing Specifications (T_A = –40°C to 85°C)

SYMBOL	DESCRIPTION	MIN	UNITS
t_{DS}	Data Valid to CLK Rising	10	ns
t_{DH}	Data Held Valid after CLK Rises	20	ns
t_{CH}	CLK HIGH	25	ns
t_{CL}	CLK LOW	25	ns
t_{CSS}	$\overline{CS}$ LOW to CLK Rising	15	ns
t_{CSH}	CLK HIGH to $\overline{CS}$ Rising	0	ns
t_{LD1}	$\overline{LOAD}$ HIGH to CLK Rising	10	ns
t_{LD2}	CLK Rising to $\overline{LOAD}$ LOW	30	ns
t_{LDRW}	$\overline{LOAD}$ LOW Time	30	ns
t_{LDDL}	LDAC LOW Time	100	ns
t_{LDDH}	LDAC HIGH Time	150	ns
t_{LDDD}	LDAC Rising from $\overline{LOAD}$ LOW	40	ns
t_{RSSS}	RESETSEL Valid to RESET HIGH	0	ns
t_{RSSH}	RESET HIGH to RESETSEL Not Valid	100	ns
t_{RSTL}	RESET LOW Time	10	ns
t_{RSTH}	RESET HIGH Time	10	ns
t_S	Settling Time	10	µs

Figure 65 shows a DAC7634 in a 4-mA to 20-mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left[\left(\frac{2.5\ V - 0.5\ V}{125\ \Omega}\right) \times \left(\frac{N}{65,536}\right)\right] + \left(\frac{0.5\ V}{125\ \Omega}\right) \quad (3)$$

At full-scale, the output current is 16 mA, plus the 4 mA, for the zero current. At zero scale, the output current is the offset current of 4 mA (0.5 V/125 Ω).

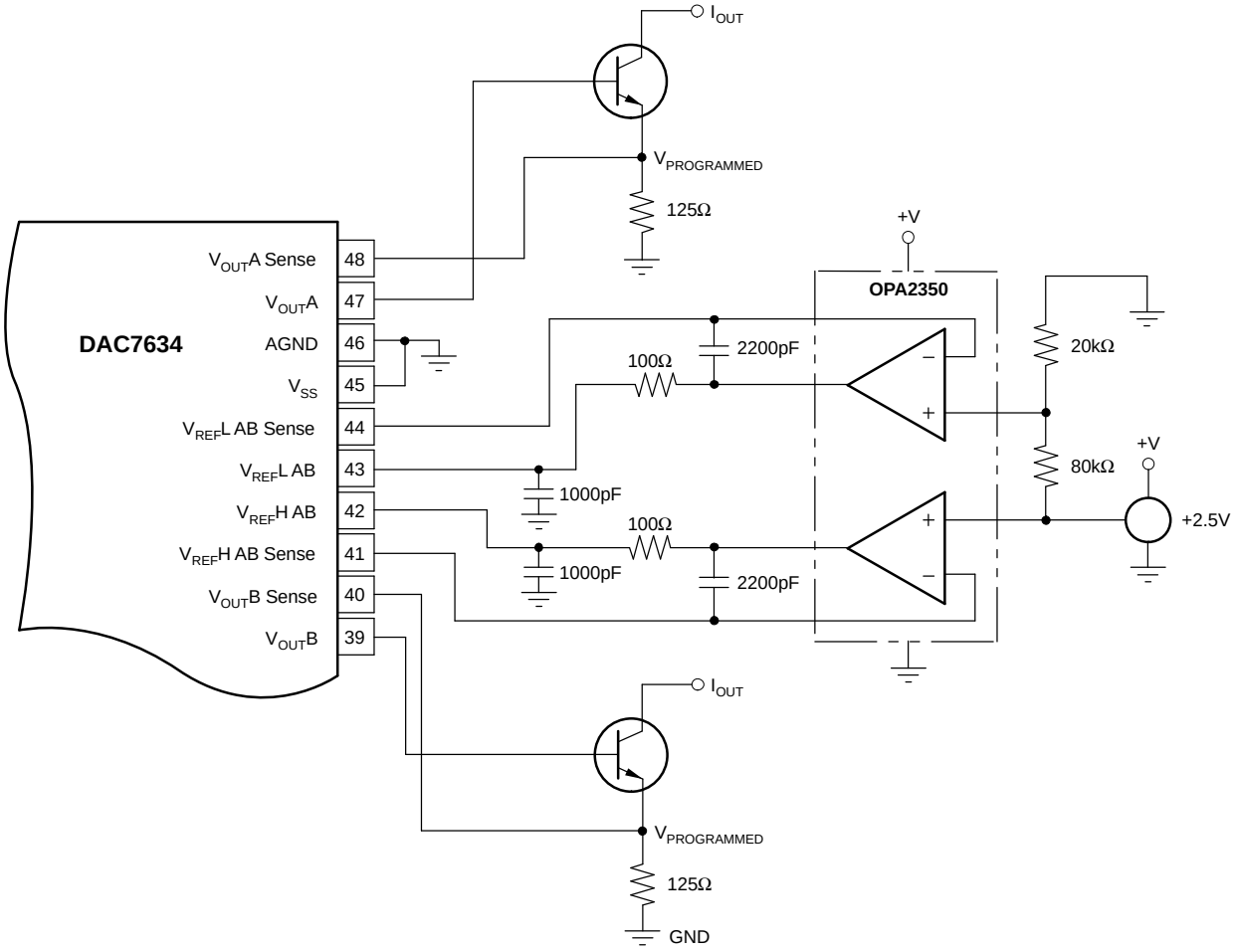


Figure 65. 4 mA to 20 mA Digitally Controlled Current Source (1/2 DAC7634)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC7634E	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E B
DAC7634E.A	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E B
DAC7634E/1K	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E B
DAC7634E/1K.A	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E B
DAC7634EB	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E
DAC7634EB.A	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E
DAC7634EBG4	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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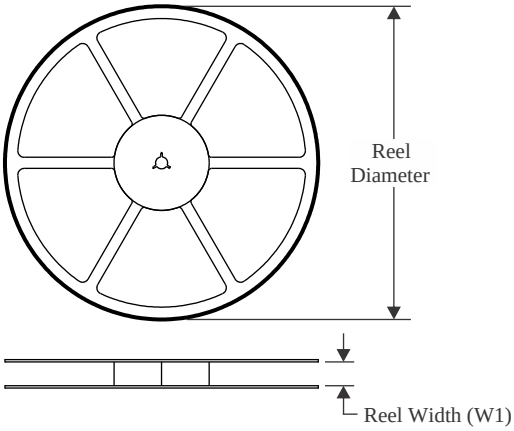
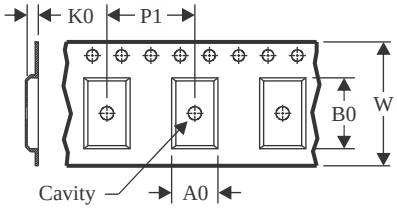
TAPE AND REEL INFORMATION

REEL DIMENSIONS

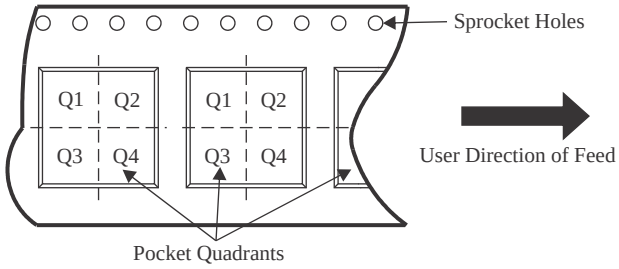


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

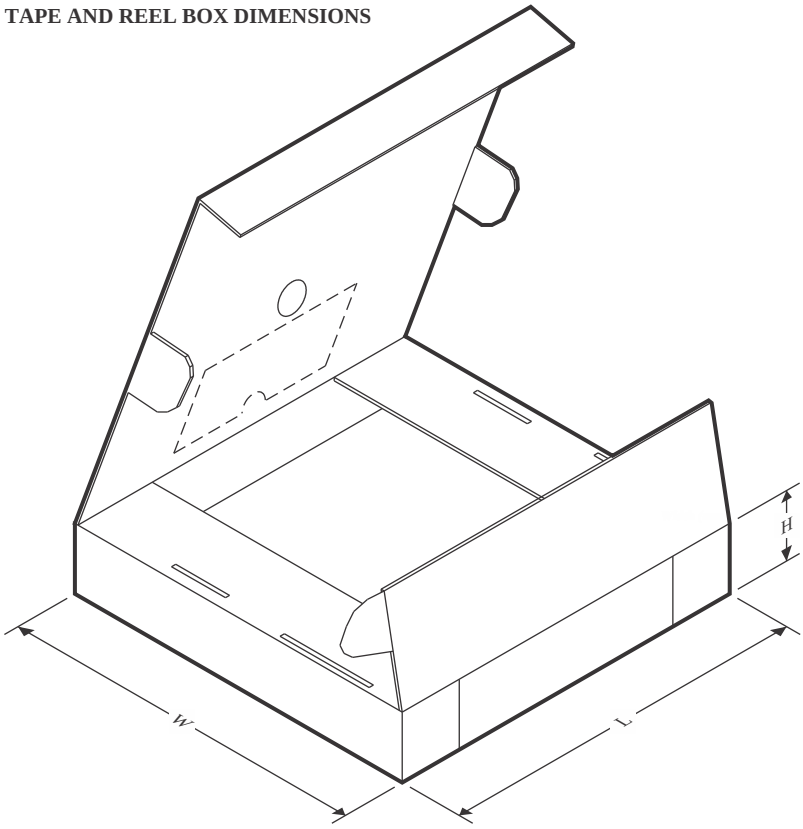
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7634E/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

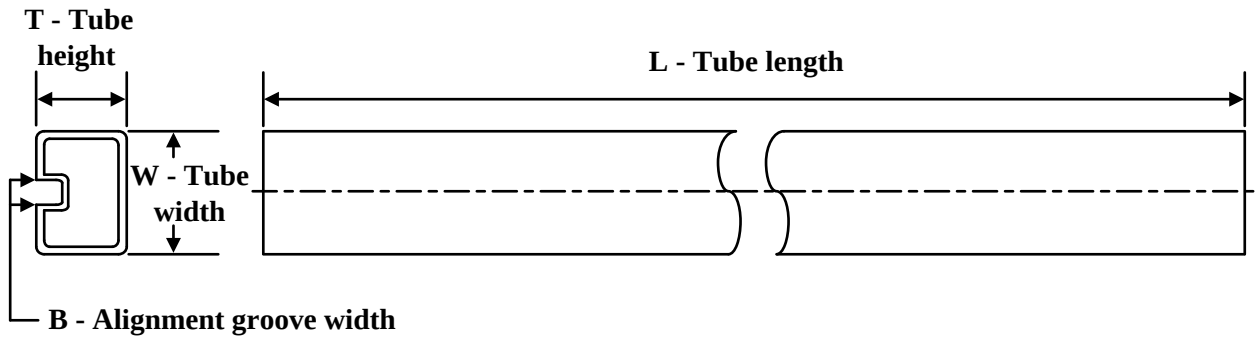
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7634E/1K	SSOP	DL	48	1000	356.0	356.0	53.0

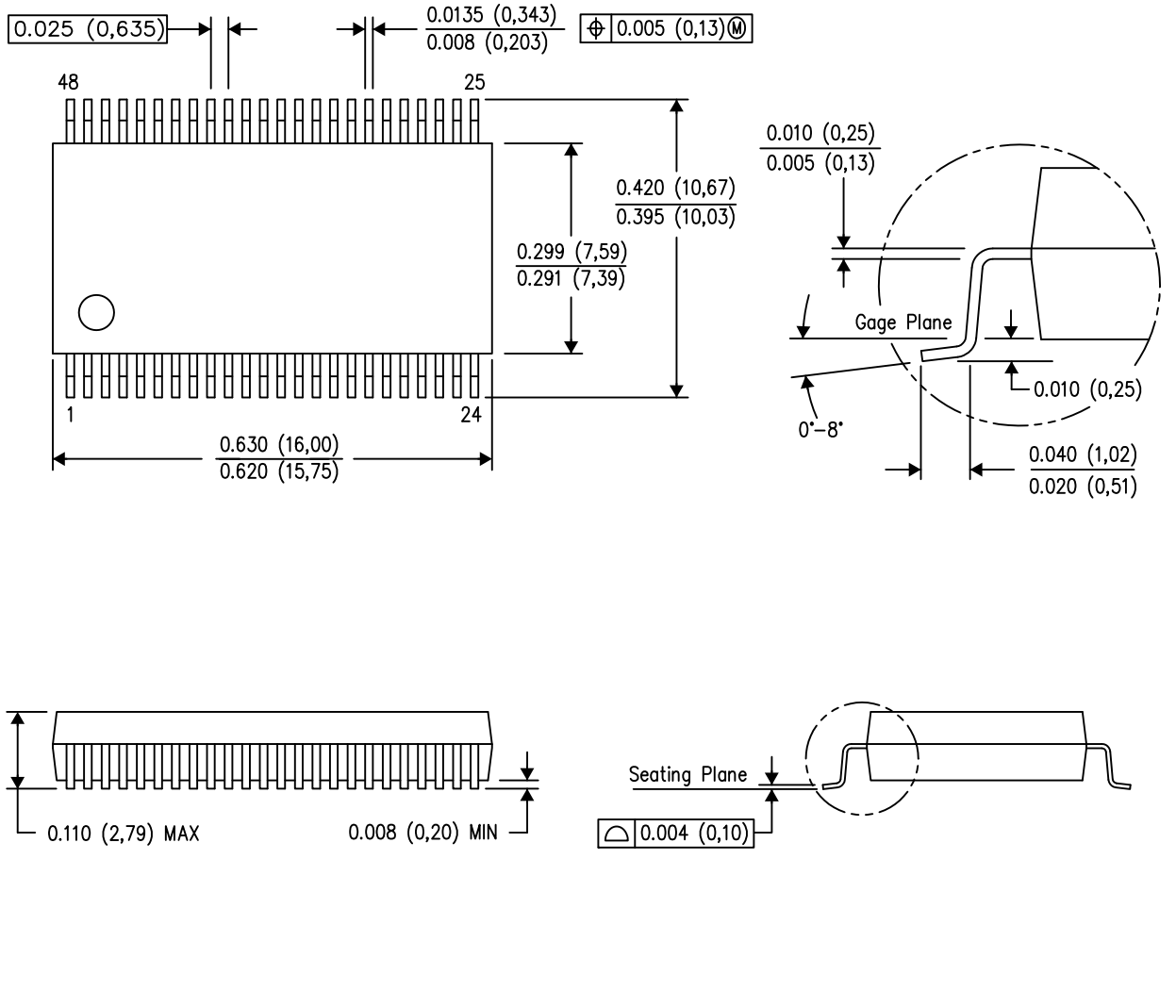
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC7634E	DL	SSOP	48	25	473.7	14.24	5110	7.87
DAC7634E.A	DL	SSOP	48	25	473.7	14.24	5110	7.87
DAC7634EB	DL	SSOP	48	25	473.7	14.24	5110	7.87
DAC7634EB.A	DL	SSOP	48	25	473.7	14.24	5110	7.87
DAC7634EBG4	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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