12-Bit, Ultra-Low Glitch, Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Relative Accuracy (INL): ±0.35LSB**
- **Ultra-Low Glitch Energy: 0.1nV-s**
- **Low Power Operation: 100µA at 2.7V**
- **Power-On Reset to Zero Scale**
- **Power Supply: 2.7V to 5.5V Single Supply**
- **Power-Down: 0.05µA at 2.7V**
- **12-Bit Linearity and Monotonicity**
- **Rail-to-Rail Voltage Output**
- **Settling Time: 5µs (Max)**
- **SPI-Compatible Serial Interface with Schmitt-Trigger Input: Up to 50MHz**
- **Daisy-Chain Capability**
- **Asynchronous Hardware Clear to Zero Scale**
- **Specified Temperature Range: – 40°C to +105°C**
- **Small, 2 x 3 mm, 12-Lead SON Package**

APPLICATIONS

- **Portable, Battery-Powered Instruments**
- **Digital Gain and Offset Adjustment**
- **Programmable Voltage and Current Sources**
- **Programmable Attenuators**
- **Industrial Process Control**

DESCRIPTION

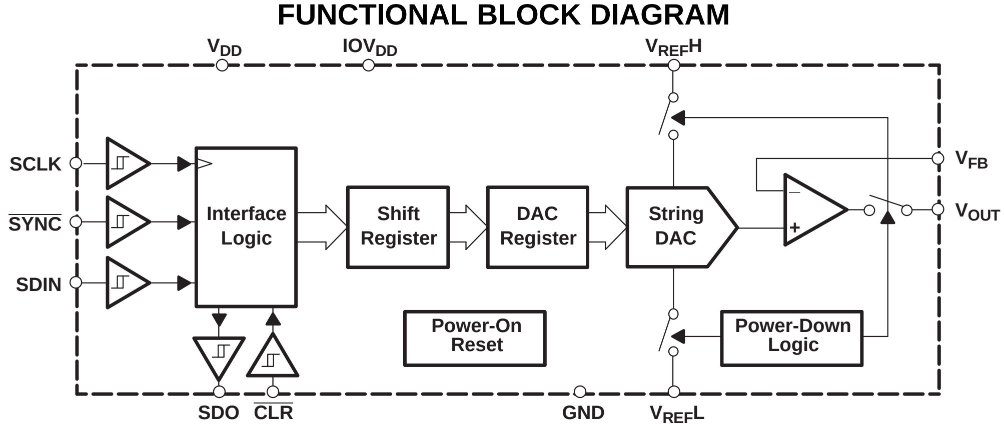
The DAC7551 is a single-channel, voltage-output digital-to-analog converter (DAC) with exceptional linearity and monotonicity, and a proprietary architecture that minimizes glitch energy. The low-power DAC7551 operates from a single 2.7V to 5.5V supply. The DAC7551 output amplifiers can drive a 2kΩ, 200pF load rail-to-rail with 5µs settling time; the output range is set using an external voltage reference.

The 3-wire serial interface operates at clock rates up to 50MHz and is compatible with SPI™, QSPI™, Microwire™, and DSP interface standards. The parts incorporate a power-on-reset circuit to ensure that the DAC output powers up to 0V and remains there until a valid write cycle to the device takes place. The part contains a power-down feature that reduces the current consumption of the device to under 2µA.

Small size and low-power operation make the DAC7551 ideally suited for battery-operated, portable applications. The power consumption is typically 0.5mW at 5V, 0.23mW at 3V, and reduces to 1µW in power-down mode.

The DAC7551 is available in a 12-lead SON package and is specified over –40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC7551	SON-12	DRN	–40°C to +105°C	D51

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		UNIT
V_{DD} , IOV_{DD} to GND		–0.3V to 6V
Digital input voltage to GND		–0.3V to V_{DD} + 0.3V
V_{OUT} to GND		–0.3V to V_{DD} + 0.3V
Operating temperature range		–40°C to +105°C
Storage temperature range		–65°C to +150°C
Junction temperature (T_J Max)		+150°C
Power dissipation (DRN)		$(T_J \text{ max} – T_A)/\theta_{JA}$
Thermal impedance, θ_{JA}		79°C/W
Thermal impedance, θ_{JC}		48.57°C/W
ESD rating	Human body model (HBM)	4000V
	Charged device model (CDM)	1500V

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

all specifications at –40°C to +105°C, V_{DD} = 2.7V to 5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = GND, R_L = 2kΩ to GND, and C_L = 200pF to GND (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE(1)					
Resolution		12			Bits
Relative accuracy			±0.35	±1	LSB
Differential nonlinearity	Specified monotonic by design		±0.08	± 0.5	LSB
Offset error				±12	mV
Zero-scale error	All zeroes loaded to DAC register			±12	mV
Gain error				±0.15	%FSR
Full-scale error				±0.5	%FSR
Zero-scale error drift			7		µV/°C
Gain temperature coefficient			3		ppm of FSR/°C
PSRR	V_{DD} = 5V		0.75		mV/V
OUTPUT CHARACTERISTICS(2)					
Output voltage range		2 x $V_{REF}L$		$V_{REF}H$	V
Output voltage settling time	R_L = 2kΩ, 0pF < C_L < 200pF			5	µs
Slew rate			1.8		V/µs
Capacitive load stability	R_L = ∞		470		pF
	R_L = 2kΩ		1000		
Digital-to-analog glitch impulse	1 LSB change around major carry		0.1		nV-s
Digital feedthrough			0.1		nV-s
Output noise density	10kHz offset frequency		120		nV/$\sqrt{Hz}$
Total harmonic distortion	f_{OUT} = 1kHz, f_S = 1MSPS, BW = 20kHz		–85		dB
DC output impedance			1		Ω
Short-circuit current	V_{DD} = 5V		50		mA
	V_{DD} = 3V		20		
Power-up time	Coming out of power-down mode, V_{DD} = 5V		15		µs
	Coming out of power-down mode, V_{DD} = 3V		15		
REFERENCE INPUT					
$V_{REF}H$ Input range		0		V_{DD}	V
$V_{REF}L$ Input range	$V_{REF}L < V_{REF}H$	0	GND	V_{DD}	V
Reference input impedance			100		kΩ
Reference current	$V_{REF} = V_{DD}$ = 5V		50	100	µA
	$V_{REF} = V_{DD}$ = 3V		30	60	
LOGIC INPUTS(2)					
Input current				±1	µA
V_{IN_L}, Input low voltage	IOV_{DD} ≥ 2.7V			0.3 IOV_{DD}	V
V_{IN_H}, Input high voltage	IOV_{DD} ≥ 2.7V	0.7 IOV_{DD}			V
Pin capacitance				3	pF

(1) Linearity tested using a reduced code range of 30 to 4065; output unloaded.
(2) Specified by design and characterization; not production tested. For 1.8V < IOV_{DD} < 2.7V, it is recommended that V_{IH} ≥ 0.8 IOV_{DD}, and V_{IL} ≤ 0.2 IOV_{DD}.

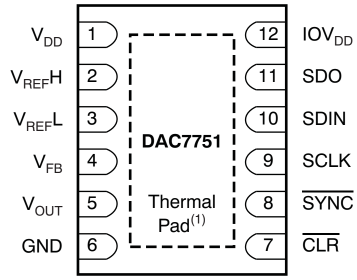
ELECTRICAL CHARACTERISTICS (continued)

all specifications at –40°C to +105°C, V_{DD} = 2.7V to 5.5V, $V_{REF}H$ = V_{DD}, $V_{REF}L$ = GND, R_L = 2kΩ to GND, and C_L = 200pF to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
V_{DD}			2.7		5.5	V
IOV_{DD} (3)			1.8		V_{DD}	V
I_{DD} (4)	Normal operation (DAC active and excluding load current)	V_{DD} = 3.6V to 5.5V, V_{IH} = IOV_{DD}, V_{IL} = GND		150	200	μA
		V_{DD} = 2.7V to 3.6V, V_{IH} = IOV_{DD}, V_{IL} = GND		100	150	
	All power-down modes	V_{DD} = 3.6V to 5.5V, V_{IH} = IOV_{DD}, V_{IL} = GND		0.2	2	μA
		V_{DD} = 2.7V to 3.6V, V_{IH} = IOV_{DD}, V_{IL} = GND		0.05	2	
POWER EFFICIENCY						
I_{OUT}/I_{DD}		I_{LOAD} = 2mA, V_{DD} = 5V		93		%
TEMPERATURE RANGE						
Specified performance			–40		+105	°C

(3) IOV_{DD} operates down to 1.8V with slightly degraded timing, as long as $V_{IH} \geq 0.8\ IOV_{DD}$ and $V_{IL} \leq 0.2\ IOV_{DD}$.
(4) I_{DD} tested with digital input code = 0032.

PIN CONFIGURATION



Pin Descriptions

PIN		DESCRIPTION
NO.	NAME	
1	V_{DD}	Analog voltage supply input
2	$V_{REF}H$	Positive reference voltage input
3	$V_{REF}L$	Negative reference voltage input
4	V_{FB}	DAC amplifier sense input.
5	V_{OUT}	Analog output voltage from DAC
6	GND[(1)]	Ground.
7	$\overline{\text{CLR}}$	Asynchronous input to clear the DAC registers. When $\overline{\text{CLR}}$ is low, the DAC register is set to 000h and the output voltage to 0V.
8	$\overline{\text{SYNC}}$	Frame synchronization input. The falling edge of the $\overline{\text{SYNC}}$ pulse indicates the start of a serial data frame shifted out to the DAC7551.
9	SCLK	Serial clock input
10	SDIN	Serial data input
11	SDO	Serial data output
12	IOV_{DD}	I/O voltage supply input

(1) Thermal pad should be connected to GND.

SERIAL WRITE OPERATION

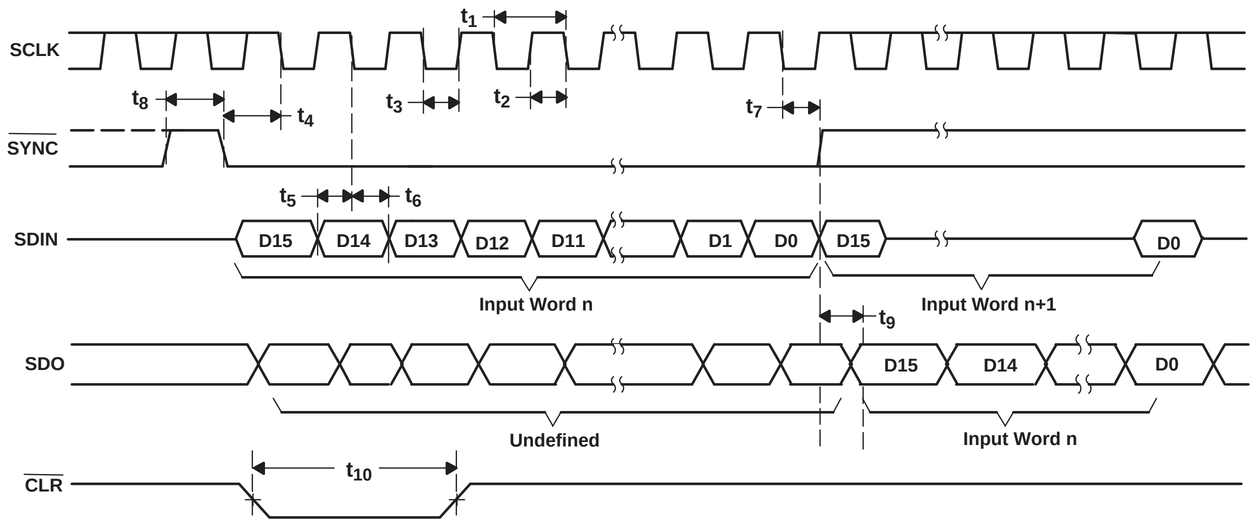


Figure 1. Serial Write Operation Timing Diagram

TIMING CHARACTERISTICS[(1)(2)]

All specifications at –40°C to +105°C, V_{DD} = 2.7V to 5.5V, and R_L = 2kΩ to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_1 [(3)]	SCLK cycle time	V_{DD} = 2.7V to 3.6V	20			ns
		V_{DD} = 3.6V to 5.5V	20			
t_2	SCLK HIGH time	V_{DD} = 2.7V to 3.6V	6.5			ns
		V_{DD} = 3.6V to 5.5V	6.5			
t_3	SCLK LOW time	V_{DD} = 2.7V to 3.6V	6.5			ns
		V_{DD} = 3.6V to 5.5V	6.5			
t_4	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time	V_{DD} = 2.7V to 3.6V	4			ns
		V_{DD} = 3.6V to 5.5V	4			
t_5	Data setup time	V_{DD} = 2.7V to 3.6V	3			ns
		V_{DD} = 3.6V to 5.5V	3			
t_6	Data hold time	V_{DD} = 2.7V to 3.6V	3			ns
		V_{DD} = 3.6V to 5.5V	3			
t_7	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	V_{DD} = 2.7V to 3.6V	0		t_1– 10ns[(4)]	ns
		V_{DD} = 3.6V to 5.5V	0		t_1– 10ns[(4)]	
t_8	Minimum $\overline{\text{SYNC}}$ HIGH time	V_{DD} = 2.7V to 3.6V	20			ns
		V_{DD} = 3.6V to 5.5V	20			
t_9	SCLK falling edge to SDO valid	V_{DD} = 2.7V to 3.6V	10			ns
		V_{DD} = 3.6V to 5.5V	10			
t_{10}	$\overline{\text{CLR}}$ pulse width low	V_{DD} = 2.7V to 3.6V	10			ns
		V_{DD} = 3.6V to 5.5V	10			

(1) All input signals are specified with $t_R = t_F$ = 1ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See Figure 1, Serial Write Operation timing diagram.
(3) Maximum SCLK frequency is 50MHz at V_{DD} = 2.7V to 5.5V.
(4) SCLK falling edge to $\overline{\text{SYNC}}$ rising edge time shold not exceed (t_1– 10ns) in order to latch the correct data.

TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

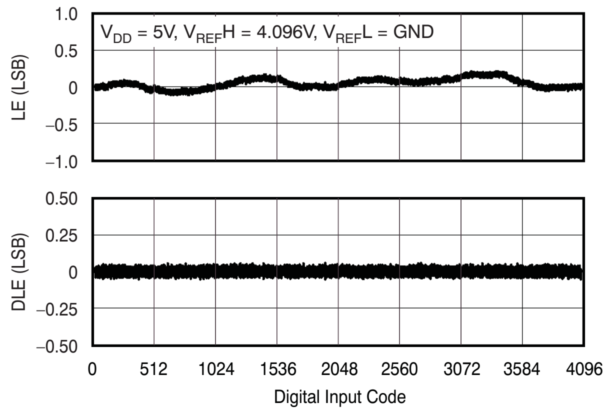


Figure 2.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

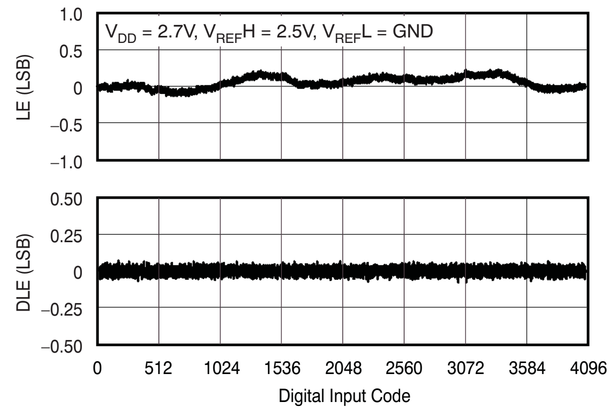


Figure 3.

ZERO-SCALE ERROR vs FREE-AIR TEMPERATURE

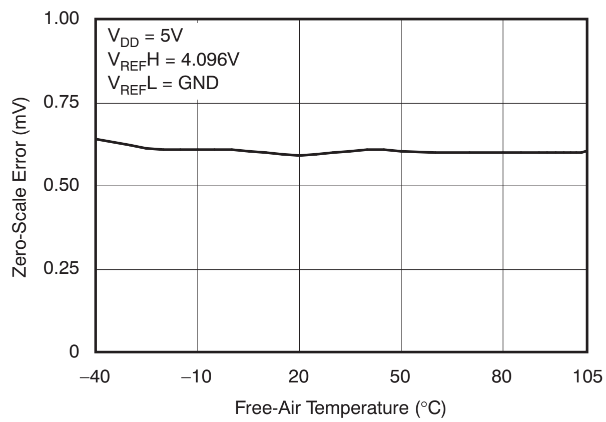


Figure 4.

ZERO-SCALE ERROR vs FREE-AIR TEMPERATURE

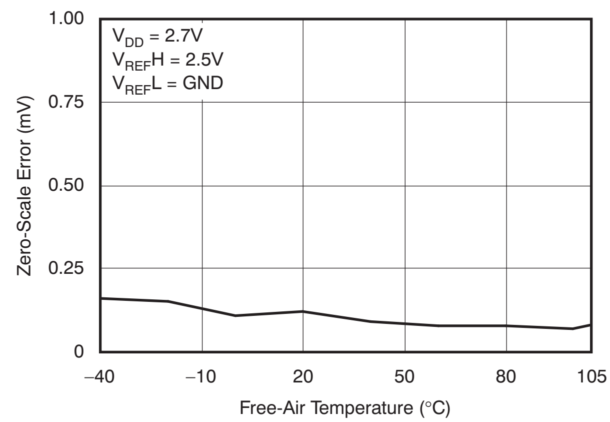


Figure 5.

FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

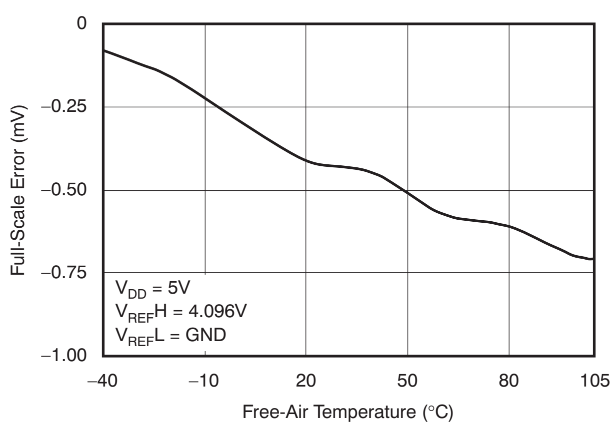


Figure 6.

FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

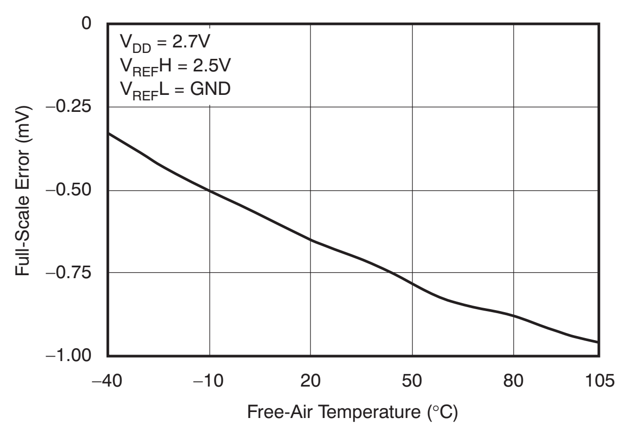


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

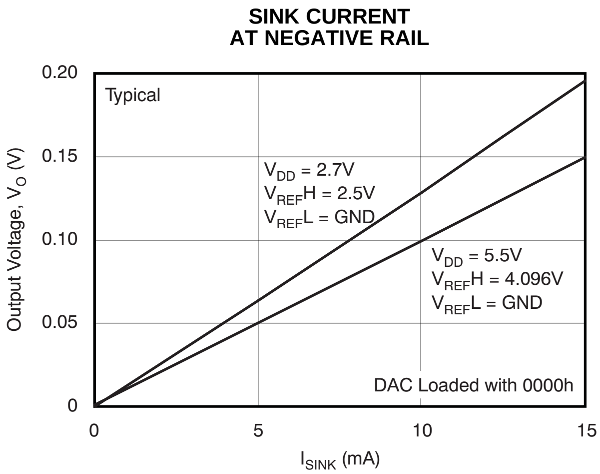


Figure 8.

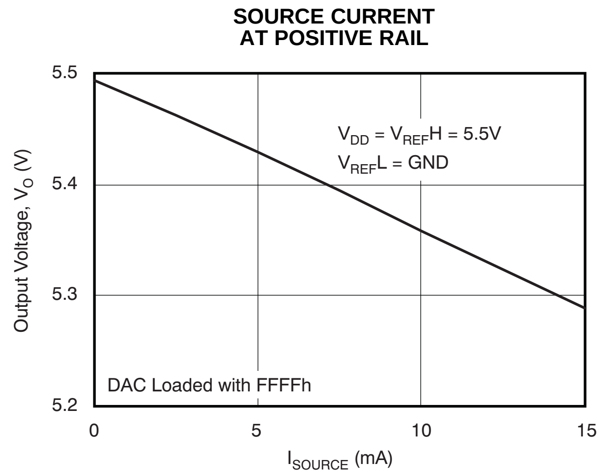


Figure 9.

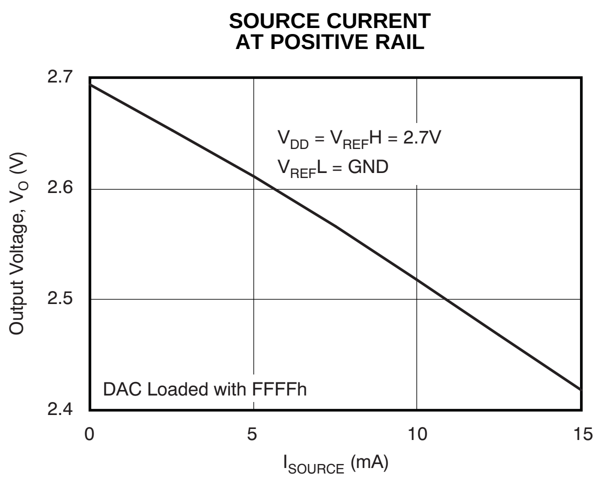


Figure 10.

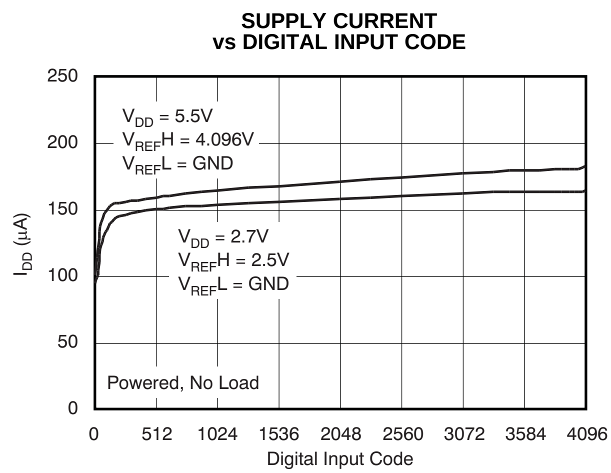


Figure 11.

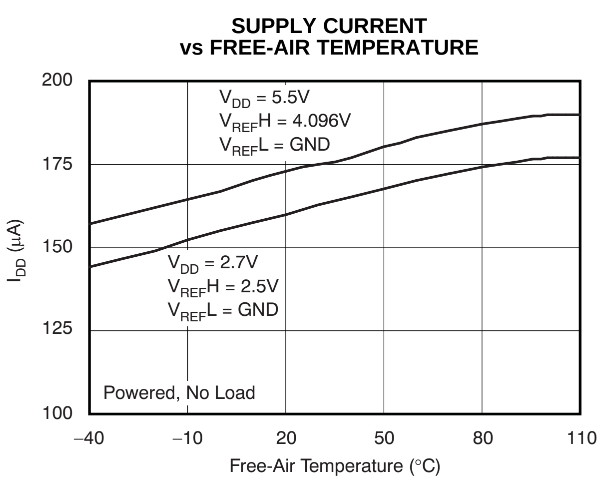


Figure 12.

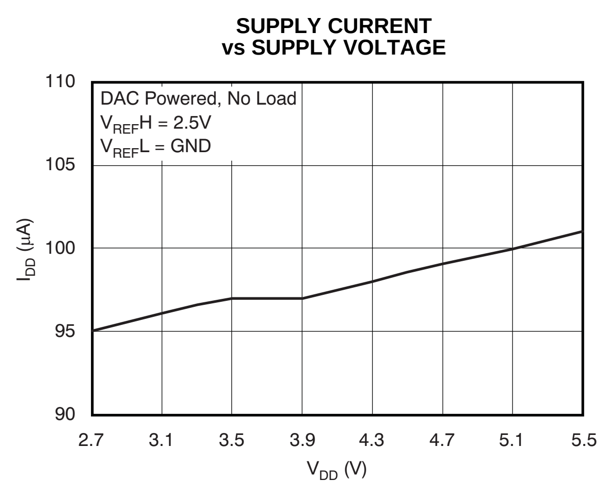


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

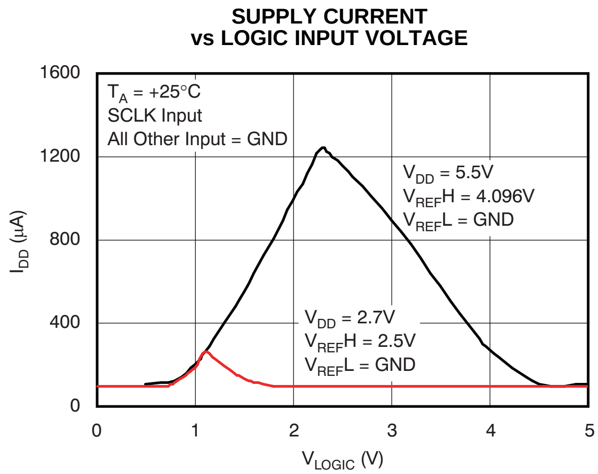


Figure 14.

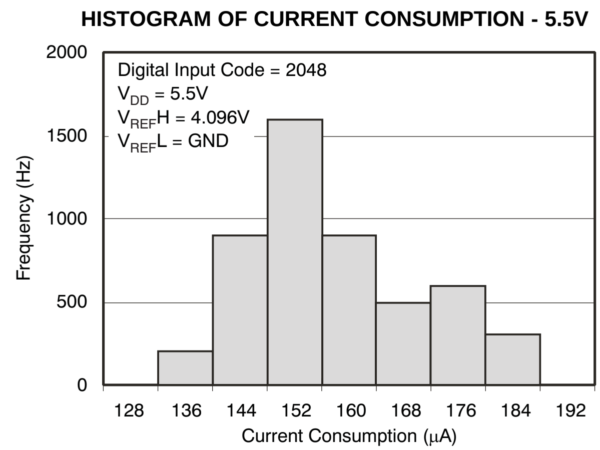


Figure 15.

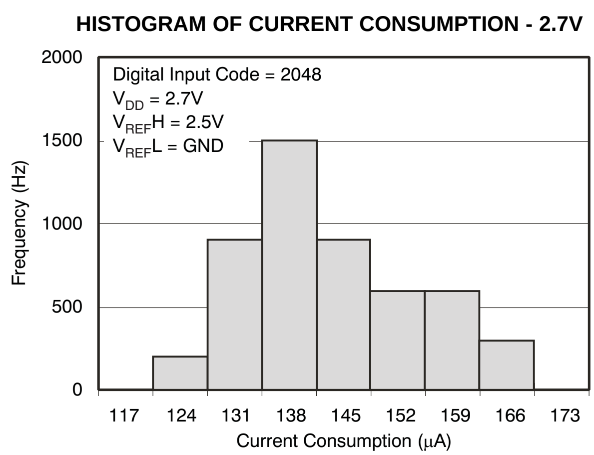


Figure 16.

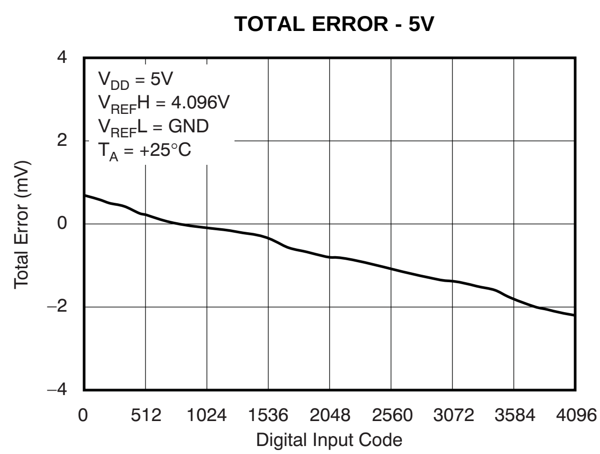


Figure 17.

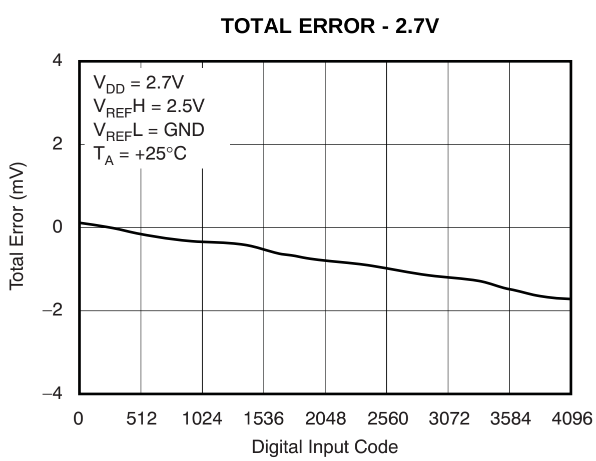


Figure 18.

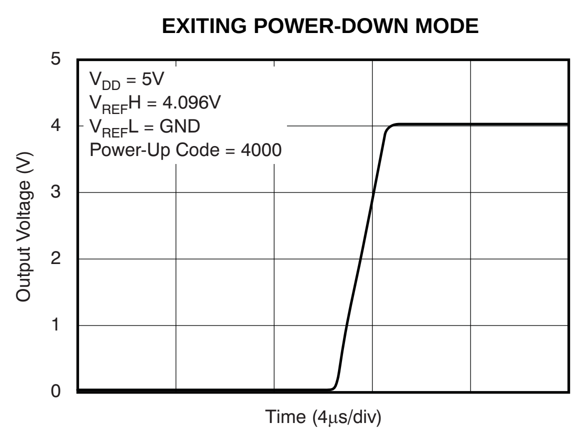


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

LARGE-SIGNAL SETTLING TIME - 5V

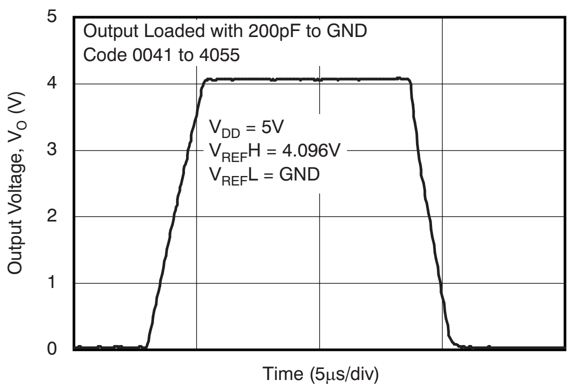


Figure 20.

LARGE-SIGNAL SETTLING TIME - 2.7V

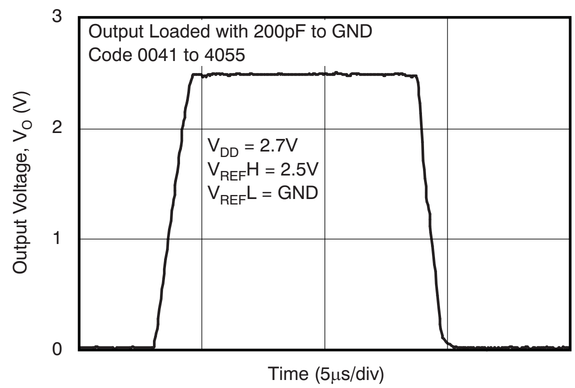


Figure 21.

MIDSCALE GLITCH

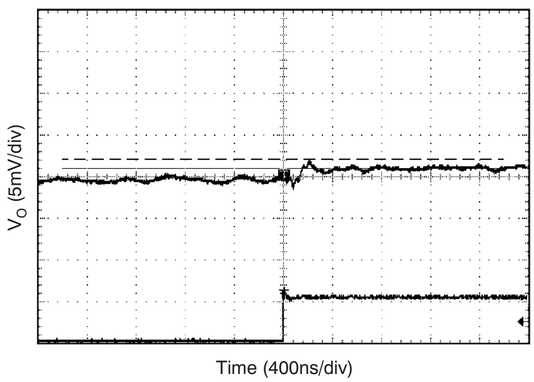


Figure 22.

WORST-CASE GLITCH

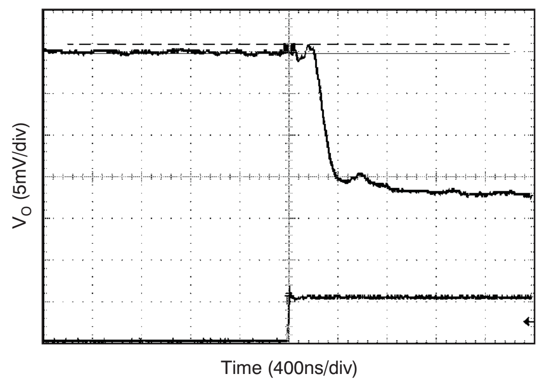


Figure 23.

DIGITAL FEEDTHROUGH ERROR

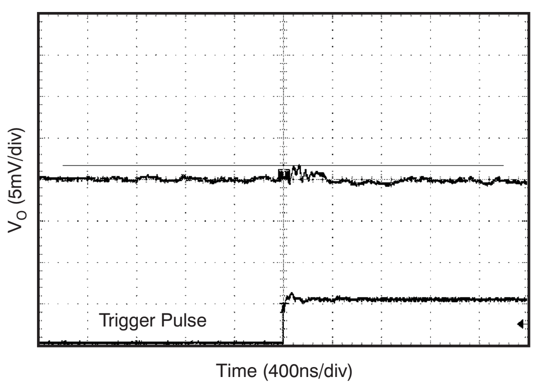


Figure 24.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

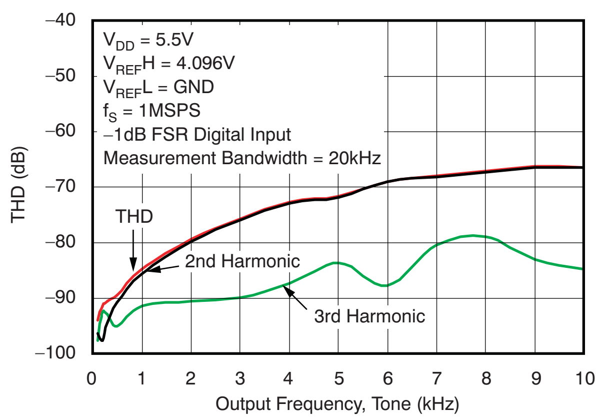


Figure 25.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The architecture of the DAC7551 consists of a string DAC followed by an output buffer amplifier. Figure 26 shows a generalized block diagram of the DAC architecture.

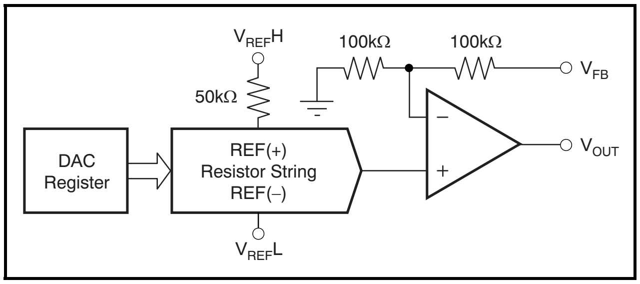


Figure 26. Typical DAC Architecture

The input coding to the DAC7551 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = 2 \times V_{REF}L + (V_{REF}H - V_{REF}L) \times D/4096$$

Where D = decimal equivalent of the binary code that is loaded to the DAC register, which ranges from 0 to 4095.

RESISTOR STRING

The resistor string section is shown in Figure 27. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. It is specified monotonic because it is a string of resistors.

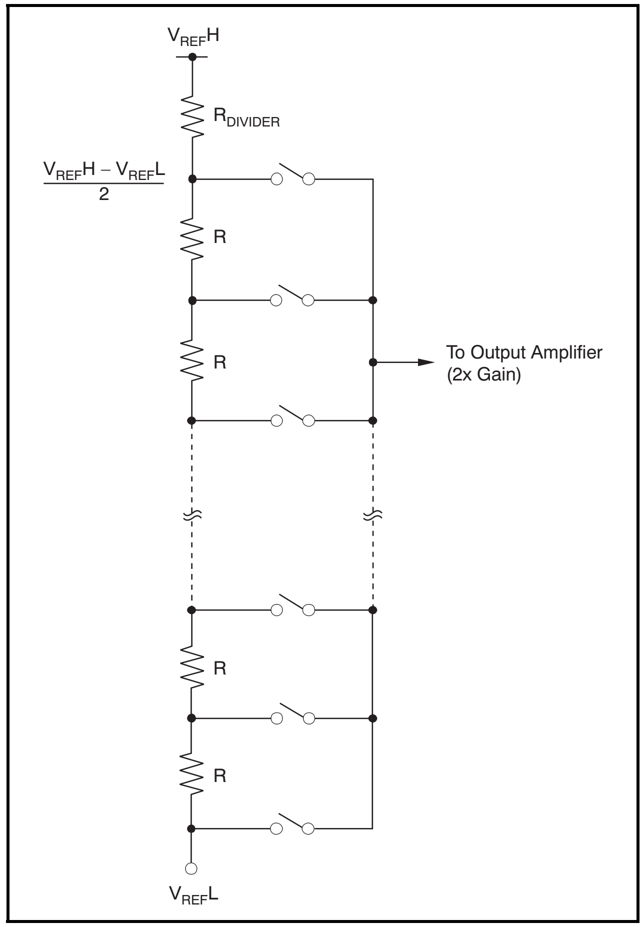


Figure 27. Typical Resistor String

OUTPUT BUFFER AMPLIFIERS

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0V to V_{DD}. It is capable of driving a load of 2kΩ in parallel with up to 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1.8V/µs with a half-scale settling time of 3µs with the output unloaded.

DAC External Reference Input

The DAC7551 contains $V_{REF}H$ and $V_{REF}L$ reference inputs, which are unbuffered. The $V_{REF}H$ reference voltage can be as low as 0.25V, and as high as V_{DD} because there is no restriction of headroom and footroom from any reference amplifier.

It is recommended to use a buffered reference in the external circuit (for example, the REF3140). The input impedance is typically 100kΩ.

Amplifier Sense Input

The DAC7551 contains an amplifier feedback input pin, V_{FB}. For voltage output operation, V_{FB} must be externally connected to V_{OUT}. For better DC accuracy, this connection should be made at load points. The V_{FB} pin is also useful for a variety of applications, including digitally-controlled current sources. The feedback input pin is internally connected to the DAC amplifier negative input terminal through a 100kΩ resistor. The amplifier negative input terminal internally connects to ground through another 100kΩ resistor (Figure 26). These connections form a gain-of-two, noninverting, amplifier configuration. Overall gain remains one because the resistor string has a divide-by-two configuration. The resistance seen at the V_{FB} pin is approximately 200kΩ to ground.

Power-On Reset

On power up, all registers are cleared and the DAC channel is updated with zero-scale voltage. The DAC output remains in this state until valid data are written. This setup is particularly useful in applications where it is important to know the state of the DAC output while the device is powering up. In order to not turn on ESD protection devices, V_{DD} and IOV_{DD} should be applied before any other pin (such as $V_{REF}H$) is brought high. The power-up sequence of V_{DD} and IOV_{DD} is irrelevant. Therefore, IOV_{DD} can be brought up before V_{DD}, or vice-versa.

Power Down

The DAC7551 has a flexible power-down capability. During a power-down condition, the user has flexibility to select the output impedance of the DAC. During power-down operation, the DAC can have either 1kΩ, 100kΩ, or Hi-Z output impedance to ground.

Asynchronous Clear

The DAC7551 output is asynchronously set to zero-scale voltage immediately after the $\overline{CLR}$ pin is brought low. The $\overline{CLR}$ signal resets all internal registers and therefore behaves like the Power-On Reset. The DAC7551 updates at the first rising edge of the $\overline{SYNC}$ signal that occurs after the $\overline{CLR}$ pin is brought back to high.

IOVDD and Level Shifters

The DAC7551 can be used with different logic families that require a wide range of supply voltages. To enable this useful feature, the IOV_{DD} pin must be connected to the logic supply voltage of the system. All DAC7551 digital input and output pins are equipped with level-shifter circuits. Level shifters at the input pins ensure that external logic-high voltages are translated to the internal logic-high voltage, with no additional power dissipation. Similarly, the level shifter for the SDO pin translates the internal logic-high voltage (V_{DD}) to the external logic-high level (IOV_{DD}). For single-supply operation, the IOV_{DD} pin can be tied to the V_{DD} pin.

SERIAL INTERFACE

The DAC7551 is controlled over a versatile 3-wire serial interface, which operates at clock rates up to 50MHz and is compatible with SPI, QSPI, Microwire, and DSP interface standards.

16-Bit Word and Input Shift Register

The input shift register is 16 bits wide. DAC data are loaded into the device as a 16-bit word under the control of a serial clock input, SCLK, as shown in Figure 1, the Serial Write Operation timing diagram. The 16-bit word, illustrated in Table 1, consists of four control bits followed by 12 bits of DAC data. The data format is straight binary with all zeroes corresponding to 0V output and all ones corresponding to full-scale output (V_{REF} – 1LSB). Data are loaded MSB first (bit 15) where the first two bits (DB15 and DB14) are *don't care* bits. Bit 13 and bit 12 (DB13 and DB12) determine either normal mode operation or power-down mode (see Table 1).

The $\overline{SYNC}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low, observing the minimum $\overline{SYNC}$ to SCLK falling edge setup time, t_4. After $\overline{SYNC}$ goes low, serial data is shifted into the device input shift register on the falling edges of SCLK for 16 clock pulses.

The SPI interface is enabled after $\overline{SYNC}$ becomes low and the data are continuously shifted into the shift register at each falling edge of SCLK. When $\overline{SYNC}$ is brought high, the last 16 bits stored in the shift register are latched into the DAC register, and the DAC updates.

Daisy-Chain Operation

Daisy-chain operation is used for updating serially-connected devices on the rising edge of $\overline{SYNC}$.

As long as $\overline{SYNC}$ is high, the SDO pin is in a high-impedance state. When $\overline{SYNC}$ is brought low the output of the internal shift register is tied to the SDO pin. As long as $\overline{SYNC}$ is low, SDO duplicates the SDIN signal with a 16-cycle delay. To support multiple devices in a daisy chain, SCLK and $\overline{SYNC}$ signals are shared across all devices, and SDO of one DAC7551 should be tied to the SDIN of the next DAC7551. For *n* devices in such a daisy chain, 16*n* SCLK cycles are required to shift the entire input data stream. After 16*n* SCLK falling edges are received, following a falling $\overline{SYNC}$, the data stream becomes complete and $\overline{SYNC}$ can be brought high to update *n* devices simultaneously. SDO operation is specified at a maximum SCLK speed of 10MHz.

In daisy-chain mode, the use of a weak pull-down resistor on the SDO output pin, which provides the SDIN data for the next device in the chain, is recommended. For standalone operation, the maximum clock speed is 50MHz. For daisy-chain operation, the maximum clock speed is 10MHz.

INTEGRAL AND DIFFERENTIAL LINEARITY

The DAC7551 uses precision thin-film resistors providing exceptional linearity and monotonicity. Integral linearity error is typically within ±0.35LSBs, and differential linearity error is typically within ±0.08LSBs.

GLITCH ENERGY

The DAC7551 uses a proprietary architecture that minimizes glitch energy. The code-to-code glitches are so low that they are usually buried within the wide-band noise and cannot be easily detected. The DAC7551 glitch is typically well under 0.1nV-s. Such low glitch energy provides more than a ten-time improvement over industry alternatives.

Table 1. Serial Interface Programming

CONTROL				DATA BITS	
DB15	DB14	DB13 (PD1)	DB12 (PD0)	DB11–DB0	FUNCTION
X	X	0	0	data	Normal mode
X	X	0	1	X	Powerdown 1kΩ
X	X	1	0	X	Powerdown 100kΩ
X	X	1	1	X	Powerdown Hi-Z

APPLICATION INFORMATION

WAVEFORM GENERATION

As a result of the exceptional linearity and low glitch of the DAC7551, the device is well-suited for waveform generation (from DC to 10kHz). The DAC7551 large-signal settling time is 5μs, supporting an update rate of 200kSPS. However, the update rates can exceed 1MSPS if the waveform to be generated consists of small voltage steps between consecutive DAC updates. To obtain a high dynamic range, REF3140 (4.096V) or REF02 (5.0V) are recommended for reference voltage generation.

GENERATING ±5V, ±10V, AND ±12V OUTPUTS FOR PRECISION INDUSTRIAL CONTROL

Industrial control applications can require multiple feedback loops consisting of sensors, ADCs, MCUs, DACs, and actuators. Loop accuracy and loop speed are the two important parameters of such control loops.

Loop Accuracy

DAC offset, gain, and the integral linearity errors are not factors in determining the accuracy of the loop. As long as a voltage exists in the transfer curve of a monotonic DAC, the loop can find it and settle to it. On the other hand, DAC resolution and differential linearity do determine the loop accuracy, because each DAC step determines the minimum incremental change the loop can generate. A DNL error less than –1LSB (non-monotonicity) can create loop instability. A DNL error greater than +1LSB implies unnecessarily large voltage steps and missed voltage targets. With high DNL errors, the loop loses its stability, resolution, and accuracy. Offering 12-bit ensured monotonicity and ±0.08LSB typical DNL error, DAC755x devices are great choices for precision control loops.

Loop Speed

Many factors determine the control loop speed, such as ADC conversion time, MCU speed, and DAC settling time. Typically, the ADC conversion time, and the MCU computation time are the two major factors that dominate the time constant of the loop. DAC settling time is rarely a dominant factor because ADC conversion times usually exceed DAC conversion times. DAC offset, gain, and linearity errors can slow the loop down only during the start-up. Once the loop reaches its steady-state operation, these errors do not affect loop speed any further. Depending on the ringing characteristics of the loop transfer function, DAC glitches can also slow the loop down. With its 1MSPS (small-signal) maximum data update rate, DAC7551 can support high-speed control loops. Ultralow glitch energy of the DAC7551 significantly improves loop stability and loop settling time.

GENERATING INDUSTRIAL VOLTAGE RANGES

For control loop applications, DAC gain and offset errors are not important parameters. This consideration could be exploited to lower trim and calibration costs in a high-voltage control circuit design. Using a quad operational amplifier (OPA4130), and a voltage reference (REF3140), the DAC7551 can generate the wide voltage swings required by the control loop.

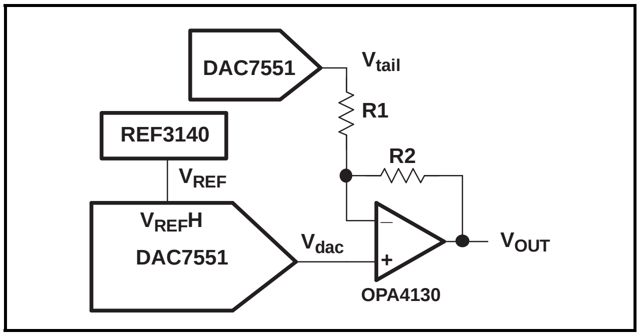


Figure 28. Low-cost, Wide-swing Voltage Generator for Control Loop Applications

The output voltage of the configuration is given by:

$$V_{OUT} = V_{REF}\left(\frac{R2}{R1} + 1\right)\frac{SDIN}{4096} - V_{tail}\left(\frac{R2}{R1}\right) \quad (1)$$

Fixed R1 and R2 resistors can be used to coarsely set the gain required in the first term of the equation. Once R2 and R1 set the gain to include some minimal over-range, a single DAC7551 could be used to set the required offset voltages. Residual errors are not an issue for loop accuracy because offset and gain errors could be tolerated. One DAC7551 can provide the V_{tail} voltages, while four additional DAC7551 devices can provide V_{dac} voltages to generate four high-voltage outputs. A single SPI interface is sufficient to control all five DAC7551 devices in a daisy-chain configuration.

For ±5V operation:

R1 = 10kΩ, R2 = 15kΩ, V_{tail} = 3.33V, V_{REF} = 4.096V

For ±10V operation:

R1 = 10kΩ, R2 = 39kΩ, V_{tail} = 2.56V, V_{REF} = 4.096V

For ±12V operation:

R1 = 10kΩ, R2 = 49kΩ, V_{tail} = 2.45V, V_{REF} = 4.096V

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC7551IDRNR	Active	Production	USON (DRN) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D51
DAC7551IDRNR.B	Active	Production	USON (DRN) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D51
DAC7551IDRNT	Active	Production	USON (DRN) | 12	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D51
DAC7551IDRNT.B	Active	Production	USON (DRN) | 12	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D51
DAC7551IDRNTG4	Active	Production	USON (DRN) | 12	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D51

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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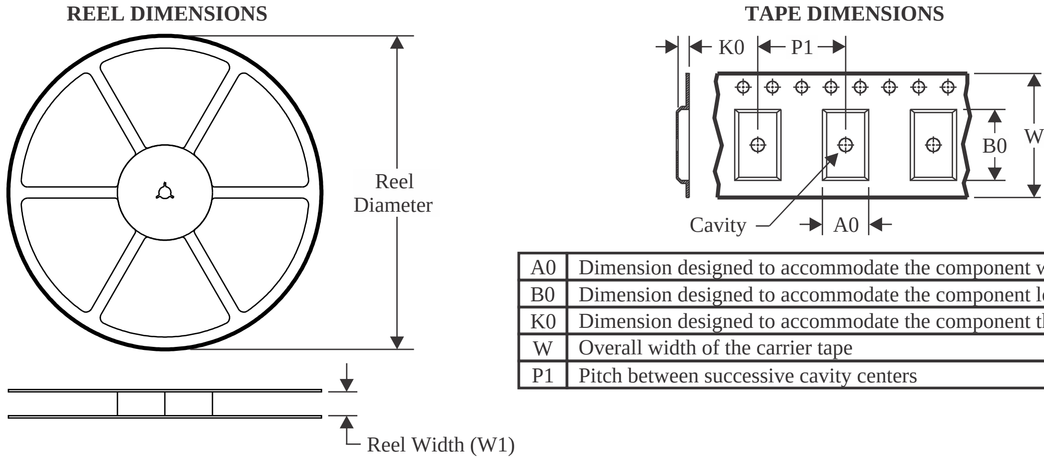
OTHER QUALIFIED VERSIONS OF DAC7551 :

- Automotive : DAC7551-Q1

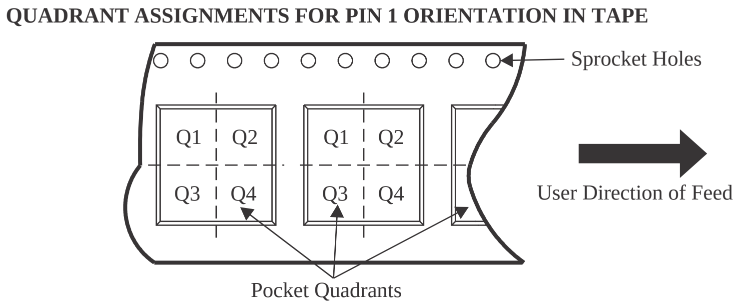
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



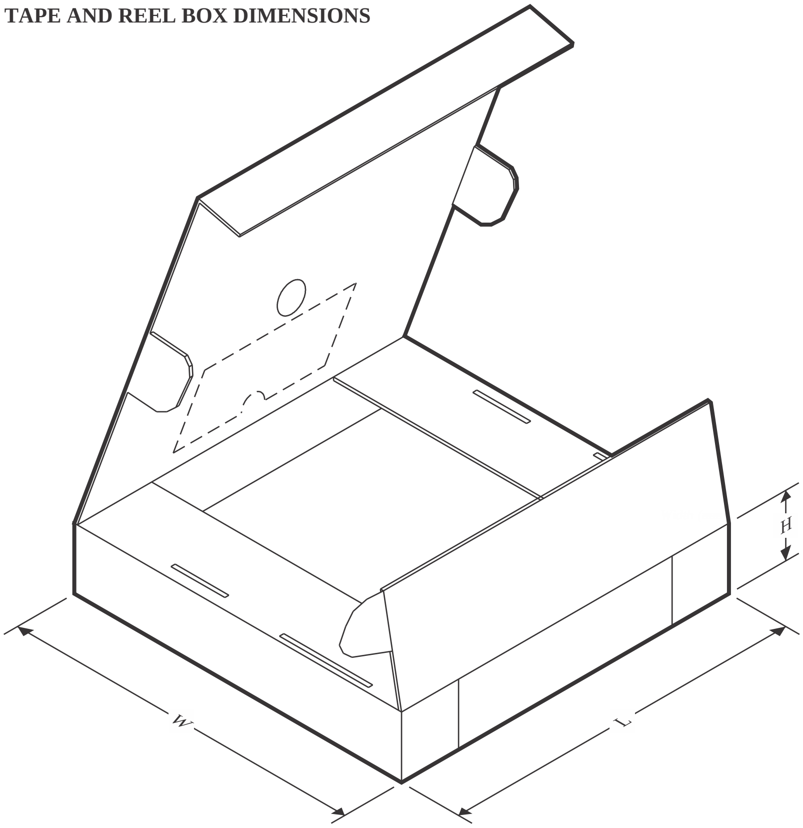
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7551IDRNR	USON	DRN	12	3000	330.0	12.4	2.3	3.3	0.7	4.0	12.0	Q1
DAC7551IDRNT	USON	DRN	12	250	180.0	12.5	2.3	3.3	0.7	4.0	12.0	Q1

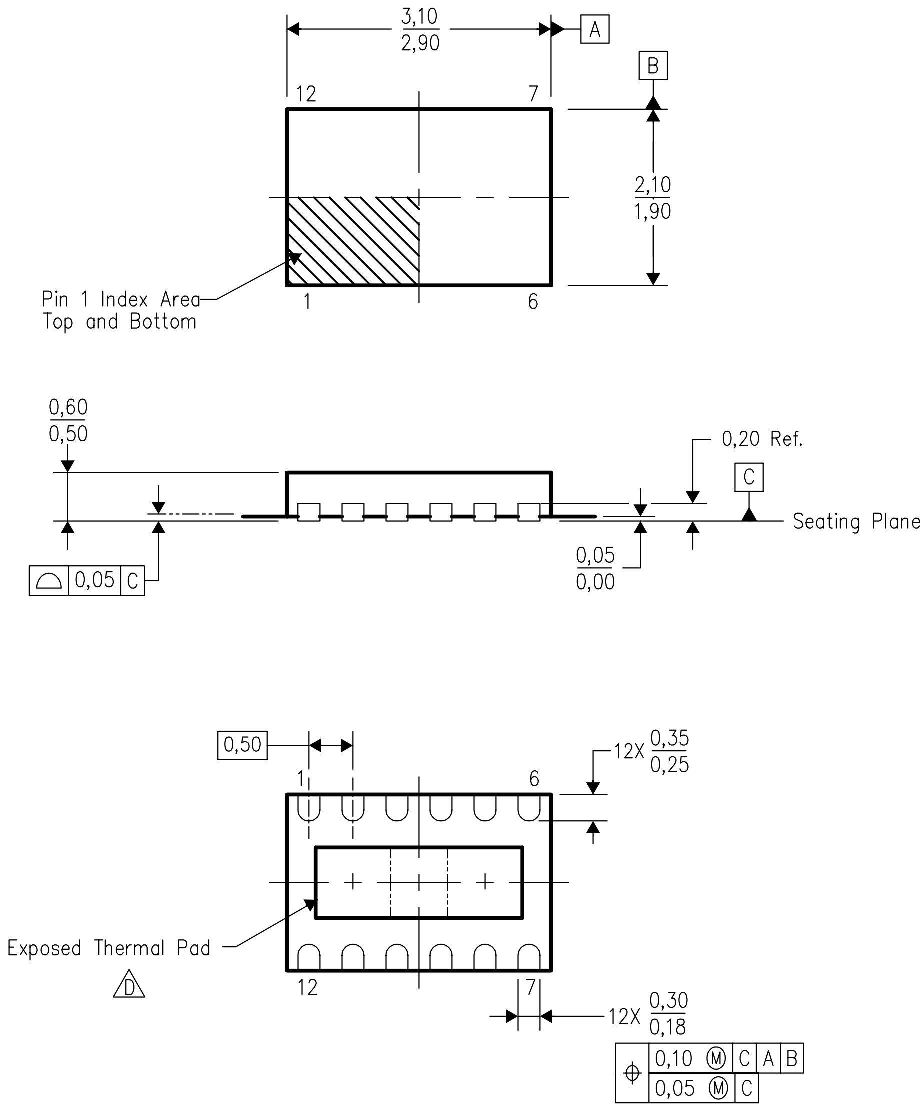
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7551IDRNR	USON	DRN	12	3000	338.0	355.0	50.0
DAC7551IDRNT	USON	DRN	12	250	205.0	200.0	33.0

DRN (R-PDSO-N12) PLASTIC SMALL OUTLINE



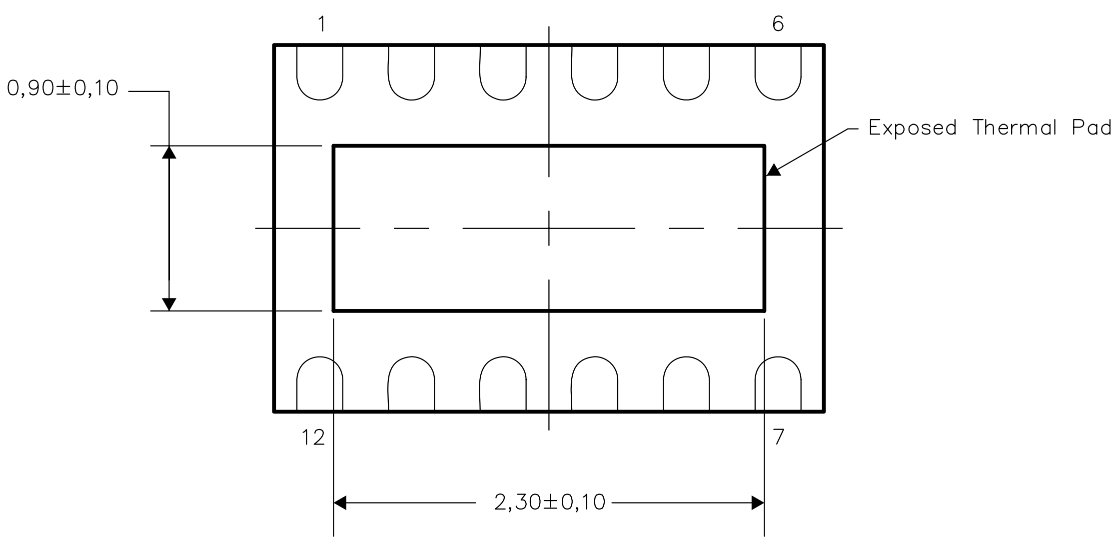
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. SON (Small Outline No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO-229.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

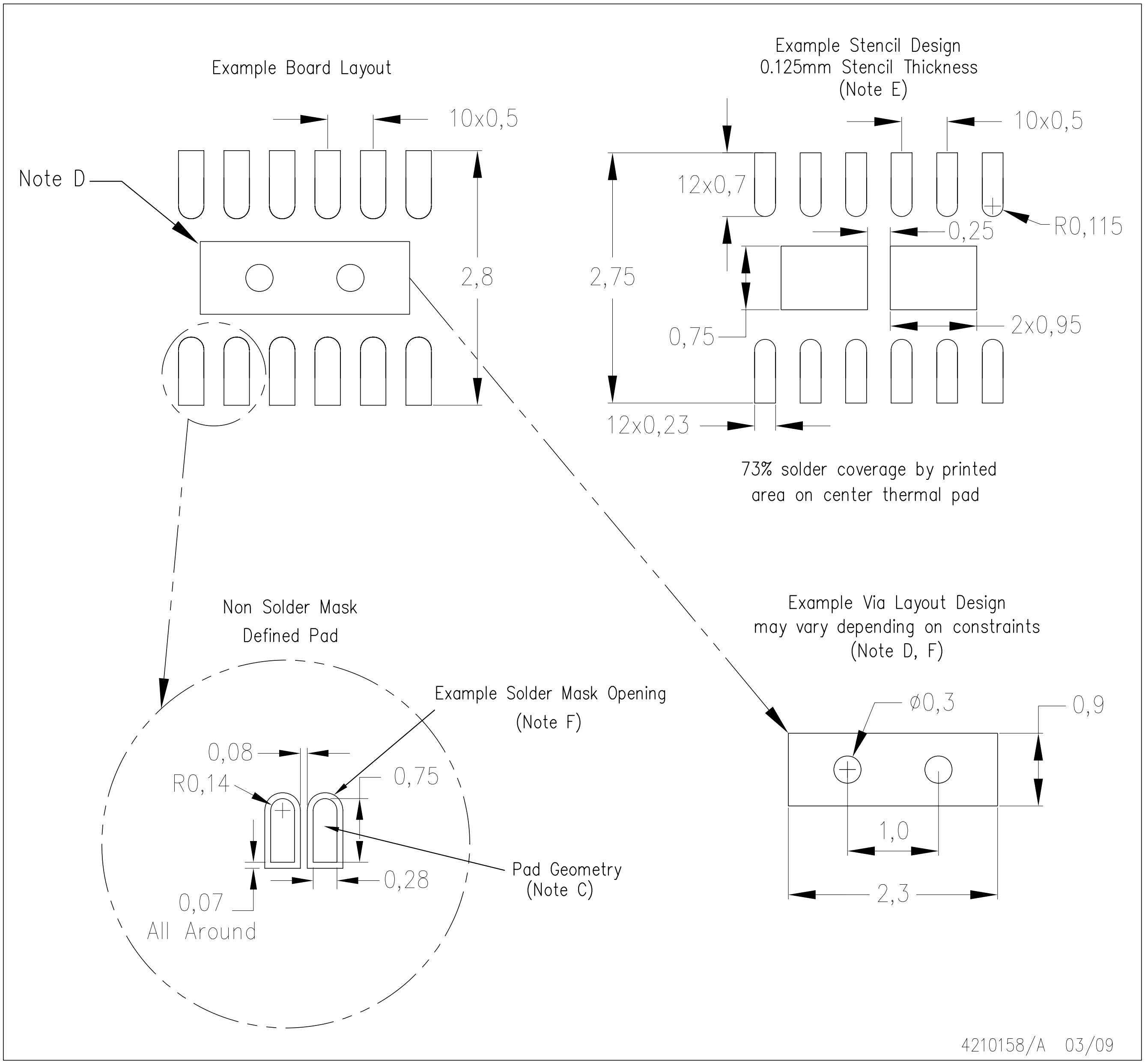


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRN (R–PUSON–N12)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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