CSD85302L 20 V Dual N-Channel NexFET™ Power MOSFET

1 Features

- Common Drain Configuration
- Low On-Resistance
- Small Footprint of 1.35 mm × 1.35 mm
- Pb Free and Halogen Free
- RoHS Compliant
- ESD HBM Protection >2.5 kV

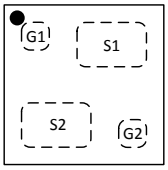
2 Applications

- USB Type-C/PD
- Battery Management
- Battery Protection

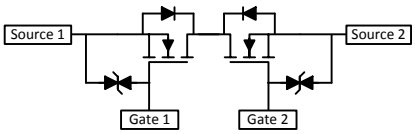
3 Description

This 20 V, 18.7 mΩ, 1.35 mm × 1.35 mm LGA Dual NexFET™ power MOSFET is designed to minimize resistance in the smallest footprint. Its small footprint and common drain configuration make the device ideal for battery-powered applications in small handheld devices.

Top View



Configuration



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{S1S2}	Source-to-Source Voltage	20		V
Q_g	Gate Charge Total (4.5 V)	6		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.4		nC
$R_{S1S2(on)}$	Source-to-Source On-Resistance	V_{GS} = 2.5 V	29	mΩ
		V_{GS} = 4.5 V	20	mΩ
		V_{GS} = 6.5 V	18.7	mΩ
$V_{GS(th)}$	Threshold Voltage	0.9		V

Ordering Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD85302L	3000	7-Inch Reel	1.35 × 1.35 mm Land Grid Array (LGA) Package	Tape and Reel
CSD85302LT	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

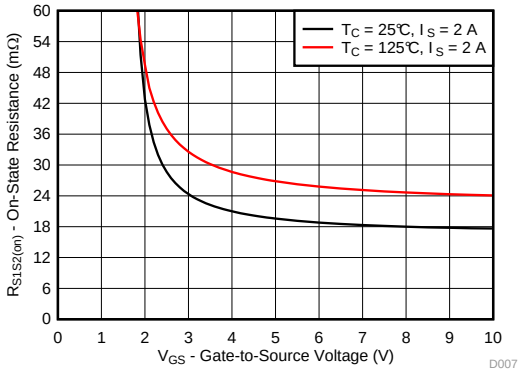
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{S1S2}	Source-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_S	Continuous Source Current(1)	7	A
I_{SM}	Pulsed Source Current(2)	37	A
P_D	Power Dissipation(1)	1.7	W
$V_{(ESD)}$	Human Body Model (HBM)	2.5	kV
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Typical $R_{\theta JA}$ = 75°C/W when mounted on a 1 inch^2, 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max $R_{\theta JA}$ = 90°C/W, pulse duration ≤100 µs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge

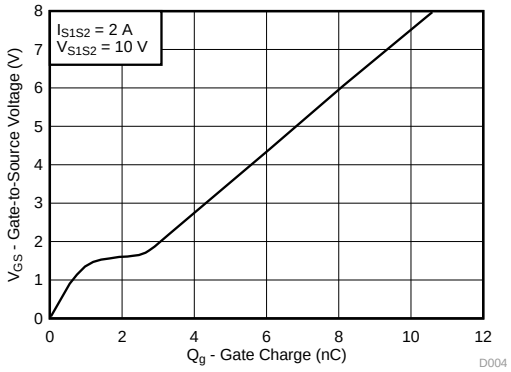


Table of Contents

4 Revision History

DATE	REVISION	NOTES
November 2015	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{S1S2}	Source-to-source voltage	V_{GS} = 0 V, I_S = 250 µA	20			V
I_{S1S2}	Source-to-source leakage current	V_{GS} = 0 V, V_{S1S2} = 16 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{S1S2} = 0 V, V_{GS} = 6 V			0.5	µA
		V_{S1S2} = 0 V, V_{GS} = 10V			4	µA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{S1S2} = V_{GS}, I_S = 250 µA	0.68	0.9	1.3	V
$R_{S1S2(on)}$	Source-to-source on-resistance	V_{GS} = 2.5 V, I_S = 2 A	20	29	36	mΩ
		V_{GS} = 4.5 V, I_S = 2 A	14	20	24	mΩ
		V_{GS} = 6.5 V, I_S = 2 A	13	18.7	22.5	mΩ
g_{fs}	Transconductance	V_{S1S2} = 2 V, I_S = 2 A		19		S
DYNAMIC CHARACTERISTICS(1)						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{S1S2} = 10 V, f = 1 MHz		718	933	pF
C_{oss}	Output capacitance			92	120	pF
C_{rss}	Reverse transfer capacitance			61	79	pF
Q_g	Gate charge total (4.5 V)	V_{S1S2} = 10 V, I_S = 2 A		6.0	7.8	nC
Q_{gd}	Gate charge gate-to-drain			1.4		nC
Q_{gs}	Gate charge gate-to-source			1.2		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.6		nC
Q_{oss}	Output charge	V_{S1S2} = 10 V, V_{GS} = 0 V		2.3		nC
$t_{d(on)}$	Turn-on delay time	V_{S1S2} = 10 V, V_{GS} = 4.5 V, I_{S1S2} = 2 A, R_G = 0 Ω		37		ns
t_r	Rise time			54		ns
$t_{d(off)}$	Turn-off delay time			173		ns
t_f	Fall time			99		ns

(1) Charge and timing values specified are per single FET.

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		75		°C/W
	Junction-to-ambient thermal resistance(2)		175		°C/W

(1) Device mounted on FR4 material with 1 $inch^2$ (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

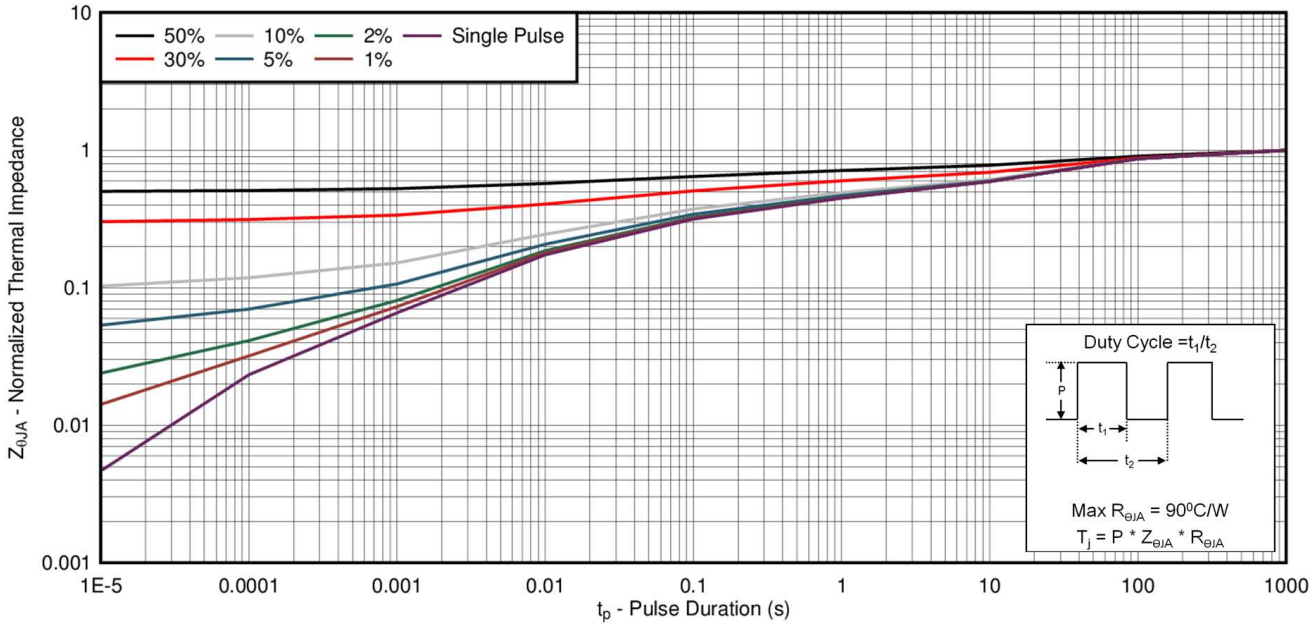


Figure 1. Transient Thermal Impedance

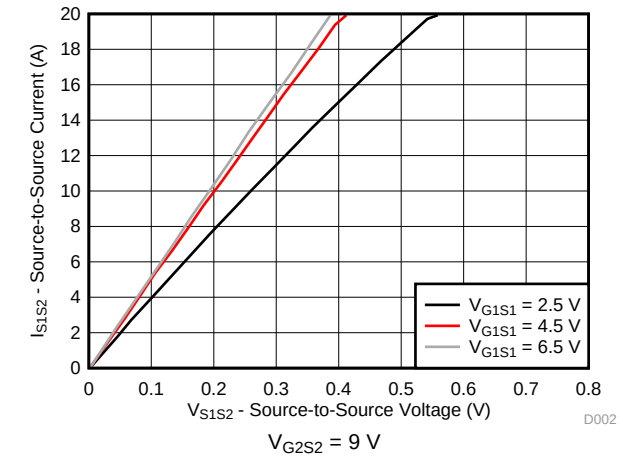


Figure 2. Saturation Characteristics

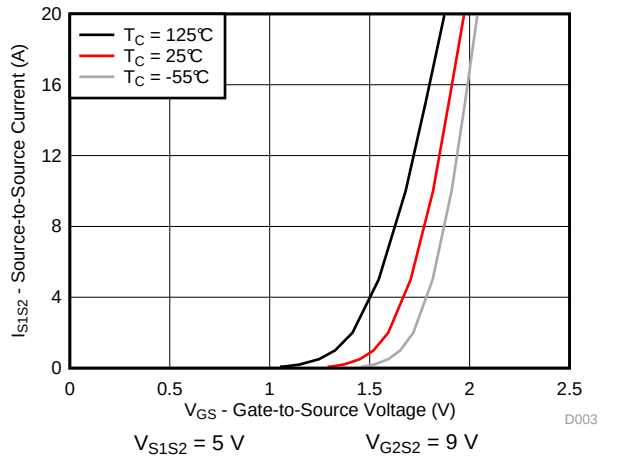


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

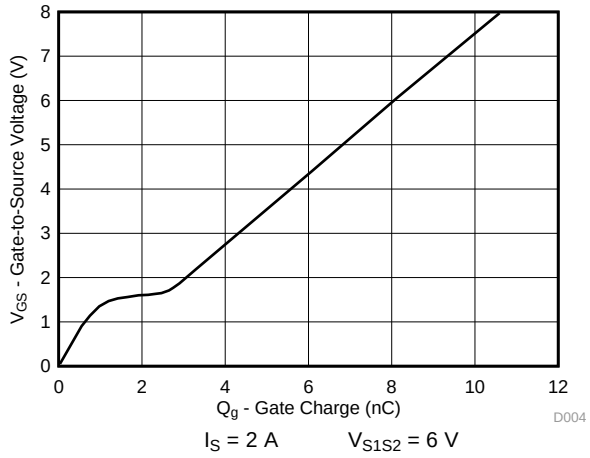


Figure 4. Gate Charge

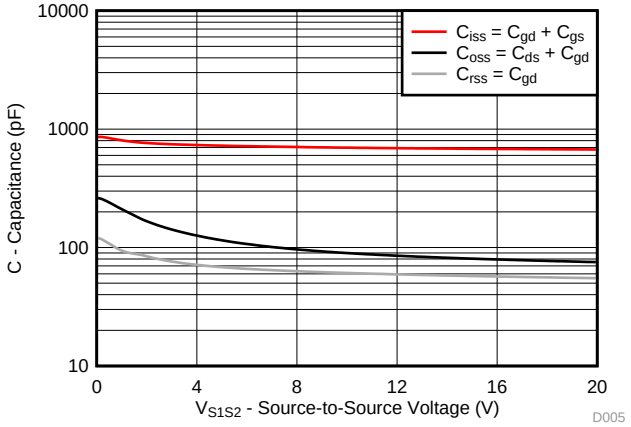


Figure 5. Capacitance

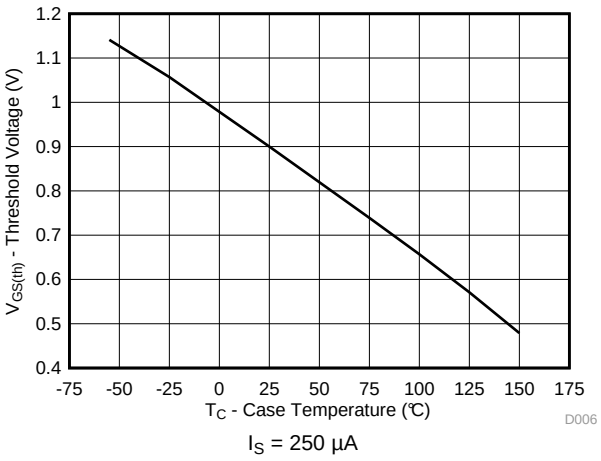


Figure 6. Threshold Voltage vs Temperature

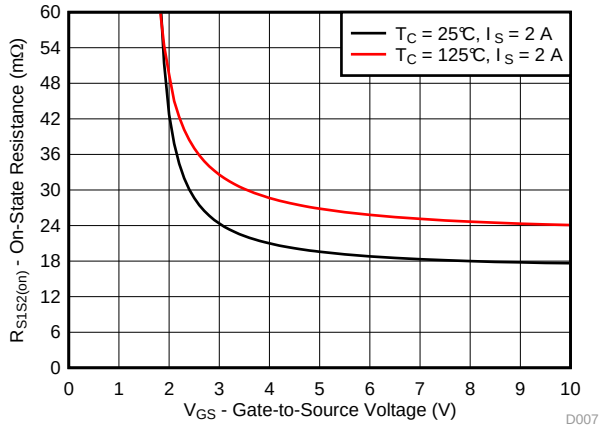


Figure 7. On-State Source-to-Source Resistance vs Gate-to-Source Voltage

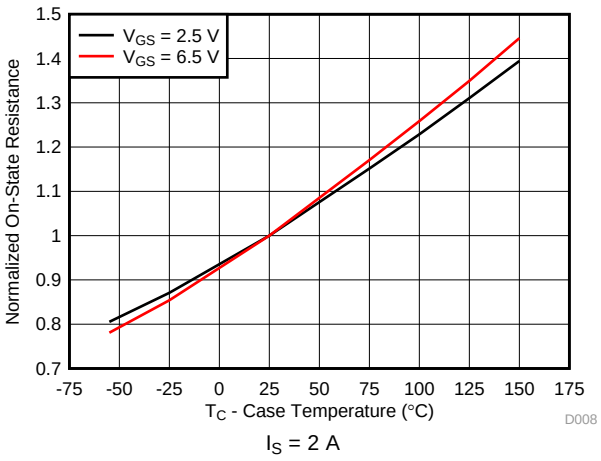


Figure 8. Normalized On-State Resistance vs Temperature

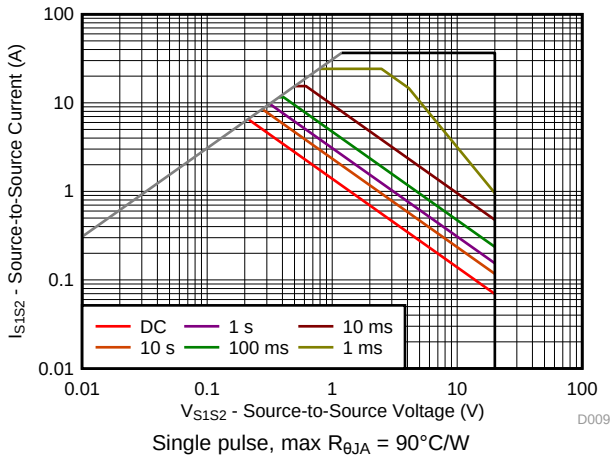


Figure 9. Maximum Safe Operating Area

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

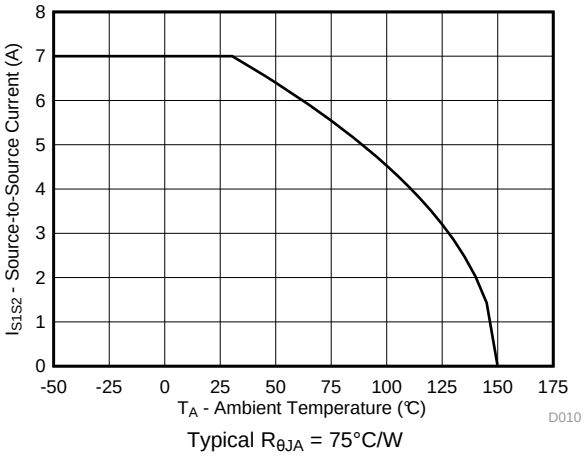


Figure 10. Maximum Source Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

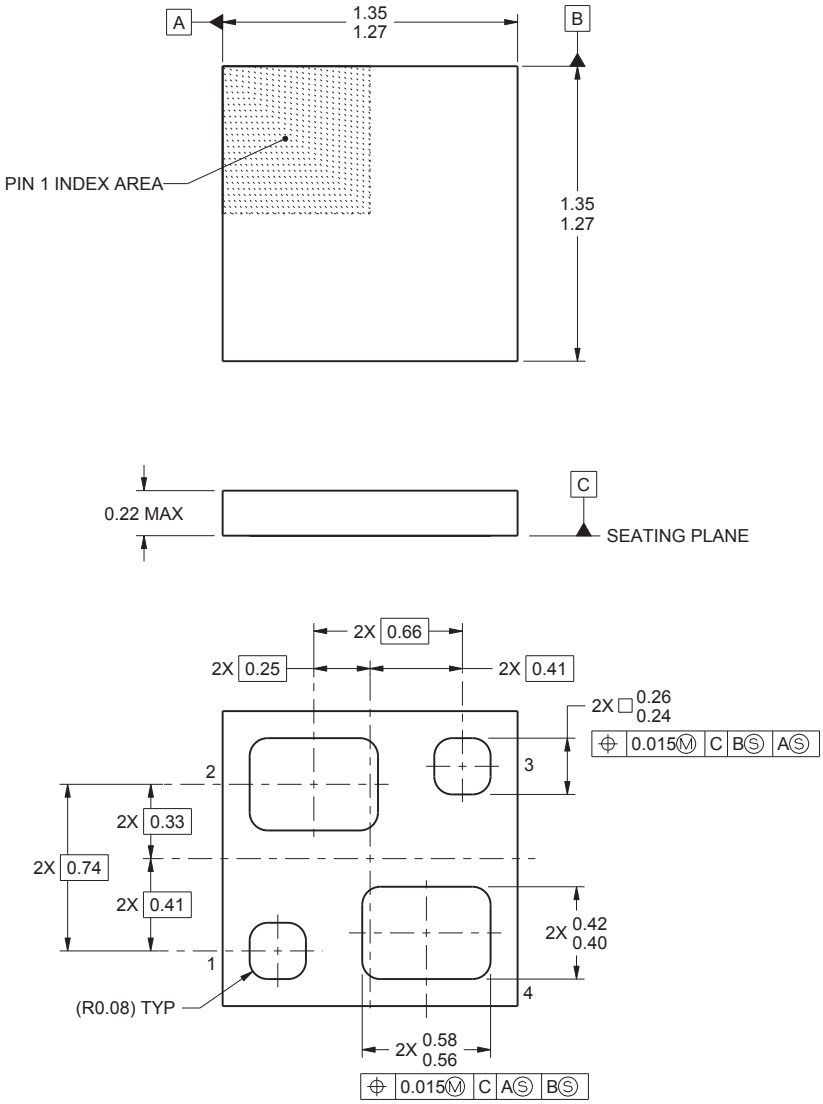
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Dimensions

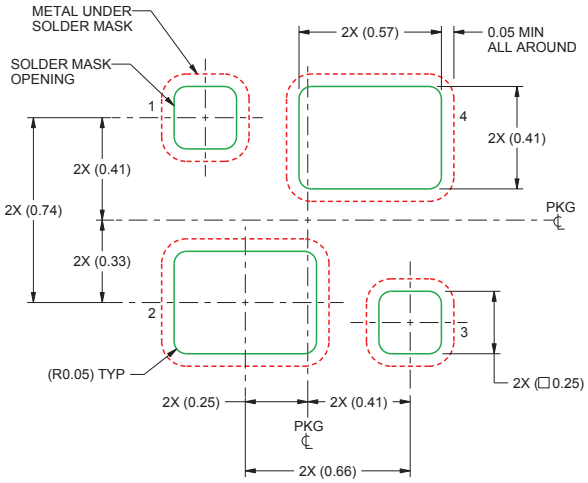


Pin Configuration

PIN NUMBER	NAME
1	G1
2	S2
3	G2
4	S1

1. All linear dimensions are in millimeters.

7.2 Recommended PCB Pattern

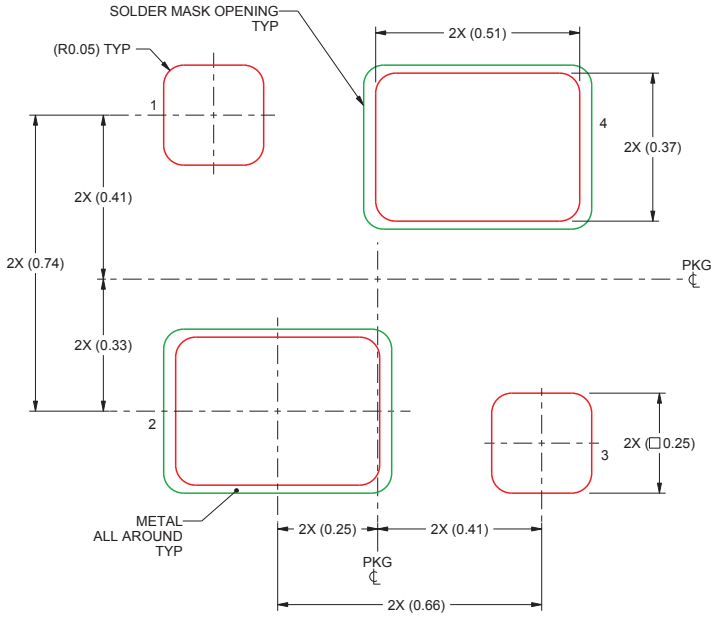


Land Pattern Example

Solder Mask Defined

Scale: 50X

7.3 Recommended Stencil Pattern



Solder Paste Example

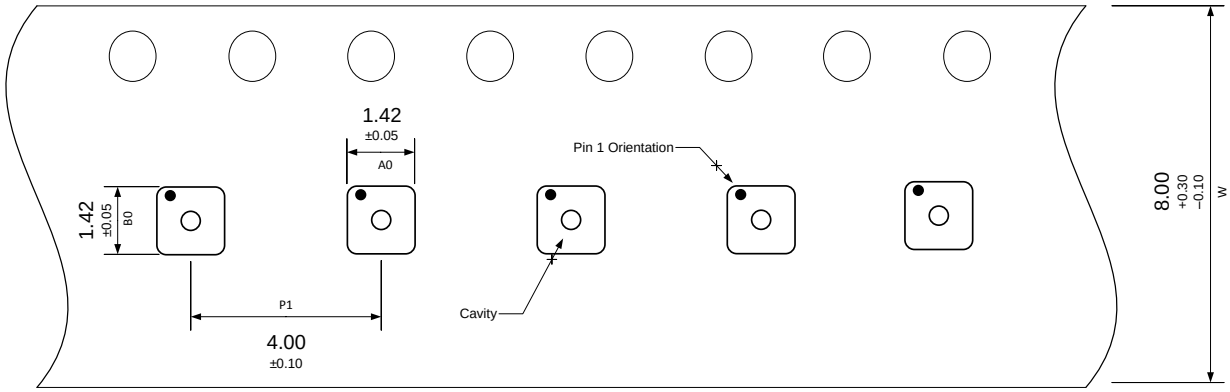
Based on 0.1 mm thick stencil

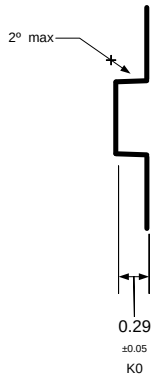
Pads 2 and 4: 81% printed on solder coverage by area

Scale: 80X

1. All linear dimensions are in millimeters.
2. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7.4 Q3A Tape and Reel Information





All Measurements in Millimeters (mm)

Notes: 1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. MSL1 260°C (IR and convection) PbF-reflow compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD85302L	Active	Production	PICOSTAR (YME) | 4	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	85302
CSD85302L.B	Active	Production	PICOSTAR (YME) | 4	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	85302
CSD85302LT	Active	Production	PICOSTAR (YME) | 4	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	85302
CSD85302LT.B	Active	Production	PICOSTAR (YME) | 4	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	85302

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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