ADS61Bx9 14-/12-Bit, 250MSPS ADCs With Integrated Analog Buffer

1 Features

- Integrated high impedance analog input buffer
- Maximum sample rate: 250MSPS
- 14-Bit resolution – ADS61B49
- 12-Bit resolution – ADS61B29
- 790mW Total power dissipation at 250MSPS
- Double Data Rate (DDR) LVDS and parallel CMOS output options
- Programmable fine gain up to 6dB for SNR/SFDR trade-off and $1V_{pp}$ full-scale operation
- DC offset correction
- Supports input clock amplitude down to $400mV_{PP}$ differential
- 48-QFN package (7mm × 7mm)
- Pin compatible with ADS6149 family

2 Applications

- Multicarrier, wide bandwidth communications
- Wireless multi-carrier communications infrastructure
- Software defined radio
- Power amplifier linearization feedback ADC
- 802.16d/e
- Test and measurement instrumentation
- High definition video
- Medical imaging
- Radar systems

3 Description

The ADS61B49 (ADS61B29) is a 14-bit (12-bit) A/D converter with a sampling rate up to 250 MSPS. It combines high dynamic performance and low power consumption in a compact 48-QFN package. An integrated analog buffer makes it well-suited for multi-carrier, wide bandwidth communications applications. The buffer maintains constant performance and input impedance across a wide frequency range.

The ADS61B49 (ADS61B29) has fine gain options that can be used to improve SFDR performance at lower full-scale input ranges. It includes a dc offset correction loop that can be used to cancel the ADC offset. Both Double Data Rate (DDR) LVDS and parallel CMOS digital output interfaces are available. At lower sampling rates, the ADC automatically operates at scaled down power with no loss in performance.

It includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. The device is specified over the industrial temperature range (–40°C to 85°C).

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS61B49	RGZ (QFN-48)	7.0mm × 7.0mm
ADS61B29	RGZ (QFN-48)	7.0mm × 7.0mm

(1) For the most current package and ordering information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

	ANALOG BUFFER	250 MSPS	210 MSPS
ADS614x 14-Bit Family	NO	ADS6149	ADS6148
	YES	ADS61B49	
ADS612Xx 12-Bit Family	NO	ADS6129	ADS6128
	YES	ADS61B29	

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4 Pin Configuration and Functions

4.1 Pin Configuration and Functions (LVDS Mode) — ADS61B49 and ADS61B29

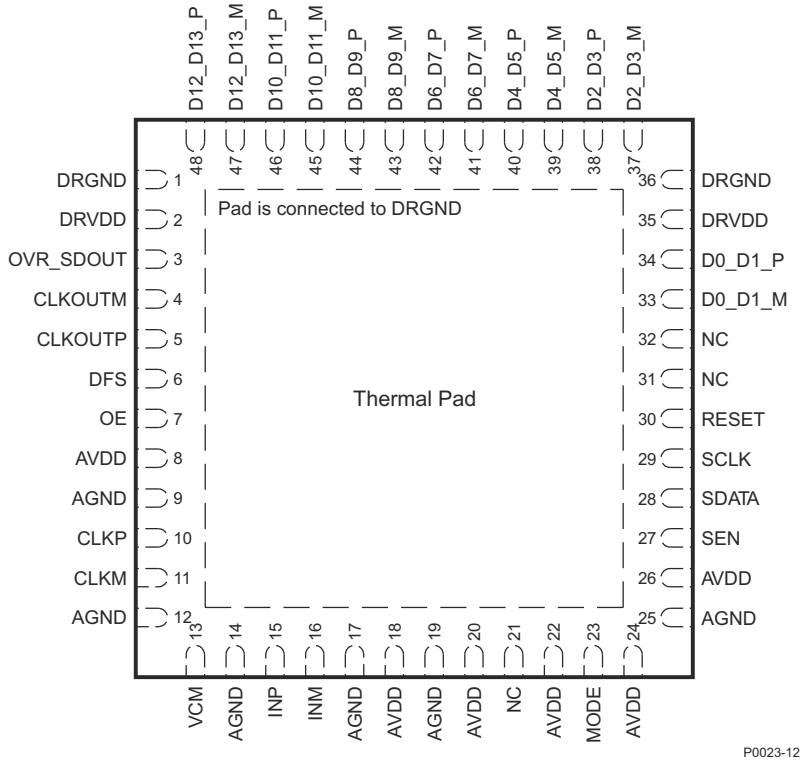


Figure 4-1. Pin Configuration (LVDS mode) — ADS61B49

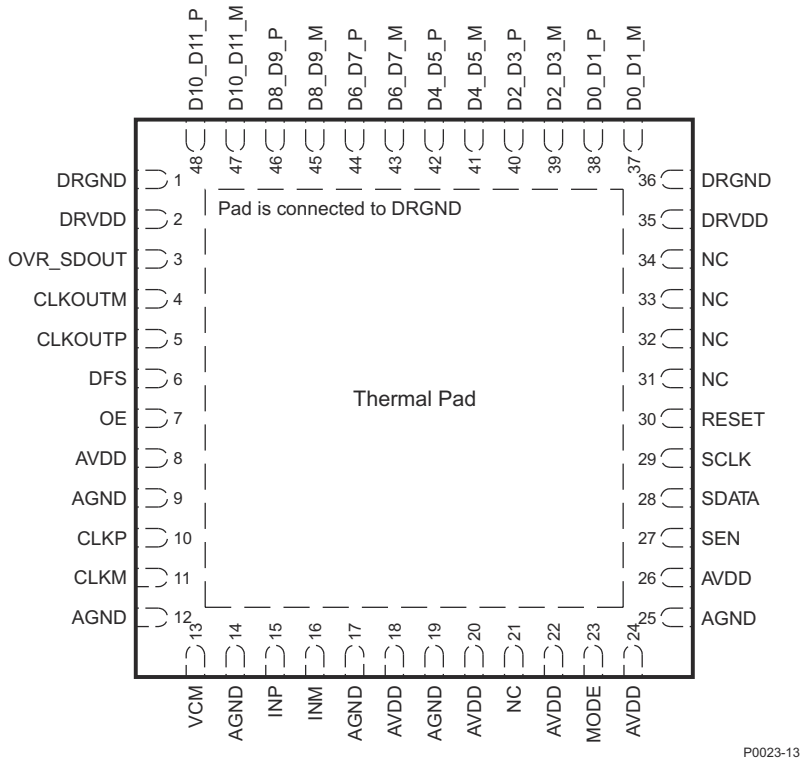


Figure 4-2. Pin Configuration (LVDS mode) — ADS61B29

Table 4-1. Pin Functions

PIN		I/O	NO. of PINS	DESCRIPTION
NAME	NO.			
AVDD	8, 18, 20, 22, 24, 26	I	6	3.3-V analog power supply
AGND	9, 12, 14, 17, 19, 25	I	6	Analog ground
CLKP, CLKM	10, 11	I	2	Differential clock input
INP, INM	15, 16	I	2	Differential analog input
VCM	13	IO	1	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.
RESET	30	I	1	Serial interface RESET input. When using serial interface mode, the user MUST initialize the internal registers through a hardware RESET by applying a high-going pulse on this pin or by using the software reset option. Refer to the *SERIAL INTERFACE* section. In parallel interface mode, the user has to tie the RESET pin permanently high. (SDATA and SEN are used as parallel pin controls in this mode.) The pin has an internal 100-kΩ pull-down resistor.
SCLK	29	I	1	Serial interface clock input. The pin has an internal 100-kΩ pull-down resistor.
SDATA	28	I	1	This pin functions as the serial interface data input when RESET is low. It functions as the power-down control pin when RESET is tied high. See Table 6-3 for detailed information. The pin has an internal 100-kΩ pull-down resistor.
SEN	27	I	1	This pin functions as the serial interface enable input when RESET is low. It functions as the output clock edge control when RESET is tied high. See Table 6-4 for detailed information. The pin has an internal 100-kΩ pull-up resistor to AVDD.
OE	7	I	1	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD
DFS	6	I	1	Data format select input. This pin sets the data format (2s complement or offset binary) and the LVDS/CMOS output interface type. See Table 6-5 for detailed information.
MODE[1]	23	I	1	Not used. See Table 6-6 and note below for detailed information.
CLKOUTP	5	O	1	Differential output clock, true
CLKOUTM	4	O	1	Differential output clock, complement
D0_D1_P	See Figure 4-1 and Figure 4-2	O	1	Differential output data D0 and D1 multiplexed, true
D0_D1_M		O	1	Differential output data D0 and D1 multiplexed, complement
D2_D3_P		O	1	Differential output data D2 and D3 multiplexed, true
D2_D3_M		O	1	Differential output data D2 and D3 multiplexed, complement
D4_D5_P		O	1	Differential output data D4 and D5 multiplexed, true
D4_D5_M		O	1	Differential output data D4 and D5 multiplexed, complement
D6_D7_P		O	1	Differential output data D6 and D7 multiplexed, true
D6_D7_M		O	1	Differential output data D6 and D7 multiplexed, complement
D8_D9_P		O	1	Differential output data D8 and D9 multiplexed, true
D8_D9_M		O	1	Differential output data D8 and D9 multiplexed, complement
D10_D11_P		O	1	Differential output data D10 and D11 multiplexed, true
D10_D11_M		O	1	Differential output data D10 and D11 multiplexed, complement
D12_D13_P		O	1	Differential output data D12 and D13 multiplexed, true
D12_D13_M		O	1	Differential output data D12 and D13 multiplexed, complement
OVR_SDOUT	3	O	1	It is a CMOS output with logic levels determined by the DRVDD supply. It functions as an out-of-range indicator after a reset and when register bit <SERIAL READOUT> = 0. It functions as the serial register readout pin when register bit <SERIAL READOUT> = 1.
DRVDD	2, 35	I	2	1.8-V digital and output buffer supply
DRGND	1, 36, PAD	I	2	Digital and output buffer ground

Table 4-1. Pin Functions (continued)

PIN		I/O	NO. of PINS	DESCRIPTION
NAME	NO.			
NC	See Figure 4-1 and Figure 4-2			Do not connect

(1) In the next generation pin-compatible ADC family, MODE is converted to a digital control pin for certain reserved functions. So, the selection of the internal or external reference and low speed functions are supported using MODE. In a system board using the ADS61x9/x8, the MODE pin can be routed to a digital controller. This avoids board modification if migrating to the next generation ADC.

4.2 Pin Configuration and Functions (CMOS Mode) – ADS61B49 and ADS61B29

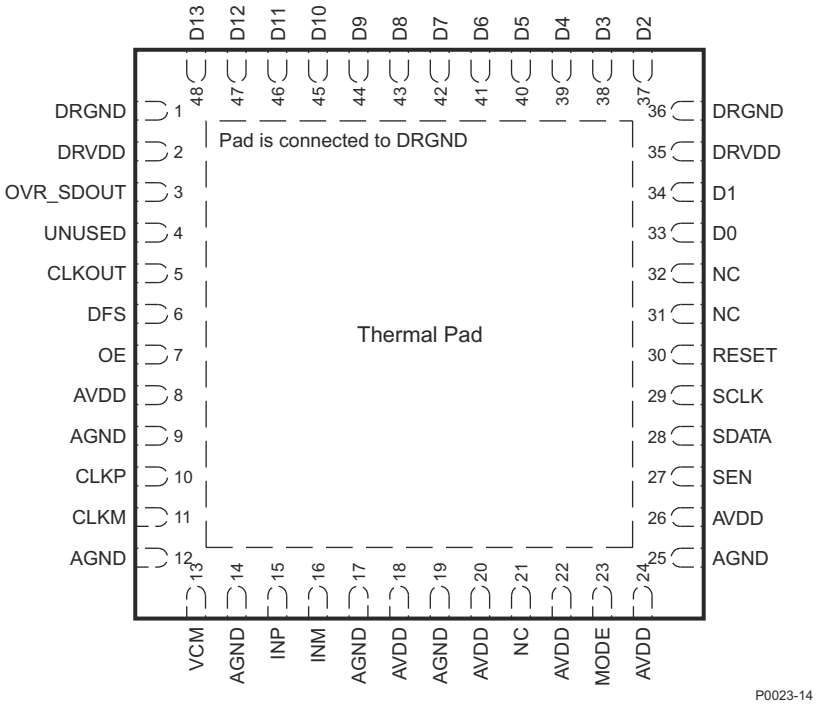


Figure 4-3. Pin Configuration (CMOS mode) – ADS61B49

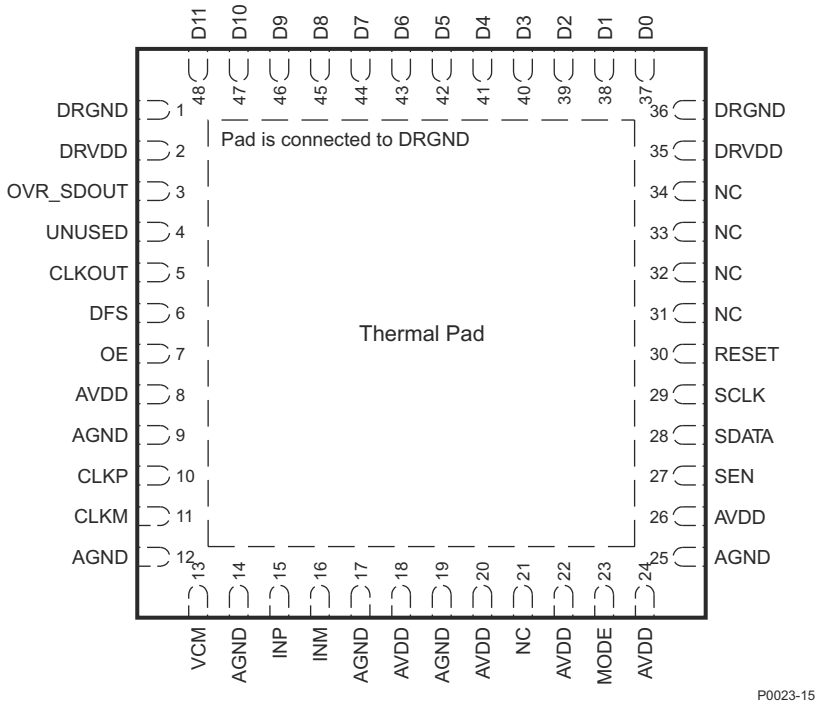


Figure 4-4. Pin Configuration (CMOS mode) – ADS61B29

Table 4-2. Pin Functions

PIN		I/O	NO. of PINS	DESCRIPTION
NAME	NO.			
AVDD	8, 18, 20, 22, 24, 26	I	6	3.3-V analog power supply
AGND	9, 12, 14, 17, 19, 25	I	6	Analog ground
CLKP, CLKM	10, 11	I	2	Differential clock input
INP, INM	15, 16	I	2	Differential analog input
VCM	13	IO	1	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.
RESET	30	I	1	Serial interface RESET input. When using serial interface mode, the user MUST initialize the internal registers through a hardware RESET by applying a high-going pulse on this pin or by using the software reset option. Refer to the *SERIAL INTERFACE* section. In parallel interface mode, the user has to tie the RESET pin permanently high. (SDATA and SEN are used as parallel pin controls in this mode.) The pin has an internal 100-kΩ pull-down resistor.
SCLK	29	I	1	Serial interface clock input. The pin has an internal 100-kΩ pull-down resistor.
SDATA	28	I	1	This pin functions as the serial interface data input when RESET is low. It functions as the power-down control pin when RESET is tied high. See Table 6-3 for detailed information. The pin has an internal 100-kΩ pull-down resistor.
SEN	27	I	1	This pin functions as the serial interface enable input when RESET is low. It functions as the output clock edge control when RESET is tied high. See Table 6-4 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DVDD.

Table 4-2. Pin Functions (continued)

PIN		I/O	NO. of PINS	DESCRIPTION
NAME	NO.			
DFS	6	I	1	Data format select input. This pin sets the data format (2s complement or offset binary) and the LVDS/CMOS output interface type. See Table 6-5 for detailed information.
MODE(1)	23	I	1	Not used. See Table 6-6 and note below for detailed information.
CLKOUT	5	O	1	CMOS output clock
OE	7	I	1	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD
D0–D13	See Figure 4-3 and Figure 4-4	O	14/12	14-bit/12-bit CMOS output data
OVR_SDOUT	3	O	1	It is a CMOS output with logic levels determined by the DRVDD supply. It functions as an out-of-range indicator after a reset and when register bit <SERIAL READOUT> = 0. It functions as the serial register readout pin when <SERIAL READOUT> = 1.
DRVDD	2, 35	I	2	1.8-V digital and output buffer supply
DRGND	1, 36, PAD	I	2	Digital and output buffer ground
UNUSED	4		1	Unused pin in CMOS mode
NC	See Figure 4-3 and Figure 4-4			Do not connect

(1) In the next generation pin-compatible ADC family, MODE is converted to a digital control pin for certain reserved functions. So, the selection of the internal or external reference and low speed functions are supported using MODE. In a system board using the ADS61x9/x8, the MODE pin can be routed to a digital controller. This avoids board modification while migrating to the next generation ADC.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
	Supply Voltage, AVDD	-0.3 to 3.9	V
	Supply Voltage, DRVDD	-0.3 to 2.2	V
	Voltage between AGND and DRGND	-0.3 to 0.3	V
	Voltage between AVDD to DRVDD (when AVDD leads DRVDD)	0 to 3.3	V
	Voltage between DRVDD to AVDD (when DRVDD leads AVDD)	-1.5 to 1.8	V
	Voltage applied to analog input pins - INP, INM	-0.3 to minimum (3.6, AVDD + 0.3)	V
	Voltage applied to input pins - CLKP, CLKM(2), RESET, SCLK, SDATA, SEN, DFS and MODE	-0.3 to (AVDD + 0.3)	V
T_A	Operating free-air temperature range	-40 to 85	°C
T_J	Max Operating junction temperature	125	°C
T_{stg}	Storage temperature range	-65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is < 0.3V.) This prevents the ESD protection diodes at the clock input pins from turning on.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		3	3.3	3.6	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
	Differential input voltage range			2		V_{pp}
	Input common-mode voltage (different than ADS6149 family)			2.3 ±0.1		V
	Maximum analog input frequency with 2Vpp input amplitude(1)			500		MHz
	Maximum analog input frequency with 1Vpp input amplitude(1)			800		MHz
CLOCK INPUT						
	Input clock sample rate		1		250	MSPS
	Input clock amplitude differential (V_{CLKP}–V_{CLKM})	Sine wave, ac-coupled	0.3	1.5		V_{pp}
		LVPECL, ac-coupled		1.6		
		LVDS, ac-coupled		0.7		
		LVCMOS, single-ended, ac-coupled		3.3		V
	Input clock duty cycle		40%	50%	60%	
DIGITAL OUTPUTS						
C_L	Maximum external load capacitance from each output pin to DRGND			5		pF
R_L	Differential load resistance between the LVDS output pairs (LVDS mode)			100		Ω
T_A	Operating free-air temperature		–40		85	°C

(1) See the *Theory of Operations* in the applications section.

5.3 Electrical Characteristics – ADS61B49 and ADS61B29

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode unless otherwise noted.
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 1.8 V

PARAMETER		ADS61B49/ADS61B29 250 MSPS			UNIT
		MIN	TYP	MAX	
ANALOG INPUT					
	Differential input voltage range		2		V_{PP}
	Differential input resistance (at dc), See Figure 7-2		10		kΩ
	Differential input capacitance, See Figure 7-3		2		pF
	Analog input bandwidth		750		MHz
	Analog Input common-mode current (per input pin)		2		µA
	VCM common-mode output voltage (different than ADS6149 family)		2.3		V
	VCM output current capability		±4		mA
DC ACCURACY					
	Offset error	-15	±2	+15	mV
	Temperature coefficient of offset error		0.005		mV/°C
	Variation of offset error with supply		0.3		mV/V
E_{GREF}	Gain error due to internal reference inaccuracy alone	-2.5	±0.2	+2.5	%FS
E_{GCHAN}	Gain error of channel alone		0.2		%FS
	Temperature coefficient of EGCHAN		.001		Δ%/°C
POWER SUPPLY					
I_{AVDD}	Analog supply current		200		mA
I_{DRVDD}	Output buffer supply current, LVDS interface with 100Ω external termination		70		mA
	Output buffer supply current, CMOS interface F_{in} = 3MHz, 10pF external load capacitance		56		mA
	Analog power		660	730	mW
	Digital power LVDS interface		130	160	mW
	Digital power CMOS interface, F_{in} = 3MHz, 10pF external load capacitance		101		mW
	Global power down		20	75	mW
	Standby		120		mW

5.4 Electrical Characteristics – ADS61B49 and ADS61B29

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode unless otherwise noted.
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 1.8 V

PARAMETER		ADS61B49 250 MSPS			ADS61B29 250 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SNR Signal-to-noise ratio, **LVDS**	F_{in} = 20MHz		72.3			70.1		dBFS
	F_{in} = 80MHz		72			69.8		
	F_{in} = 100MHz		71.6			69.6		
	F_{in} = 170MHz	68.5	70.7		66.5	69		
	F_{in} = 300MHz		69			67.8		
SINAD Signal-to-noise and distortion ratio, **LVDS**	F_{in} = 20MHz		72.5			70.3		dBFS
	F_{in} = 80MHz		71.8			69.7		
	F_{in} = 100MHz		71.6			69.5		
	F_{in} = 170MHz	67.5	70		65.7	68.4		
	F_{in} = 300MHz		67.1			66.3		
ENOB Effective number of bits	F_{in} = 170MHz (using SINAD in dBFS)		11.3			11.1		LSB
DNL Differential non-linearity		-0.95	±0.4	1	-0.5	±0.2	1	LSB
INL Integrated non-linearity		-5	±2	5	-2.5	±1	2.5	LSB

5.5 Electrical Characteristics – ADS61B49 and ADS61B29

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode unless otherwise noted.
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 1.8 V

PARAMETER		ADS61B49/ADS61B29 250 MSPS			UNIT
		MIN	TYP	MAX	
SFDR Spurious free dynamic range	F_{in} = 20MHz		92		dBc
	F_{in} = 80MHz		86		
	F_{in} = 100MHz		86		
	F_{in} = 170MHz (all spurs/harmonics)	74	84		
	F_{in} = 170MHz (excluding 2nd harmonic)	77	87		
	F_{in} = 300MHz		76		
THD Total harmonic distortion	F_{in} = 20MHz		89		dBc
	F_{in} = 80MHz		83		
	F_{in} = 100MHz		82		
	F_{in} = 170MHz	72	79		
	F_{in} = 300MHz		73		
HD2, Second harmonic distortion	F_{in} = 20MHz		94		dBc
	F_{in} = 80MHz		90		
	F_{in} = 100MHz		88		
	F_{in} = 170MHz	74	84		
	F_{in} = 300MHz		76		
HD3 Third harmonic distortion	F_{in} = 20MHz		93		dBc
	F_{in} = 80MHz		86		
	F_{in} = 100MHz		85		
	F_{in} = 170MHz	77	87		
	F_{in} = 300MHz		76		
Worst Spur Other than second, third harmonics	F_{in} = 20MHz		96		dBc
	F_{in} = 80MHz		94		
	F_{in} = 100MHz		94		
	F_{in} = 170MHz	80	92		
	F_{in} = 300MHz		90		
IMD 2-tone inter-modulation distortion	F1 = 46MHz, F2 = 50MHz, Each tone at –7dBFS		94		dBFS
	F1 = 185MHz, F2 = 190MHz, Each tone at –7dBFS		90		
Input overload recovery	Recovery to within 1% (of final value) for 6dB overload with sine wave input		1		Clock Cycles
PSRR AC power supply rejection ratio	For 100mV_{pp} signal on AVDD supply		25		dB

5.6 Digital Characteristics – ADS61B49 and ADS61B29

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 3.3 V, DRVDD = 1.8 V

PARAMETER		TEST CONDITIONS	ADS61B49/ADS61B29			UNIT
			MIN	TYP	MAX	
DIGITAL INPUTS – RESET, SCLK, SDATA, SEN(1)						
High-level input voltage		All digital inputs support 1.8V and 3.3V CMOS logic levels	1.3			V
Low-level input voltage					0.4	V
High-level input current	SDATA, SCLK(2)	V_{High} = 3.3V		16		µA
	SEN(3)	V_{High} = 3.3V		10		
Low-level input current	SDATA, SCLK	V_{Low} = 0V		0		µA
	SEN	V_{Low} = 0V		–20		
Input capacitance				4		pF
DIGITAL OUTPUTS – CMOS INTERFACE (Pins D0 to D13 and OVR_SDOUT)						
High-level output voltage		with I_{OH} = 1mA	DRVDD -0.1	DRVDD		V
Low-level output voltage		with I_{OL} = 1mA		0	0.1	V
Output capacitance (internal to device)				2		pF
DIGITAL OUTPUTS – LVDS INTERFACE (Pins D0_D1_P/M to D12_D13_P/M)(5)						
V_{ODH}, High-level output voltage(4)			275	350	425	mV
V_{ODL}, Low-level output voltage(4)			–425	–350	–275	mV
V_{OCM}, Common-mode output voltage		Capacitance inside the device, from either output to ground	1	1.2	1.3	V
Output capacitance				2		pF

(1) SCLK, SDATA, SEN function as digital input pins in serial configuration mode.
(2) SDATA, SCLK have internal 200kΩ pull-down resistor.
(3) SEN has internal 100kΩ pull-up resistor to AVDD.
(4) With external 100Ω termination
(5) OVR_SDOUT has CMOS output logic levels, determined by DRVDD voltage.

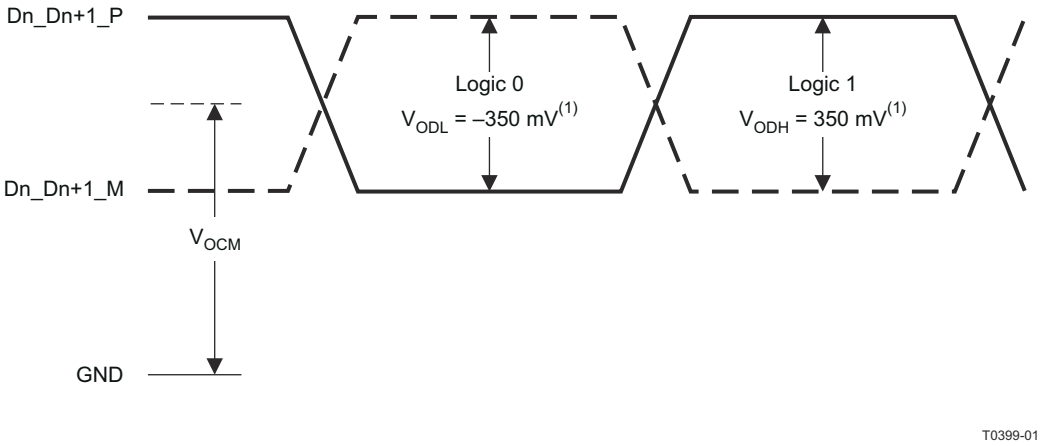


Figure 5-1. LVDS Voltage Levels

5.7 Timing Requirements – LVDS and CMOS Modes

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 5 pF(2), R_{LOAD} = 100 Ω(3), Low Speed mode disabled, unless otherwise noted.
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 1.7 V to 1.9 V.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay		0.7	1.2	1.7	ns
t_j	Aperture jitter			170		fs rms
	Wake-up time	Time to valid data after coming out of STANDBY mode		0.3	1	µs
		Time to valid data after coming out of PDN GLOBAL mode		25	100	µs
		Time to valid data after stopping and restarting the input clock		10		Clock Cycles
	ADC Latency(8)	Default, after reset		18		Clock Cycles
DDR LVDS MODE (4)						
t_{su}	Data setup time	Data valid (5) to zero-crossing of CLKOUTP	0.8	1.2		ns
t_h	Data hold time	Zero-crossing of CLKOUT to data becoming invalid(5)	0.25	0.6		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *80MSPS ≤ Sampling frequency ≤ 250MSPS*		0.2 × t_s + t_{delay}		ns
	t_{delay}		5	6.2	7.5	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP–CLKOUTM) *80MSPS ≤ Sampling frequency ≤ 250MSPS*		52%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100mV to 100mV Fall time measured from 100mV to –100mV *1MSPS ≤ Sampling frequency ≤ 250MSPS*	0.08	0.14	0.2	ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100mV to 100mV Fall time measured from 100mV to –100mV 1MSPS ≤ Sampling frequency ≤ 250MSPS	0.08	0.14	0.2	ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		40		ns
PARALLEL CMOS MODE(7)						
t_{START}	Input clock to data delay	Input clock rising edge cross-over to start of data valid(6)			3.2	ns
t_{DV}	Data valid time	Time interval of valid data(6)	0.7	1.5		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *80MSPS ≤ Sampling frequency ≤ 150MSPS*		0.78 × t_s + t_{delay}		ns
	t_{delay}		5	6.5	8	ns
	Output clock duty cycle	Duty cycle of differential clock, (CLKOUT) *80MSPS ≤ Sampling frequency ≤ 150MSPS*		50%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD, *1MSPS ≤ Sampling frequency ≤ 250MSPS*	0.7	1.2	2	ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD, *1MSPS ≤ Sampling frequency ≤ 150MSPS*	0.5	1	1.5	ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		20		ns

(1) Timing parameters are specified by design and characterization and not tested in production.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(5) Data valid refers to logic high of +100mV and logic low of –100mV.
(6) Data valid refers to logic high of 1.26V and logic low of 0.54V.
(7) For F_s > 150MSPS, it is recommended to use external clock for data capture and NOT the device output clock signal (CLKOUT).
(8) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.

Table 5-1. LVDS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY, MSPS	SETUP TIME, ns			HOLD TIME, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
210	1.0	1.4		0.4	0.8	
190	1.1	1.5		0.5	0.9	
170	1.3	1.7		0.7	1.1	
150	1.6	1.9		0.9	1.2	
125	1.9	2.2		1.1	1.4	
<80 *Enable low speed mode*	2.5			2.0		
				t_{PDI}, ns		
				MIN	TYP	MAX
$1 \le F_s \le 80$, *Enable low speed mode*					8.2	

Table 5-2. CMOS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY, MSPS	TIMINGS SPECIFIED WITH RESPECT TO INPUT CLOCK					
	t_{START}, ns			DATA VALID TIME, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
210			1.7	1.6	2.4	
190			0.4	2.2	3.0	
170			5.1	2.4	3.6	
150			4.8	3.0	4.3	

SAMPLING FREQUENCY, MSPS	TIMINGS SPECIFIED WITH RESPECT TO CLKOUT					
	SETUP TIME, ns			HOLD TIME, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
150	2.0	3.2		1.5	2.2	
125	2.9	4		2.2	2.7	
<80 *Enable low speed mode*	5.0			3.8		
				t_{PDI}, ns		
				MIN	TYP	MAX
$1 \le F_s \le 80$, *Enable low speed mode*					14	

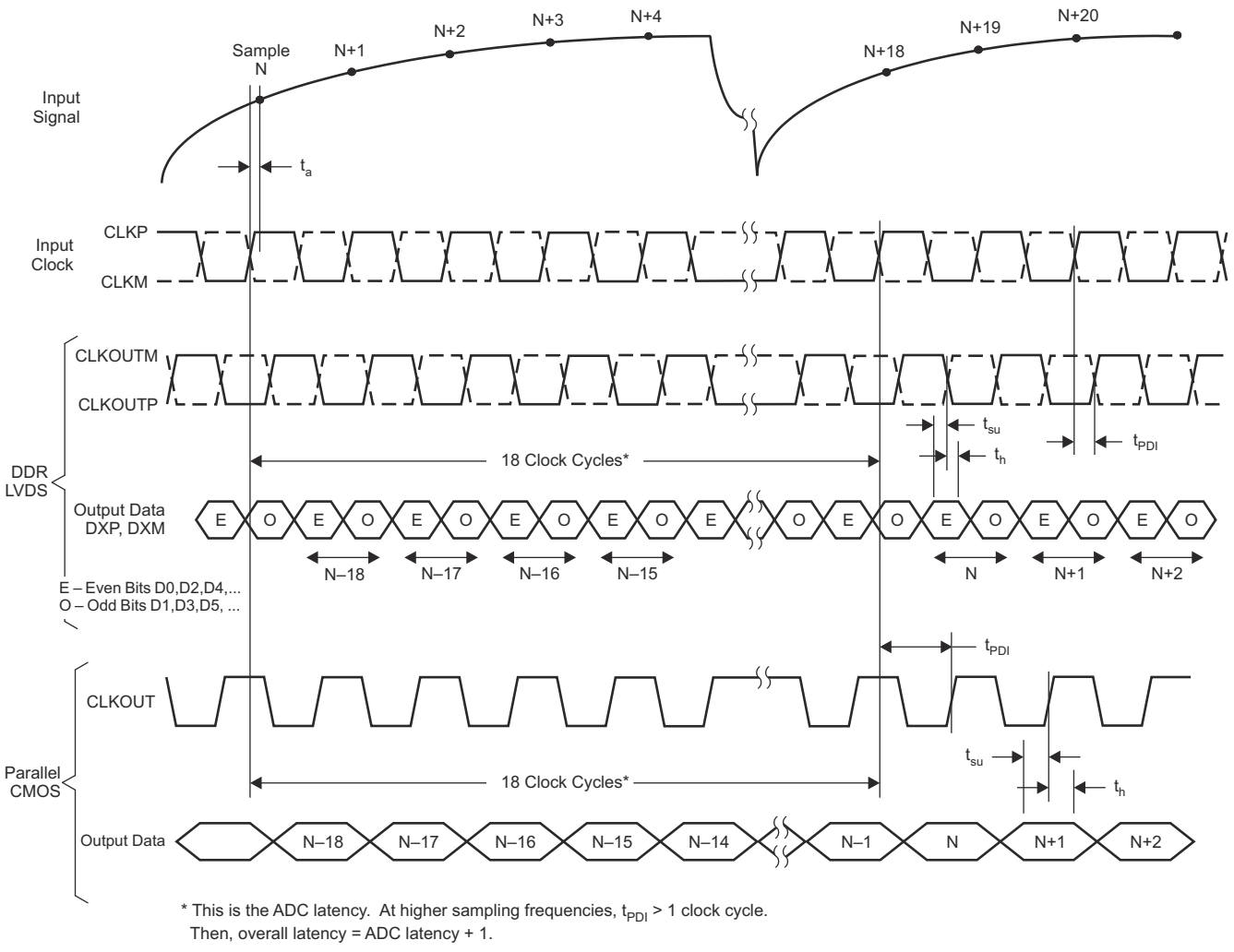


Figure 5-2. Latency Diagram

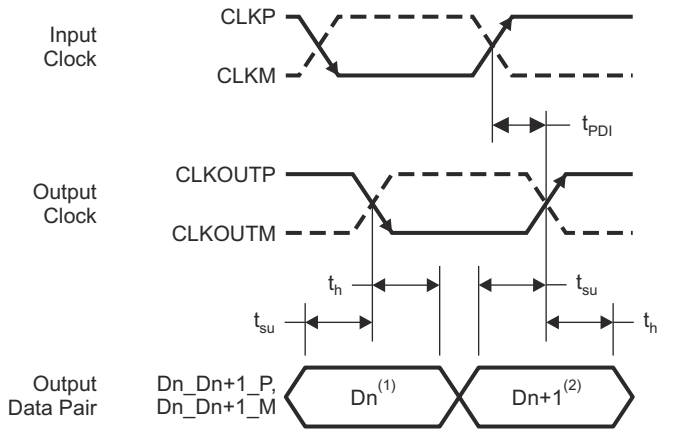
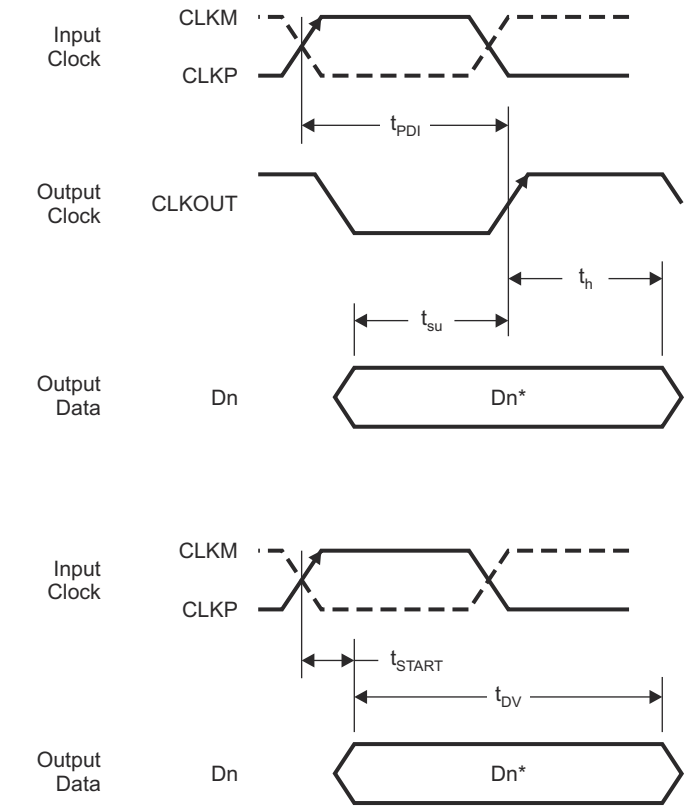


Figure 5-3. LVDS Mode Timing



*Dn – Bits D0, D1, D2, ...

T0107-05

Figure 5-4. CMOS Mode Timing

5.8 Typical Characteristics - ADS61B49

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

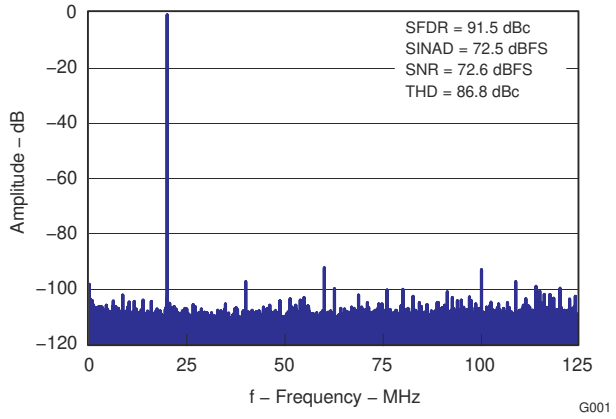


Figure 5-5. FFT for 20 MHz Input Signal

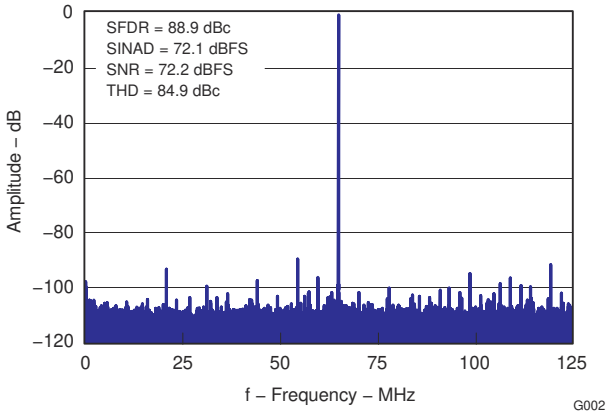


Figure 5-6. FFT for 65 MHz Input Signal

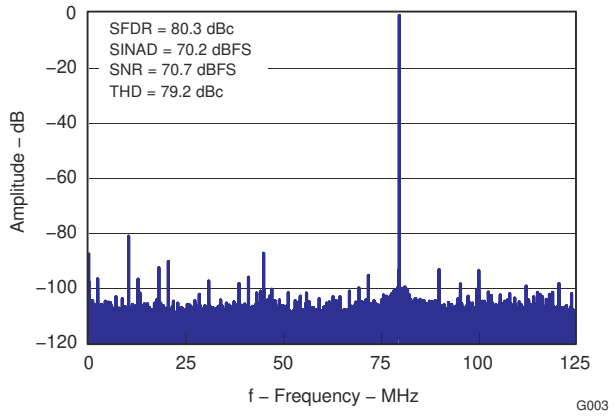


Figure 5-7. FFT for 170 MHz Input Signal

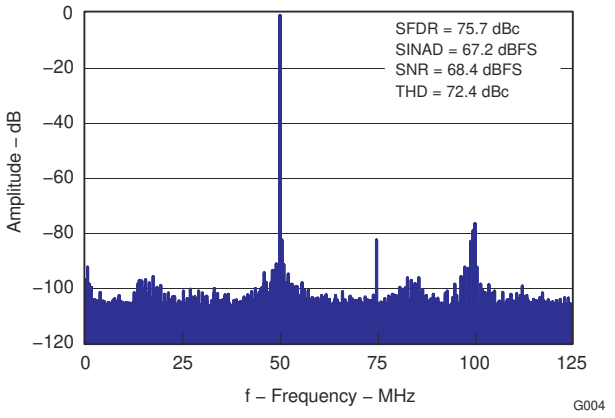


Figure 5-8. FFT for 300 MHz Input Signal

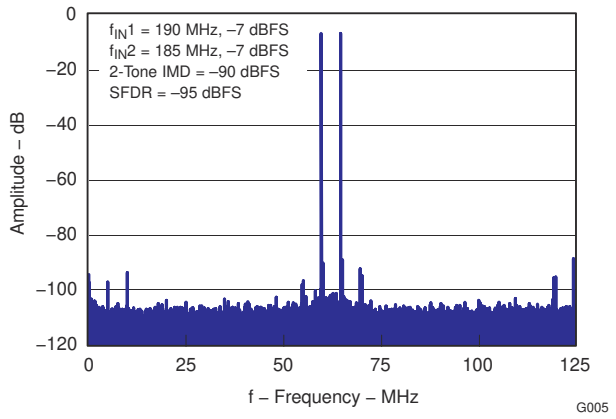


Figure 5-9. FFT for 2-Tone Input Signal (IMD)

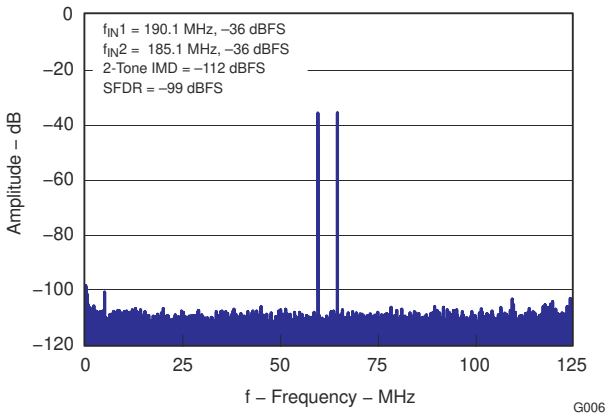


Figure 5-10. FFT for 2-Tone Input Signal (IMD)

5.8 Typical Characteristics - ADS61B49 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

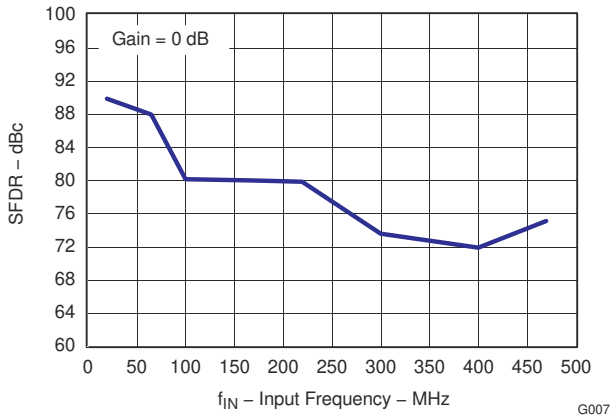


Figure 5-11. SFDR vs Input Frequency

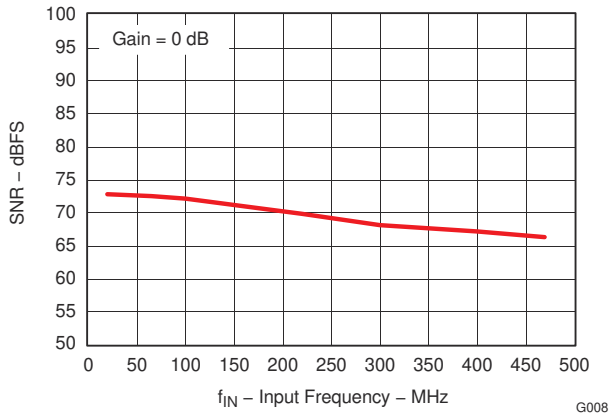


Figure 5-12. SNR vs Input Frequency

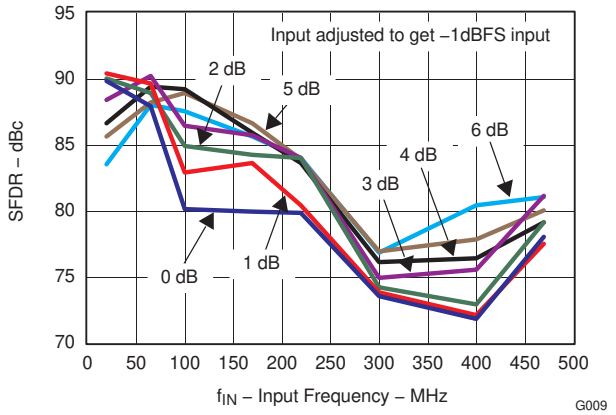


Figure 5-13. SFDR vs Input Frequency and Internal Gain

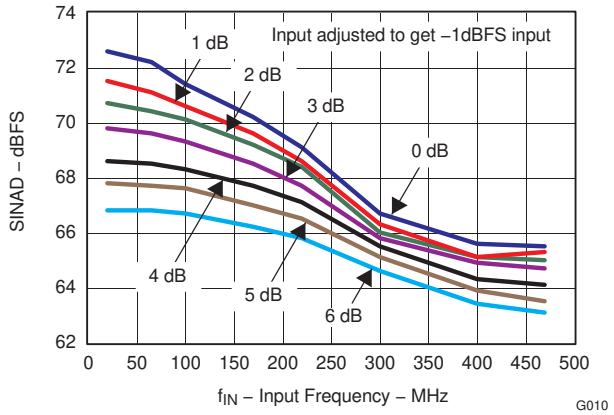


Figure 5-14. SINAD vs Input Frequency and Internal Gain

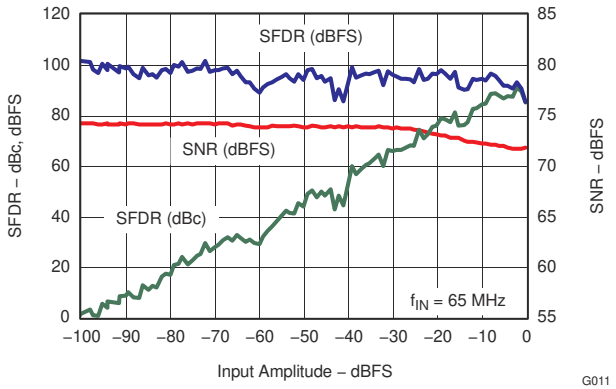


Figure 5-15. Performance vs Input Amplitude

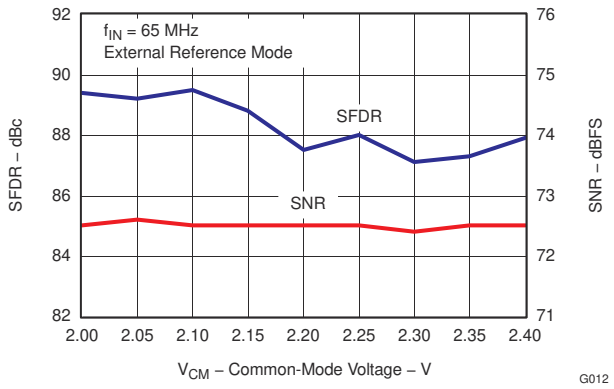


Figure 5-16. Performance vs Input Common-Mode Voltage

5.8 Typical Characteristics - ADS61B49 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

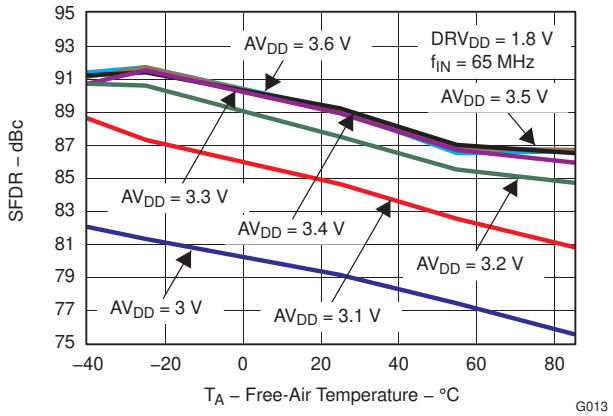


Figure 5-17. SFDR vs Temperature and AVDD

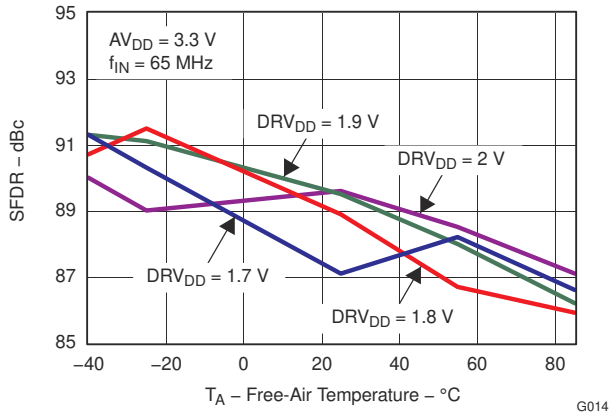


Figure 5-18. SFDR vs Temperature and DRVDD

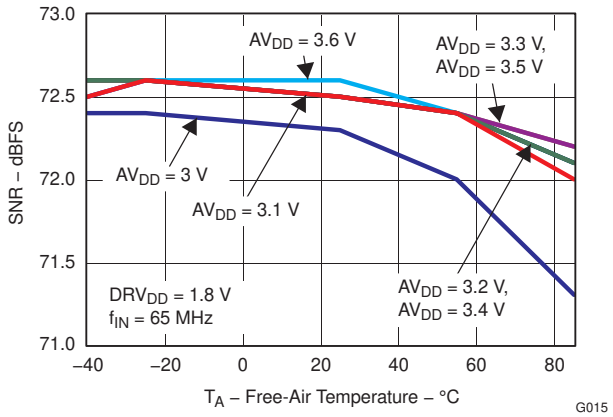


Figure 5-19. SNR vs Temperature and AVDD

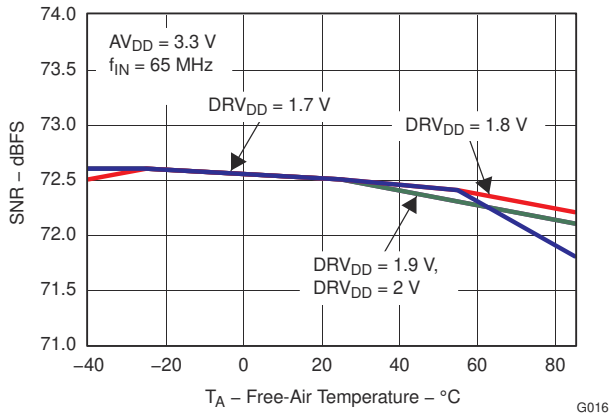


Figure 5-20. SNR vs Temperature and DRVDD

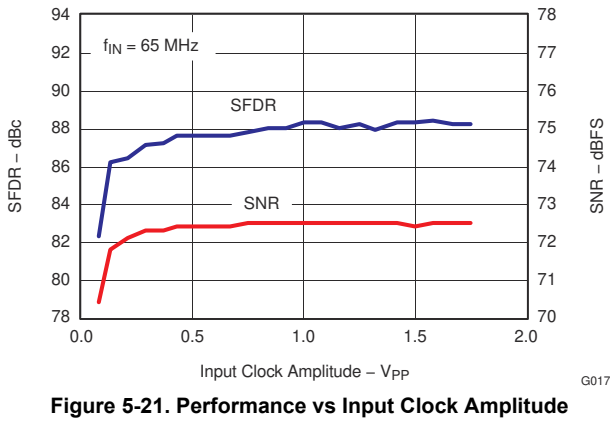


Figure 5-21. Performance vs Input Clock Amplitude

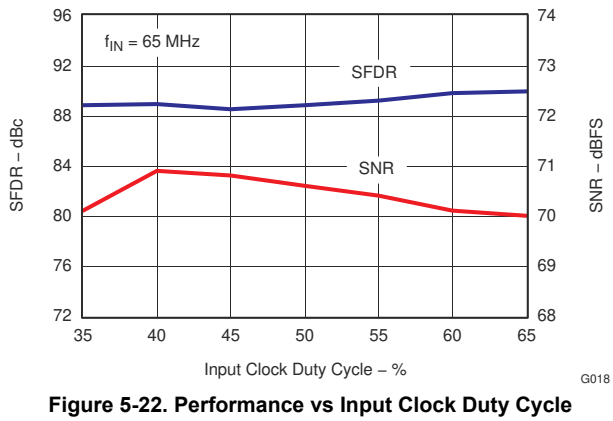


Figure 5-22. Performance vs Input Clock Duty Cycle

5.8 Typical Characteristics - ADS61B49 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

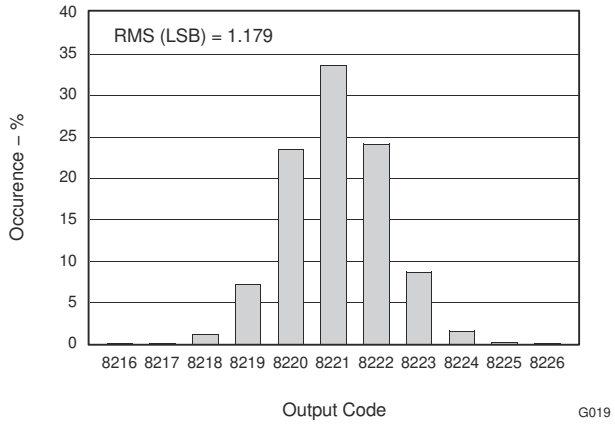


Figure 5-23. Output Noise Histogram

5.9 Typical Characteristics - ADS61B29

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

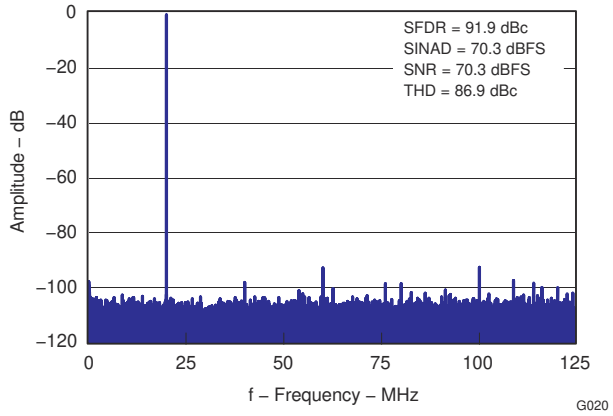


Figure 5-24. FFT for 20 MHz Input Signal

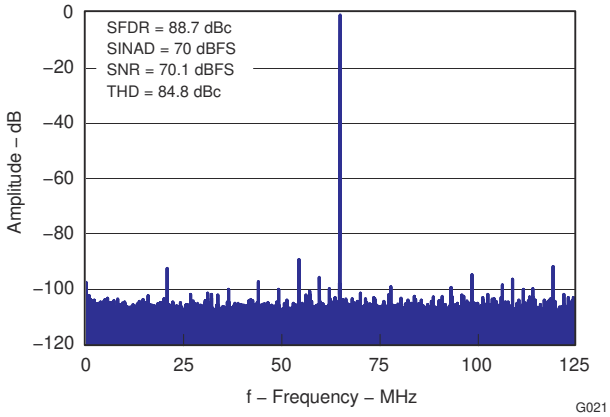


Figure 5-25. FFT for 65 MHz Input Signal

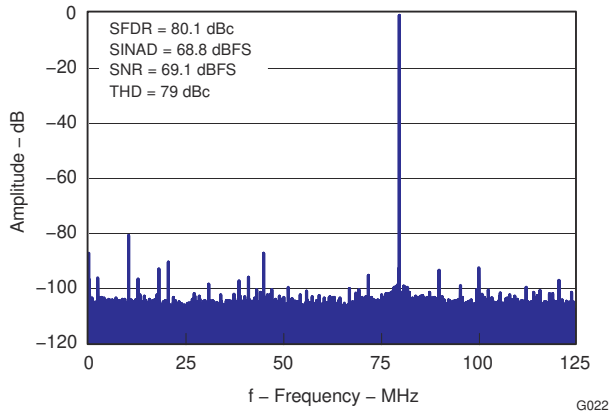


Figure 5-26. FFT for 170 MHz Input Signal

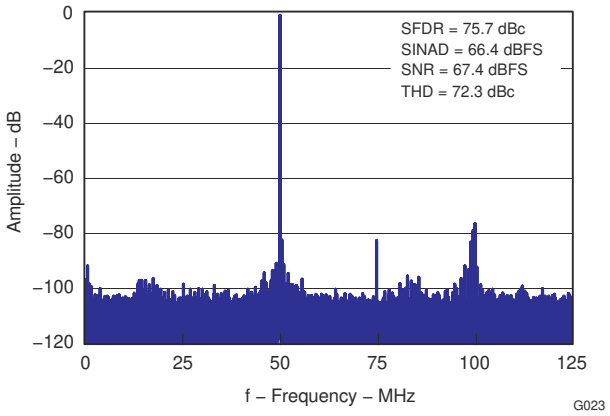


Figure 5-27. FFT for 300 MHz Input Signal

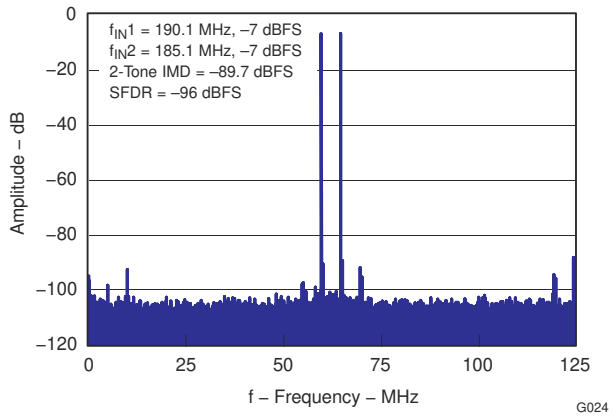


Figure 5-28. FFT for 2-Tone Input Signal (IMD)

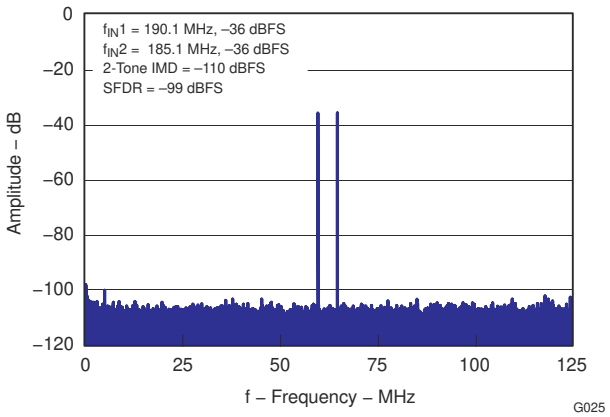


Figure 5-29. FFT for 2-Tone Input Signal (IMD)

5.9 Typical Characteristics - ADS61B29 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

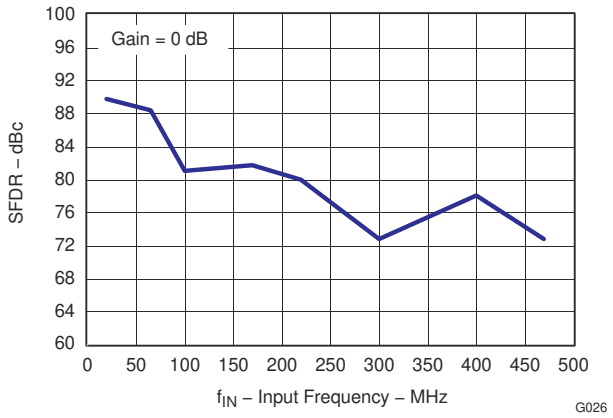


Figure 5-30. SFDR vs Input Frequency

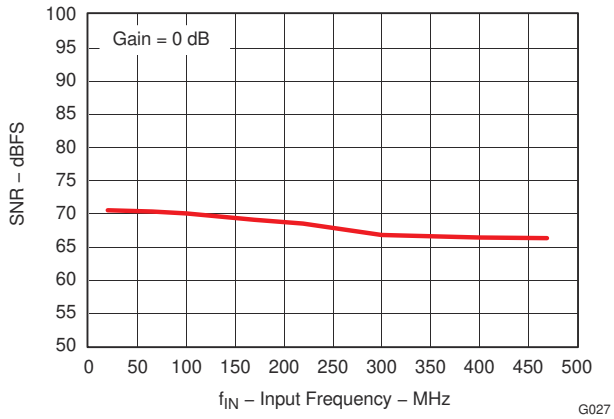


Figure 5-31. SNR vs Input Frequency

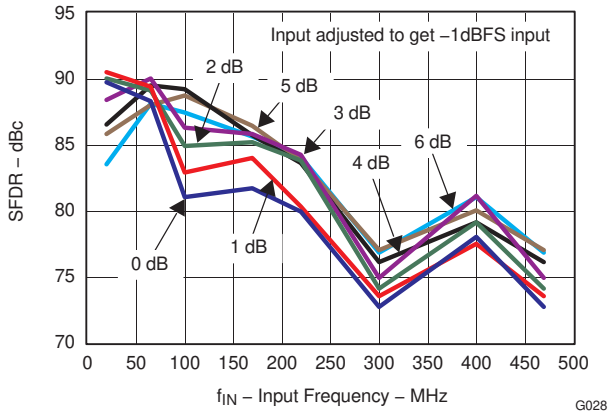


Figure 5-32. SFDR vs Input Frequency and Internal Gain

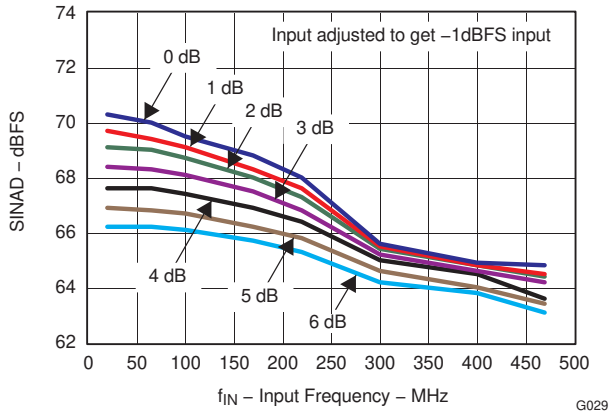


Figure 5-33. SINAD vs Input Frequency and Internal Gain

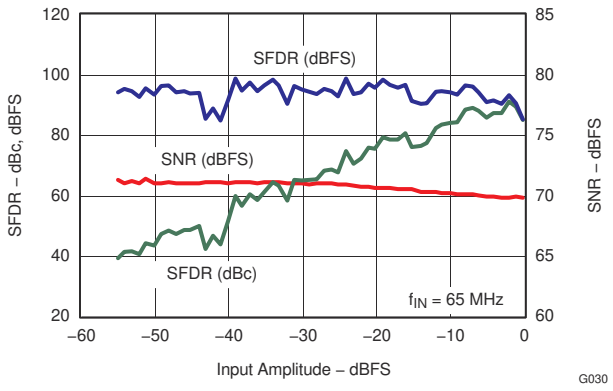


Figure 5-34. Performance vs Input Amplitude

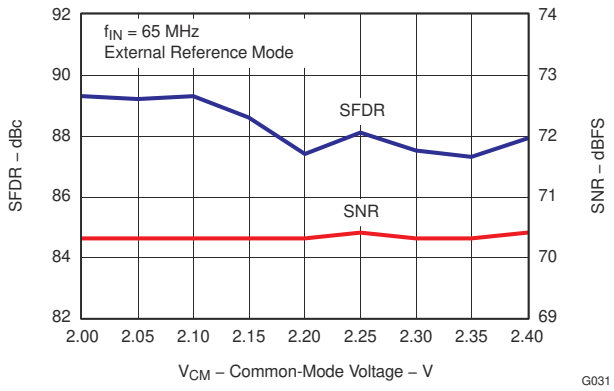


Figure 5-35. Performance vs Input Common-Mode Voltage

5.9 Typical Characteristics - ADS61B29 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

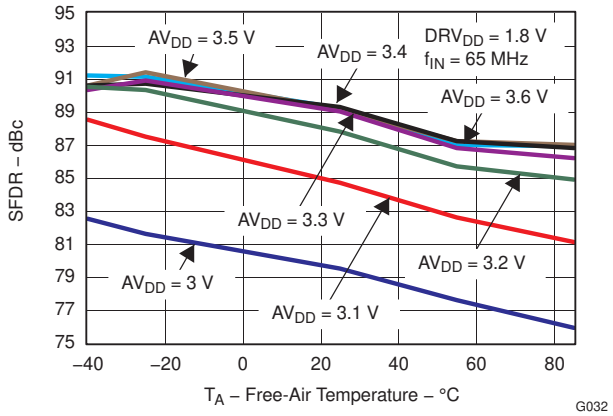


Figure 5-36. SFDR vs Temperature and AVDD

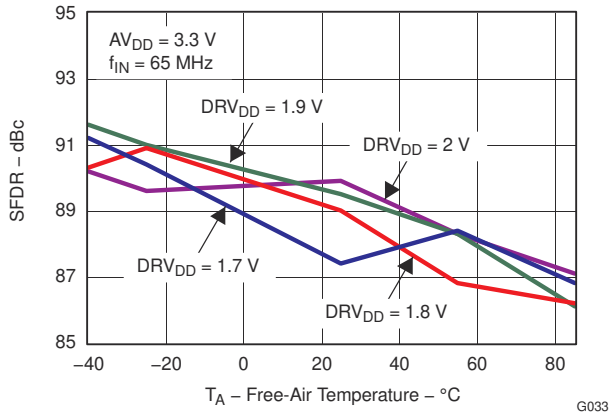


Figure 5-37. SFDR vs Temperature and DRVDD

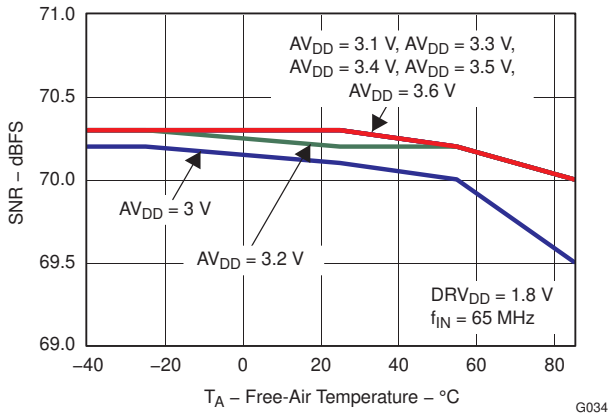


Figure 5-38. SNR vs Temperature and AVDD

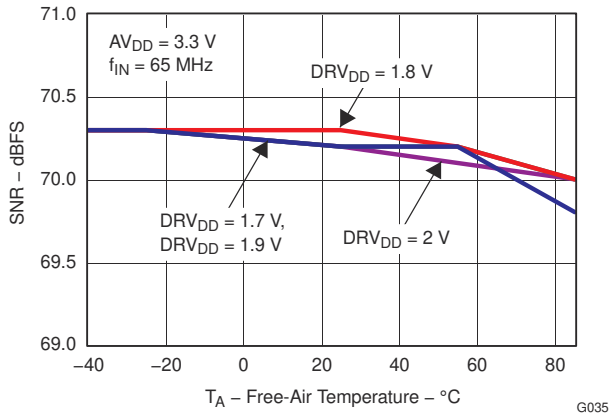


Figure 5-39. SNR vs Temperature and DRVDD

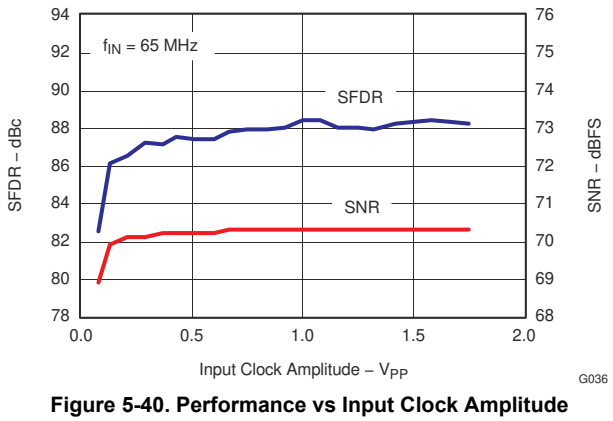


Figure 5-40. Performance vs Input Clock Amplitude

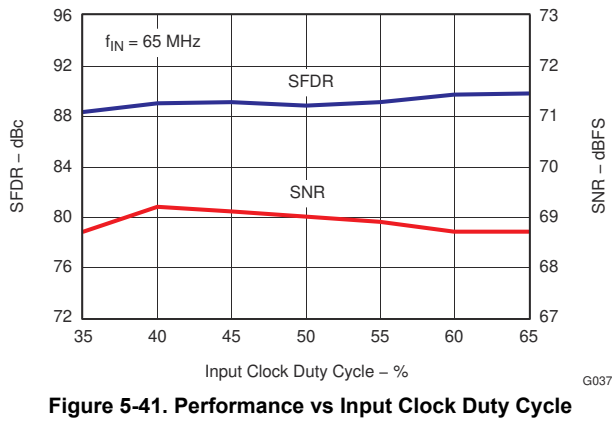


Figure 5-41. Performance vs Input Clock Duty Cycle

5.9 Typical Characteristics - ADS61B29 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

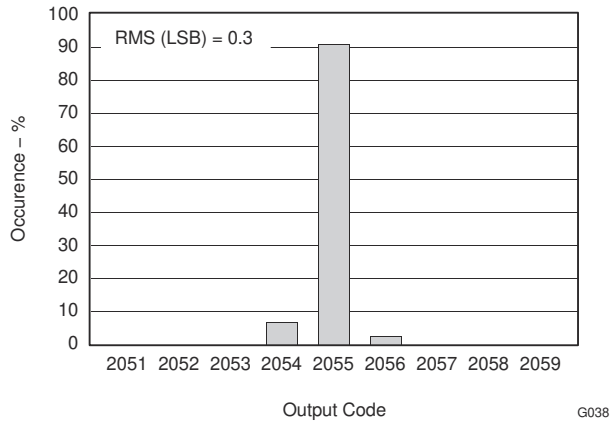


Figure 5-42. Output Noise Histogram

5.10 Typical Characteristics - Common Plots (both ADS61B49/61B29)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

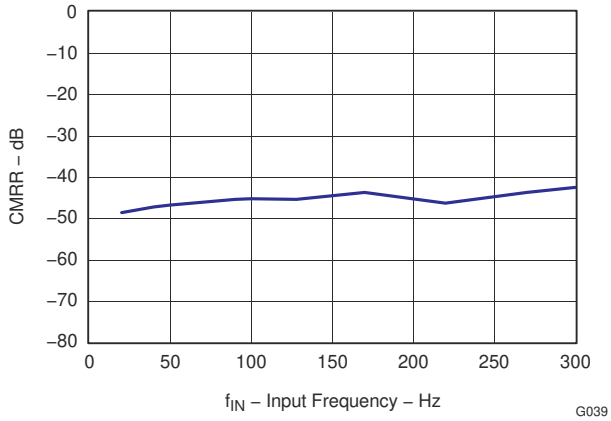


Figure 5-43. CMRR vs Input Frequency

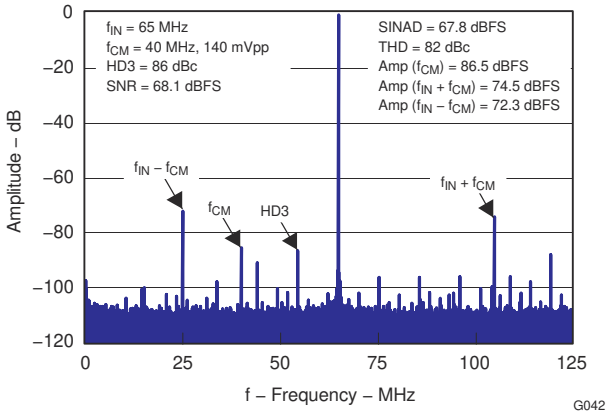


Figure 5-44. FFT Showing Effects of Common-Mode Signal

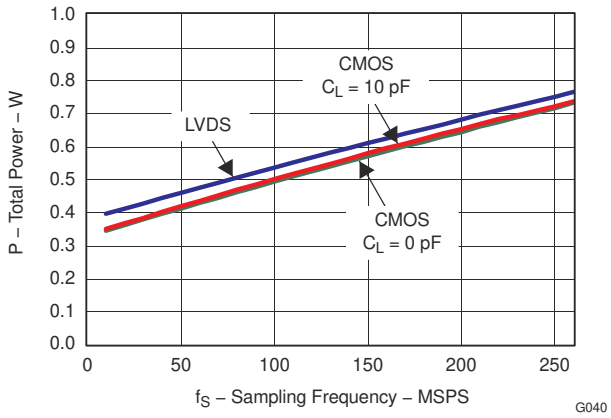


Figure 5-45. Total Power vs Sampling Frequency

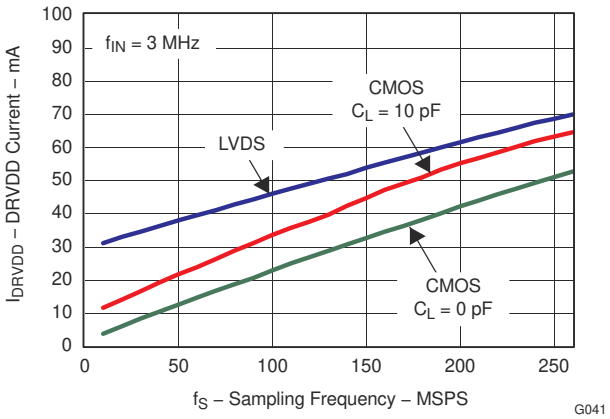


Figure 5-46. DRVDD Current vs Sampling Frequency

5.11 Contour Plots - ADS61B49/ADS61B29

Plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

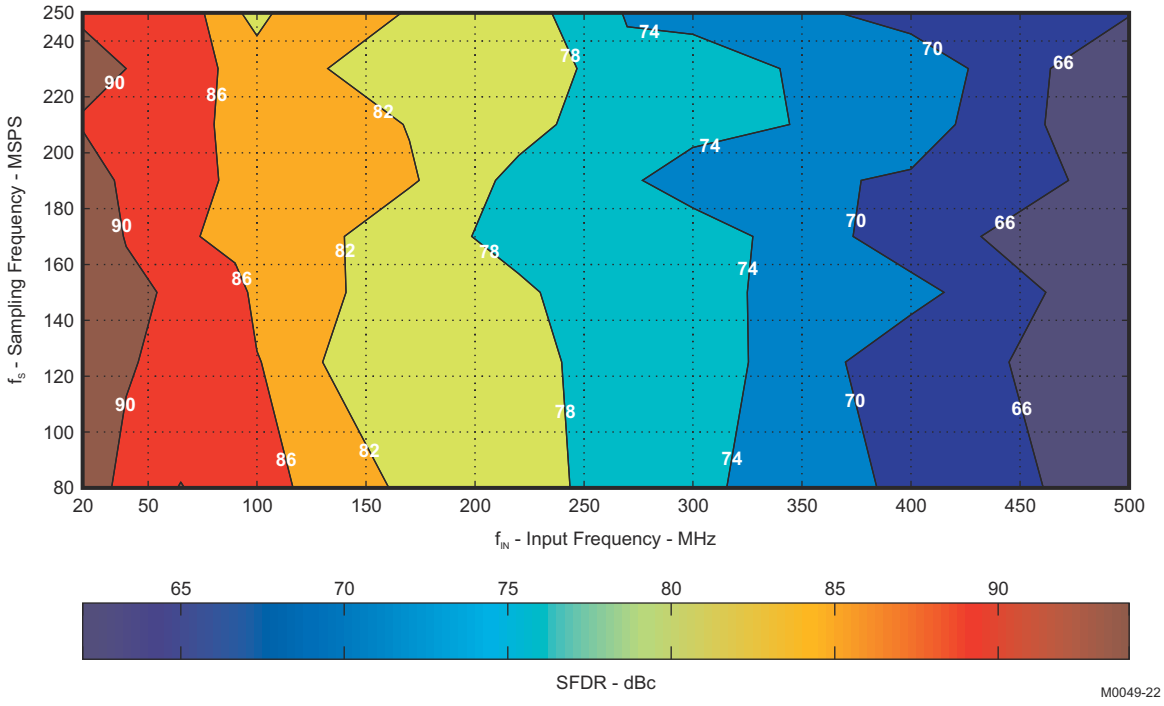


Figure 5-47. SFDR Contour Plot (0-dB gain)

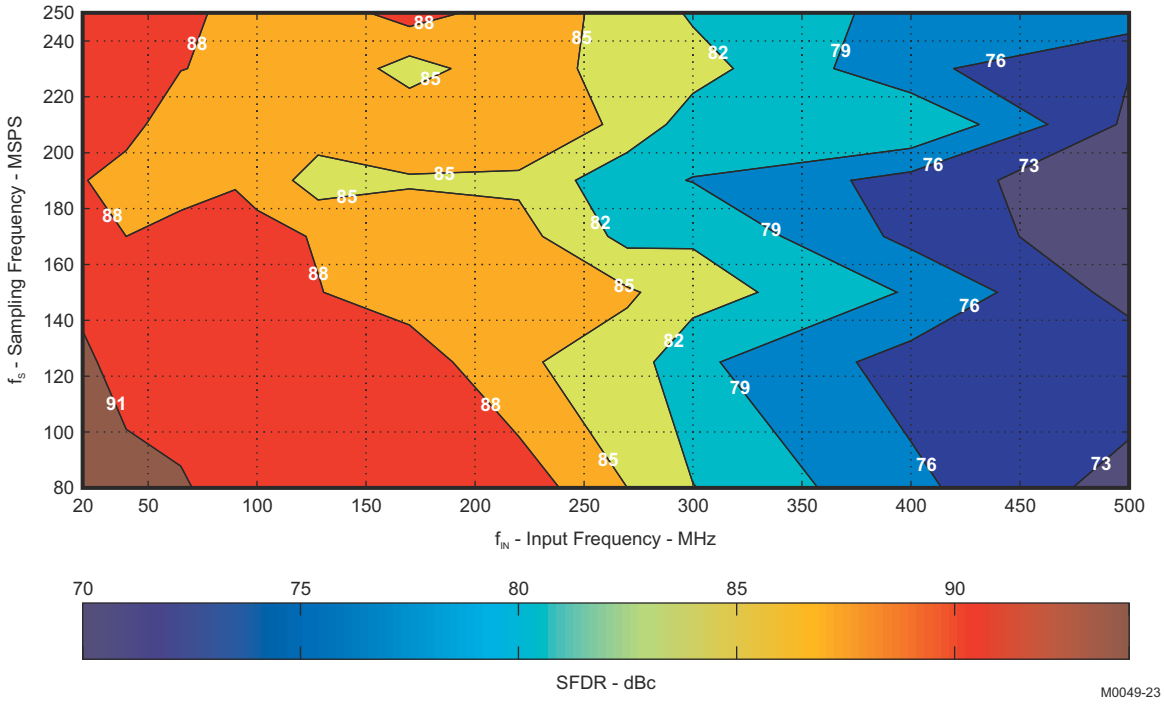


Figure 5-48. SFDR Contour Plot (6-dB gain)

5.12 Contour Plots - ADS61B49

Plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

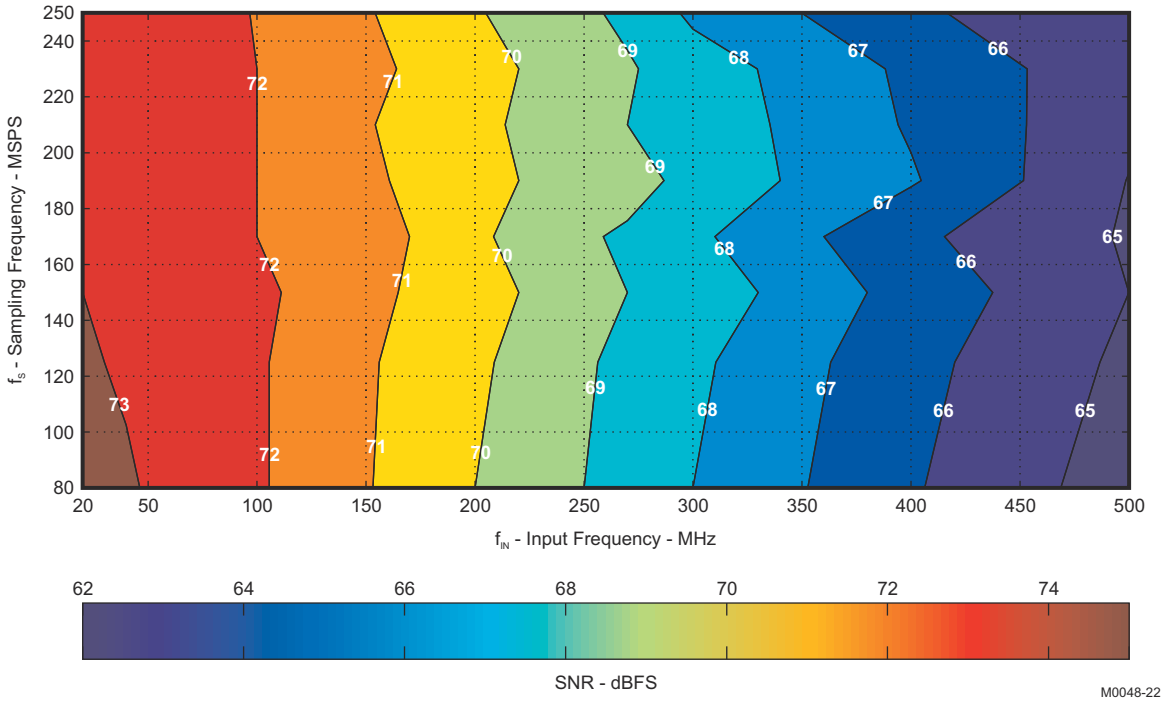


Figure 5-49. SNR Contour Plot (0-dB gain)

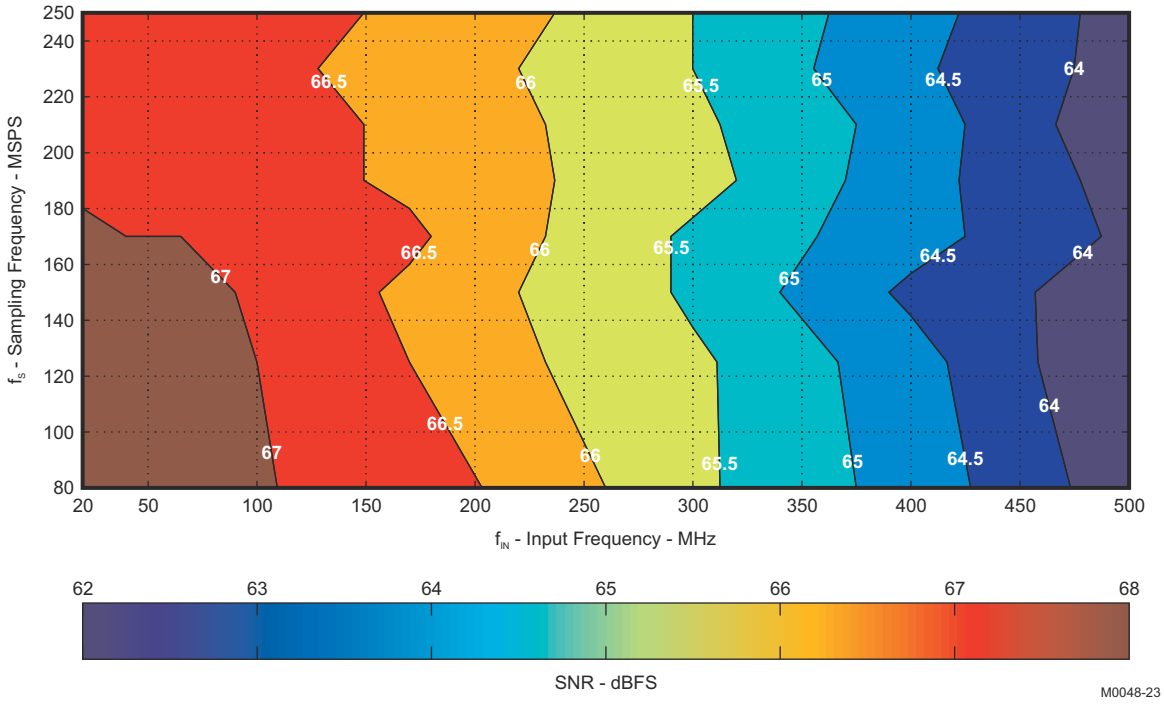


Figure 5-50. SNR Contour Plot (6-dB gain)

5.13 Contour Plots - ADS61B29

Plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

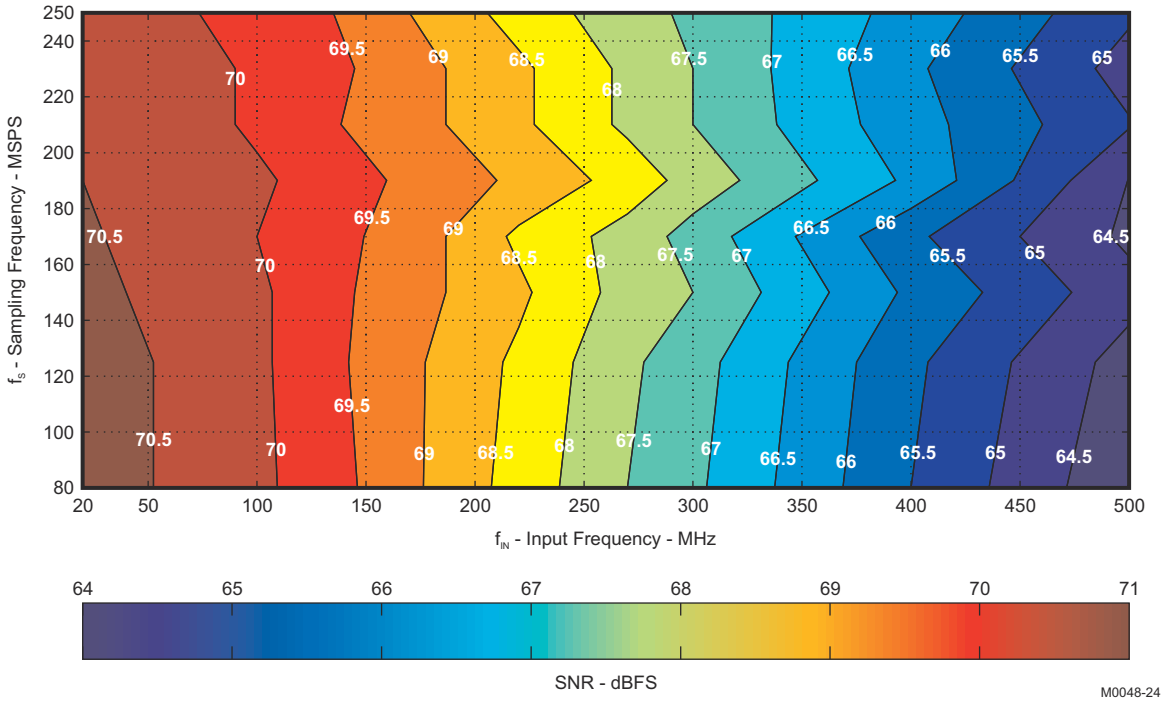


Figure 5-51. SNR Contour Plot (0-dB gain)

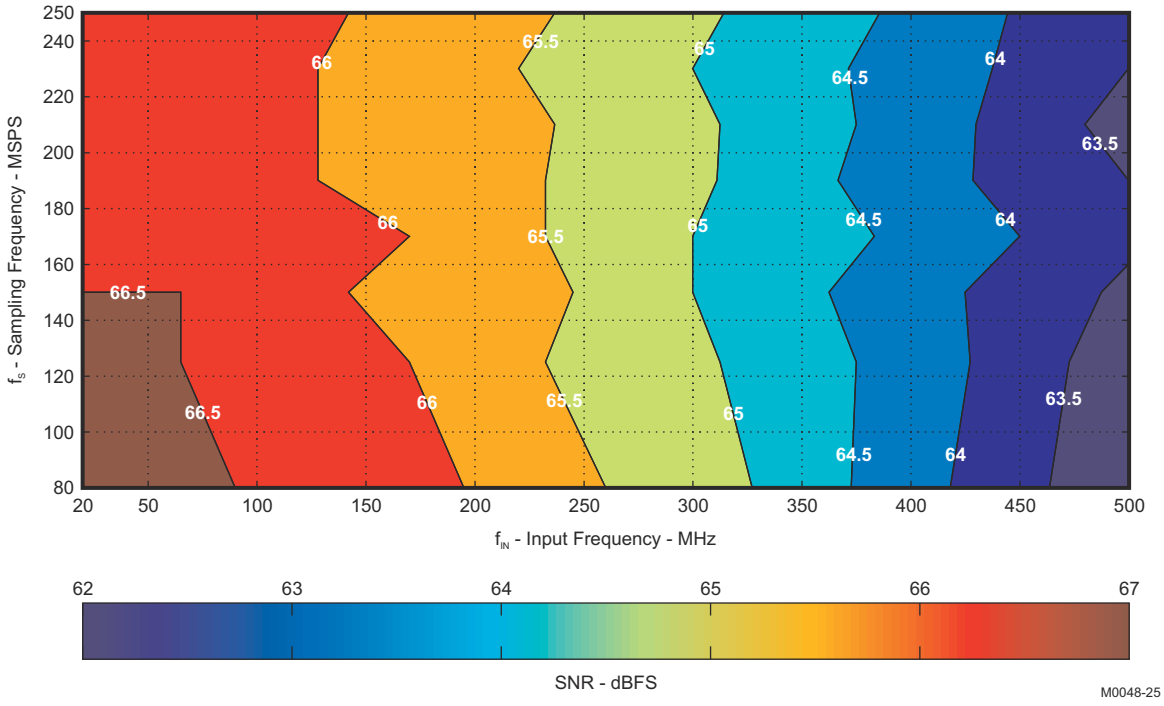
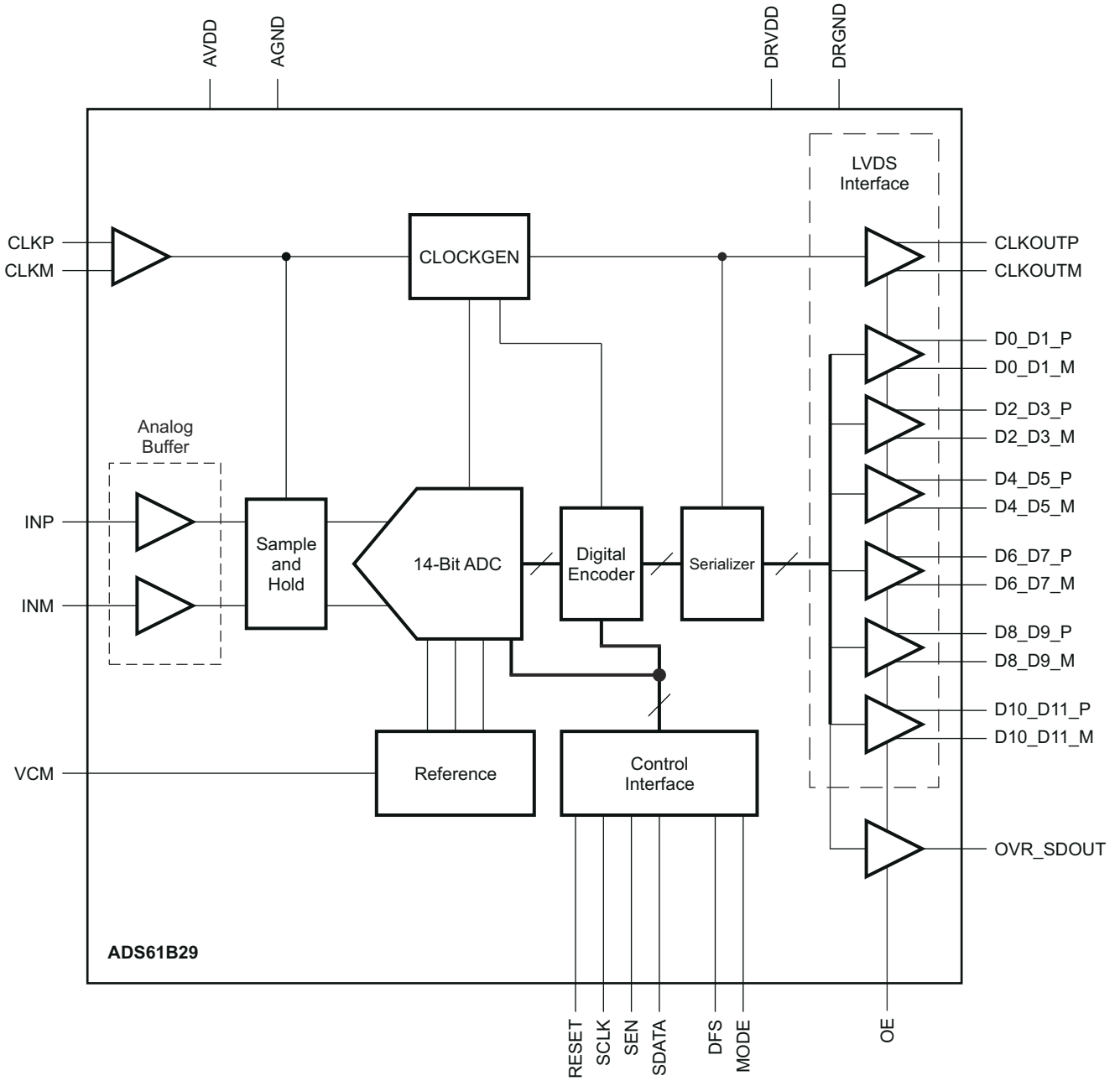


Figure 5-52. SNR Contour Plot (6-dB gain)

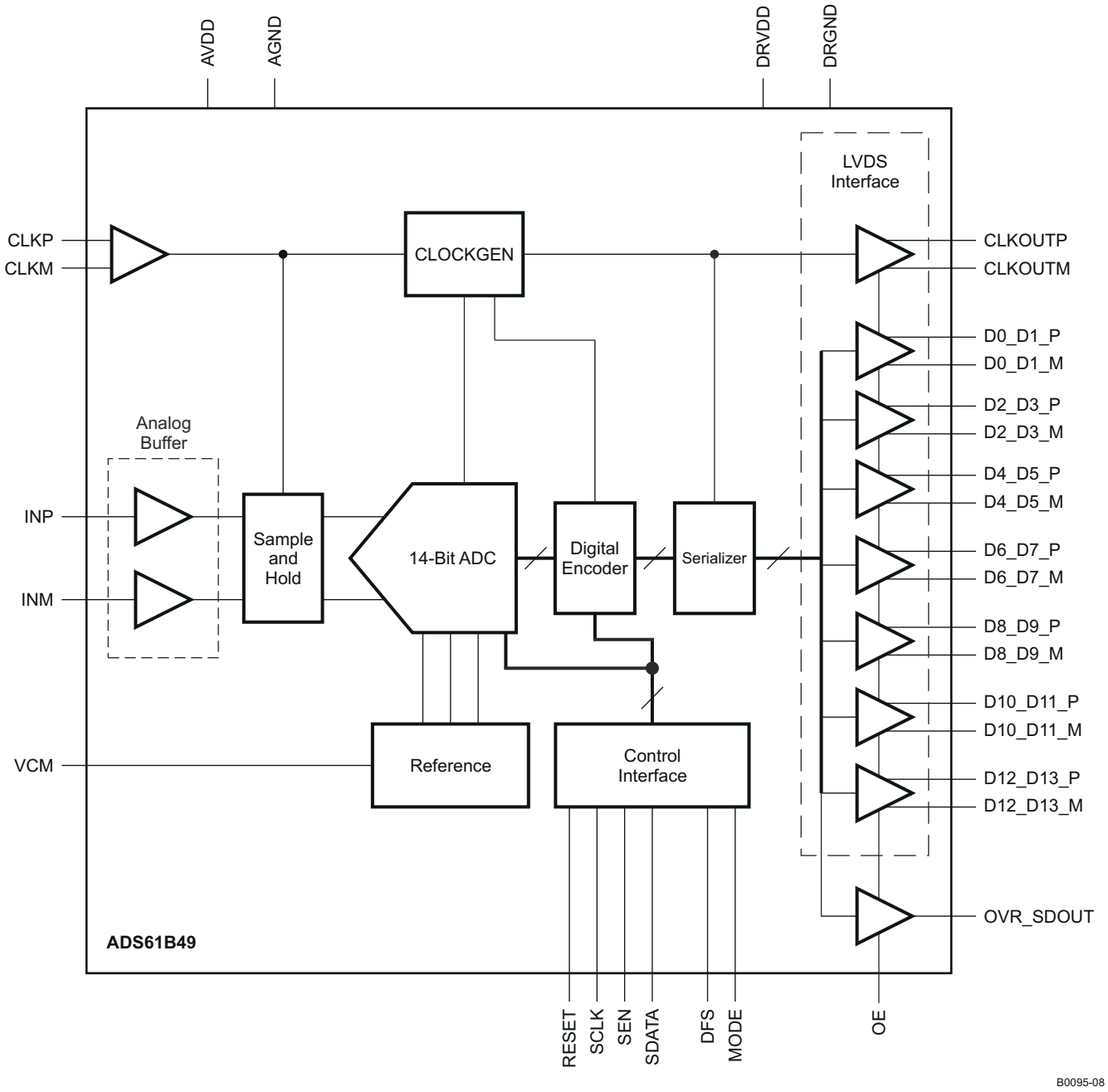
6 Detailed Description

6.1 Functional Block Diagrams

6.1.1 ADS61B29 Block Diagram



6.1.2 ADS61B49 Block Diagram



6.2 Feature Description

6.2.1 Device Configuration

The ADS61B49/29 can be configured independently using either parallel interface control or serial interface programming.

6.2.2 Parallel Configuration Only

To put the device in parallel configuration mode, keep RESET tied to high (DRVDD).

Now, pins DFS, MODE, SEN, and SDATA can be used to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 6-3 to Table 6-6). There is no need to apply reset.

In this mode, SEN and SDATA function as parallel interface control pins. Frequently used functions can be controlled in this mode – standby, selection between LVDS/CMOS output formats, 2s complement/straight binary output format, and position of the output clock edge.

Table 6-1 briefly describes the modes controlled by the parallel pins.

Table 6-1. Parallel Pin Functions

PIN	TYPE OF CONTROL	CONTROL MODES
DFS	Analog	Data format and LVDS/CMOS output interface.
MODE	Analog	In the ADS61B49/B29, external reference is not supported. Prior use of the MODE pin in the ADS6149/29 family is therefore not the same in the ADS61B49/B29 family. In the next generation pin-compatible ADC family, MODE is converted to a digital control pin for certain reserved functions. The MODE pin can be routed to a digital controller for possible future migration to a next generation ADC.
SEN	Analog	CLKOUT edge programmability.
SDATA	Digital	Global power down (ADC, internal references and output buffers are powered down)

6.2.3 Serial Interface Configuration Only

To exercise this mode, first the serial registers have to be reset to their default values and the RESET pin has to be kept low.

SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC.

The registers can be reset either by applying a pulse on the RESET pin or by setting the <RESET> bit (D7 in register 0x00) high. The serial interface section describes register programming and register reset in more detail.

Since the parallel pin DFS is not to be used in this mode, it has to be tied to ground.

6.2.4 Configuration Using Both The Serial Interface and Parallel Controls

For increased flexibility, an additional configuration mode is supported wherein a combination of serial interface registers and parallel pin control (DFS) can be used to configure the device.

To exercise this mode, the serial registers have to be reset to their default values and the RESET pin has to be kept low.

SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the <RESET> bit (D7 in register 0x00) high. The serial interface section describes register programming and register reset in more detail.

The parallel interface control pin DFS can be used and its function is determined by the appropriate voltage levels as described in Table 6-3. The voltage levels can be easily derived, by using a resistor string as illustrated with an example as shown in Figure 6-1.

Since some functions can be controlled using both the parallel pins and serial registers, the priority between the two is determined by a priority table as listed in Table 6-2.

Table 6-2. Priority Between Parallel Pins and Serial Registers

FUNCTION	PRIORITY
Int/ext reference - not used	MODE is not used in this device (legacy from the ADS6149 and future family this pin could be redefined)
Data format selection	DFS pin controls this selection ONLY if the register bits **<DATA FORMAT>** = 00, otherwise **<DATA FORMAT>** controls the selection
LVDS or CMOS interface selection	DFS pin controls this selection ONLY if the register bits **<LVDS CMOS>** = 00, otherwise **<LVDS CMOS>** controls the selection

6.2.5 Description of Parallel Pins

Table 6-3. SDATA – Digital Control Pin

SDATA	DESCRIPTION
0	Normal operation (default)
AVDD	Global power down. ADC, internal references and the output buffers are powered down.

Table 6-4. SEN – Analog Control Pin

SEN	DESCRIPTION – OUTPUT CLOCK EDGE PROGRAMMABILITY(1)
0	**LVDS:** Data and output clock transitions are aligned **CMOS:** Setup time increases by ($6xT_s$/26), hold time reduces by ($6xT_s$/26)
(3/8)AVDD	**LVDS:** Setup time decreases by ($4xT_s$/26), hold time increases by ($4xT_s$/26) **CMOS:** Setup time increases by ($9xT_s$/26), hold time reduces by ($9xT_s$/26)
(5/8)AVDD	**LVDS:** Setup time increases by ($4xT_s$/26), hold time reduces by ($4xT_s$/26) **CMOS**: Setup time increases by ($3xT_s$/26), hold time reduces by ($3xT_s$/26)
AVDD	Default output clock position (setup/hold timings of output data with respect to this clock position is specified in the timing characteristics table).

(1) T_s = 1 / sampling frequency

Table 6-5. DFS – Analog Control Pin

DFS	DESCRIPTION
0	2s complement data and DDR LVDS output
(3/8)AVDD	2s complement data and parallel CMOS output
(5/8)AVDD	Offset binary data and parallel CMOS output
AVDD	Offset binary data and DDR LVDS output

Table 6-6. MODE – Analog Control Pin

MODE	DESCRIPTION
Not used	In the ADS61B49/B29, external reference is not supported. The prior use of the MODE pin in ADS6149/29 family is therefore not the same in the ADS61B49/B29 family. In the next generation pin-compatible ADC family, MODE could be converted to a digital control pin for certain reserved functions. The MODE pin can be routed to a digital controller for possible future migration to a next generation ADC.

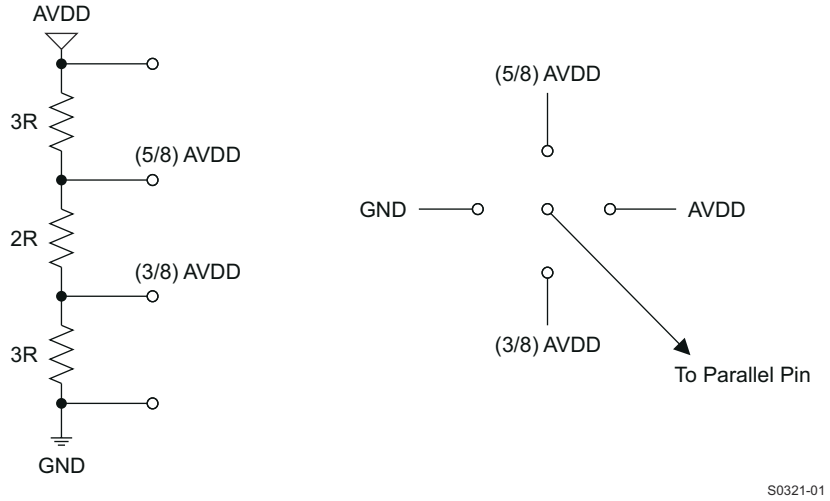


Figure 6-1. Simple Scheme to Configure Parallel Pins SEN and SCLK

6.2.6 Serial Interface

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address, and the remaining 8 bits are the register data. The interface can work with a SCLK frequency from 20 MHz down to very low speeds (few hertz) and also with a non-50% SCLK duty cycle.

6.2.6.1 Register Initialization

After power-up, the internal registers MUST be initialized to their default values. This can be done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on the RESET pin (of width greater than 10 ns) as shown in Figure 6-2.

   OR

2. By applying a software reset. Using the serial interface, set the **<RESET>** bit (D7 in register 0x00) to high. This initializes the internal registers to their default values and then self-resets the **<RESET>** bit to low. In this case the RESET pin is kept low.

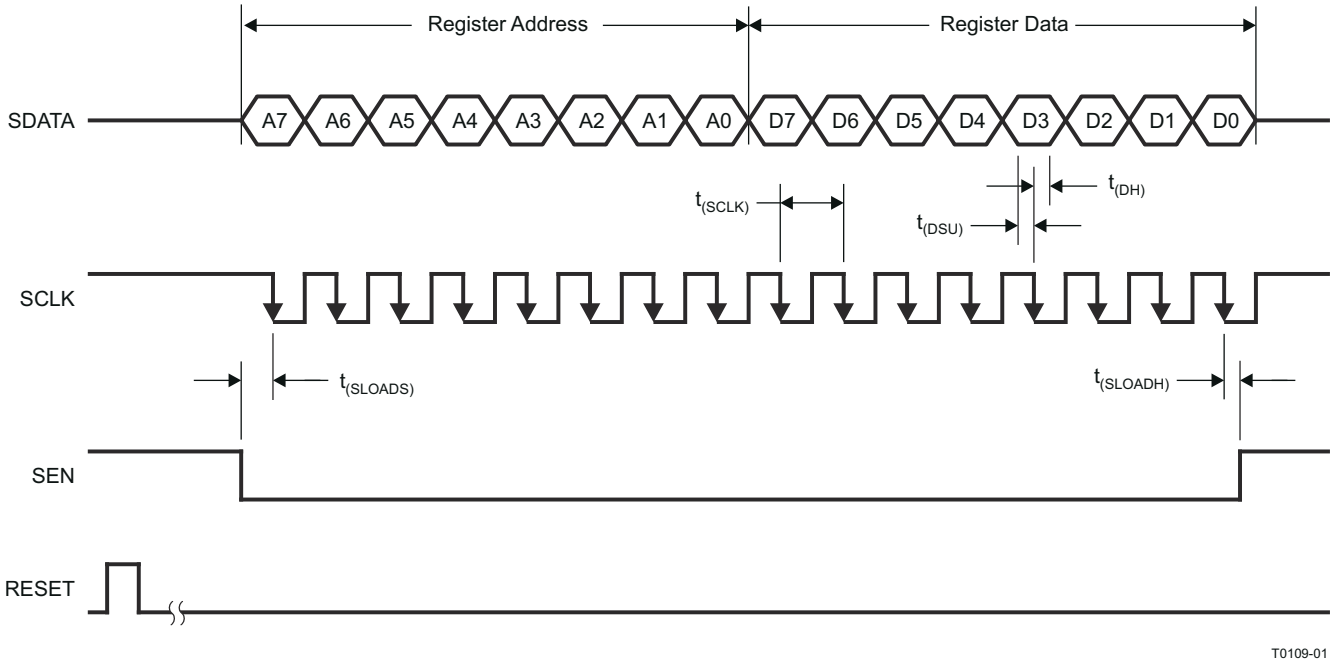


Figure 6-2. Serial Interface Timing

6.2.7 Serial Interface Timing Characteristics

Typical values at 25°C, min and max values across the full temperature range
T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 1.8 V, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (= 1/ t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DS}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

6.2.8 Serial Register Readout

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. First, set register bit <SERIAL READOUT> = 1. This also disables any further writes into the registers (EXCEPT register bit <SERIAL READOUT> itself).
2. Initiate a serial interface cycle specifying the address of the register (A7-A0) whose content has to be read.
3. The device outputs the contents (D7-D0) of the selected register on the OVR_SDOUT pin.
4. The external controller can latch the contents at the falling edge of SCLK.
5. To enable register writes, reset register bit <SERIAL READOUT> = 0.

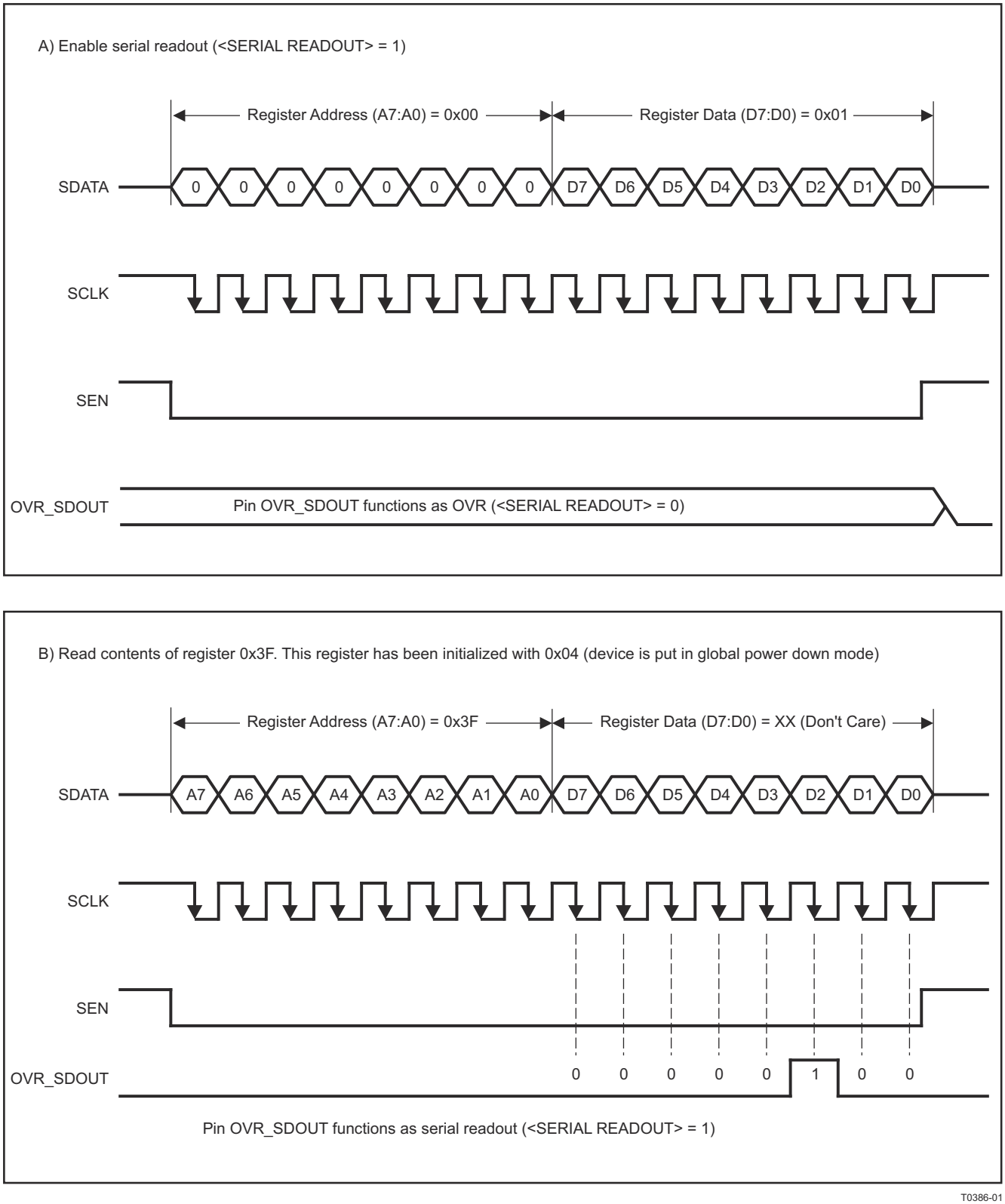


Figure 6-3. Serial Readout

6.2.9 Reset Timing

Typical values at 25°C, min and max values across the full temperature range
T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay time	Delay from power-up of AVDD and DRVDD to RESET pulse active		1		ms
t_2	Reset pulse width	Pulse width of active RESET signal that resets the serial registers	10			ns
					1	µs
t_3	Delay time	Delay from RESET disable to SEN active	100			ns

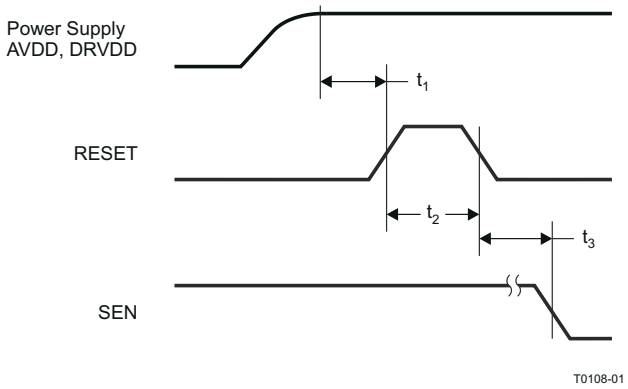


Figure 6-4. Reset Timing Diagram

6.3 Serial Register Map

Table 6-7. Summary of Functions Supported by Serial Interface

REGISTER ADDRESS	REGISTER FUNCTIONS(1)							
A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	<RESET> *Software Reset*	0	0	0	0	0	0	<SERIAL READOUT>
20	0	0	0	0	0	<ENABLE LOW SPEED MODE>	0	0
3F	0	<REF> (RESERVED)		0	0	<PDN GLOBAL>	<STANDBY>	<PDN OBUF>
41	<LVDS CMOS> *Output interface*		0	0	0	0	0	0
44	<CLKOUT POSN> *Output clock position control*						0	0
50	0	0	0	0	0	<DATA FORMAT> *2s complement or offset binary*		0
51	<CUSTOM PATTERN LOW>							
52	0	0	<CUSTOM PATTERN HIGH>					
53	0	<ENABLE OFFSET CORR>	0	0	0	0	0	0
55	<FINE GAIN >					<OFFSET CORR TIME CONSTANT> Offset correction time constant		
62	0	0	0	0	0	<TEST PATTERNS>		
63	0	0	<PROGRAM OFFSET PEDESTAL >					

(1) Multiple functions in a register can be programmed in a single write operation.

6.3.1 Description of Serial Registers

A)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	<RESET> *Software Reset*	0	0	0	0	0	0	<SERIAL READOUT>

D7 <RESET>

1 Software reset applied – resets all internal registers and self-clears to 0.

D0 <SERIAL READOUT>

0 Serial readout disabled

1 Serial readout enabled, pin OVR_SDOUT functions as serial data readout.

B)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
20	0	0	0	0	0	<ENABLE LOW SPEED MODE>	0	0

D2 <ENABLE LOW SPEED MODE>

0 Low speed mode disabled. Use for sampling frequency > 80 MSPS

1 Enable low speed mode for sampling frequencies ≤ 80MSPS.

C)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
3F	0	<REF>(RESERVED)		0	0	<PDN GLOBAL>	<STANDBY>	<PDN OBUF>

D6,D5 <REF> RESERVED (Not used)

In the ADS61B49/61B29, external reference mode is not supported. See ADS6149/6129 non-buffered ADCs if an external reference is required. This register controls the reference mode in those devices.

D2 <PDN GLOBAL>

0 Normal operation

1 Total power down – ADC, internal references and output buffers are powered down. Slow wake-up time.

D1 <STANDBY>

0 Normal operation

1 ADC alone powered down. Internal references, output buffers are active. Quick wake-up time

D0 <PDN OBUF> Power down output buffer

0 Output buffer enabled

1 Output buffer powered down

D)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
41	<LVDS CMOS>		0	0	0	0	0	0

D7,D6 <LVDS CMOS>

00 DFS pin controls LVDS or CMOS interface selection

10 DDR LVDS interface

11 Parallel CMOS interface

E)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
44	CLKOUT POSN> *Output clock position control*						0	0

LVDS Interface

D7-D5	<CLKOUT POSN> Output clock rising edge position
000	Default output clock position (refer to timing specification table)
100	Default output clock position (refer to timing specification table)
101	Rising edge shifted by + (4/26)T_s
110	Rising edge aligned with data transition
111	Rising edge shifted by - (4/26)T_s

D4-D2	<CLKOUT POSN> Output clock falling edge position
000	Default output clock position (refer to timing specification table)
100	Default output clock position (refer to timing specification table)
101	Falling edge shifted by + (4/26)T_s
110	Falling edge aligned with data transition
111	Falling edge shifted by - (4/26)T_s

CMOS Interface

D7-D5	<CLKOUT POSN> Output clock rising edge position
000	Default output clock position (refer to timing specification table)
100	Default output clock position (refer to timing specification table)
101	Rising edge shifted by + (4/26)T_s
110	Rising edge shifted by + (6/26)T_s
111	Rising edge aligned with data transition

D4-D2	<CLKOUT POSN> Output clock falling edge position
000	Default output clock position (refer to timing specification table)
100	Default output clock position (refer to timing specification table)
101	Falling edge shifted by + (4/26)T_s
110	Falling edge shifted by + (6/26)T_s
111	Falling edge aligned with data transition

F)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
50	0	0	0	0	0	<DATA FORMAT> *2s complement or offset binary*		0

D2,D1	<DATA FORMAT>
00	DFS pin controls data format selection
10	2s complement
11	Offset binary

G)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
51	<Custom LOW>							
52			<Custom HIGH>					

D7–D0 <CUSTOM LOW>

8 lower bits of custom pattern available at the output instead of ADC data.

D5–D0 **<CUSTOM HIGH>**

6 upper bits of custom pattern available at the output instead of ADC data

H)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
53	0	<ENABLE OFFSET CORR> *Offset correction enable*	0	0	0	0	0	0

D6 **<ENABLE OFFSET CORR>**

0 Offset correction disabled

1 Offset correction enabled

I)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
55	<FINE GAIN>				<OFFSET CORR TC> *Offset correction time constant*			

D7–D4 **<FINE GAIN>** Gain programmability in 0.5-dB steps

0000 0-dB gain, default after reset

0001 0.5-dB gain

0010 1.0-dB gain

0011 1.5-dB gain

0100 2.0-dB gain

0101 2.5-dB gain

0110 3.0-dB gain

0111 3.5-dB gain

1000 4.0-dB gain

1001 4.5-dB gain

1010 5.0-dB gain

1011 5.5-dB gain

1100 6.0-dB gain

D3–D0 **<OFFSET CORR TC>** Time constant of correction loop in number of clock cycles. See *Offset Correction* in application section.

0000 256 k

0001 512 k

0010 1 M

0011 2 M

0100 4 M

0101 8 M

0110 16 M

0111 32 M

1000 64 M

1001 128 M

1010 256 M

1011 512 M

1100 to 1111 Reserved

J)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
62	0	0	0	0	0	<TEST PATTERNS>		

D2–D0 **<TEST PATTERNS>** Test patterns to verify data capture

000	Normal operation
001	Outputs all zeros
010	Outputs all ones
011	Outputs toggle pattern
100	Outputs digital ramp
101	Outputs custom pattern
110	Unused
111	Unused

K)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
63	0	0	<OFFSET PEDESTAL>					

D5–D0 **<OFFSET PEDESTAL>** When the offset correction is enabled, the final converged value after the offset is corrected is the ADC mid-code value.

A pedestal can be added to the final converged value by programming these bits. For example, See *Offset Correction* in application section.

011111	Mid-code + 31 LSB
011110	Mid-code + 30 LSB
011101	Mid-code + 29 LSB
....	
000000	Mid-code
111111	Mid-code - 1 LSB
111110	Mid-code - 2 LSB
....	
100000	Mid-code - 32 LSB

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Theory of Operation

The ADS61B49/29 are high performance, low power 14-bit and 12-bit A/D converters with maximum sampling rates up to 250 MSPS. The primary difference from the ADS6149/29 is the addition of an integrated analog buffer (hence B in the device name).

The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline resulting in a data latency of 18 clock cycles. The output is available as 14-bit/12-bit data, in DDR LVDS or CMOS and coded in either straight offset binary or binary 2s complement format.

The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to about 500MHz (with 2-Vpp amplitude) and about 800MHz (with 1-Vpp amplitude) before the performance becomes ill-behaved. This is separate from the full power analog bandwidth of 750MHz, which is only an indicator of signal amplitude versus frequency.

7.1.2 Analog Input

The analog input consists of an integrated input buffer followed by a switched-capacitor based differential sample and hold architecture. The addition of a buffer provides isolation from the non-linear impedance and switching transients of the switched-capacitor circuit. With a constant input impedance, the ADC is easier to drive and to reproduce data sheet measurements. For wide-band applications, like power amplifier linearization, the signal gain across frequency is more consistent. Spectral performance variance across frequency is also reduced.

This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 2.3 V, available on the VCM pin. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM+ 0.5 V and VCM – 0.5 V, resulting in a 2-V_{pp} differential input swing.

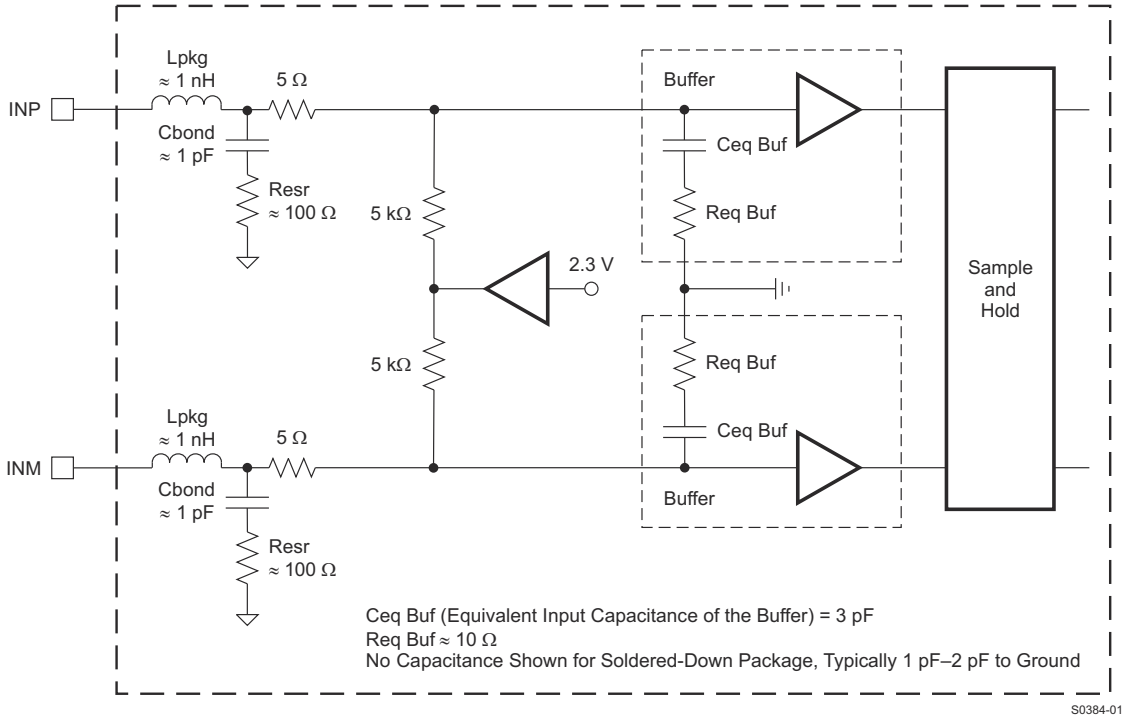


Figure 7-1. Analog Input Equivalent Circuit

The input sampling circuit has a high 3-dB bandwidth that extends up to 750 MHz (measured from the input pins to the sampled voltage).

7.1.2.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω resistor in series with each input pin is recommended to dampen out ringing caused by package parasitics.

Due to the integrated high impedance buffer in the ADS61B49/29 family, the filtering of the glitches with an external R-C-R filter suggested for the ADS6149/29 family is not required. The drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance must be considered. Figure 7-2 and Figure 7-3 show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) looking into the ADC input pins. These figures compare the buffered ADS61B49 to the non-buffered ADS6149.

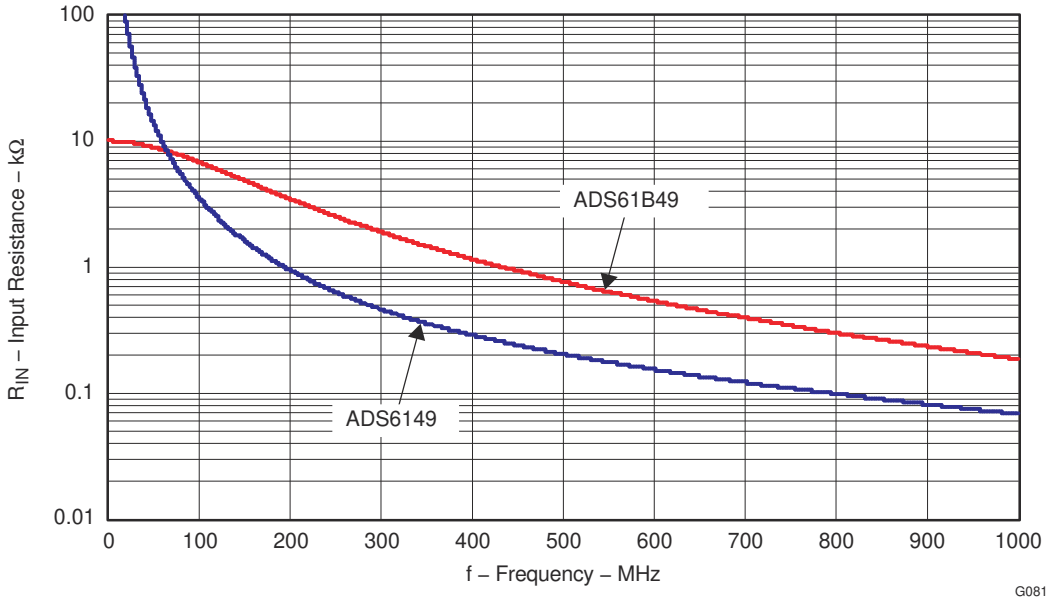


Figure 7-2. ADC Analog Input Resistance Across Frequency

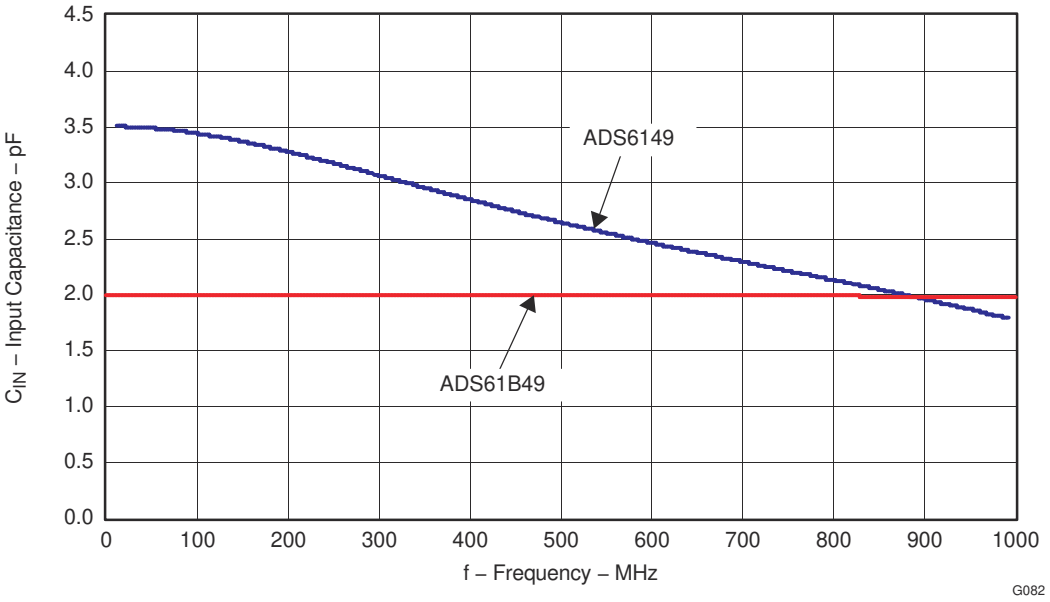


Figure 7-3. ADC Analog Input Capacitance Across Frequency

7.1.2.2 Driving Circuit

Two example driving circuit configurations are shown in Figure 7-4 and Figure 7-5 – one optimized for low input frequencies and the other for high input frequencies. Notice in both cases that the board circuitry is simplified compared to the non-buffered ADS6149. In Figure 7-4, a single transformer is used and is suited for low input frequencies and works for some high frequency applications as well. To optimize even-harmonic performance at high input frequencies (> 2nd Nyquist), the use of back-to-back transformers is recommended (see Figure 7-5).

Note that both drive circuits have been terminated by 50-Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage.

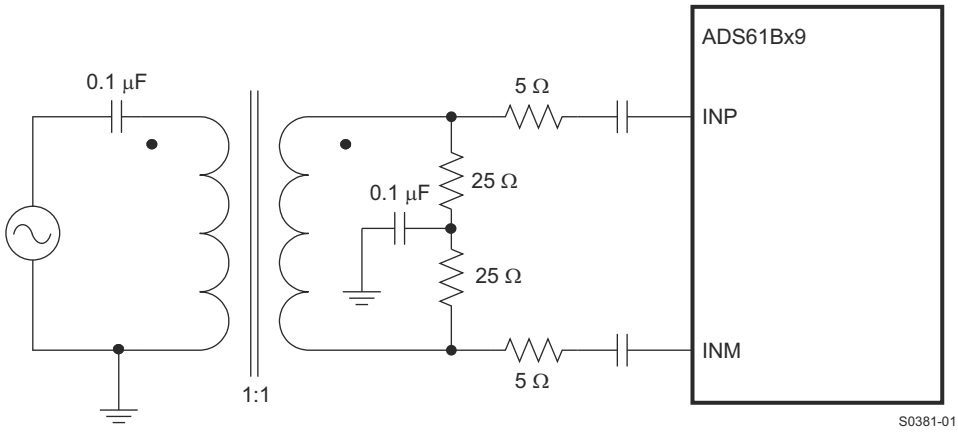


Figure 7-4. Drive Circuit for Low Frequencies

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair may be required between the two transformers as shown in the figures. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side have to be chosen to achieve an effective 50 Ω (in the case of 50-Ω source impedance).

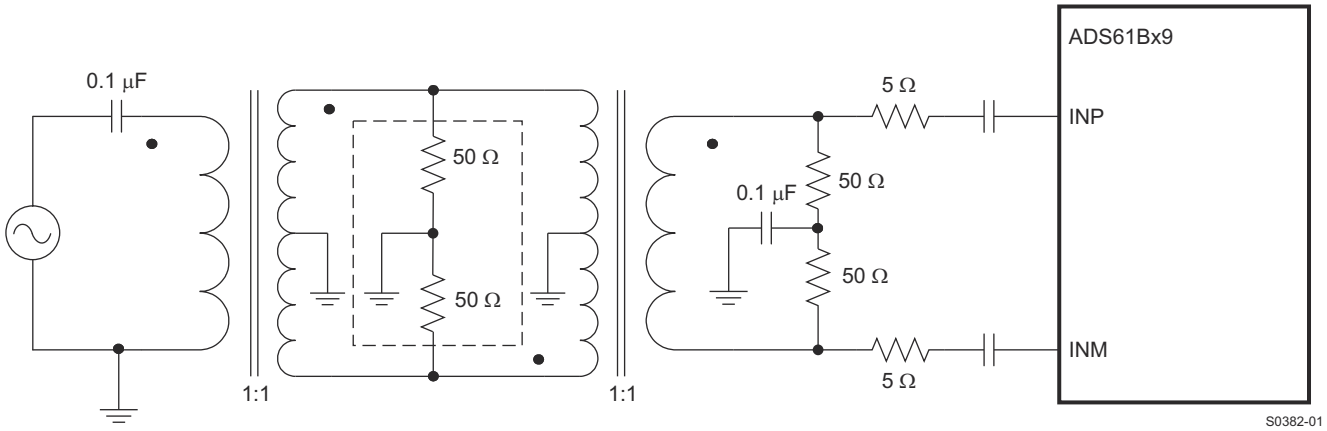


Figure 7-5. Drive Circuit for High Frequencies

7.1.2.3 Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1-µF low-inductance capacitor connected to ground. The input common-mode voltage is nominally 2.3 V, which is 1.5 V for the ADS6149.

7.1.3 Reference

The ADS61B49/29 have built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the on-chip integration of the requisite reference capacitors eliminates the need for external decoupling. External reference mode is not supported. The reference generates the VCM output (2.3 V).

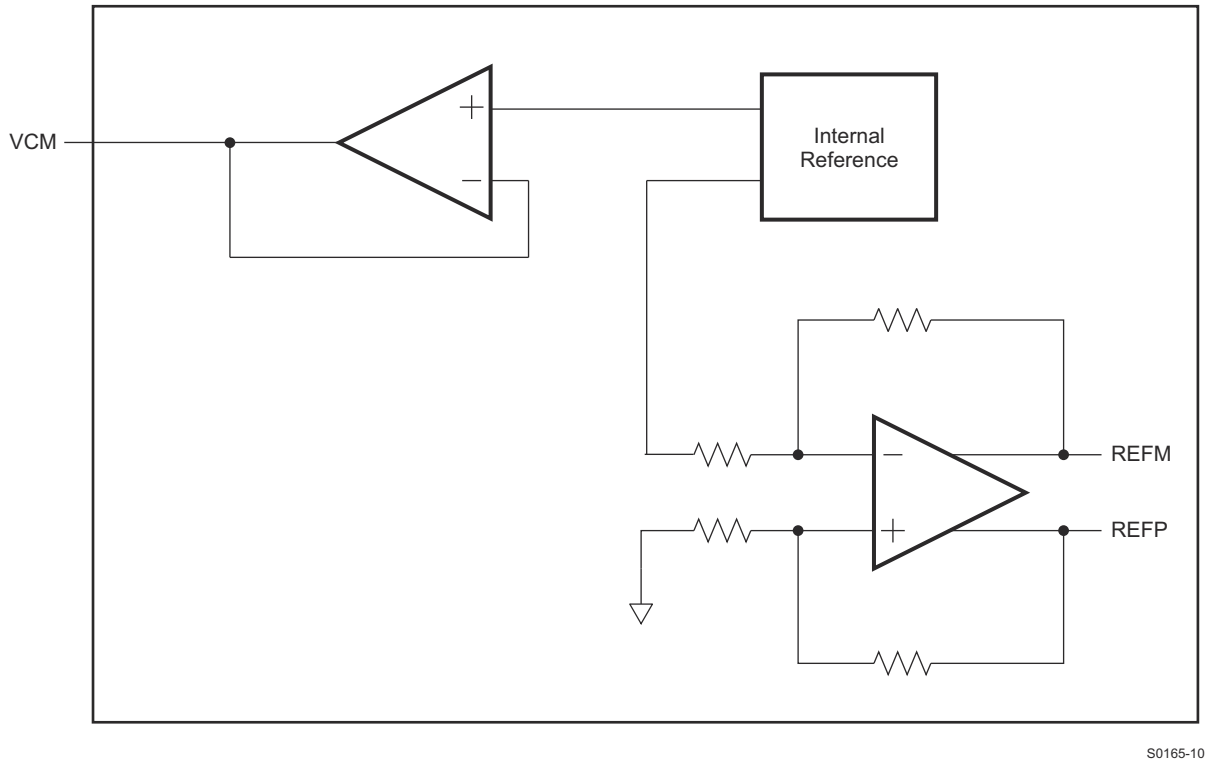


Figure 7-6. Reference Section

7.1.4 Clock Input

The ADS61B49/29 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS) with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS clock sources.

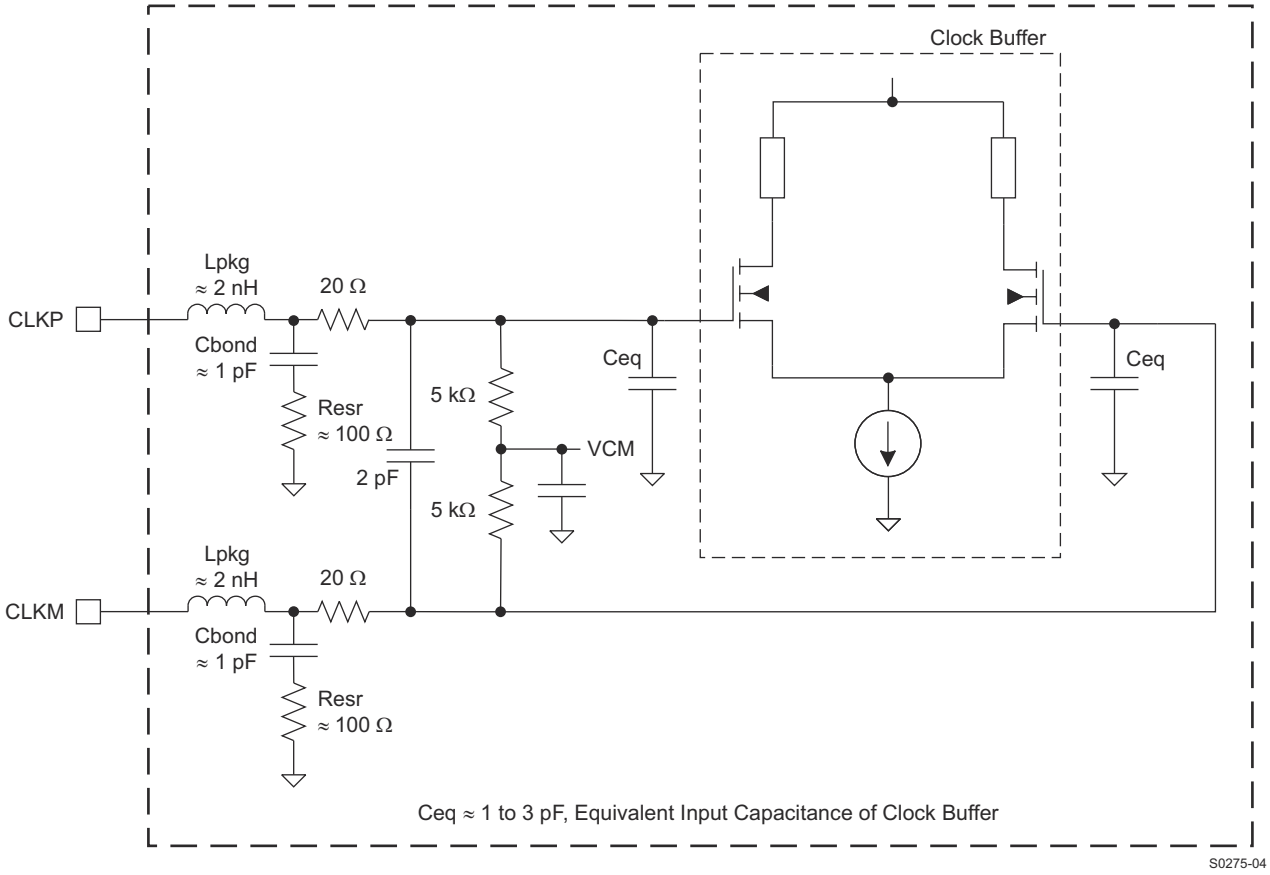


Figure 7-7. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 7-9. For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

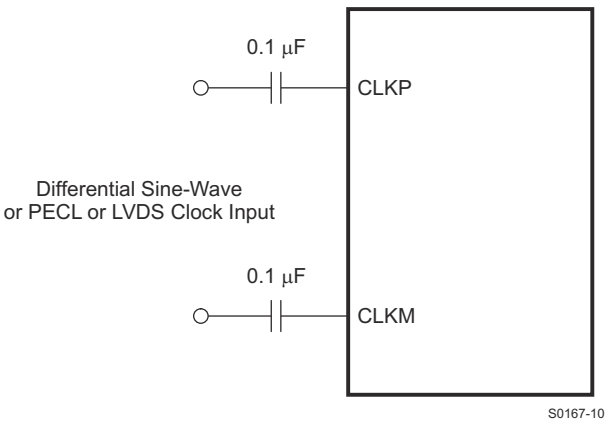


Figure 7-8. Differential Clock Driving Circuit

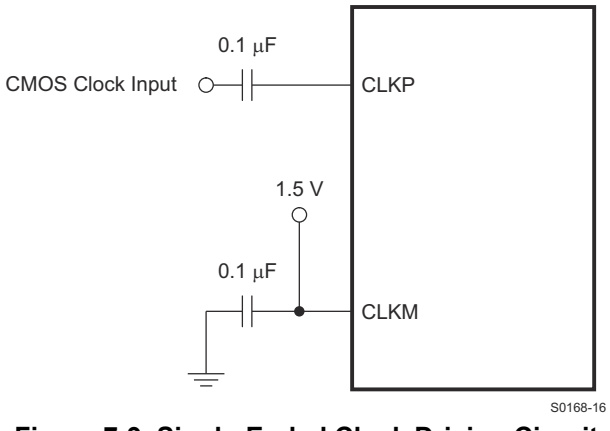


Figure 7-9. Single-Ended Clock Driving Circuit

7.1.5 Fine Gain Control

The ADS61B49/29 include gain settings that can be used to get improved SFDR performance (compared to no gain) or to reduce the required full-scale input voltage. The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 7-1.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades about 0.5–1 dB. The SNR degradation is less at high input frequencies. As a result, the fine gain is useful at high input frequencies as the SFDR improvement is significant with marginal degradation in SNR.

So, the fine gain can be used to trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

Table 7-1. Full-Scale Range Across Gains

GAIN, dB	TYPE	FULL-SCALE, V_{PP}
0	Default after reset	2 V
1	Fine, programmable	1.78
2		1.59
3		1.42
4		1.26
5		1.12
6		1.00

7.1.6 Offset Correction

The ADS61B49/29 have an internal offset correction algorithm that estimates and corrects the dc offset up to ±10 mV. The correction can be enabled using the serial register bit <ENABLE OFFSET CORR>. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using register bits <OFFSET CORR TIME CONSTANT> as described in Table 7-2.

After the offset is estimated, the correction can be locked in by setting <OFFSET CORR TIME CONSTANT> = 0. Once locked, the last estimated value is used for offset correction every clock cycle. Note that offset correction is disabled by default after a reset.

Figure 7-10 shows the time response of the offset correction algorithm, after it is enabled.

Table 7-2. Time Constant of Offset Correction Algorithm

<OFFSET CORR TIME CONSTANT> D3-D0	TIME CONSTANT (T_{CCLK}), NUMBER OF CLOCK CYCLES	TIME CONSTANT, sec (T_{CCLK} x 1/F_s)[1]
0000	256 k	1 ms
0001	512 k	2 ms
0010	1 M	4 ms
0011	2 M	8 ms
0100	4 M	17 ms
0101	8 M	33 ms
0110	16 M	67 ms
0111	32 M	134 ms
1000	64 M	268 ms
1001	128 M	536 ms
1010	256 M	1.1 s
1011	512 M	2.2 s
1100	Reserved	–
1101	Reserved	–
1110	Reserved	–

Table 7-2. Time Constant of Offset Correction Algorithm (continued)

<OFFSET CORR TIME CONSTANT> D3-D0	TIME CONSTANT (T_{CCLK}), NUMBER OF CLOCK CYCLES	TIME CONSTANT, sec (T_{CCLK} x 1/F_s)(1)
1111	Reserved	–

(1) Sampling frequency, F_s = 250 MSPS

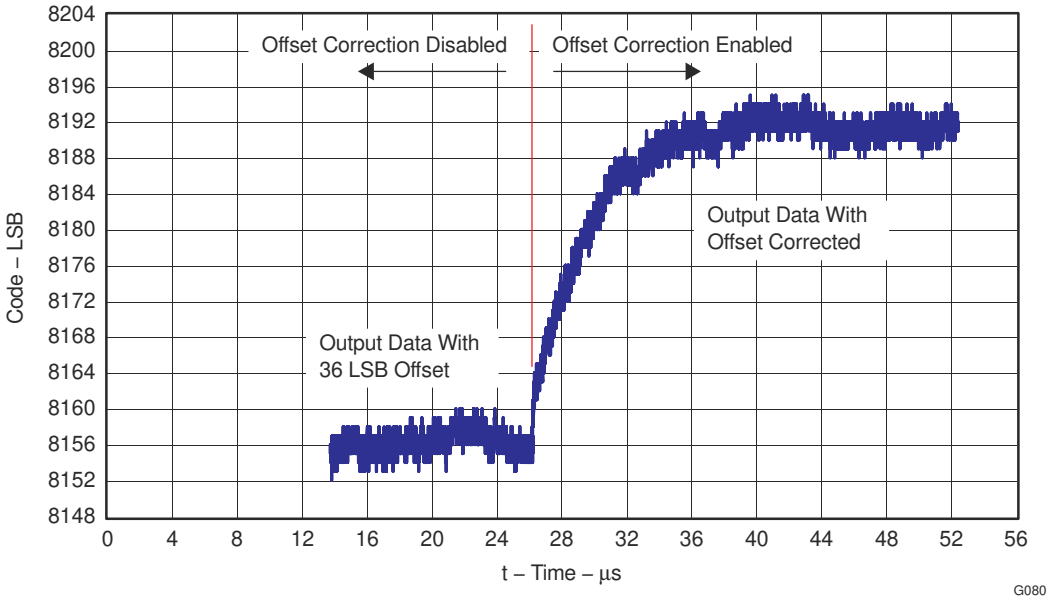


Figure 7-10. Output Code Time Response with Offset Correction Enabled

7.1.7 Power Down

The ADS61B49/29 have three power-down modes – power-down global, standby, and output buffer disable.

7.1.7.1 Power-Down Global

In this mode, the entire chip including the A/D converter, the internal reference, and the output buffers are powered down resulting in reduced total power dissipation of about 20 mW. The output buffers are in a high impedance state. The wake-up time from global power down to data becoming valid in normal mode is typically 25 µs.

This can be controlled using register bit **<PDN GLOBAL>** or using the SDATA pin (in parallel configuration mode).

7.1.7.2 Standby

Here, only the A/D converter is powered down and the internal references are active, resulting in a fast wake-up time of 300 ns. The total power dissipation in standby is about 120 mW.

This can be controlled using register bit **<STANDBY>**.

7.1.7.3 Output Buffer Disable

The output buffers can be disabled and put in a high impedance state – wakeup time from this mode is fast, about 40 ns. This can be controlled using register bit **<PDN OBUF>**.

7.1.7.4 Input Clock Stop

In addition to the above, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 120 mW.

7.1.8 Power Supply Sequence

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated in the device.

7.1.9 Digital Output Information

The ADS61B49/29 provide 14-bit/12-bit data and an output clock synchronized with the data.

7.1.9.1 Output Interface

Two output interface options are available – double data rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit **<ODI>** or using the DFS pin in parallel configuration mode.

7.1.9.2 DDR LVDS Outputs

In this mode, the data bits and clock are output using low voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair.

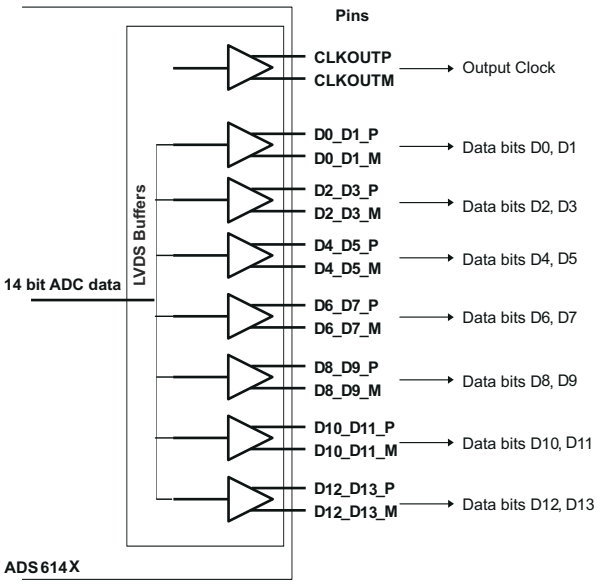


Figure 7-11. 14-Bit ADC LVDS Outputs

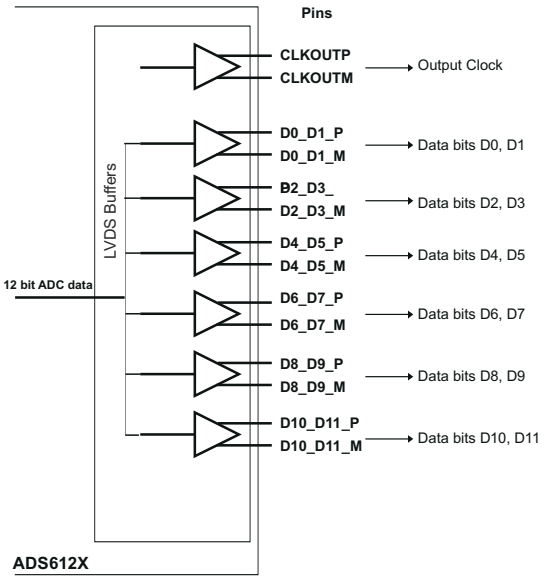


Figure 7-12. 12-Bit ADC LVDS Outputs

Even data bits D0, D2, D4… are output at the falling edge of CLKOUTP, and the odd data bits D1, D3, D5… are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all of the data bits (see Figure 7-13).

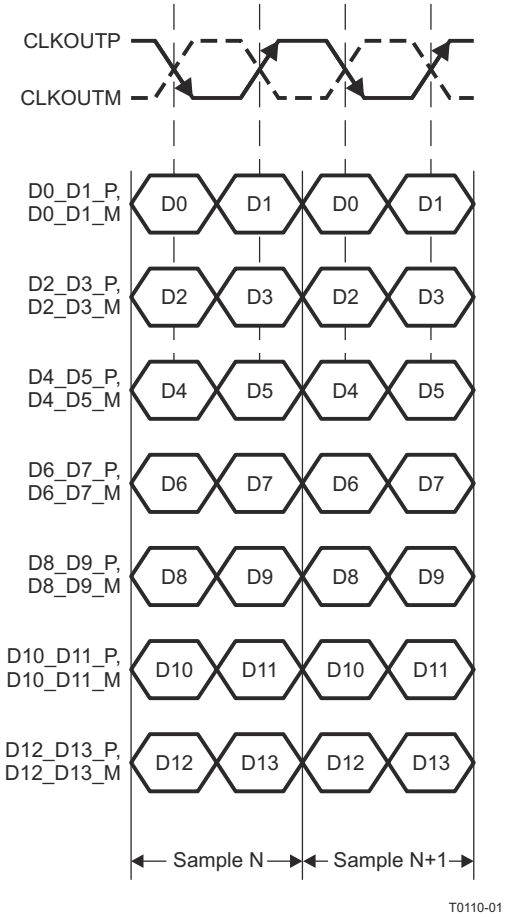


Figure 7-13. DDR LVDS Interface

7.1.9.3 LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 7-14. The buffer is designed to present an output impedance of 100 Ω (Rout). The differential outputs can be terminated at the receive end by a 100-Ω termination. The buffer output impedance behaves like a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity. Note that this internal termination cannot be disabled and its value cannot be changed.

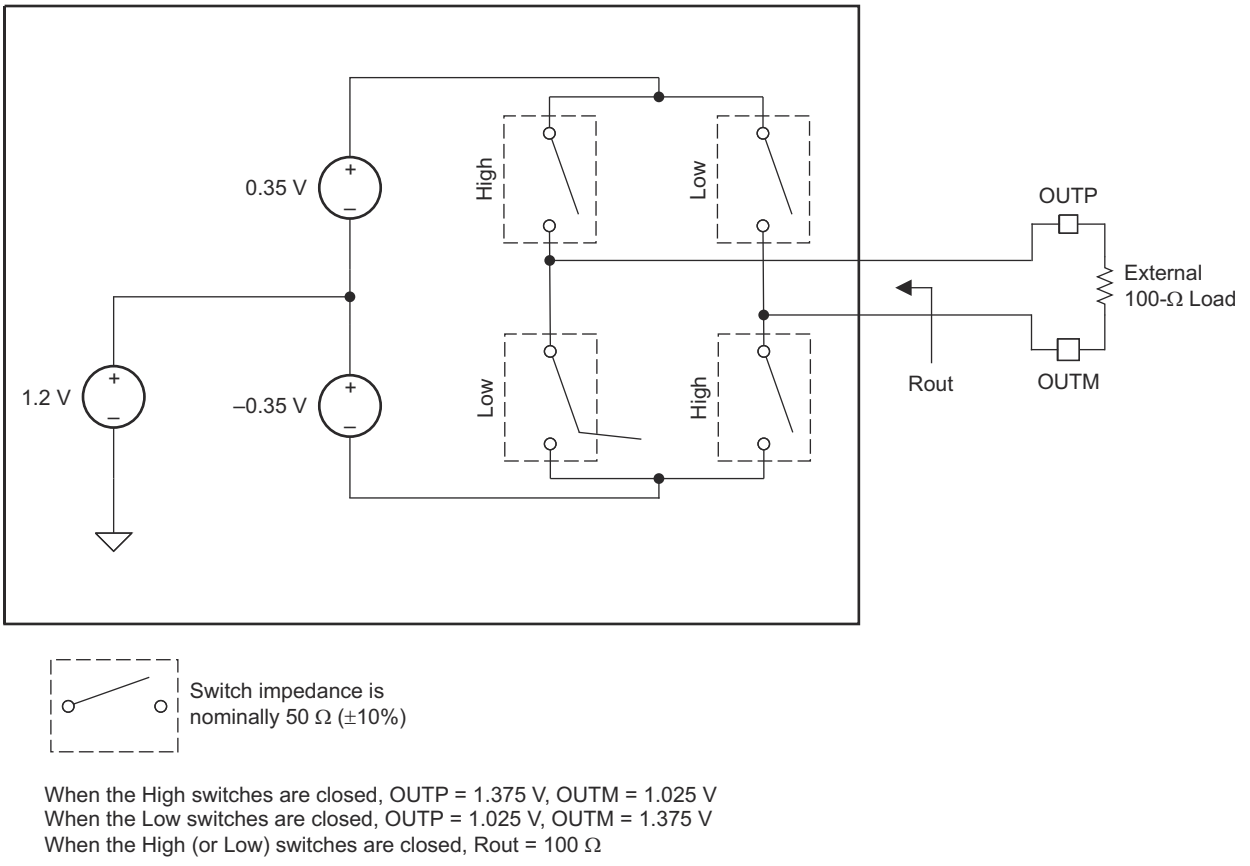


Figure 7-14. LVDS Buffer Equivalent Circuit

7.1.9.4 Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as a CMOS voltage level, every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver ***(for sampling frequencies up to approximately 150 MSPS)*** .

Up to 150 MSPS, the setup and hold timings of the output data with respect to CLKOUT are specified. It is recommended to minimize the load capacitance seen by data and clock output pins by using short traces to the receiver. Also, match the output data and clock traces to minimize the skew between them.

For sampling frequencies > 150 MSPS in CMOS mode, it is recommended to use an external clock to capture data. The input clock to output data delay and data valid times are specified for the higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture the data (see Figure 5-4). It is recommended to consider using the LVDS output mode at high sample rates due to device and board noise generated by the CMOS mode.

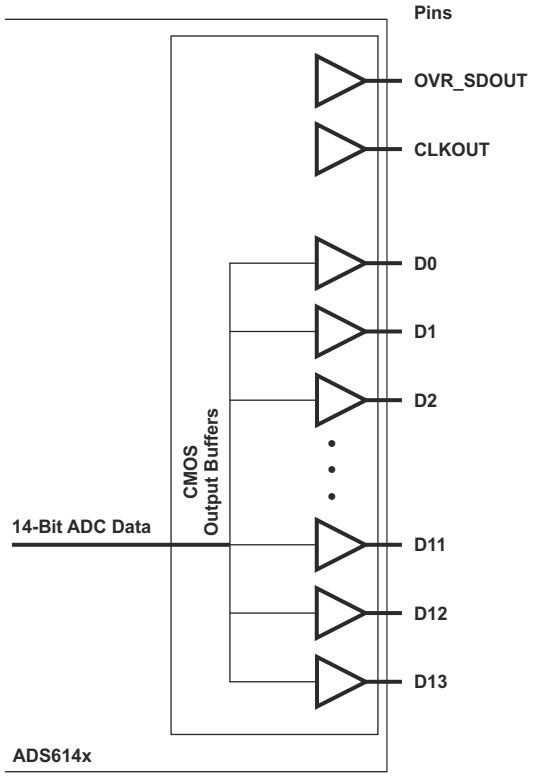


Figure 7-15. CMOS Output Interface

7.1.9.5 Output Buffer Strength Programmability

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs during the instant of sampling and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this, the CMOS output buffers are designed with a controlled drive strength to achieve the best SNR. The default drive strength also ensures a wide data stable window for load capacitances up to 5 pF.

7.1.9.6 CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In an actual application, the DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current due to CMOS output switching = C_L × DRVDD × (N × F_{AVG}),

where

C_L = load capacitance,

N x F_{AVG} = average number of output bits switching.

Figure 5-46 shows the current across the sampling frequencies with a 3-MHz analog input frequency.

7.1.9.7 Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using the serial interface register bit **<DATA FORMAT>** or controlling the DFS pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 0x3FFF in offset binary output format, and 0x1FFF in 2s complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x2000 in 2s complement output format.

7.1.10 Board Design Considerations

7.1.10.1 Grounding

A single ground plane is sufficient to achieve good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the EVM User Guide for details on layout and grounding.

7.1.10.2 Supply Decoupling

As the ADS61B49/29 already include internal decoupling, minimal external decoupling can be used without a loss in performance. Note that decoupling capacitors can help filter external power supply noise, so the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

7.1.10.3 Exposed Pad

In addition to providing a path for heat dissipation, the pad is also electrically connected to digital ground internally. So, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance.

For detailed information, see the application notes for QFN Layout Guidelines (SLOA122) and QFN/SON PCB Attachment (SLUA271).

7.1.11 Definition of Specifications

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay will be different across channels. The maximum variation is specified as aperture delay variation (channel-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error due to reference inaccuracy and error due to the channel. Both these errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from (1-0.5/100) x FS_{ideal} to (1 + 0.5/100) x FS_{ideal}.

Offset Error – The offset error is the difference, given in number of LSBs, between the actual average idle channel output code and the ideal average idle channel output code of the ADC. This quantity is often mapped into mV.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

Effective Number of Bits (ENOB) – The ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{3}$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (PD).

$$\text{THD} = 10\text{Log}^{10}\frac{P_S}{P_N} \tag{4}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR) – The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

AC Power Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then

$$\text{PSRR} = 20\text{Log}^{10}\frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \tag{5}$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from their expected values) is noted.

Common Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then

$$\text{CMRR} = 20\text{Log}^{10}\frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \tag{6}$$

Cross-Talk (only for multi-channel ADC)– This is a measure of the internal coupling of a signal from adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Cross-talk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Third-Party Products Disclaimer

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2009) to Revision C (May 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added Table of Contents, Pin Configuration and Functions sections, Specifications section, Detailed Description section, Functional Block Diagrams section, Application and Implementation section, Device and Documentation Support section, Revision History section, and Mechanical, Packaging, and Orderable Information section	1
• Added Package Information table to Description	1
• Changed Sampling Frequency from 100MSPS to 80MSPS in Timing Requirements table and Table 5-1 and Table 5-2	13
• Changed from 100MSPS to 80MSPS for ENABLE LOW SPEED MODE in Section 6.3.1	37

Changes from Revision A (December 2008) to Revision B (May 2009)	Page
• Changed DFS pin number from 8 to 6 in Section 4.1	3
• Changed DFS pin number from 8 to 6 in Section 4.2	5
• Added OE input to ADS61B29 block diagram	29
• Added OE input to ADS61B49 block diagram	30

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS61B29IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ61B29
ADS61B29IRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ61B29
ADS61B29IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ61B29
ADS61B29IRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ61B29
ADS61B49IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ61B49
ADS61B49IRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ61B49
ADS61B49IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ61B49
ADS61B49IRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ61B49

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

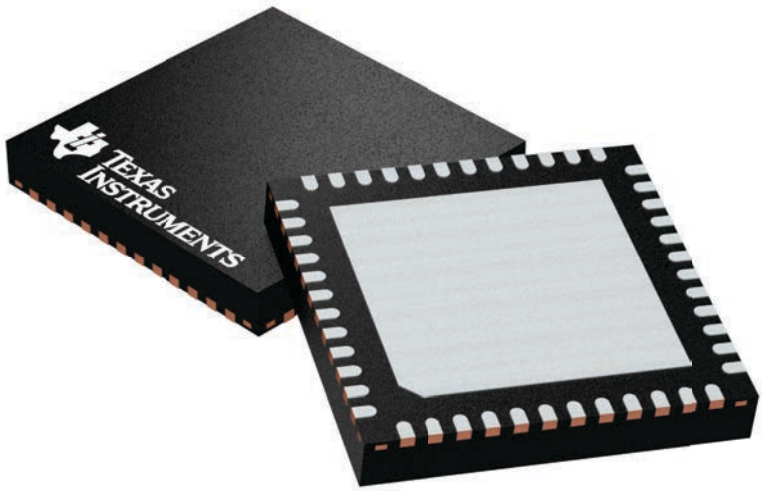
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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