TEXAS INSTRUMENTS

**ADS54T01**
SLAS918B – DECEMBER 2012 – REVISED APRIL 2022

# ADS54T01 Single 12-Bit 750-Msps Receiver and Feedback IC

## 1 Features

- Single channel
- 12-bit resolution
- Maximum clock rate: 750 Msps
- Low swing fullscale input: 1.0 Vpp
- Analog input buffer with high impedance input
- Input bandwidth (3 dB): > 1.2 GHz
- Data output interface: DDR LVDS
- 196-Pin NFBGA package (12 mm × 12 mm)
- Power dissipation: 1.2 W
- Performance at $f_{in}$ = 230 MHz IF
  - SNR: 60.7 dBFS
  - SFDR: 73 dBc
- Performance at $f_{in}$ = 700 MHz IF
  - SNR: 58.6 dBFS
  - SFDR: 64 dBc
- Receive mode: 2x decimation with low-pass or high-pass filter
- Feedback mode: burst mode output for full bandwidth DPD feedback

## 2 Applications

- Telecommunications
- Wireless infrastructure
- Power amplifier linearization
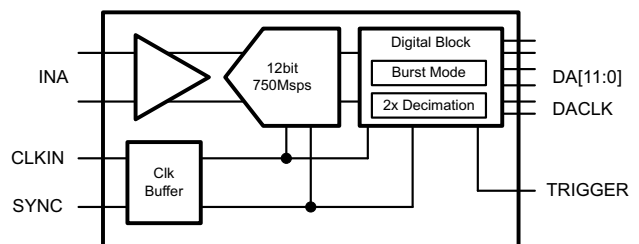
## 3 Description

The ADS54T01 is a high linearity, single channel, 12-bit, 750-Msps analog-to-digital converter (ADC) easing front end filter design for wide bandwidth receivers. The analog input buffer isolates the internal switching of the on-chip track-and-hold from disturbing the signal source as well as providing a high-impedance input.

Two output modes are available for the output data —the data can be decimated by two or the data can be output in burst mode. The burst mode output is designed specifically for DPD feedback applications where high-resolution output data is available for a short period of time. Designed for high SFDR, the ADC has low-noise performance and outstanding spurious-free dynamic range over a large input-frequency range. The device is available in a 196-pin NFBGA package and is specified over the full industrial temperature range (–40°C to 85°C).

**Device Information**

| PART NUMBER | PACKAGE[1] | BODY SIZE (NOM) |
|---|---|---|
| ADS54T01 | NFBGA (196) | 12.00 mm × 12.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Functional Block Diagram**

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## 4 Revision History

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# 5 Device Comparison

**Table 5-1. Device Comparison**

| PART NUMBER | NUMBER OF CHANNELS | SPEED GRADE |
|---|---|---|
| ADS54T02 | 2 | 750 Msps |
| ADS54T01 | 1 | 750 Msps |
| ADS54T04 | 2 | 500 Msps |

# 6 Pin Configuration and Functions

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 14 | VREF | VCM | GND | NC | NC | GND | AVDDC | AVDDC | GND | INA_P | INA_N | GND | GND | CLKINP | 14 |
| 13 | SDENB | TEST MODE | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | CLKINN | 13 |
| 12 | SCLK | SRESET | GND | AVDD33 | AVDD33 | AVDD33 | AVDD33 | AVDD33 | AVDD33 | AVDD33 | AVDD33 | GND | AVDD33 | AVDD33 | 12 |
| 11 | SDIO | ENABLE | GND | AVDD18 | AVDD18 | AVDD18 | AVDD18 | AVDD18 | AVDD18 | AVDD18 | AVDD18 | GND | AVDD18 | AVDD18 | 11 |
| 10 | SDO | IOVDD | GND | AVDD18 | GND | GND | GND | GND | GND | GND | AVDD18 | GND | TRIGGER N | TRIGGER P | 10 |
| 9 | DVDD | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | SYNCN | SYNCP | 9 |
| 8 | DVDD | DVDD | DVDD | DVDD | GND | GND | GND | GND | GND | GND | DVDD | DVDD | DVDD | DVDD | 8 |
| 7 | NC | NC | DVDD LVDS | DVDD LVDS | GND | GND | GND | GND | GND | GND | DVDD LVDS | DVDD LVDS | TRDYN | TRDYP | 7 |
| 6 | NC | NC | DVDD LVDS | DVDD LVDS | GND | GND | GND | GND | GND | GND | DVDD LVDS | DVDD LVDS | HRESN | HRESP | 6 |
| 5 | NC | NC | NC | NC | GND | GND | GND | GND | GND | GND | OVRAN | OVRAP | SYNC OUTN | SYNC OUTP | 5 |
| 4 | NC | NC | NC | NC | NC | NC | NC | DA0P | DA2P | DA4P | DA6P | DA8P | NC | NC | 4 |
| 3 | NC | NC | NC | NC | NC | NC | NC | DA0N | DA2N | DA4N | DA6N | DA8N | DA11N | DA11P | 3 |
| 2 | NC | NC | NC | NC | NC | NC | NC | DACLKP | DA1P | DA3P | DA5P | DA7P | DA10N | DA10P | 2 |
| 1 | NC | NC | NC | NC | NC | NC | NC | DACLKN | DA1N | DA3N | DA5N | DA7N | DA9N | DA9P | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | |

**Figure 6-1. ADS54T01 ZAY Package, 196-Pin NFBGA, Top View (DDR Output Mode)**

**Table 6-1. Pin Functions**

| PIN | | I/O TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| **INPUT/REFERENCE** | | | |
| INA_P/N | K14, L14 | I | Analog ADC differential input signal. |
| VCM | B14 | O | Output of the analog input common mode (nominally 1.9 V). A 0.1-µF capacitor to AGND is recommended, but not required. |
| VREF | A14 | I | Reference voltage input. A 0.1-µF capacitor to AGND is recommended. |
| **CLOCK/SYNC** | | | |
| CLKINP/N | P14, P13 | I | Differential input clock |

**Table 6-1. Pin Functions (continued)**

| PIN | | I/O TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| SYNCP/N | P9, N9 | I | Synchronization input. Inactive if logic low. When clocked in a high state initially, this is used for resetting internal clocks and digital logic and starting the SYNCOUT signal. Internal 100-Ω termination. |
| **CONTROL/SERIAL** | | | |
| SRESET | B12 | I | Serial interface reset input. Active low. Initialized internal registers during high-to-low transition. Asynchronous. Internal 50-kΩ pullup resistor to IOVDD. |
| ENABLE | B11 | I | Chip enable – active high. Power-down function can be controlled through SPI register assignment. Internal 50-kΩ pullup resistor to IOVDD. |
| SCLK | A12 | I | Serial interface clock. Internal 50-kΩ pulldown resistor. |
| SDIO | A11 | I/O | Bidirectional serial data in 3-pin mode (default). In 4-pin interface mode (register x00, D16), the SDIO pin in an input only. Internal 50-kΩ pulldown resistor. |
| SDENB | A13 | I | Serial interface enable. Internal 50-kΩ pulldown resistor. |
| SDO | A10 | O | Uni-directional serial interface data in 4-pin mode (register x00, D16). The SDO pin is tri-stated in 3-pin interface mode (default). Internal 50-kΩ pulldown resistor. |
| **DATA INTERFACE** | | | |
| DA[11:0]P/N | P3, N3, P2, N2, P1, N1, M4, M3, M2, M1, L4, L3, L2, L1, K4, K3, K2, K1, J4, J3, J2, J1, H4, H3 | O | ADC A Data Bits 11 (MSB) to 0 (LSB) in DDR output mode. Standard LVDS output. |
| DACLKP/N | H2, H1 | O | DDR differential output data clock for Bus A. Register programmable to provide either rising or falling edge to center of stable data nominal timing. |
| SYNCOUTP/N | P5, N5 | O | Synchronization output signal for synchronizing multiple ADCs. Can be disabled through the SPI. |
| OVRAP/N | M5, L5 | O | Bus A, Overrange indicator, LVDS output. A logic high signals an analog input in excess of the full-scale range. Optional SYNC output. |
| TRIGGERP/N | P10, N10 | I | Trigger used for high-resolution output data in feedback mode. Internal 100-Ω termination. |
| TRDYP/N | P7, N7 | O | Trigger ready output indicator |
| HRESP/N | P6, N6 | O | Indicator for high-resolution output data; logic high signals 12-bit output data. |
| **NO CONNECT** | | | |
| NC | A1, A2, A3, A4, A5, A6, A7, B1, B2, B3, B4, B5, B6, B7, C1, C2, C3, C4, C5, D1, D2, D3, D4, D5, D14, E1, E2, E3, E4, E14, F1, F2, F3, F4, G1, G2, G3, G4, N4, P4 | – | Do not connect to pin, leave floating. |
| TESTMODE | B13 | – | Used for factory internal test. Do not connect to pin, leave floating. |
| **POWER SUPPLY** | | | |
| AVDD33 | D12, E12, F12, G12, H12, J12, K12, L12, N12, P12 | P | 3.3-V analog supply |
| AVDDC | G14, H14 | P | 1.8-V supply for clock input |
| AVDD18 | D10, D11, E11, F11, G11, H11, J11, K11, L10, L11, N11, P11 | P | 1.8-V analog supply |

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**Table 6-1. Pin Functions (continued)**

| PIN | | I/O TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| DVDD | A8, A9, B8, B9, C8, D8, L8, M8, N8, P8 | P | 1.8-V supply for digital block |
| DVDDLVDS | C6, C7, D6, D7, L6, L7, M6, M7 | P | 1.8-V supply for LVDS outputs |
| IOVDD | B10 | P | 1.8-V for digital I/Os |
| GND | C9, C10, C11, C12, C13, C14, D9, D13, E5, E6, E7, E8, E9, E10, E13, F5, F6, F7, F8, F9, F10, F13, F14, G5, G6, G7, G8, G9, G10,H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10, L9, M9, M10, M11, M12, M13, M14,N13, N14 | GND | Ground |

(1)   The definitions below define the I/O type for each pin.
  • I = Input
  • O = Output
  • I/O = Input / Output
  • P = Power Supply
  • G = Ground

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | AVDD33 | −0.5 | 4 | V |
| | AVDDC | −0.5 | 2.3 | V |
| | AVDD18 | −0.5 | 2.3 | V |
| | DVDD | −0.5 | 2.3 | V |
| | DVDDLVDS | −0.5 | 2.3 | V |
| | IOVDD | −0.5 | 4 | V |
| Voltage applied to input pins | INA_P, INA_N | −0.5 | AVDD33 + 0.5 | V |
| | CLKINP, CLKINN | −0.5 | AVDDC + 0.5 | V |
| | SYNCP, SYNCN | −0.5 | AVDD33 + 0.5 | V |
| | SRESET, SDENB, SCLK, SDIO, SDO, ENABLE | −0.5 | IOVDD + 0.5 | V |
| Operating free-air temperature, $T_A$ | | −40 | 85 | °C |
| Operating junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | −65 | 150 | °C |

(1)    Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | ±2000 | V |

(1)    JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $T_J$ | Recommended operating junction temperature | | | 105 | °C |
| | Maximum rated operating junction temperature[1] | 125 | | | |
| $T_A$ | Recommended free-air temperature | –40 | 25 | 85 | °C |

(1)     Prolonged use at this junction temperature may increase the device failure-in-time (FIT) rate.

## 7.4 Thermal Information

| THERMAL METRIC[1] | | ADS54T01 | UNIT |
|---|---|---|---|
| | | ZAY (NFBGA) | |
| | | 196 PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance[2] | 37.6 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance[3] | 6.8 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance[4] | 16.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter[5] | 0.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter[6] | 16.4 | °C/W |

(1)     For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2)     The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3)     The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4)     The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5)     The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6)     The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

## 7.5 Electrical Characteristics

Typical values at $T_A$ = 25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **ADC Clock Frequency** | | | 40 | | 750 | MSPS |
| **Resolution** | | | 12 | | | Bits |
| **SUPPLY** | | | | | | |
| AVDD33 | | | 3.15 | 3.3 | 3.45 | V |
| AVDDC, AVDD18, DVDD, DVDDLVDS | | | 1.7 | 1.8 | 1.9 | V |
| IOVDD | | | 1.7 | 1.8 | 3.45 | V |
| **POWER SUPPLY** | | | | | | |
| $I_{AVDD33}$ | 3.3-V Analog supply current | | | 154 | 170 | mA |
| $I_{AVDD18}$ | 1.8-V Analog supply current | | | 66 | 80 | mA |
| $I_{AVDDC}$ | 1.8-V Clock supply current | | | 42 | 60 | mA |
| $I_{DVDD}$ | 1.8-V Digital supply current | Auto Correction Enabled | | 250 | 280 | mA |
| $I_{DVDD}$ | 1.8-V Digital supply current | Auto Correction Disabled | | 215 | | mA |
| $I_{DVDD}$ | 1.8-V Digital supply current | Auto Correction Disabled, decimation filter enabled | | 234 | | mA |
| $I_{DVDDLVDS}$ | 1.8-V LVDS supply current | | | 66 | 90 | mA |
| $I_{IOVDD}$ | 1.8-V I/O Voltage supply current | | | 1 | 2 | mA |

## 7.5 Electrical Characteristics (continued)

Typical values at $T_A$ = 25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $P_{dis}$ | Total power dissipation | Auto Correction Enabled, decimation filter disabled | | 1.28 | 1.75 | W |
| $P_{dis}$ | Total power dissipation | Auto Correction Disabled, decimation filter disabled | | 1.2 | | W |
| PSRR | | 250 kHz to 500 MHz | 40 | | | dB |
| Shutdown power dissipation | | | | 7 | | mW |
| Shutdown wake-up time | | | | 2.5 | | ms |
| Standby power dissipation | | | | 7 | | mW |
| Standby wake-up time | | | | 100 | | µs |
| Deep-sleep mode power dissipation | | Auto correction disabled | | 350 | | mW |
| | | Auto correction enabled | | 475 | | mW |
| Deep-sleep mode wake-up time | | | | 20 | | µs |
| Light-sleep mode power dissipation | | Auto correction disabled | | 655 | | mW |
| | | Auto correction enabled | | 780 | | mW |
| Light-sleep mode wake-up time | | | | 2 | | µs |

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## 7.6 Electrical Characteristics

Typical values at $T_A$ = 25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD/DRVDD/IOVDD = 1.8 V, –1-dBFS differential input (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **ANALOG INPUTS** | | | | | |
| Differential input full-scale | | | 1.0 | 1.25 | Vpp |
| Input common-mode voltage | | | 1.9 | ±0.1 | V |
| Input resistance | Differential at DC | | 1 | | kΩ |
| Input capacitance | Each input to GND | | 2 | | pF |
| VCM common-mode voltage output | | | 1.9 | | V |
| Analog input bandwidth (3 dB) | | | 1200 | | MHz |
| **DYNAMIC ACCURACY** | | | | | |
| Offset Error | Auto Correction Disabled | –20 | –7.5 | 20 | mV |
| | Auto Correction Enabled | –1 | 0 | 1 | mV |
| Offset temperature coefficient | | | –6.5 | | µV/°C |
| Gain error | | –5 | | 5 | %FS |
| Gain temperature coefficient | | | 0.005 | | %FS/°C |
| Differential nonlinearity | $f_{IN}$ = 230 MHz | –1 | ±0.9 | 2 | LSB |
| Integral nonlinearity | $f_{IN}$ = 230 MHz | –5 | ±1.5 | 5 | LSB |
| **CLOCK INPUT** | | | | | |
| Input clock frequency | | 40 | | 750 | MHz |
| Input clock amplitude | | | 2 | | Vpp |
| Input clock duty cycle | | 40% | 50% | 60% | |
| Internal clock biasing | | | 0.9 | | V |

Product Folder Links: ADS54T01

## 7.7 Electrical Characteristics

Typical values at $T_A$ = 25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **Auto Correction** | | | | Enabled | | | Disabled | | Vpp |
| **DYNAMIC AC CHARACTERISTICS**[1] **– Burst Mode Enabled: 12-bit High Resolution Output Data** | | | | | | | | | |
| SNR | Signal to Noise Ratio | $f_{IN}$ = 10 MHz | | 61.1 | | | 61.2 | | dBFS |
| | | $f_{IN}$ = 100 MHz | | 61.1 | | | 61.1 | | |
| | | $f_{IN}$ = 230 MHz | 59 | 60.7 | | | 60.9 | | |
| | | $f_{IN}$ = 450 MHz | | 59.9 | | | 60.5 | | |
| | | $f_{IN}$ = 700 MHz | | 58.6 | | | 59.6 | | |
| HD2,3 | Second and third harmonic distortion | $f_{IN}$ = 10 MHz | | 81 | | | 83 | | dBc |
| | | $f_{IN}$ = 100 MHz | | 76 | | | 81 | | |
| | | $f_{IN}$ = 230 MHz | | 78 | | | 79 | | |
| | | $f_{IN}$ = 450 MHz | | 75 | | | 76 | | |
| | | $f_{IN}$ = 700 MHz | | 74 | | | 76 | | |
| Non HD2,3 | Spur Free Dynamic Range (excluding second and third harmonic distortion) | $f_{IN}$ = 10 MHz | | 78 | | | 79 | | dBc |
| | | $f_{IN}$ = 100 MHz | 68 | 75 | | | 77 | | |
| | | $f_{IN}$ = 230 MHz | | 73 | | | 73 | | |
| | | $f_{IN}$ = 450 MHz | | 68 | | | 69 | | |
| | | $f_{IN}$ = 700 MHz | | 64 | | | 66 | | |
| IL | Fs/2-Fin interleaving spur | $f_{IN}$ = 10 MHz | | 90 | | | 87 | | dBc |
| | | $f_{IN}$ = 100 MHz | | 84 | | | 82 | | |
| | | $f_{IN}$ = 230 MHz | 65 | 79 | | | 76 | | |
| | | $f_{IN}$ = 450 MHz | | 72 | | | 72 | | |
| | | $f_{IN}$ = 700 MHz | | 66 | | | 69 | | |
| SINAD | Signal to noise and distortion ratio | $f_{IN}$ = 10 MHz | | 61.0 | | | 61.1 | | dBc |
| | | $f_{IN}$ = 100 MHz | | 60.8 | | | 61.0 | | |
| | | $f_{IN}$ = 230 MHz | 57.5 | 60.5 | | | 60.8 | | |
| | | $f_{IN}$ = 450 MHz | | 59.8 | | | 60.3 | | |
| | | $f_{IN}$ = 700 MHz | | 58.4 | | | 59.4 | | |
| THD | Total Harmonic Distortion | $f_{IN}$ = 10 MHz | | 76 | | | 76 | | dBc |
| | | $f_{IN}$ = 100 MHz | | 73 | | | 76 | | |
| | | $f_{IN}$ = 230 MHz | 66 | 74 | | | 74 | | |
| | | $f_{IN}$ = 450 MHz | | 74 | | | 73 | | |
| | | $f_{IN}$ = 700 MHz | | 72 | | | 74 | | |
| IMD3 | Inter modulation distortion | $F_{in}$ = 184.5 and 185.5 MHz, –7 dBFS | | 82 | | | 83 | | dBFS |
| | | $F_{in}$ = 549.5 and 550.5 MHz, –7 dBFS | | 76 | | | 77 | | |
| | Crosstalk | | | 90 | | | 90 | | dB |
| ENOB | Effective number of bits | $f_{IN}$ = 230 MHz | | 9.8 | | | 9.8 | | LSB |

(1)   SFDR and SNR calculations do not include the DC or Fs/2 bins when Auto Correction is disabled.

## 7.8 Electrical Characteristics

Typical values at $T_A$ = 25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, ADC sampling rate = 500 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input (unless otherwise noted).

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OVER-DRIVE RECOVERY ERROR** | | | | | | |
| | Input overload recovery | Recovery to within 5% (of final value) for 6-dB overload with sine wave input | | 2 | | ns |
| **SAMPLE TIMING CHARACTERISTICS** | | | | | | |
| rms | Aperture Jitter | Sample uncertainty | | 100 | | fs rms |
| | Data Latency | ADC sample to digital output, Auto correction disabled | | 38 | | Clock Cycles |
| | | ADC sample to digital output, Auto correction enabled | | 50 | | |
| | | ADC sample to digital output, Decimation filter enabled, Auto correction disabled | | 74 | | Sampling clock Cycles |
| | Over-range Latency | ADC sample to over-range output | | 12 | | Clock Cycles |

## 7.9 Electrical Characteristics

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS – SRESET, SCLK, SDENB, SDIO, ENABLE** | | | | | | |
| | High-level input voltage | All digital inputs support 1.8-V and 3.3-V logic levels. | 0.7 x IOVDD | | | V |
| | Low-level input voltage | | | | 0.3 x IOVDD | V |
| | High-level input current | | –50 | | 200 | µA |
| | Low-level input current | | –50 | | 50 | µA |
| | Input capacitance | | | 5 | | pF |
| **DIGITAL OUTPUTS – SDO** | | | | | | |
| | High-level output voltage | Iload = -100 µA | IOVDD – 0.2 | | | V |
| | | Iload = -2 mA | 0.8 x IOVDD | | | |
| | Low-level output voltage | Iload = 100 µA | | | 0.2 | V |
| | | Iload = 2 mA | | | 0.22 x IOVDD | |
| **DIGITAL INPUTS – SYNCP/N, TRIGGERP/N** | | | | | | |
| $V_{ID}$ | Differential input voltage | | 250 | 350 | 450 | mV |
| $V_{CM}$ | Input common-mode voltage | | 1.125 | 1.2 | 1.375 | V |
| $t_{SU}$ | | | 500 | | | ps |
| **DIGITAL OUTPUTS – DA[11:0]P/N, DACLKP/N, OVRAP/N, SYNCOUTP/N, TRDYP/N, HRESP/N** | | | | | | |
| $V_{OD}$ | Output differential voltage | Iout = 3.5 mA | 250 | 350 | 450 | mV |
| $V_{OCM}$ | Output common-mode voltage | Iout = 3.5 mA | 1.125 | 1.25 | 1.375 | V |
| $t_{su}$ | $F_s$ = 750 Msps | Data valid to zero-crossing of DACLK | 320 | 400 | | ps |
| $t_h$ | $F_s$ = 750 Msps | Zero-crossing of DACLK to data becoming invalid | 250 | 320 | | ps |
| $t_{PD}$ | $F_s$ = 750Msps | CLKIN falling edge to DACLK rising edge | 3.36 | 3.69 | 3.92 | ns |

Product Folder Links: *ADS54T01*

## 7.9 Electrical Characteristics (continued)

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{RISE}$ | 10% - 90% | 100 | 150 | 200 | ps |
| $t_{FALL}$ | 90% - 10% | 100 | 150 | 200 | ps |
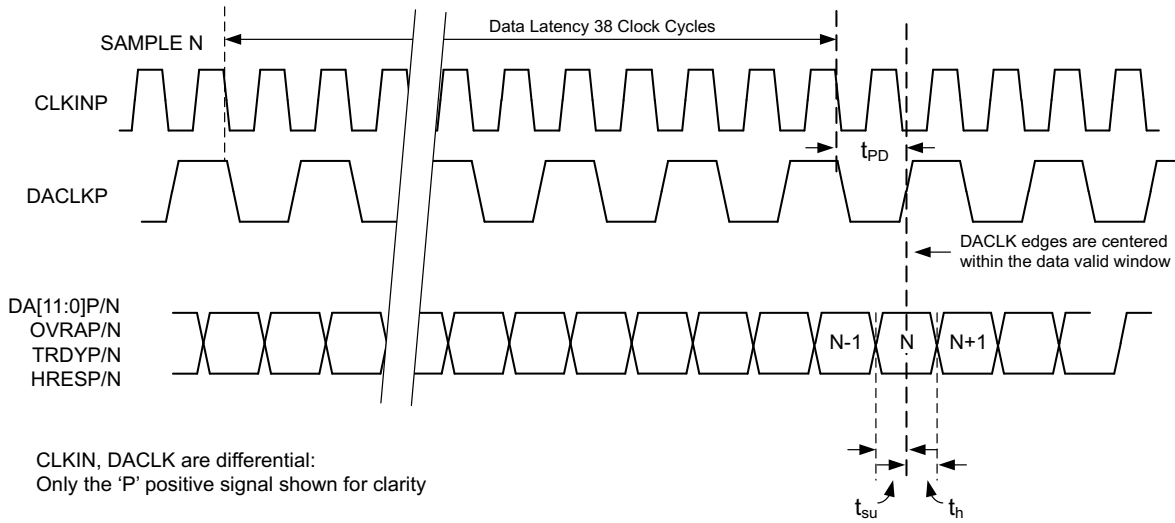


**Figure 7-1. Timing Diagram for 12-Bit DDR Output**

Product Folder Links: *ADS54T01*

## 7.10 Typical Characteristics

Typical values at $T_A$ = +25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input, unless otherwise noted.
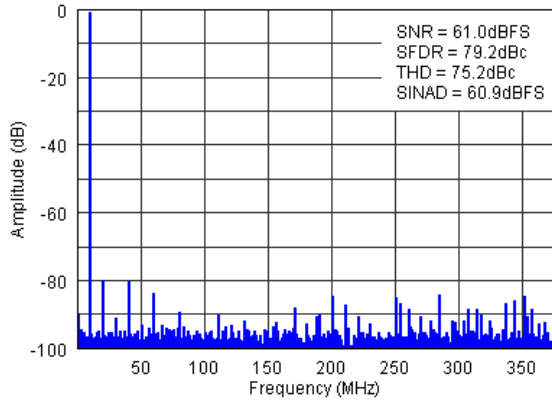


Figure 7-2. FFT for 10-MHz Input Signal (Auto On)
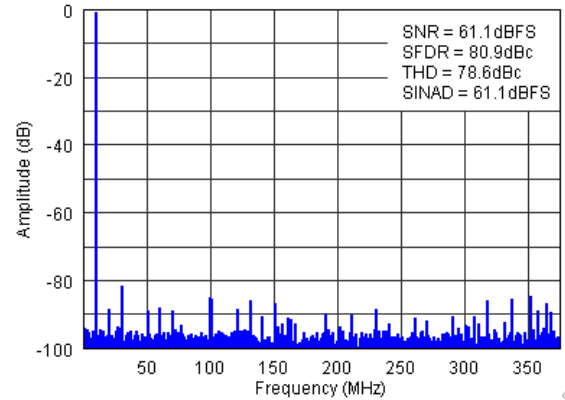


Figure 7-3. FFT for 10-MHz Input Signal (Auto Off)
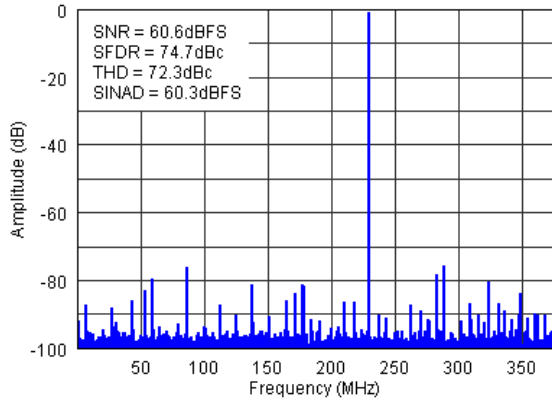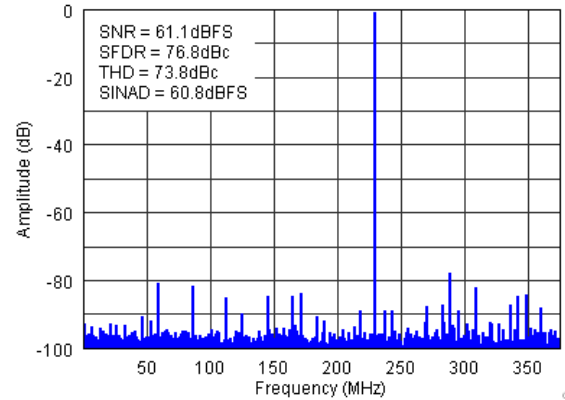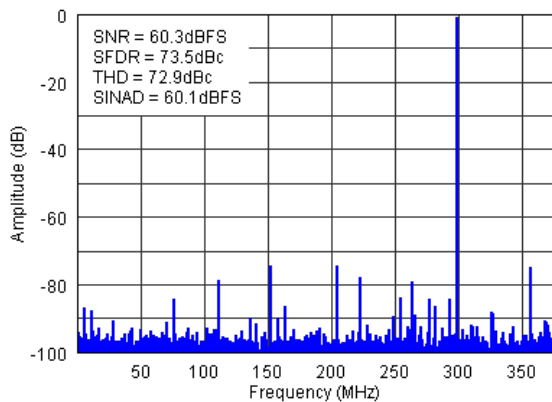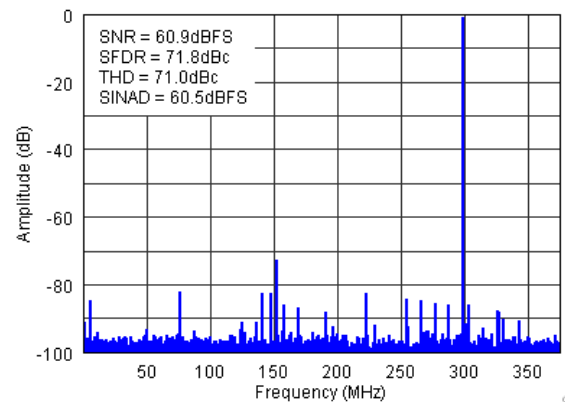


Figure 7-4. FFT for 230-MHz Input Signal (Auto On)



Figure 7-5. FFT for 230-MHz Input Signal (Auto Off)



Figure 7-6. FFT for 450-MHz Input Signal (Auto On)



Figure 7-7. FFT for 450-MHz Input Signal (Auto Off)

Product Folder Links: *ADS54T01*

## 7.10 Typical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input, unless otherwise noted.
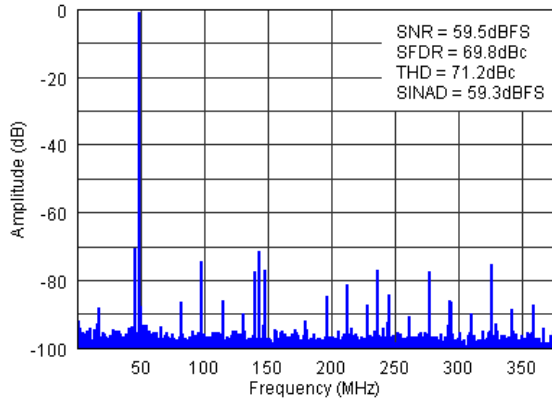


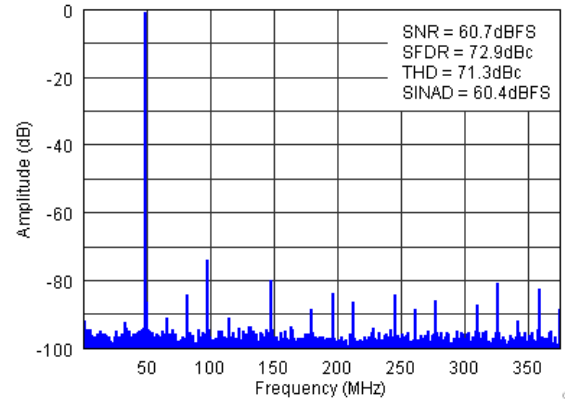Figure 7-8. FFT for 700-MHz Input Signal (Auto On)



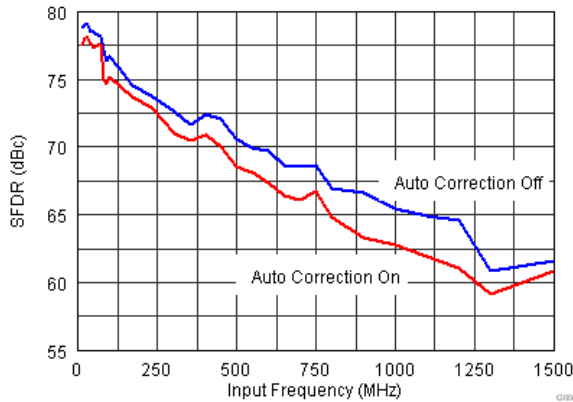Figure 7-9. FFT for 700-MHz Input Signal (Auto Off)
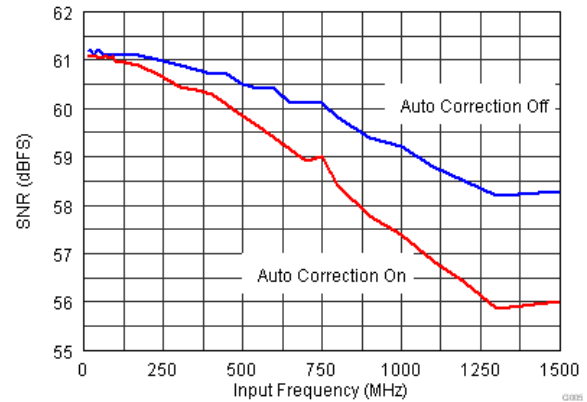


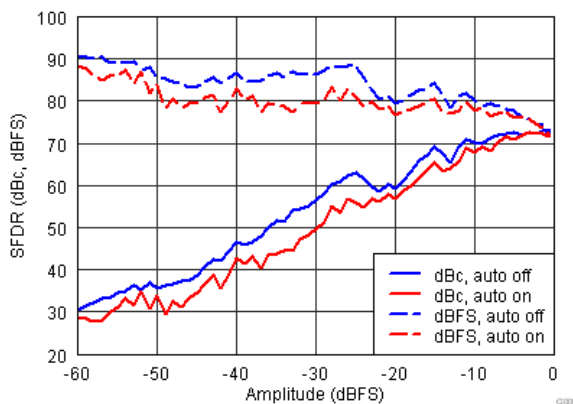Figure 7-10. SFDR vs. Input Frequency



Figure 7-11. SNR vs. Input Frequency



Figure 7-12. SFDR vs. Amplitude (fin = 230 MHz)



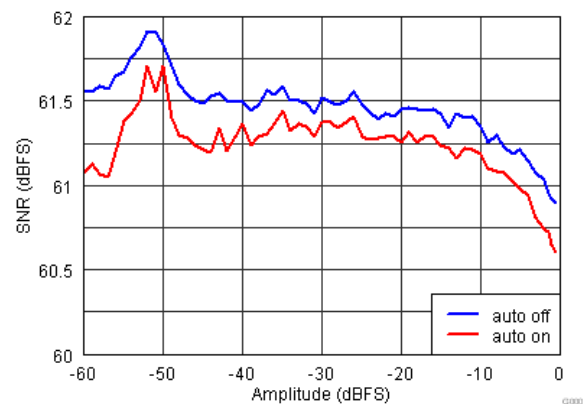Figure 7-13. SNR vs. Amplitude (fin = 230 MHz)

Product Folder Links: *ADS54T01*

## 7.10 Typical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input, unless otherwise noted.
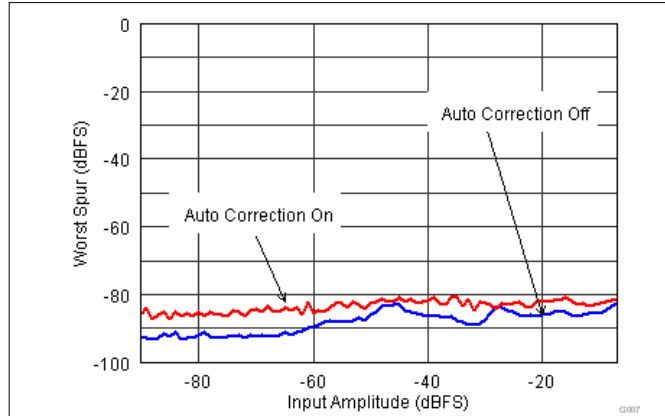
Figure 7-14. Tow Tone Performance Across Input Amplitude (fin = 185 MHz)
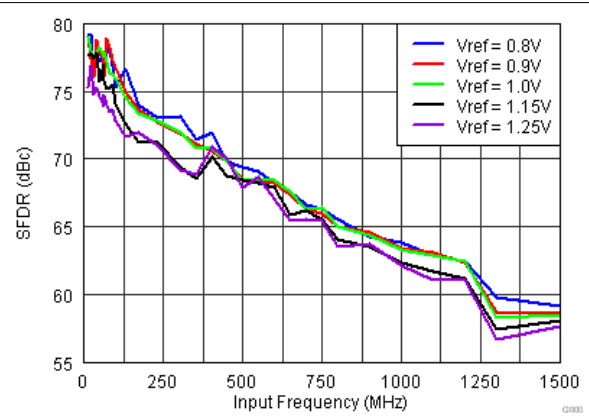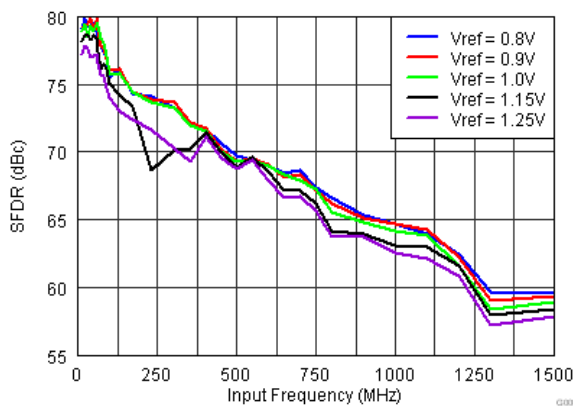
Figure 7-15. SFDR vs. Vref (Auto On)

Figure 7-16. SFDR vs. Vref (Auto Off)
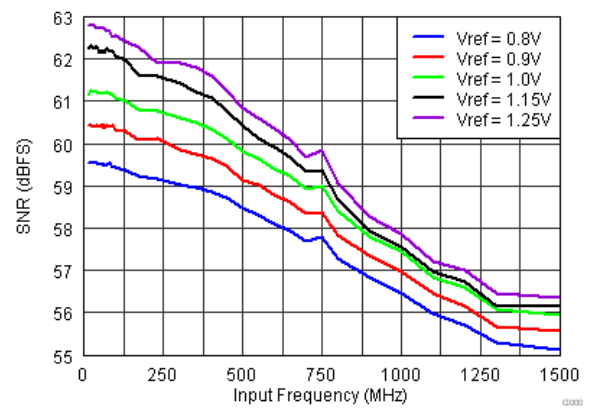
Figure 7-17. SNR vs. Vref (Auto On)
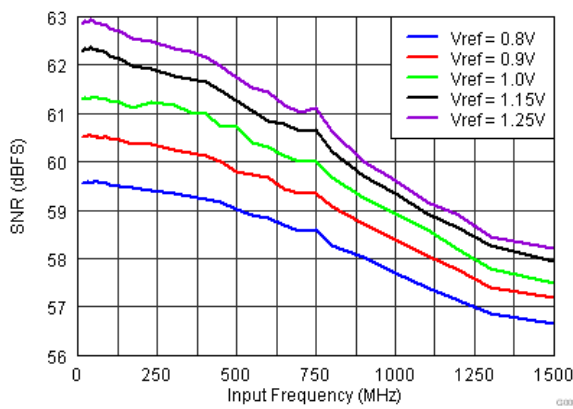
Figure 7-18. SNR vs. Vref (Auto Off)
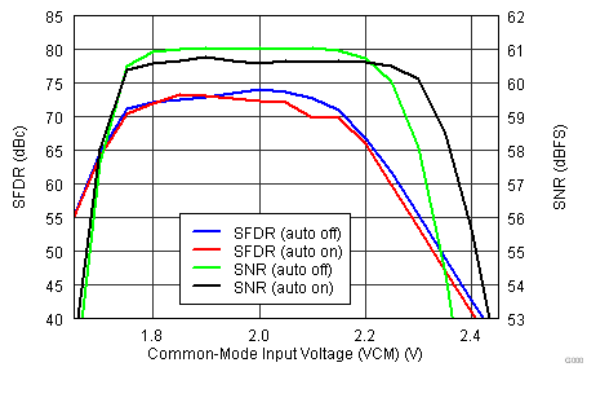
Figure 7-19. Performance Across Input Common-Mode Voltage

Product Folder Links: *ADS54T01*

## 7.10 Typical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input, unless otherwise noted.
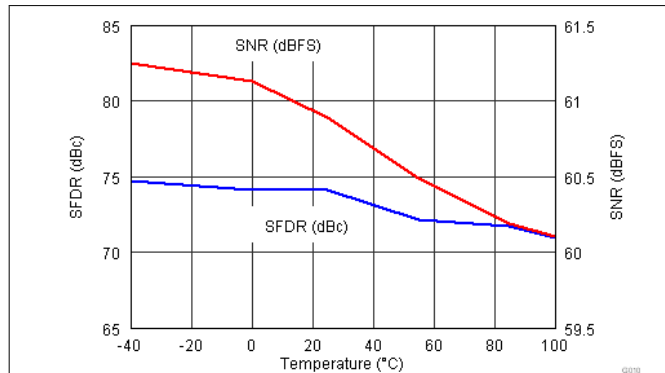
**Figure 7-20. Performance Across Temperature (fin = 230 MHz)**
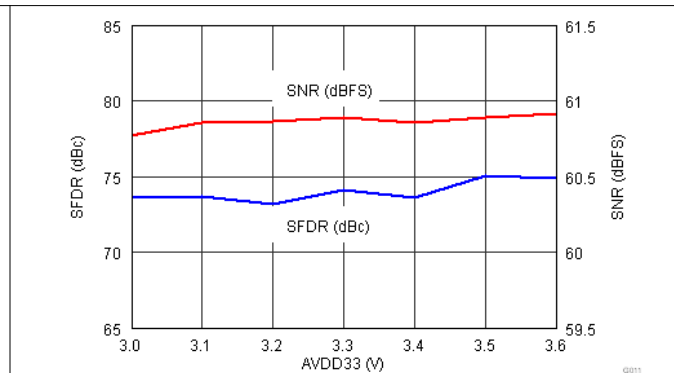
**Figure 7-21. Performance Across AVDD33 (fin = 230 MHz)**
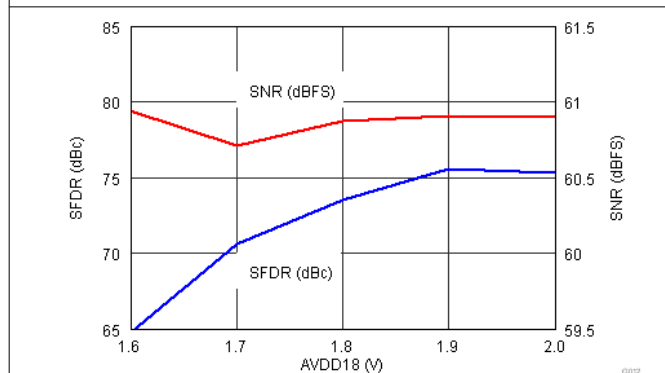
**Figure 7-22. Performance Across AVDD18 (fin = 230 MHz)**
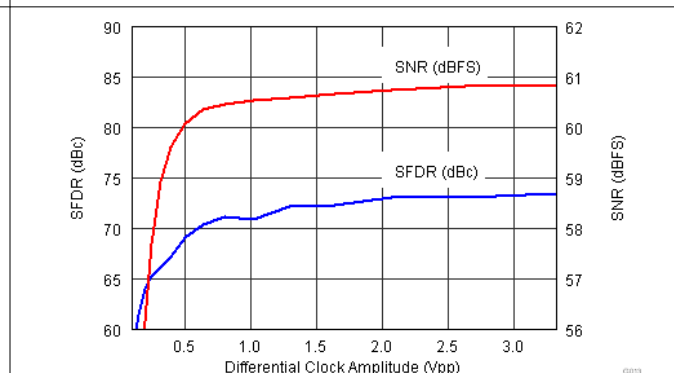
**Figure 7-23. Performance Across Clock Amplitude**
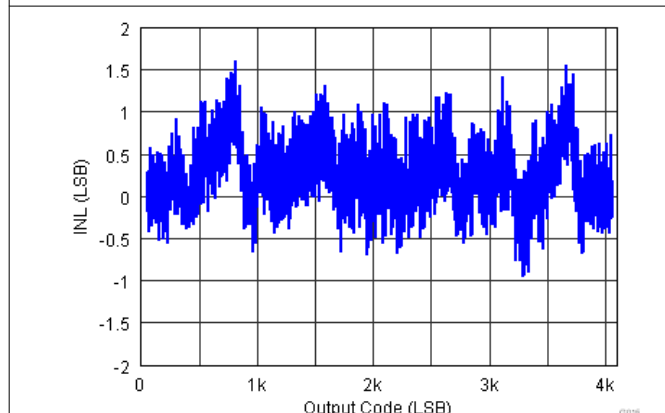
**Figure 7-24. INL**
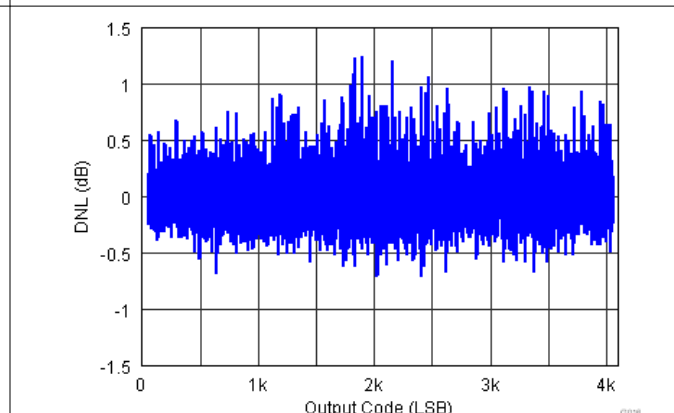
**Figure 7-25. DNL**

Product Folder Links: *ADS54T01*

## 7.10 Typical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input, unless otherwise noted.
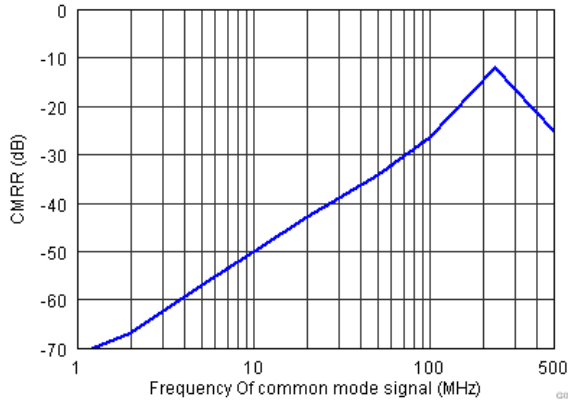


**Figure 7-26. CMRR Across Frequency**
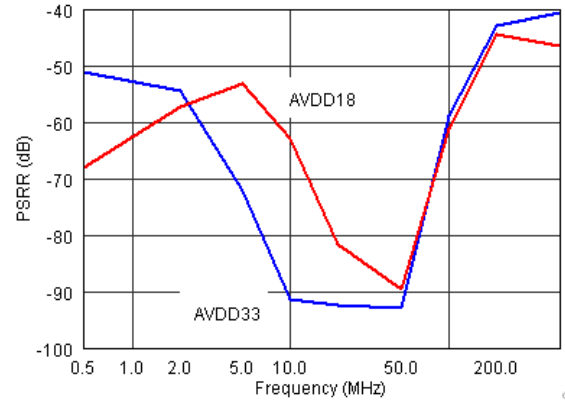


**Figure 7-27. PSRR Across Frequency**
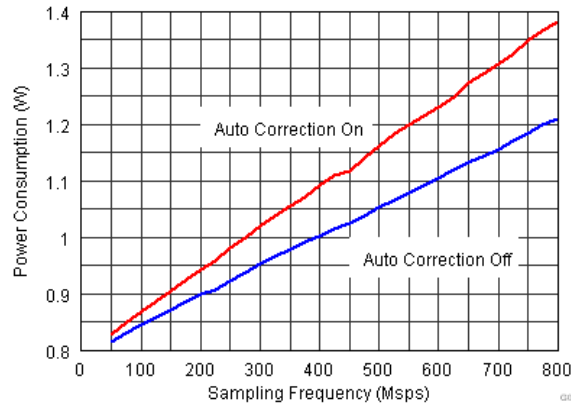


**Figure 7-28. Power Across Sampling Frequency**

Product Folder Links: *ADS54T01*

## 7.10 Typical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input, unless otherwise noted.
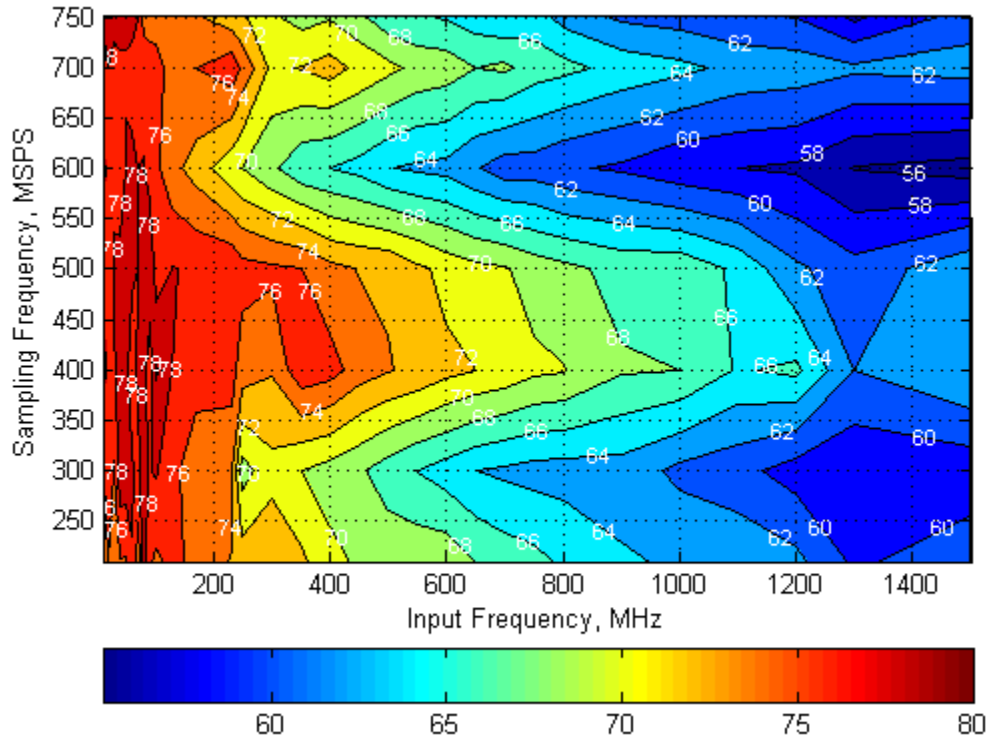
**Figure 7-29. SFDR Across Input and Sampling Frequencies (Auto On)**

## 7.10 Typical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input, unless otherwise noted.
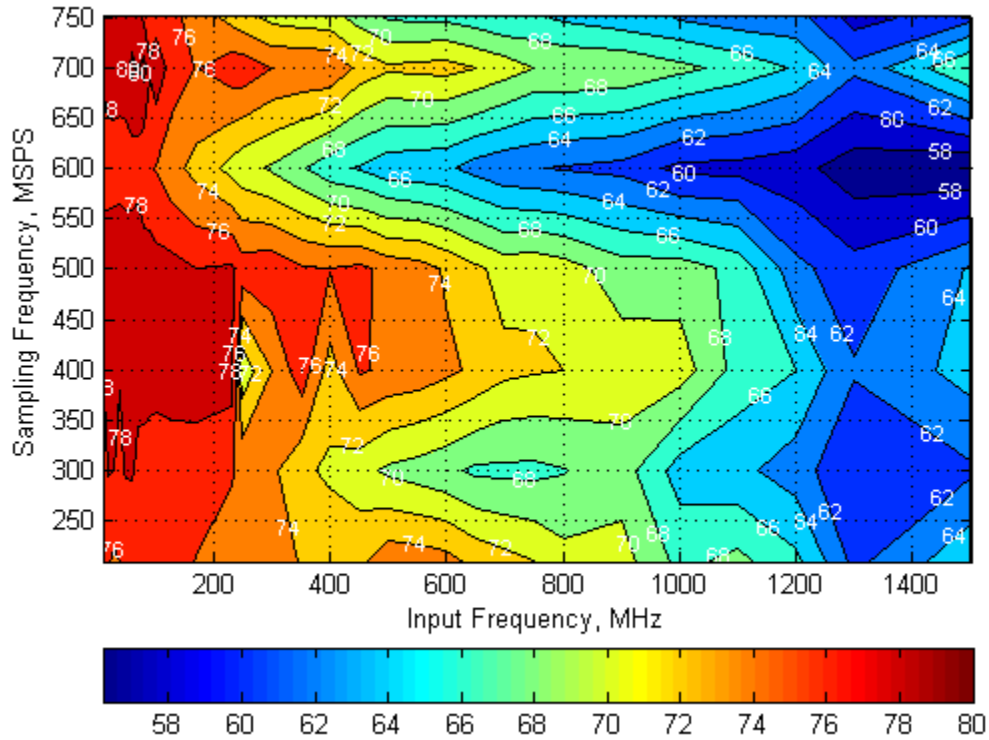


**Figure 7-30. SFDR Across Input and Sampling Frequencies (Auto Off)**

Product Folder Links: ADS54T01

## 7.10 Typical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input, unless otherwise noted.
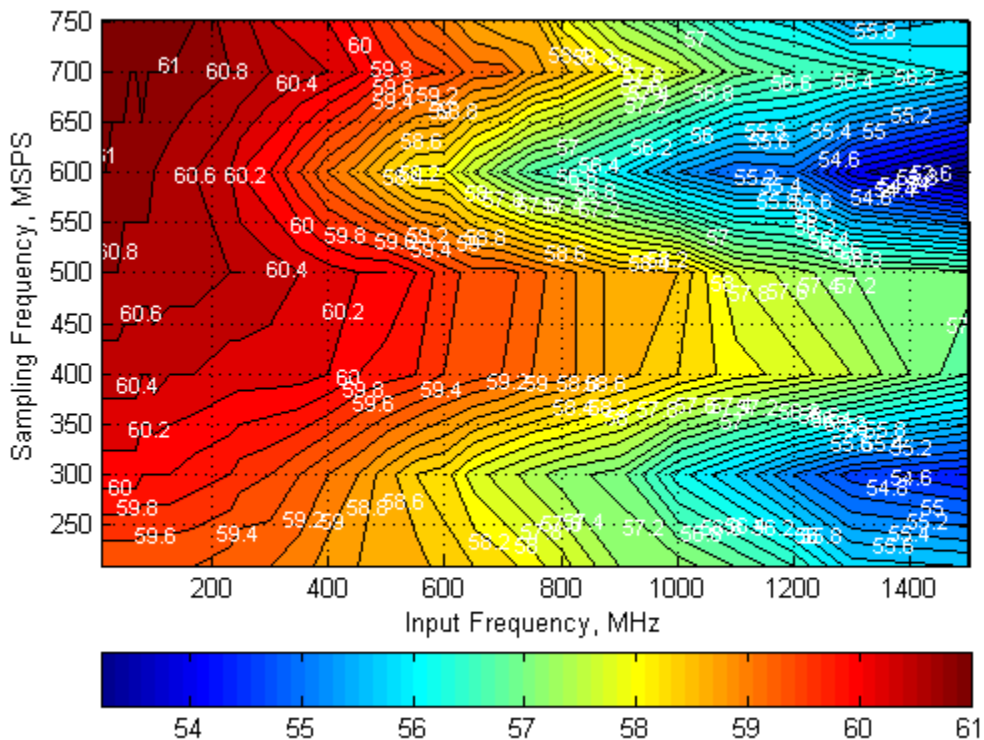


**Figure 7-31. SNR Across Input and Sampling Frequencies (Auto On)**

## 7.10 Typical Characteristics (continued)

Typical values at $T_A$ = +25°C, full temperature range is $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, ADC sampling rate = 750 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1-dBFS differential input, unless otherwise noted.
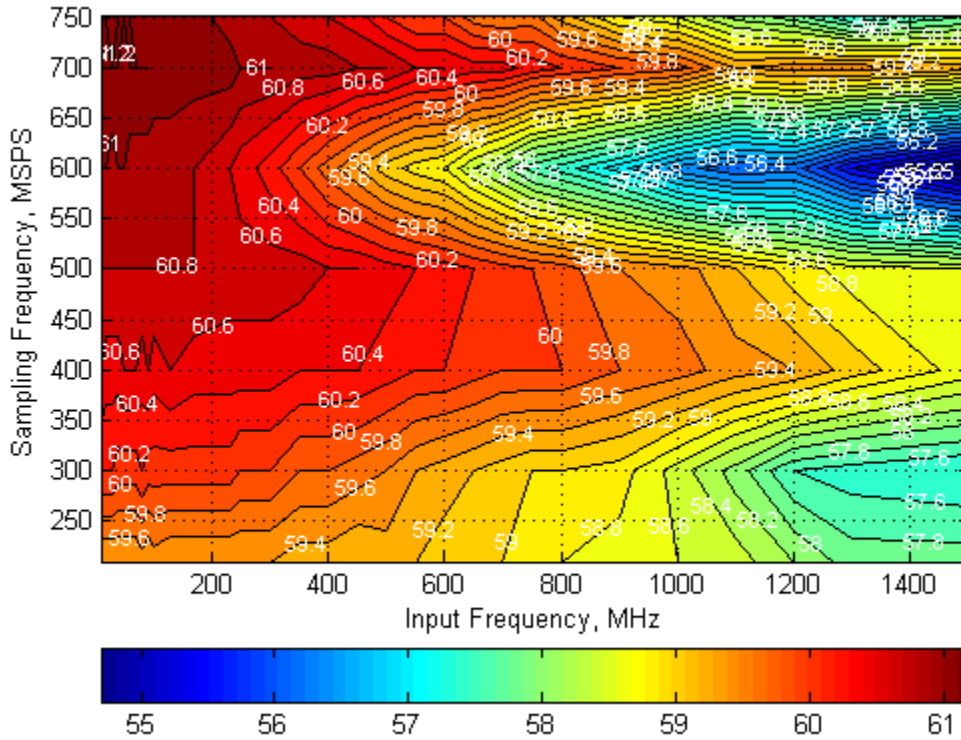


**Figure 7-32. SNR Across Input and Sampling Frequencies (Auto On)**

Product Folder Links: *ADS54T01*

# 8 Detailed Description

## 8.1 Overview

The ADS54T01 is a 12-bit, single channel ADC that operates at sampling rates of up to 750 Msps. This device has excellent SFDR over a large input frequency range and low noise performance. The ADC accepts differential signals for the clock input and analog input buffers. The analog input buffer provides an isolated signal from the source with a high-impedance input.

## 8.2 Functional Block Diagram
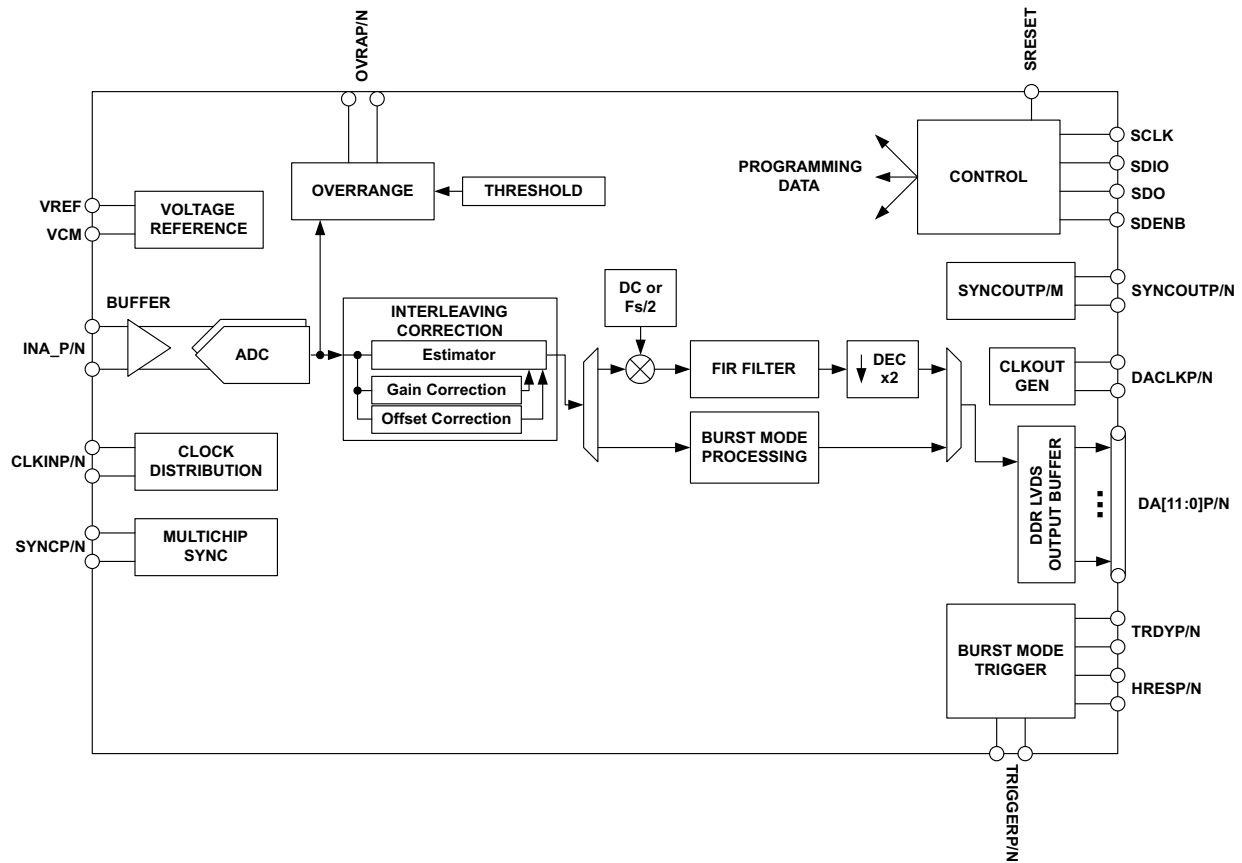


**Figure 8-1. Functional Block Diagram**

## 8.3 Feature Description

### 8.3.1 Test Pattern Output

The ADS54T01 can be configured to output different test patterns that can be used to verify the digital interface is connected and working properly.

To enable the test pattern mode, the high-performance mode 1 has to be disabled first through the SPI register write. Then different test patterns can be selected by configuring registers x3C, x3D, and x3E. All three registers must be configured for the test pattern to work properly.

First set HP1 = 0 (Addr 0x01, D01)

Internally the test pattern replaces the sampled data from the ADC. However at the LVDS outputs the output data is still subject to burst mode operation. In low-resolution output, the LSBs of the test pattern are replaced with 0 s.
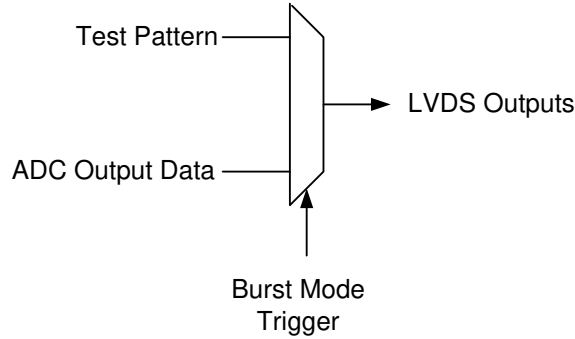
**Figure 8-2. Test Pattern Selection**

**Table 8-1. Test Pattern Register Setting**

| Register Address | All 0s | All 1s | Toggle (0xAAA => 0x555) | Toggle (0xFFF => 0x000) |
|---|---|---|---|---|
| 0x3C | 0x8000 | 0xBFFC | 0x9554 | 0xBFFC |
| 0x3D | 0x0000 | 0x3FFC | 0x2AA8 | 0x0000 |
| 0x3E | 0x0000 | 0x3FFC | 0x1554 | 0x3FFC |

**Table 8-2. Custom Pattern Register Setting**

| Register Address | Custom Pattern | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| x3C | 1 | 0 | | | | | | | | | | | | | 0 | 0 |
| x3D | 0 | 0 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 0 | 0 |
| x3E | 0 | 0 | | | | | | | | | | | | | 0 | 0 |

For normal operation, set HP1 = 1 (Addr 0x01, D01) and 0x3C, 0x3D, and 0x3E all to 0.

### 8.3.2 Clock Inputs

The ADS54T01 clock input can be driven differentially with a sine wave, LVPECL, or LVDS source with little or no difference in performance. The common-mode voltage of the clock input is set to 0.9 V using internal 2-kΩ resistors. This allows for AC coupling of the clock inputs. The termination resistors should be placed as close to the clock inputs as possible to minimize signal reflections and jitter degradation.



Recommended differential clock driving circuit
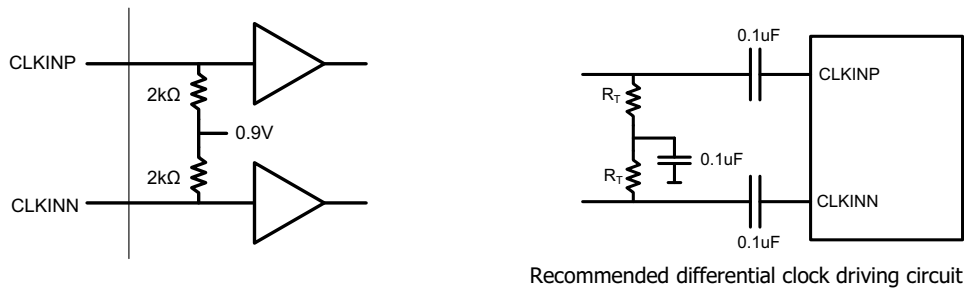
**Figure 8-3. Recommended Differential Clock Driving Circuit**

### 8.3.3 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors: the quantization noise is typically not noticeable in pipeline converters and is 72 dB for a 12-bit ADC. The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies.

Product Folder Links: ADS54T01

$$SNR_{ADC}[dBc] = -20 \times log \sqrt{\left(10 - \frac{SNR_{Quantization\_Noise}}{20}\right)^2 + \left(10 - \frac{SNR_{ThermalNoise}}{20}\right)^2 + \left(10 - \frac{SNR_{Jitter}}{20}\right)^2}$$ (1)

Use Equation 2 to calculate the SNR limitation due to sample clock jitter.

$$SNR_{Jitter}[dBc] = -20 \times log(2\pi \times f_{IN} \times t_{Jitter})$$ (2)

The total clock jitter ($t_{Jitter}$) has three components: the internal aperture jitter (100 fs for ADS54T01) which is set by the noise of the clock input buffer, the external clock jitter, and the jitter from the analog input signal. Use Equation 3 to calculate the total clock jitter.

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2}$$ (3)

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as bandpass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter.

The ADS54T01 has a thermal noise of 61.2 dBFS and internal aperture jitter of 100 fs. Figure 8-4 shows the SNR depending on amount of external jitter for different input frequencies.
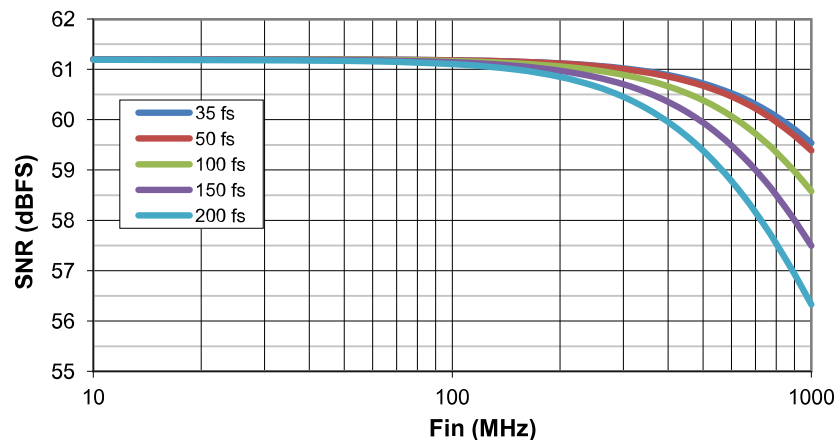


**Figure 8-4. SNR vs. Frequency and External Clock Jitter**

### 8.3.4 Analog Inputs

The ADS54T01 analog signal input is designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source which enables great flexibility in the external analog filter design as well as excellent 50 Ω matching for RF applications. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit which results in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to 1.9 V using 500-Ω resistors which allows for AC coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.25 V) and (VCM – 0.25 V), resulting in a 1.0 Vpp (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 1.2 GHz.
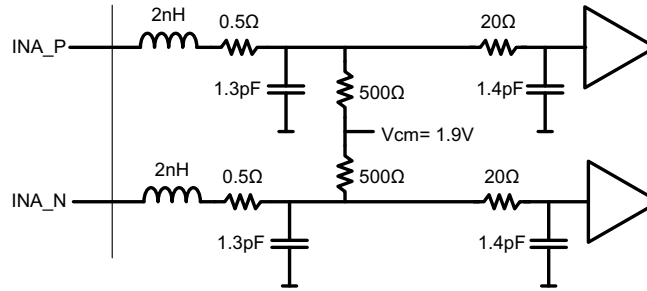
**Figure 8-5. Analog Input Internal Circuitry**

### 8.3.5 Over-Range Indication

The ADS54T01 provides a fast over-range indication on the OVRA/B pins. The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and it gets presented after just 12 clock cycles enabling a quicker reaction to an overrange event. The OVR threshold can be configured using SPI register writes.

The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the over-range threshold bits. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESH bits] /16). After reset, the default value of the over-range threshold is set to 15 (decimal) which corresponds to a threshold of 0.56 dB below full scale (20 × log(15/16)).
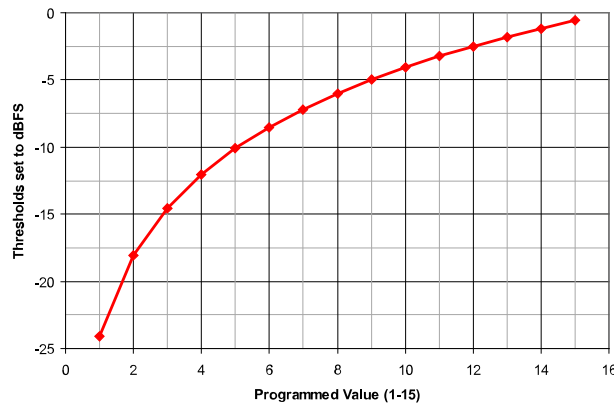


**Figure 8-6. OVR Detection Threshold**

### 8.3.6 Interleaving Correction

The data converter channel consists of two interleaved ADCs each operating at half of the ADC sampling rate but 180° out of phase from each other. The front end track and hold circuitry is operating at the full ADC sampling rate which minimizes the timing mismatch between the two interleaved ADCs. In addition, the ADS54T01 is equipped with internal interleaving correction logic that can be enabled through a SPI register write.
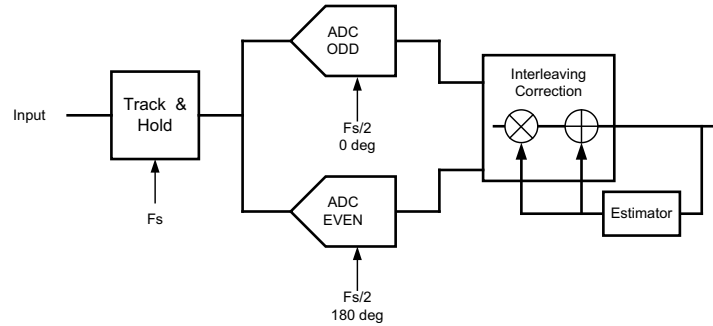


**Figure 8-7. Interleaving Correction Block Diagram**

The interleaving operation creates 2 distinct and interleaving products:

- Fs/2 – Fin: this spur is created by gain timing mismatch between the ADCs. Since internally the front end track and hold is operated at the full sampling rate, this component is greatly improved and mostly dependent on gain mismatch.
- Fs/2 Spur: due to offset mismatch between ADCs
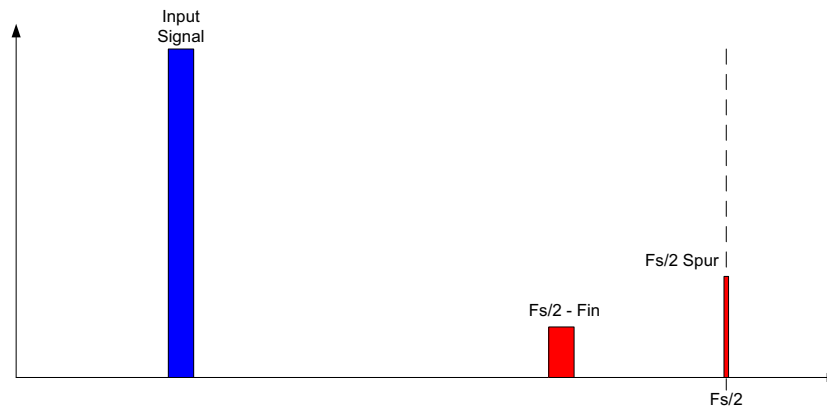


**Figure 8-8. Interleaving Correction Spurs**

The auto correction loop can be enabled through a SPI register write in address 0x01. By default, the auto correction function is disabled for lowest possible power consumption. The default settings for the auto correction function should work for most applications. However please contact Texas Instruments if further fine tuning of the algorithm is required.

The auto correction function yields best performance for input frequencies below 250 MHz.

### 8.3.7 High-Resolution Output Data

After trigger, the data outputs DA[11..0] are 12-bit resolution for $2^N$ samples, where N is a programmable register with a range $10 \le N \le 25$ (corresponding to 1024 to 33554432 samples).
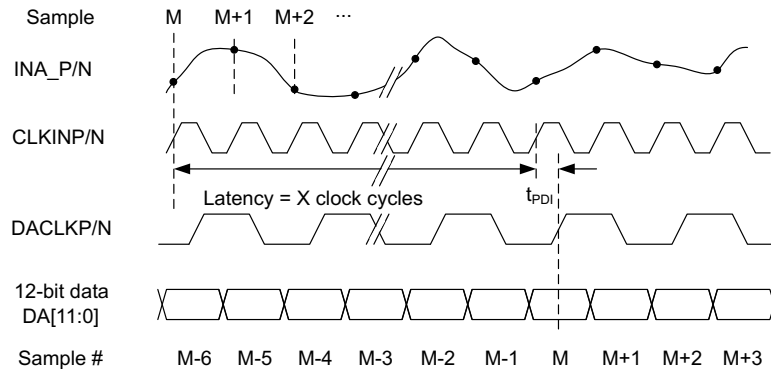
**Figure 8-9. High-Resolution Data Output Timing**

After the high-resolution data, the data output returns to low-resolution mode, the logic level of the HRES flag returns low and the trigger is locked out for $2^{(N+3)}$ samples. N is the sample integer resulting in a maximum output duty cycle of 1/9. During the trigger lockout time, a low to high transition on TRIGGERP/N will be ignored. After the $2^{N+3}$ low-resolution samples, the TRIGGERP/N is re-enabled for the next valid data burst.

### 8.3.8 Low-Resolution Output Data

There are two different options for the low-resolution output data and the selection is made through SPI register control. The data can either be output at full speed (ADC sampling rate) with the output resolution limited to 7 bit (7 MSBs). Alternatively the output resolution can be selected to 11 bit (11 MSBs) but at a reduced effective data rate where every 4$^{th}$ sample gets repeated four times.

### 8.3.9 Full Speed – 7 Bit

The output data rate and timing is exactly the same as the high-resolution data, only the output resolution is limited to the 7 MSBs.
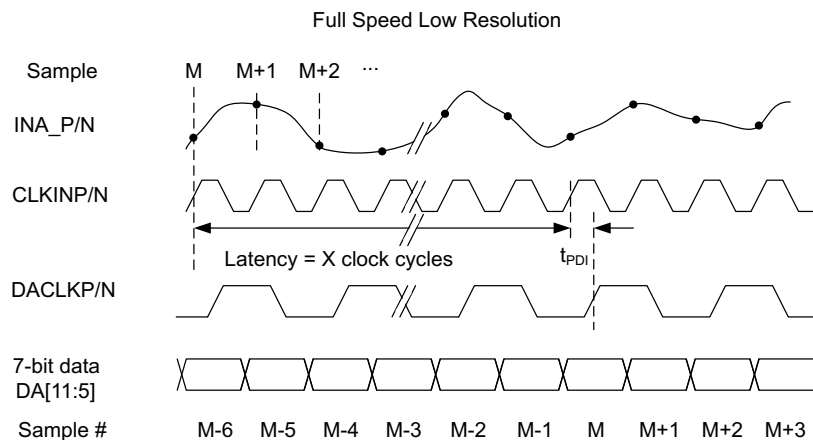


**Figure 8-10. Full-Rate, Low-Resolution Output Data Timing**

### 8.3.10 Decimated Low-Resolution Output Data

In decimated low-resolution mode, the output data is limited to 11 bits and every sample is repeated four times, so the effective data rate is 1/4 of ADC sampling rate. The latency of the ADC sample to output sample is exactly the same as for high-resolution data—there is no uncertainty in which conversion sample results in the valid output data. This is because the output continues to run at the ADC sample rate in decimated low-resolution mode where only the resolution is changed and three out of four samples are deleted.

Product Folder Links: ADS54T01
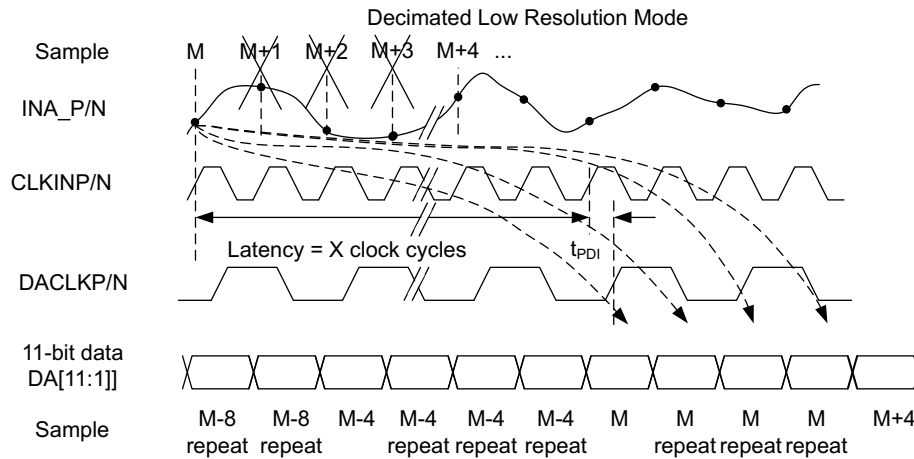
**Figure 8-11. Decimated Low-Resolution Output Data Timing Diagram**

### 8.3.11 Multi Device Synchronization

The ADS54T01 simplifies the synchronization of data from multiple ADCs in one common receiver. Upon receiving the initial SYNC input signal, the ADS54T01 resets all the internal clocks and digital logic while also starting a SYNCOUT signal which operates on a 5-bit counter (32 clock cycles). Therefore, by providing a common SYNC signal to multiple ADCs, their output data can be synchronized as the SYNCOUT signal marks a specific sample with the same latency in all ADCs. The SYNCOUT signal then can be used in the receiving device to synchronize the FIFO pointers across the different input data streams. Thus the output data of multiple ADCs can be aligned properly even if there are different trace lengths between the different ADCs.
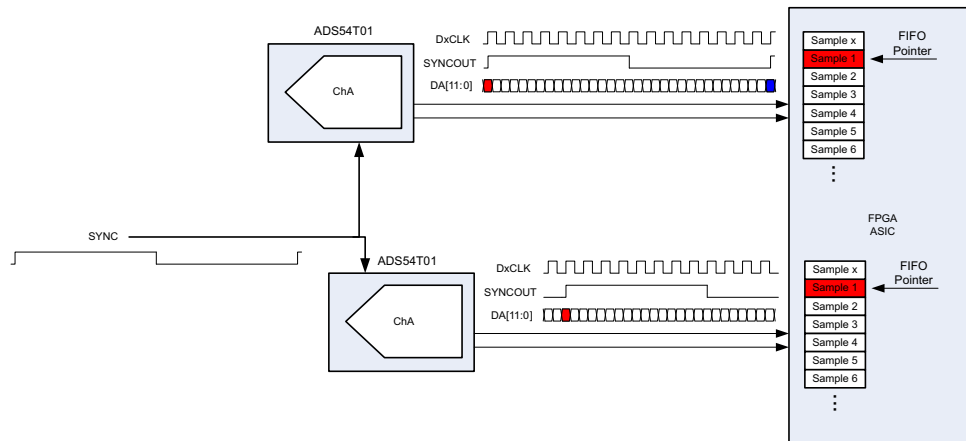


**Figure 8-12. Multi Device SYNC**

The SYNC input signal should be a one-time pulse to trigger the periodic 5-bit counter for SYNCOUT or a periodic signal repeating every 32 CLKIN clock cycles. The signal is registered on the rising edge of the ADC input clock (CLKIN). Upon registering the initial rising edge of the SYNC signal, the internal clocks and logic get reset which results in invalid output data for 36 samples (1 complete sync cycle and 4 additional samples). The SYNCOUT signal starts with the next output clock (DACLK) rising edge and operates on a 5-bit counter. If a SYNCIN rising edge gets registered at a new position, the counter gets reset and SYNCOUT starts from the new position.

The ADS54T01 output interface operates with a DDR clock, therefore the synchronization can happen on the rising edge or falling edge sample. Synchronization on the falling edge sample will result in a half cycle clock stretch of DACLK. For convenience, the SYNCOUT signal is available on the ChA output LVDS bus.

When using decimation, the SYNCOUT signal still operates on 32 clock cycles of CLKIN, but because the output data is decimated by 2, only the first 18 samples should be discarded.

Product Folder Links: *ADS54T01*
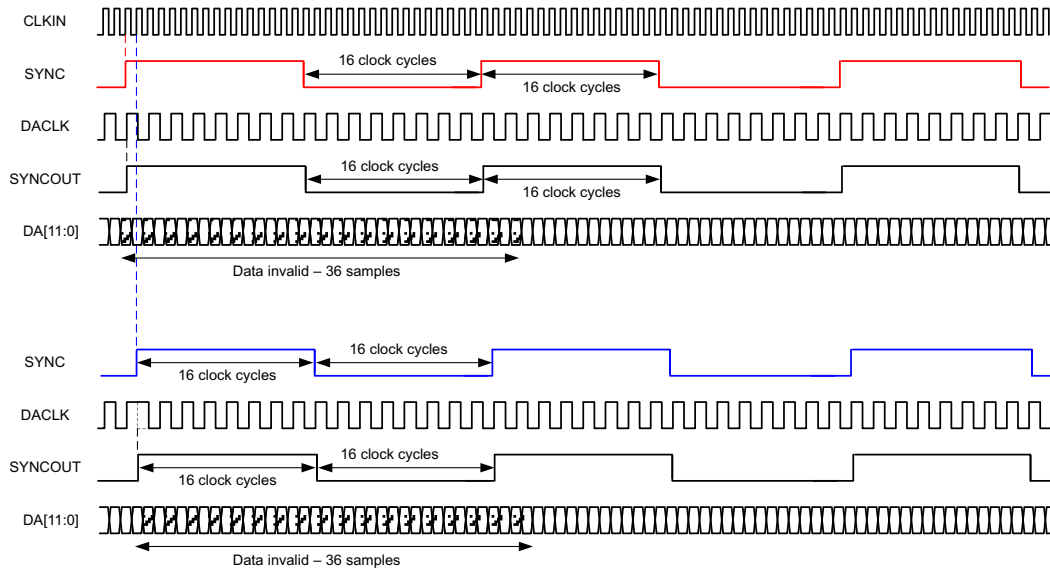
**Figure 8-13. SYNC Timing Diagram**

## 8.4 Device Functional Modes

### 8.4.1 Power-Down Modes

The ADS54T01 can be configured through a SPI write (address x37) to a standby, light, or deep sleep power mode which is controlled by the ENABLE pin. The sleep modes are active when the ENABLE pin goes low. Different internal functions stay powered up which results in different power consumption and wake up time between the two sleep modes.

**Table 8-3. Sleep Mode Power Consumption**

| Sleep Mode | Wake-Up Time | Power Consumption With Auto Correction Disabled | Power Consumption With Auto Correction Enabled |
|---|---|---|---|
| Complete Shutdown | 2.5 ms | 7 mW | 7 mW |
| Standby | 100 µs | 7 mW | 7 mW |
| Deep Sleep | 20 µs | 350 mW | 475 mW |
| Light Sleep | 2 µs | 655 mW | 780 mW |

### 8.4.2 Feedback Mode: Burst Mode

In burst mode, the output data is alternated between a high-resolution, 12-bit output of $2^N$ samples and a low-resolution, 7-bit or 11-bit output of $2^{N+3}$ samples. Burst mode is enabled through a SPI register write and there are two basic operating modes available: a manual trigger mode where the high-resolution output is initiated through an external trigger and an auto-trigger mode where the internal logic transitions to a high-resolution output immediately after transmitting the last low-resolution sample. After burst mode is enabled through a SPI register write, the ADS54T01 transmits $2^{13}$ low-resolution samples and the trigger command is locked out until completion.

The parameter N can be changed through the SPI at any time. The change will go into effect with the next output cycle, starting with the transmission of low-resolution samples. The default value for N after reset is N=10.

**Table 8-4. Burst Mode Samples Per Cycle**

| N limit | 10 (minimum) | 25 (maximum) |
|---|---|---|
| Number of low resolution samples per cycle ($2^{N+3}$) | 8,192 | 268,435,456 |
| Number of high resolution samples per cycle ($2^N$) | 1,024 | 33,554,432 |
| Total amount of samples per cycle | 9,216 | 301,989,888 |

**Table 8-4. Burst Mode Samples Per Cycle (continued)**

| N limit | 10 (minimum) | 25 (maximum) |
|---|---|---|
| Maximum number of high resolution (12-bit) samples per 1 second | 83.3M | 83.3M |

### 8.4.3 Receive Mode: Decimation Filter

Figure 8-14 shows that each channel has a digital filter in the data path.
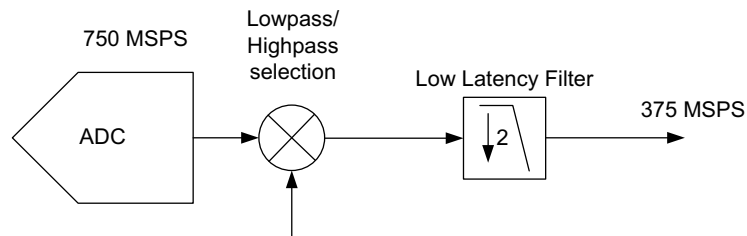


**Figure 8-14. Decimation Filter Block Diagram**

The filter can be programmed as a low-pass or a high-pass filter and the normalized frequency response of both filters. The decimation filter response has a 0.1-dB pass-band ripple with approximately 41% pass-band bandwidth. The stop-band attenuation is approximately 40 dB.
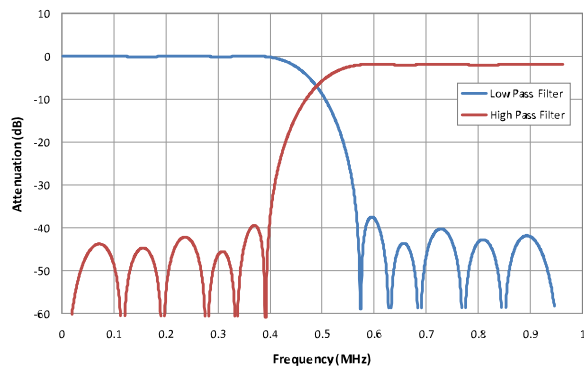


**Figure 8-15. Decimation Filter Response**
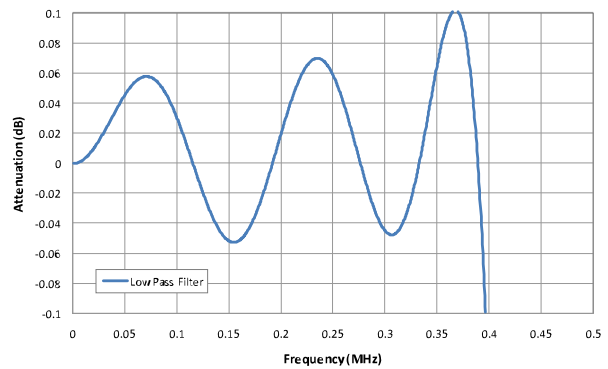


**Figure 8-16. Decimation Filter Response**

### 8.4.4 Manual Trigger Mode

The control of the high-resolution output is shown below along with the two output flags (TRDY and HRES).

Product Folder Links: *ADS54T01*
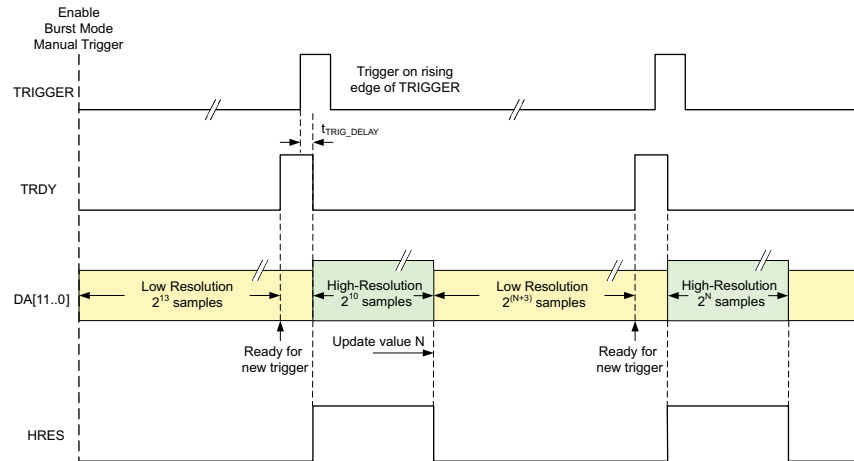
**Figure 8-17. Triggering High Resolution Mode and Lockout Time**

After enabling burst mode, the output data DA[11..0] are forced to low-resolution mode for $2^{13}$ samples. During that period, any trigger signal is ignored. The completion of the low-resolution sample cycle is signaled by a logic high on the TRDY output pins indicating that a high-resolution (12-bit) data output burst can be triggered by a low-to-high transition on the TRIGGER input. The ADC monitors the TRIGGER input at each rising edge of the input clock.

The high-resolution output data starts with a delay of $t_{TRIG\_DELAY}$ = 1-2 DACLK clock cycles and is indicated through the HRES data flag which stays high for all $2^N$ high-resolution samples. At completion the register value for N is verified and transmission of $2^{(N+3)}$ low-resolution data immediately follows. When the last low-resolution sample is output on the output data bus, the flag TRDY is asserted high again indicating the end of the lockout period and the next $2^N$ high-resolution samples can be triggered again.

### 8.4.5 Auto Trigger Mode

This mode is enabled by setting the auto trigger bit through a SPI register write and the DA data outputs start in low resolution for $2^{13}$ samples. Immediately following completion of transmission of the last low resolution sample, the outputs automatically start transmitting $2^{10}$ high-resolution samples without the need for external trigger ensuring maximum efficiency. Any input signal on the TRIGGER pins is ignored and the TRDY flag will go high only for one clock cycle with the start of the high-resolution data.

The output flag HRES is aligned with the $2^N$ high-resolution output samples and the parameter N can be changed until the next output cycle starts again with low-resolution output data.
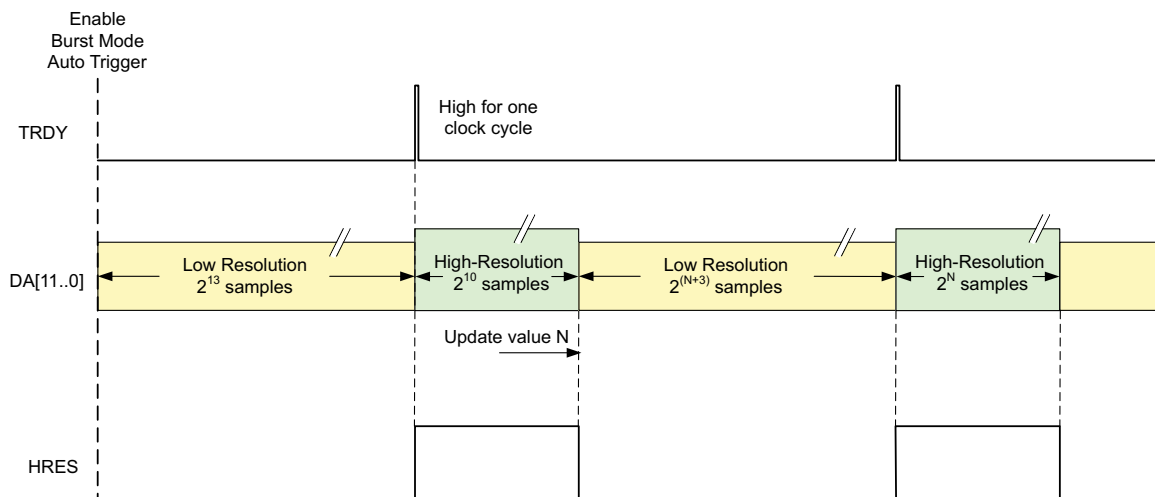


**Figure 8-18. Auto Trigger Mode Timing Diagram**

Product Folder Links: ADS54T01

## 8.5 Programming

The serial interface (SIF) included in the ADS54T01 is a simple 3 or 4 pin interface. In normal mode, 3 pins are used to communicate with the device. There is an enable (SDENB), a clock (SCLK) and a bidirectional IO port (SDIO). If the user would like to use the 4-pin interface one write must be implemented in the 3-pin mode to enable 4-pin communications. In this mode, the SDO pin becomes the dedicated output. The serial interface has an 8-bit address word and a 16-bit data word. The first rising edge of SCLK after SDENB goes low will latch the read/write bit. If a high is registered, then a read is requested. If it is low, then a write is requested. SDENB must be brought high again before another transfer can be requested. The signal diagram is shown below:

### 8.5.1 Device Initialization

After power up, TI recommends to initialize the device through a hardware reset by applying a logic low pulse on the SRESETb pin (of width greater than 20 ns), as shown in Figure 8-19. This resets all internal digital blocks (including SPI registers) to their default condition.
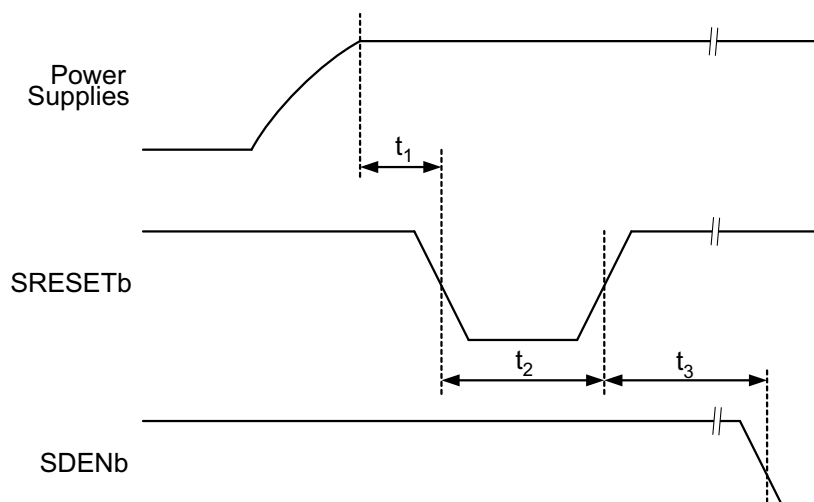


**Figure 8-19. Device Initialization Timing Diagram**

**Table 8-5. Reset Timing**

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_1$ | Power-on delay | Delay from power up to active low RESET pulse | 3 | | | ms |
| $t_2$ | Reset pulse width | Active low RESET pulse width | 20 | | | ns |
| $t_3$ | Register write delay | Delay from RESET disable to SDENb active | 100 | | | ns |

Recommended Device Initialization Sequence:

1. Power up
2. Reset ADS54T01 using hardware reset.
3. Apply clock and input signal.
4. Set register 0x01 bit D15 to "1" (ChA Corr EN) to enable gain/offset correction circuit and other desired registers.
5. Set register 0x03 bit D14 to "1" (Start Auto Corr ChA). This clears and resets the accumulator values in the DC and gain correction loop.
6. Set register 0x03 bit D14 to "0" (Start Auto Corr ChA). This starts the DC and gain auto-correction loop.

### 8.5.2 Serial Register Write

The internal register of the ADS54T01 can be programmed following these steps:

1. Drive SDENB pin low
2. Set the R/W bit to "0" (bit A7 of the 8-bit address)

3. Initiate a serial interface cycle specifying the address of the register (A6 to A0) whose content has to be written
4. Write 16-bit data which is latched on the rising edge of SCLK
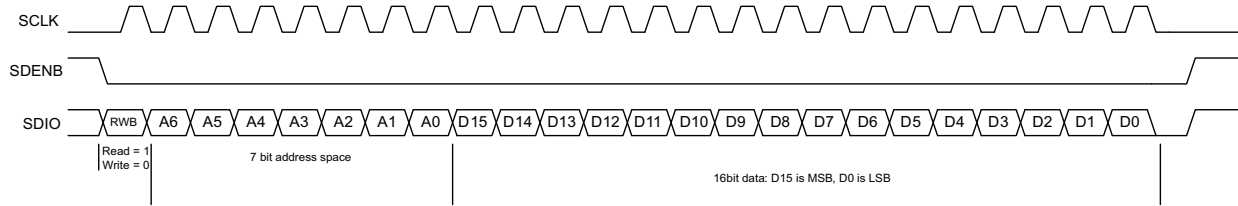


**Figure 8-20. Serial Register Write Timing Diagram**

**Table 8-6. Timing Requirements**

| PARAMETER | | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|
| f$_{SCLK}$ | SCLK frequency (equal to 1/t$_{SCLK}$) | >DC | | 20 | MHz |
| t$_{SLOADS}$ | SDENB to SCLK setup time | 25 | | | ns |
| t$_{SLOADH}$ | SCLK to SDENB hold time | 25 | | | ns |
| t$_{DSU}$ | SDIO setup time | 25 | | | ns |
| t$_{DH}$ | SDIO hold time | 25 | | | ns |

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: TMIN = –40°C to TMAX = +85°C, AVDD3V = 3.3 V, AVDD, DRVDD = 1.9 V, unless otherwise noted.

### 8.5.3 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDO/SDIO pins. This read-back mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Drive SDENB pin low
2. Set the RW bit (A7) to "1". This setting disables any further writes to the registers
3. Initiate a serial interface cycle specifying the address of the register (A6 to A0) whose content has to be read.
4. The device outputs the contents (D15 to D0) of the selected register on the SDO/SDIO pin
5. The external controller can latch the contents at the SCLK rising edge.
6. To enable register writes, reset the RW register bit to "0".
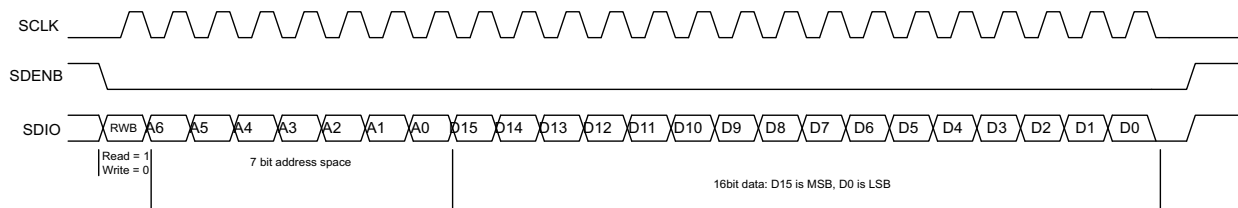


**Figure 8-21. Serial Register Read Timing Diagram**

Product Folder Links: *ADS54T01*

## 8.6 Register Maps

### 8.6.1 Serial Register Map

**Table 8-7. Serial Registers**

| A7–A0 IN HEX | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 3/4 Wire SPI | DecFil/Burst | 0 | High/Low Pass | 0 | 0 | 0 | 0 | 0 | 0 | Burst rate | 0 | 0 | Auto Trigger | 0 | 0 |
| 1 | Corr EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Data Format | 0 | Hp Mode1 | 0 |
| 2 | 0 | 1 | 1 | 0 | 0 | Over-range threshold | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 0 | DC Offset Corr | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| E | Sync Select | | | | | | | | | | | | | | 0 | 0 |
| F | Sync Select | | | | 0 | 0 | 0 | 0 | 0 | VREF Set | | | 0 | 0 | 0 | 0 |
| 1A | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 2B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Temp Sensor | | | | | | | | |
| 2C | Reset | | | | | | | | | | | | | | | |
| 34 | 0 | 0 | Burst Mode N | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 37 | Sleep Modes | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 38 | HP Mode2 | | | | | | | LP Mode | TEMP EN | BIAS EN | SYNC EN | TRIGEN | 1 | 1 | 1 | 1 |
| 3A | LVDS Current Strength | | | LVDS SW | | Internal LVDS Termination | | 0 | 0 | 0 | 0 | DACLK EN | DBCLK EN | 0 | OVRA EN | OVRB EN |
| 66 | LVDS Output Bus A EN | | | | | | | | | | | | | | | |

Register Data[1]

(1) Multiple functions in a register can be programmed in a single write operation.

### 8.6.2 Description of Serial Interface Registers

| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 3/4 Wire SPI | Dec Fil/ Burst | 0 | High/ Low Pass | 0 | 0 | 0 | 0 | 0 | 0 | Burst rate | 0 | 0 | Auto Trigger | 0 | 0 |

Register Data

| D15 | **3/4 Wire SPI** Default 0 | Enables 4-bit serial interface when set |
|---|---|---|
| 0 | 3-wire SPI is used with SDIO pin operating as bidirectional I/O port | |
| 1 | 4-wire SPI is used with SDIO pin operating as data input and SDO pin as data output port. | |

| D14 | **DecFil/ Burst** Default 0 | 2x decimation filter (Receive Mode) is enabled when bit is set |
|---|---|---|
| 0 | Burst mode enable | |
| 1 | 2x decimation filter enabled | |

| D12 | **High/Low Pass** Default 0 | (Decimation filter must be enabled first: set bit D14) |
|---|---|---|
| 0 | Low Pass | |
| 1 | High Pass | |

| D5 | **Burst Rate** Default 0 | Low resolution output data rate in burst mode |
|---|---|---|
| 0 | Low resolution (9-bit) full output rate | |
| 1 | Decimated low resolution output (4x decimation, 11-bit resolution) | |

| D2 | **Auto Trigger** Default 0 | Enables auto trigger mode in burst mode without the need to control the trigger pin. |
|---|---|---|
| 0 | Manual trigger mode using the external trigger input pin | |
| 1 | Auto trigger mode enabled | |

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | Corr EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Data Format | 0 | HP Mode1 | 0 |

| | | |
|---|---|---|
| D15 | **Corr EN (should be enabled for maximum performance)** | |
| | Default 0 | |
| 0 | auto gain correction disabled | |
| 1 | auto gain correction enabled | |
| D3 | **Data Format** | |
| | Default 0 | |
| 0 | Two's complement | |
| 1 | Offset Binary | |
| D1 | **HP Mode 1** | |
| | Default 0 | |
| 1 | Must be set to 1 for optimum performance | |

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 2 | 0 | 1 | 1 | 0 | 0 | Over-range threshold | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| D14 | Read back 1. | |
| D13 | Read back 1. | |
| D10-D7 | **Over-range threshold** | The over-range detection is triggered 12 output clock cycles after the overload condition occurs. The threshold at which the OVR is triggered = 1.0V x [decimal value of <Over-range threshold>]/16. After power up or reset, the default value is 15 (decimal) which corresponds to a OVR threshold of 0.56dB below fullscale (20*log(15/16)). This OVR threshold is applicable to both channels. |
| | Default 1111 | |
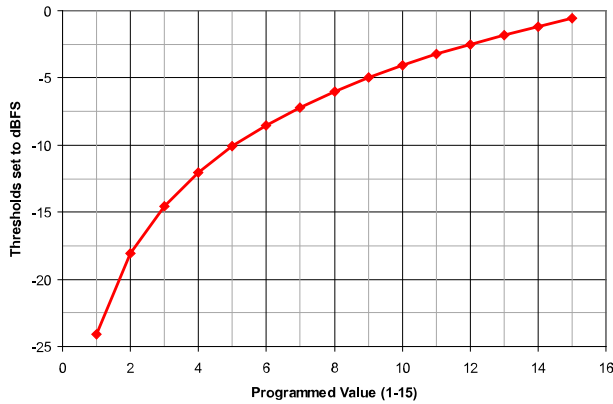


**Figure 8-22. Over-range Threshold vs. Programmed Value**

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 3 | 0 | DC Offset Coff | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

| | | |
|---|---|---|
| D14 | **DC Offset Corr** | Starts DC offset correction loop |
| | Default 1 | |
| 0 | Starts offset correction loop | |
| 1 | DC offset correction loop is cleared | |
| D11, 9, 8, 4, 3 | Must be set to 1 for maximum performance | |
| | Default 1 | |

Product Folder Links: *ADS54T01*

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| E | Sync Select | | | | | | | | | | | | | | 0 | 0 |

| | | |
|---|---|---|
| D15-D2 | **Sync Select**<br>Default 1010 1010 1010 10 | Sync selection for the clock generator block (also need to see address 0x0F) |
| 0000 0000 0000 00 | Sync is disabled | |
| 0101 0101 0101 01 | Sync is set to one shot (one time synchronization only) | |
| 1010 1010 1010 10 | Sync is derived from SYNC input pins | |
| 1111 1111 1111 11 | not supported | |

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| F | Sync Select | | | | 0 | 0 | 0 | 0 | 0 | VREF Sel | | | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| D15-D12 | **Sync Select**<br>Default 1010 1010 1010 10 | Sync selection for the clock generator block |
| 0000 | Sync is disabled | |
| 0101 | Sync is set to one shot (one time synchronization only) | |
| 1010 | Sync is derived from SYNC input pins | |
| 1111 | not supported | |
| D6-D4 | **VREF SEL**<br>Default 000 | Internal voltage reference selection |
| 000 | 1.0 V | |
| 001 | 1.25 V | |
| 010 | 0.9 V | |
| 011 | 0.8 V | |
| 100 | 1.15 V | |
| Others | external reference | |

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1A | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

| | |
|---|---|
| D14, 11, 9, 8, 4, 3 | Must be set to 1 for maximum performance<br>Default 1 |

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 2B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Temp Sensor | | | | | | | | |

| | | |
|---|---|---|
| D8-D0 | **Temp Sensor** | Internal temperature sensor value – read only |

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 2C | Reset | | | | | | | | | | | | | | | |

| | | |
|---|---|---|
| D15-D0 | **Reset**<br>Default 0000 | This is a software reset to reset all SPI registers to their default value. Self clears to 0. |
| 1101001011110000 | Perform software reset | |

Product Folder Links: *ADS54T01*

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 34 | 0 | 0 | Burst Mode N | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D13-D10 | **Burst Mode N**<br>Default 0000 | This is the parameter that sets the amount of high resolution samples in burst mode |
|---|---|---|
| 0000 | N = 10 | |
| 0001 | N = 11 | |
| ... | ... | |
| 1111 | N = 25 | |

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 37 | Sleep Modes | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D15-D14 | **Sleep Modes**<br>Default 00 | Sleep mode selection which is controlled by the ENABLE pin. Sleep modes are active when ENABLE pin goes low. | |
|---|---|---|---|
| 000000 | Complete shut down | Wake up time 2.5 ms | |
| 100000 | Standby mode | Wake up time 100 µs | |
| 110000 | Deep sleep mode | Wake up time 20 µs | |
| 110101 | Light sleep mode | Wake up time 2 µs | |

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 38 | HP Mode 2 | | | | | | | LP Mode | TEMP EN | FUSE Bias EN | SYNC EN | TRIG EN | 1 | 1 | 1 | 1 |

| D15-D9 | **HP Mode 2**<br>Default 111111111 | |
|---|---|---|
| 1 | Set to 1 for normal operation | |

| D8 | **LP Mode**<br>Default 1 | Low power mode |
|---|---|---|
| 0 | Set to 0 to turn off unused output buffers | |

| D7 | **TEMP EN**<br>Default 1 | Temperature sensor enable |
|---|---|---|
| 1 | Set to 1 to enable the temperature sensor | |

| D6 | **FUSE BIAS EN**<br>Default 1 | Enables internal bias voltages. Can be disabled after power up for power savings. |
|---|---|---|
| 0 | Internal fuse bias powered down | |
| 1 | Internal fuse bias enabled | |

| D5 | **SYNC EN**<br>Default 1 | Enables the SYNC input buffer. |
|---|---|---|
| 0 | SYNC input buffer disabled | |
| 1 | SYNC input bffer enabled | |

| D4 | **TRIG EN**<br>Default 1 | Enables the TRIGGER input buffer. |
|---|---|---|
| 0 | TRIGGER input buffer disabled | |
| 1 | TRIGGER input bffer enabled | |

| D3-D0 | Read back 1 | |
|---|---|---|

Product Folder Links: *ADS54T01*

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 3A | LVDS Current Strength | | | LVDS SW | | Internal LVDS Termination | | 0 | 0 | 0 | 0 | DACLK EN | 0 | 0 | OVRA EN | 0 |

| | | | |
|---|---|---|---|
| D15-D13 | **LVDS Current Strength** Default 000 | | LVDS output current strength. |
| 000 | 2 mA | 100 | 3 mA |
| 001 | 2.25 mA | 101 | 3.25 mA |
| 010 | 2.5 mA | 110 | 3.5 mA |
| 011 | 2.75 mA | 111 | 3.75 mA |

| | | |
|---|---|---|
| D12-D11 | **LVDS SW** Default 01 | LVDS driver internal switch setting – correct range must be set for setting in D15-D13 |
| 01 | 2 mA to 2.75 mA | |
| 11 | 3mA to 3.75mA | |

| | | |
|---|---|---|
| D10-D9 | **Internal LVDS Termination** Default 00 | Internal termination |
| 00 | 2 kΩ | |
| 01 | 200 Ω | |
| 10 | 200 Ω | |
| 11 | 100 Ω | |

| | | |
|---|---|---|
| D4 | **DACLK EN** Default 1 | Enable DACLK output buffer |
| 0 | DACLK output buffer powered down | |
| 1 | DACLK output buffer enabled | |

| | | |
|---|---|---|
| D1 | **OVRA EN** Default 1 | Enable OVRA output buffer |
| 0 | OVRA output buffer powered down | |
| 1 | OVRA output buffer enabled | |

| Register Address | Register Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7-A0 in hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 66 | LVDS Output Bus EN | | | | | | | | | | | | | | | |

| | | |
|---|---|---|
| D15-D0 | **LVDS Output Bus EN** Default FFFF | Individual LVDS output pin power down |
| 0 | Output is powered down | |
| 1 | Output is enabled | |
| D15 | corresponds to TRDYP/N (pins N7, P7) | |
| D14 | corresponds to HRESP/N (pins N6, P6) | |
| D13 | SYNCOUTP/N (pins N5, P5) | |
| D12 | Pins N4, P4 (no connect pins) which are not used and should be powered down for power savings | |
| D11-D0 | corresponds to DA11-DA0 | |

# 9 Power Supply Recommendations

The device requires a 1.8-V nominal supply for AVDDC, AVDD18, DVDD, DVDDLVDS, and IOVDD. The device also requires a 3.3-V supply for AVDD33. There are no specific sequence power-supply requirements during device power-up. AVDDC, AVDD18, DVDD, DVDDLVDS, IOVDD and AVDD33 can power up in any order.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

TI Glossary        This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ADS54T01IZAY | Active | Production | NFBGA (ZAY) \| 196 | 160 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | ADS54T01I |
| ADS54T01IZAY.B | Active | Production | NFBGA (ZAY) \| 196 | 160 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | ADS54T01I |
| ADS54T01IZAYR | Active | Production | NFBGA (ZAY) \| 196 | 1000 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | ADS54T01I |
| ADS54T01IZAYR.B | Active | Production | NFBGA (ZAY) \| 196 | 1000 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | ADS54T01I |

**(1) Status:** For more details on status, see our product life cycle.

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|----------------|
| ADS54T01IZAYR | NFBGA | ZAY | 196 | 1000 | 330.0 | 24.4 | 12.3 | 12.3 | 2.3 | 16.0 | 24.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**

*All dimensions are nominal

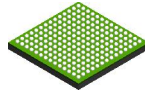| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS54T01IZAYR | NFBGA | ZAY | 196 | 1000 | 350.0 | 350.0 | 43.0 |

## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS54T01IZAY | ZAY | NFBGA | 196 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.4 | 11.2 | 19.65 |
| ADS54T01IZAY.B | ZAY | NFBGA | 196 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.4 | 11.2 | 19.65 |

### ZAY0196A

A | 12.1 / 11.9 | B

BALL A1 CORNER

12.1 / 11.9

1.4 MAX

C

0.45 / 0.35 TYP

BALL TYP

SEATING PLANE

0.12 C

10.4 TYP

SYMM ₵

(0.8) TYP

(0.8) TYP

P
N
M
L
K
J
H
G
F
E
D
C
B
A

10.4 TYP

SYMM ₵

196X ⌀ 0.55 / 0.45

⌀ 0.15 Ⓜ C AⓈ BⓈ
⌀ 0.05 Ⓜ C

0.8 TYP

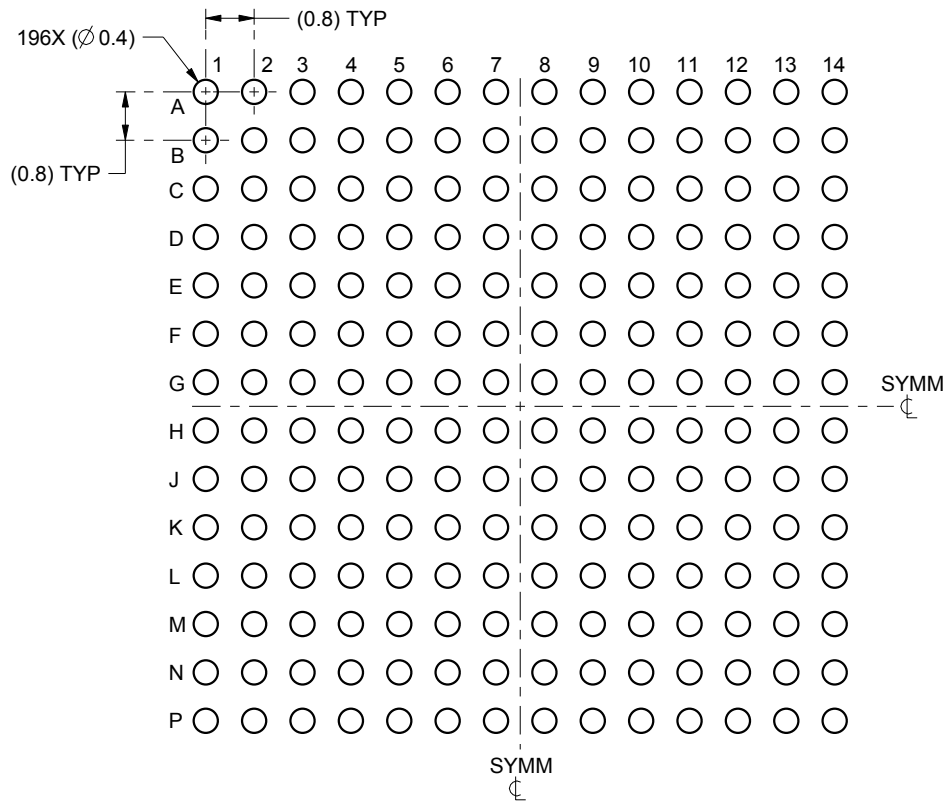1  2  3  4  5  6  7  8  9  10  11  12  13  14

BALL A1 CORNER

0.8 TYP
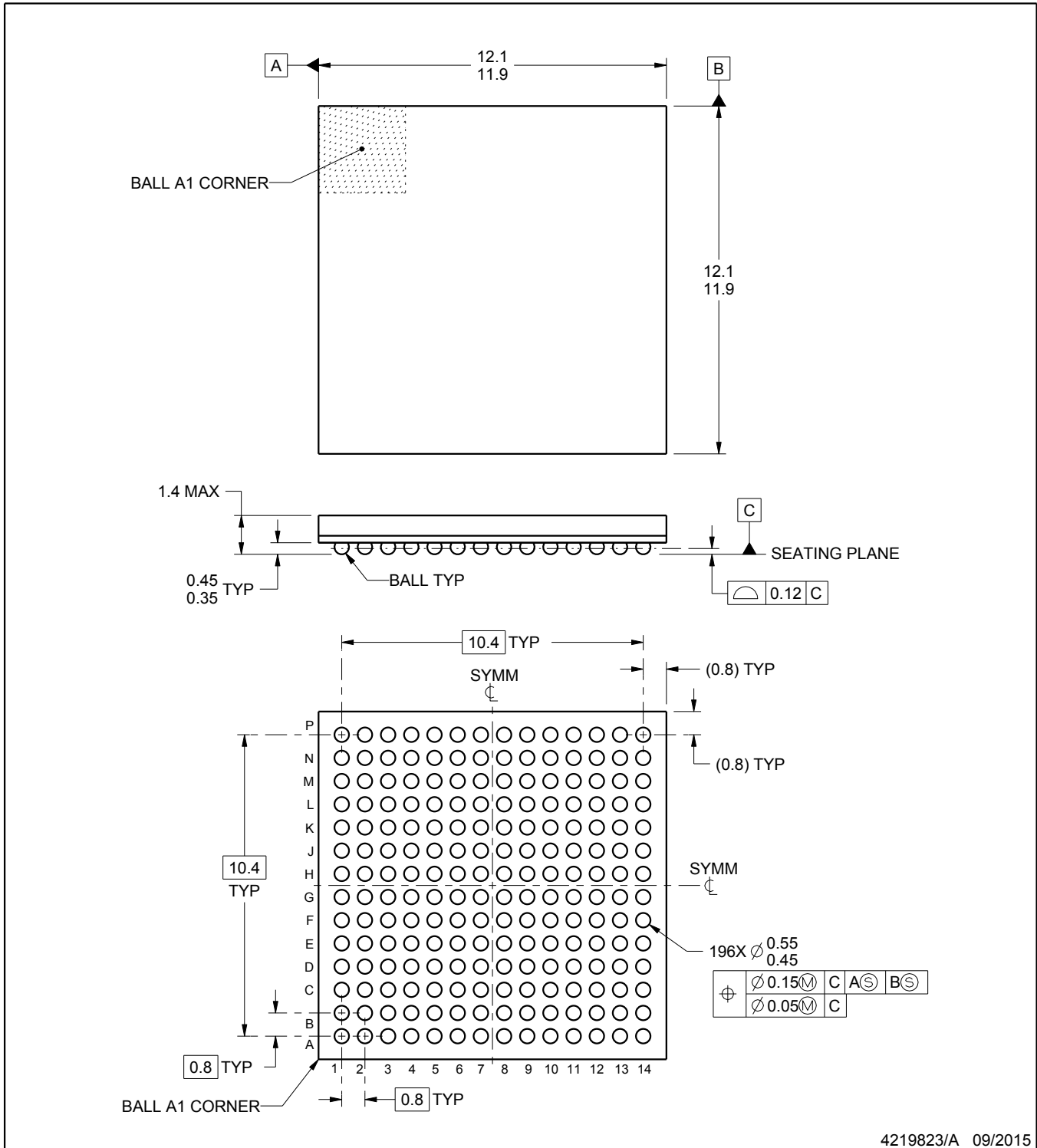
4219823/A  09/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

LAND PATTERN EXAMPLE
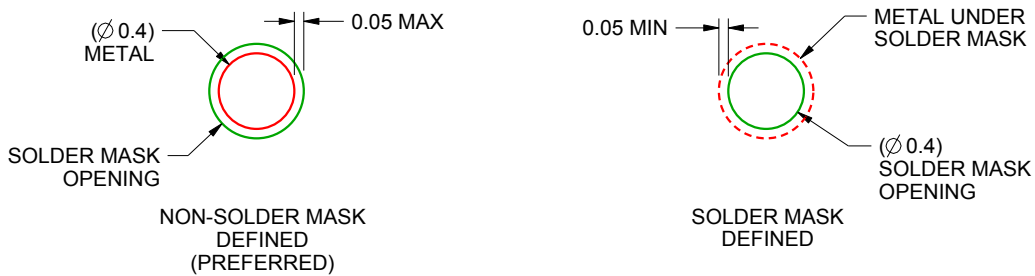SCALE:8X

SOLDER MASK DETAILS
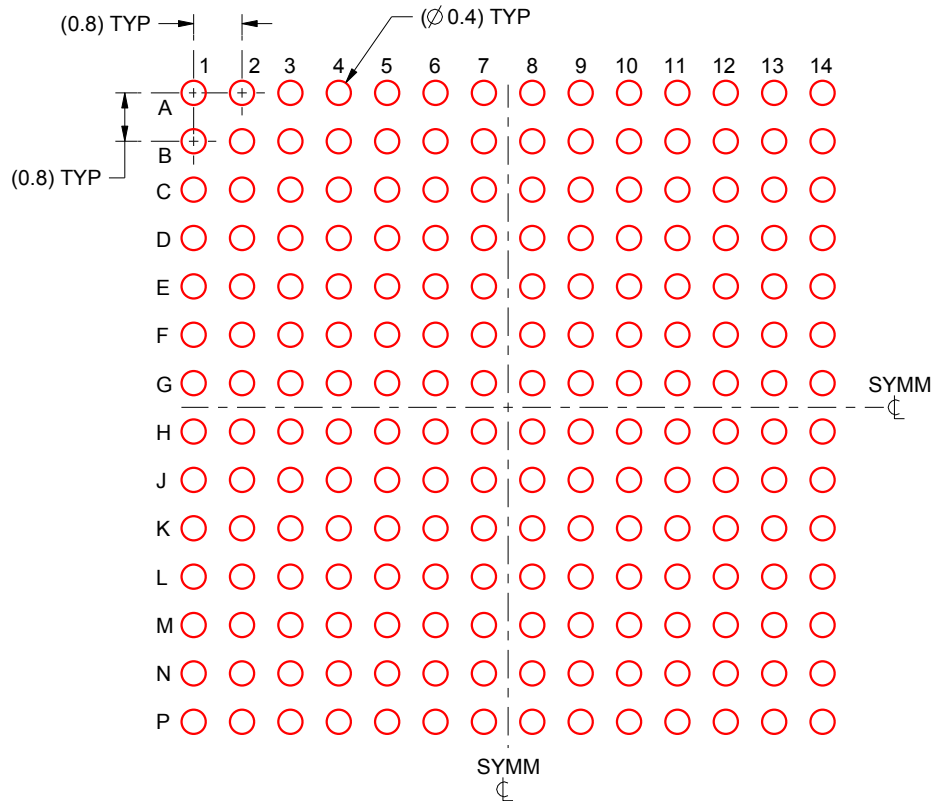NOT TO SCALE

4219823/A  09/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

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## ZAY0196A

SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4219823/A   09/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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