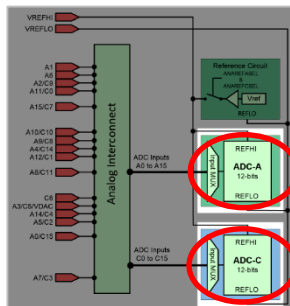


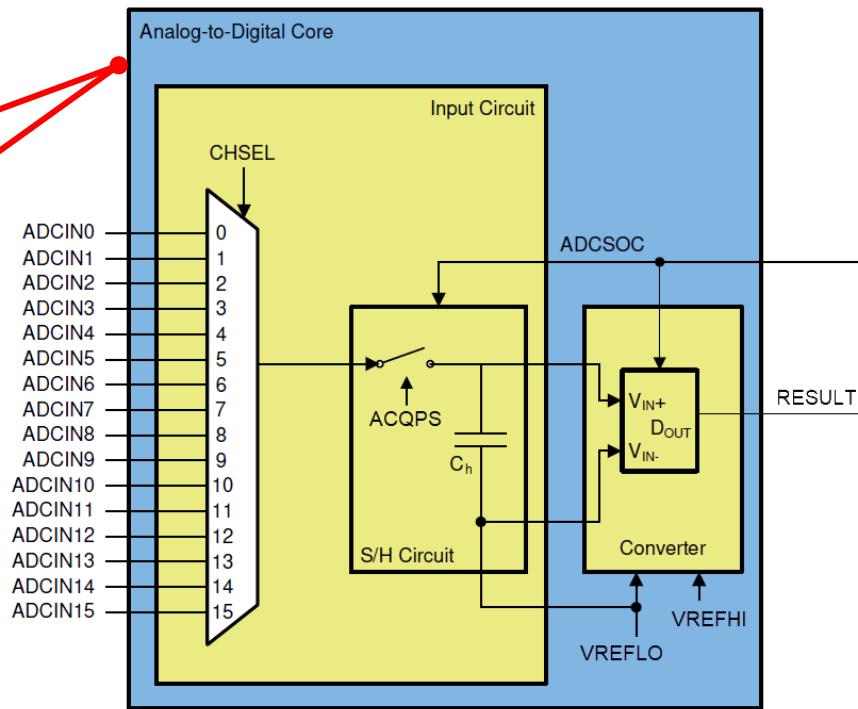
C2000 ADC Video Series

Analog-to-Digital Converter (ADC) Core

ADC Core



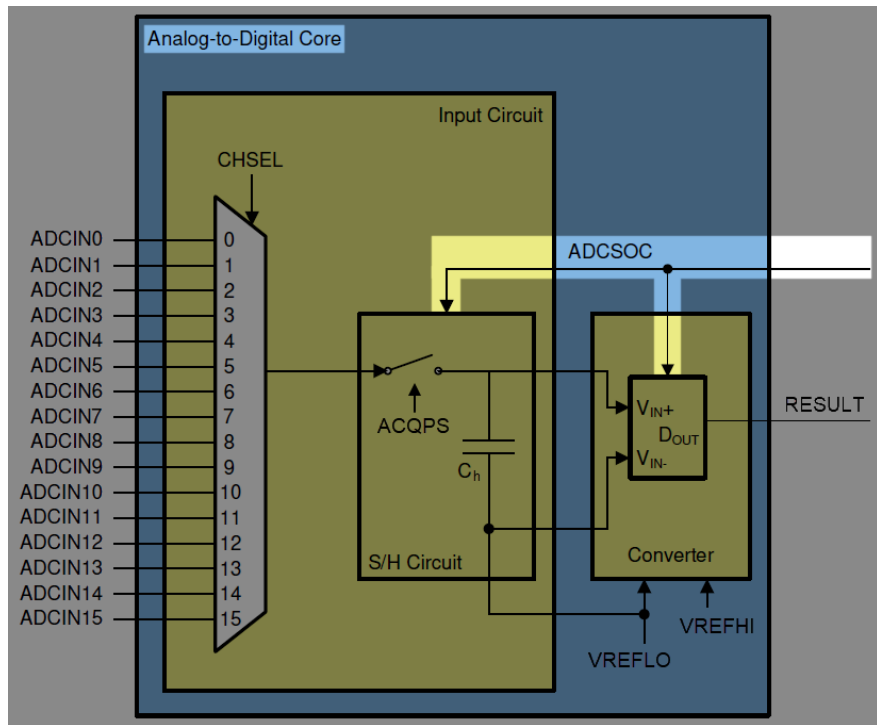
- Each ADC on device has identical core architectures



- Each ADC operates independently of the other
- The ADC behavior can be tuned for various use cases through software configuration

ADC Core: SOC Trigger

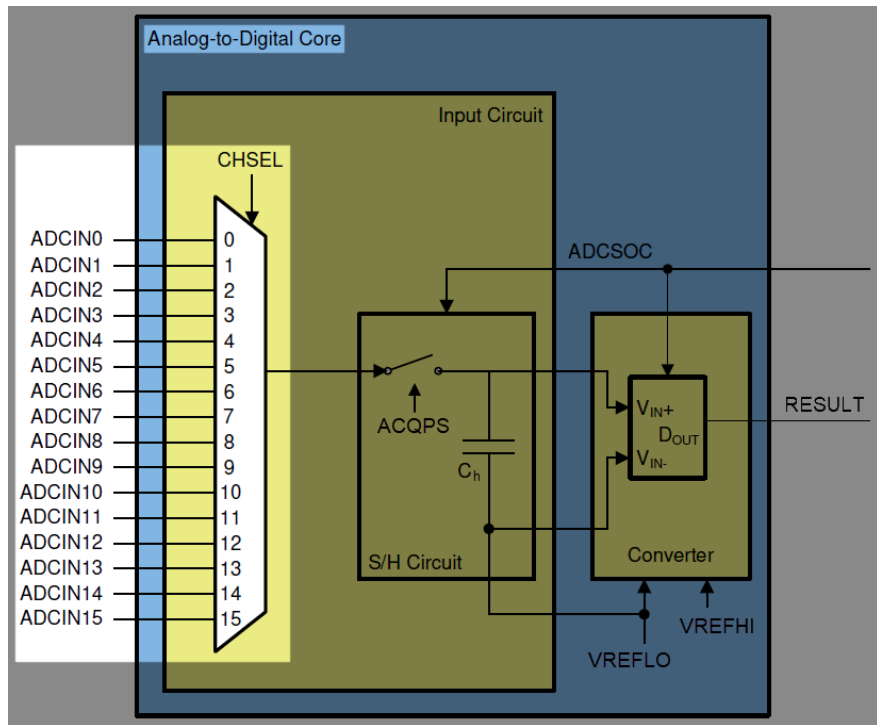
- The default state for the ADC core is to IDLE
- A conversion is initiated by an incoming Start of Conversion (SOC) trigger signal



- The SOC trigger can be derived from various sources:
 - EPWM Time Match
 - Software Write
 - Timer Interrupt
 - GPIO Input

ADC Core: Channel Selection

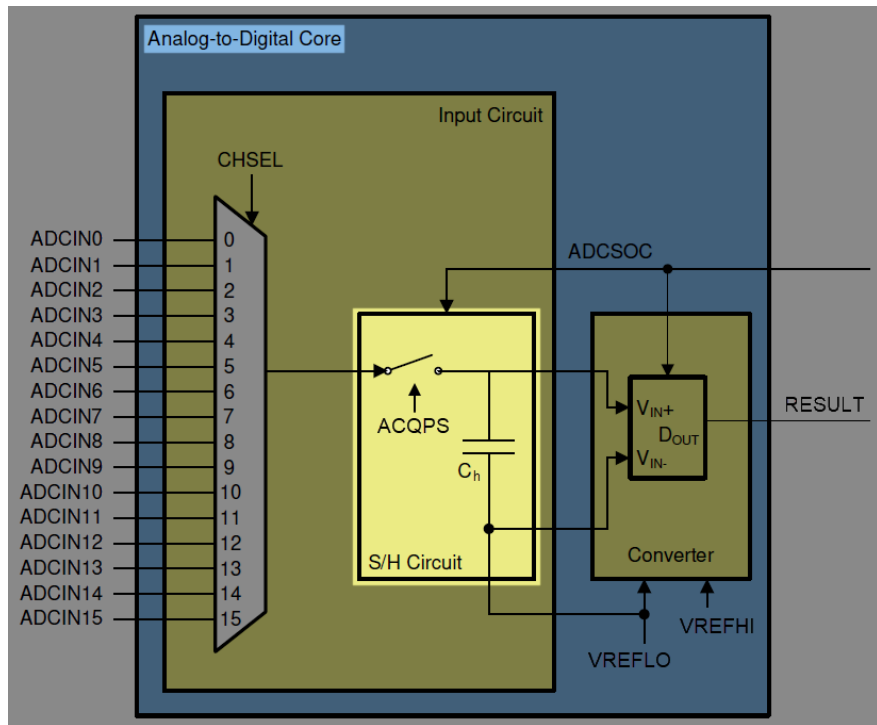
- The first step in converting an analog signal is to enable the ADCIN channel specified by CHSEL
- The ADC can only convert one channel at a time



- The ADC design allows for 16 channels, but some are not mapped to a pin

ADC Core: ACQPS

- The Sample and Hold (S/H) Circuit will charge the C_h capacitor by connecting the sampling switch for the duration specified by the Acquisition Pre-Scaler (ACQPS) value



- An ACQPS that is too short will stop the charging of C_h before its voltage matches ADCIN
- An ACQPS that is too long will delay the conversion step unnecessarily

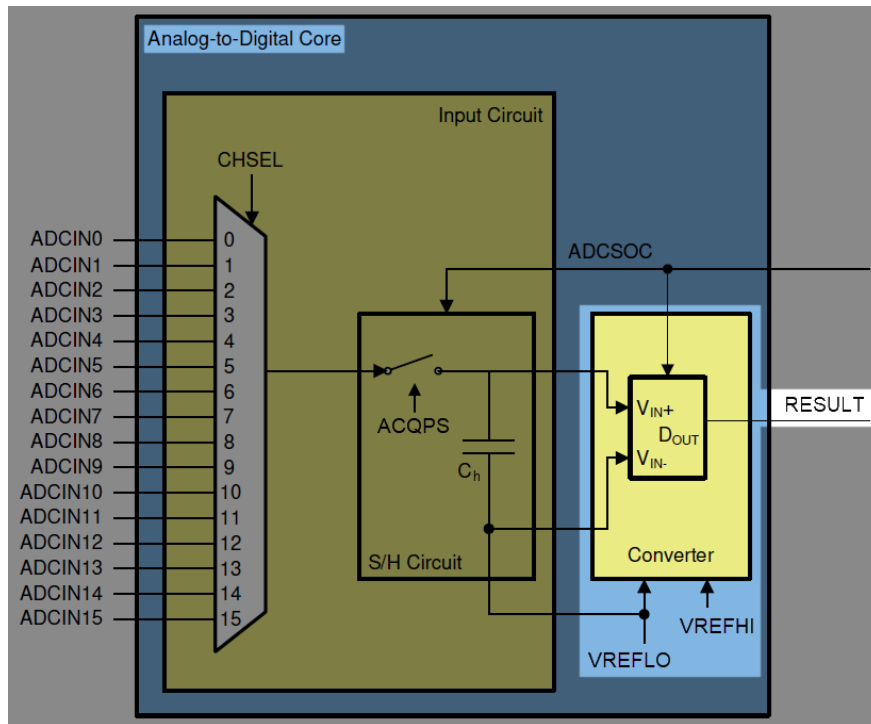
ADC Core: Converter

- The converter will calculate the digital representation of the voltage on C_h

- The approximate digital value is:

$$\text{12-bit: } 2^{12} \times \frac{V_{Ch}}{V_{REF}}$$

$$\text{16-bit: } 2^{16} \times \frac{V_{Ch}}{V_{REF}}$$



- The converter will leak high-speed switching noise into V_{REF} while active
- Proper decoupling is required to keep $V_{REFHI} - V_{REFLO}$ stable during conversions

ADC Resources

- Analog Subsystem Training Module and Guided Lab in [C2000 Academy](#)
- [TI Precision Labs ADC Series](#)
- ADC Application Reports
 - [Input Signal Circuit Design](#)
 - [Charge Sharing Circuit Design](#)
 - [Simulating Charge Sharing Circuits](#)
 - [Mitigating Channel-to-Channel Cross-talk](#)