

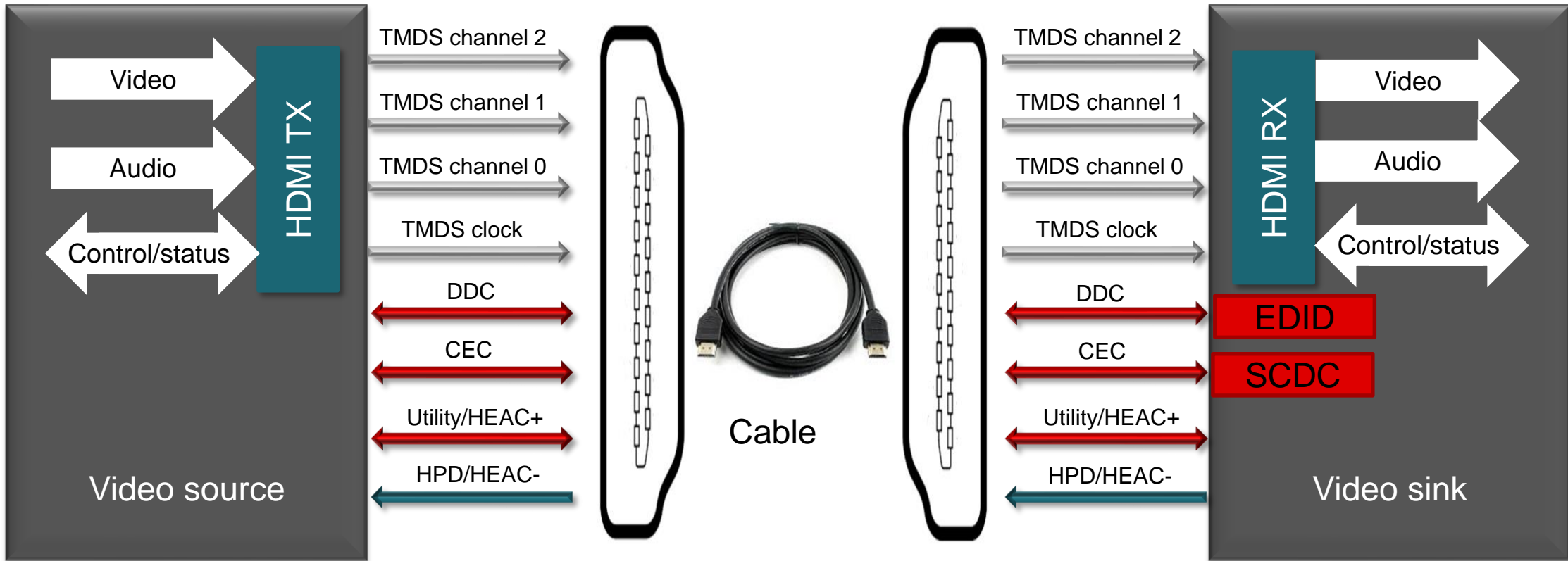
# Understanding HDMI DDC Overview

## TI Precision Labs – Video Interface

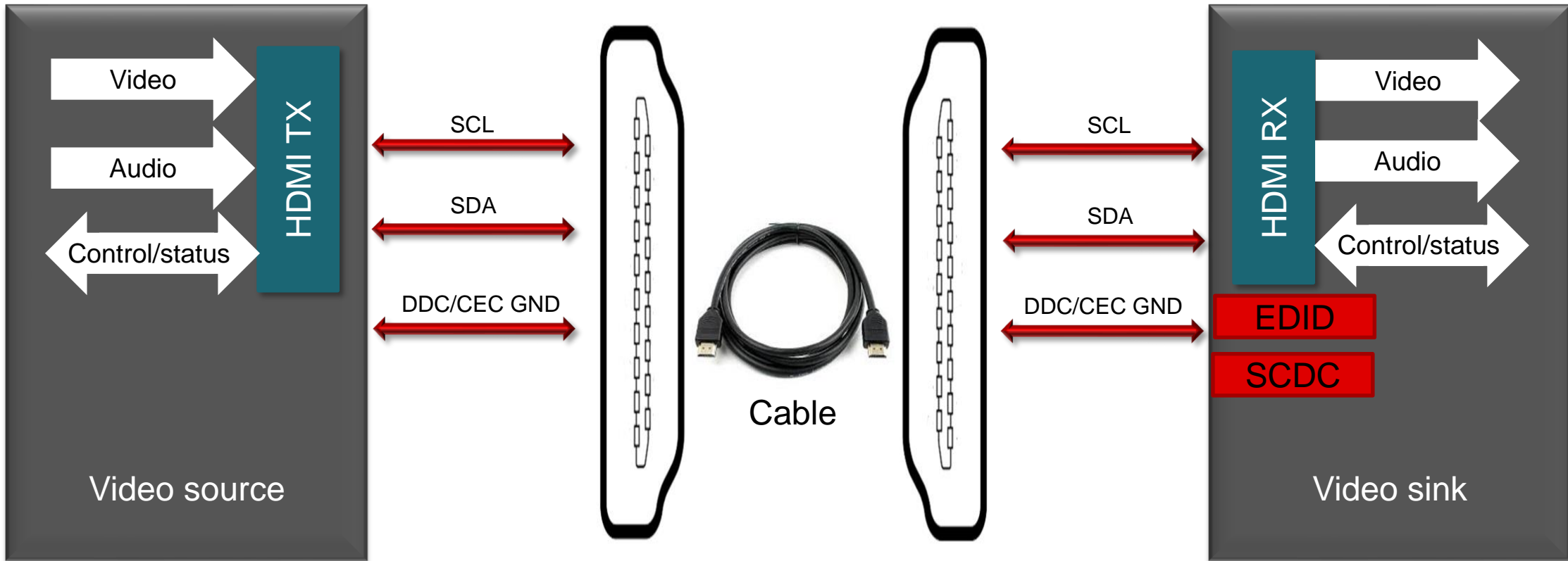
Prepared by David Liu

Presented by

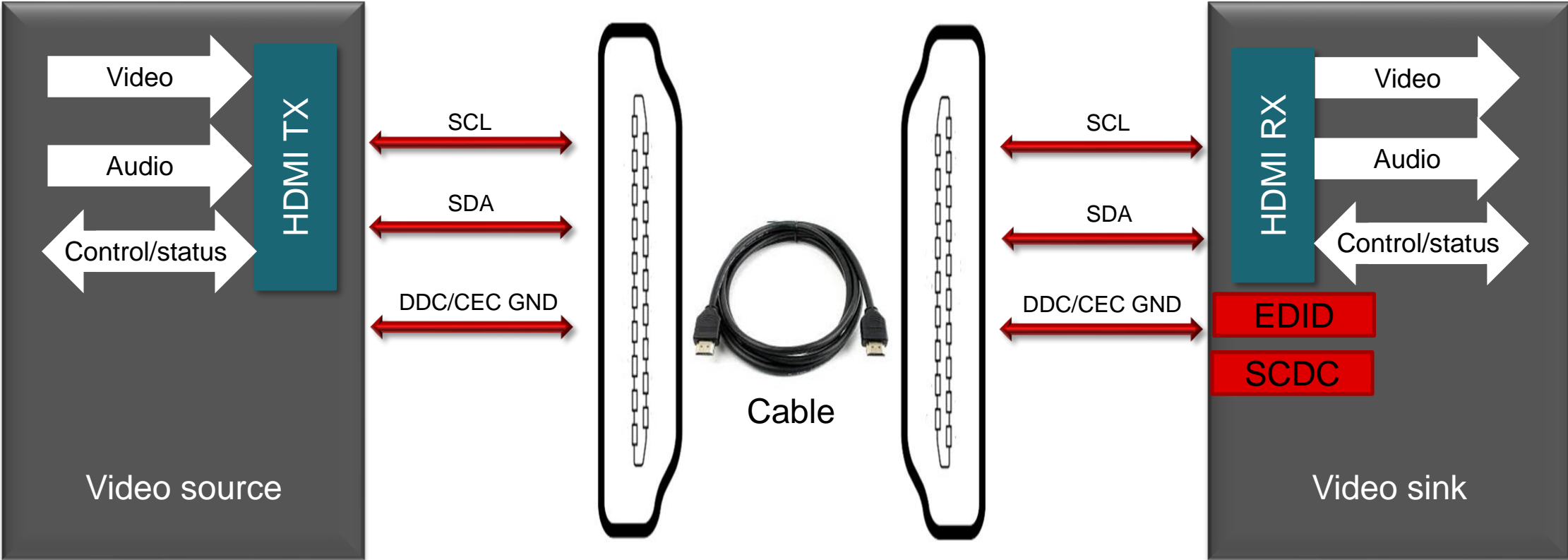
# HDMI signal interface



# Display Data Channel (DDC)



# Status and Control Data Channel (SCDC)



# SCDC HDMI 1.4b/2.0 TMDS configuration register

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x20	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	TMDS_Bit_CLK_Ratio	Scrambling_Enable

*TMDS configuration register for HDMI 1.4b and HDMI 2.0*

- TMDS\_BIT\_CLK\_RATIO= 1, HDMI2.0
- TMDS\_BIT\_CLK\_RATIO= 0, HDMI1.4

# SCDC HDMI 2.1 sink configuration register

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x31	FFE_LEVELS				FRL_RATE			

*Sink Configuration Register for HDMI2.1*

- Bit[3:0] = 0, Disable FRL
- Bit[3:0] = 1, 3Gbps on 3 lanes (0, 1, 2)
- Bit[3:0] = 2, 6Gbps on 3 lanes (0, 1, 2)
- Bit[3:0] = 3, 6Gbps on 4 lanes
- Bit[3:0] = 4, 8Gbps on 4 lanes
- Bit[3:0] = 5, 10Gbps on 4 lanes
- Bit[3:0] = 6, 12Gbps on 4 lanes

# HDMI1.4/2.0/2.1 configuration register summary

	TMDS_BIT_CLK_RATIO	FRL_RATE
HDMI1.4b	0	0
HDMI2.0	1	0
HDMI2.1	0	1,2,3,4,5, or 6

# HDMI 2.1 link training SCDC registers

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x40	DSC_DECODE_FAIL	FLT_READY	RSVD	LANE3_LOCKED	CH2_LN2_LOCKED	CH1_LN1_LOCKED	CH0_LN0_LOCKED	CLK_DETECTED

*Status Flag Register*

Sink sets to 1 when it is ready for link training.  
Clear it when the link training is successful

# HDMI 2.1 link training SCDC registers

Sink sets to 1 when Link Training is successful and ready to receive video

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	RSVD	RESD_UPDATE	FLT_UPDATE	FRL_START	Source_Test_Update	RR_Test	CED_Update	Status_Update

*Update Flag Register*

Sink sets to 1 when a value is changed in the register offset 0x41 and 0x42. The video source writes a 1 to this bit to clear it

# SCDC HDMI 2.1 sink configuration register

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x41	LN1_LTP_REQ				LN0_LTP_REQ			
0x42	LN3_LTP_REQ				LN2_LTP_REQ			

*Sink Configuration Register for HDMI2.1*

# Short quiz

True or false: The video source does not use DDC to determine the capabilities and characteristics of the video sink

# Short quiz

**FALSE**

True or false: The video source does not use DDC to determine the capabilities and characteristics of the video sink

**False.** The capabilities and characteristics of the video sink is communicated using the DDC interface.

# Short quiz

True or false: The link training is introduced in the HDMI2.1 specification

# Short quiz



True or false: The link training is introduced in the HDMI2.1 specification

**True.** The link training is used by the video source and sink to prepare the video lanes for data transmission when initializing the link for FRL or HDMI2.1 operation

# Short quiz

True or false: Source can start the HDMI2.1 link training any time it wants

## Short quiz

**FALSE**

True or false: Source can start the HDMI2.1 link training any time it wants

**False.** Source has to wait until the sink set the FLT\_READY bit

# Short quiz

True or false: TMDS\_BIT\_CLK\_RATIO bit is set to 1 for HDMI1.4b

## Short quiz

**FALSE**

True or false: TMDS\_BIT\_CLK\_RATIO bit is set to 1 for HDMI1.4b

**False.** TMDS\_BIT\_CLK\_RATIO bit is set to 0 for HDMI1.4b and set to 1 for HDMI2.0



© Copyright 2024 Texas Instruments Incorporated. All rights reserved.

This material is provided strictly “as-is,” for informational purposes only, and without any warranty.  
Use of this material is subject to TI’s **Terms of Use**, viewable at [TI.com](https://www.ti.com)