

Low Distortion Design – 2

TIPL 1322

TI Precision Labs – Op Amps

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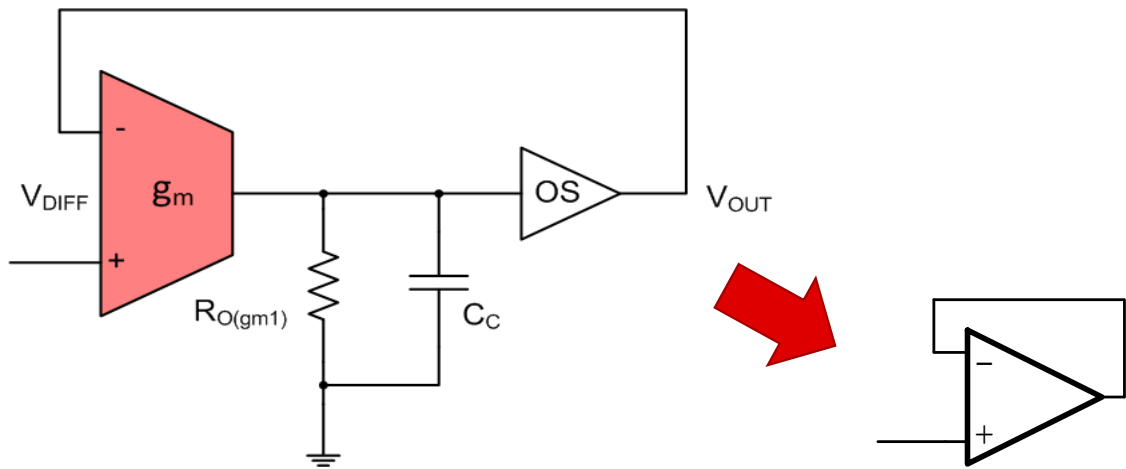
Prerequisites: Noise 1 – 3

(TIPL1311 – TIPL1313)



Hello, and welcome to part 2 of the TI Precision Labs series on designing low distortion op amp circuitry. This video will focus on sources for distortion from the op amp's internal input stage. Specifically we will look at how the amplitude of the differential input signal effects distortion, as well as distortion from common mode limitations and input impedance as a function of common mode voltage.

A Simplified Internal Op Amp Design

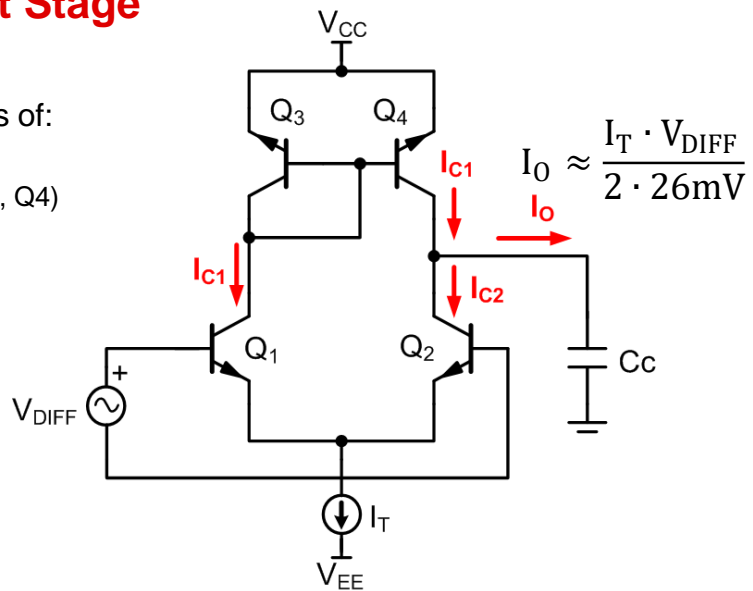


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This slide shows the block diagram of a simplified internal op amp design. The input is represented by the transconductance block g_m . This stage will source or sink current into a compensation capacitor C_c , depending on the differential voltage between its inputs. C_c is generally referred to as the miller compensation capacitor. The voltage across the compensation capacitor is buffered by an output stage amplifier. Finally, a portion of the output is fed back to the input stage as negative feedback. Let's take a closer look at the input stage.

A Basic Op Amp Input Stage

- A basic op amp input consists of:
 - A differential pair (Q1, Q2)
 - A current mirror active load (Q3, Q4)
 - A tail current source (IT)



The input stage is classically a differential pair of transistors, shown here with Q1 and Q2. This differential pair has a current mirror in the collector leg, shown here as Q3 and Q4, and a tail current source, shown here as I_T . The current that the input stage sources or sinks into the miller compensation capacitor is roughly the tail current times the differential input voltage divided by two times the thermal voltage, which is approximately 26mV. But this is really just a small signal approximation. Let's examine a graph of output current versus differential input voltage.

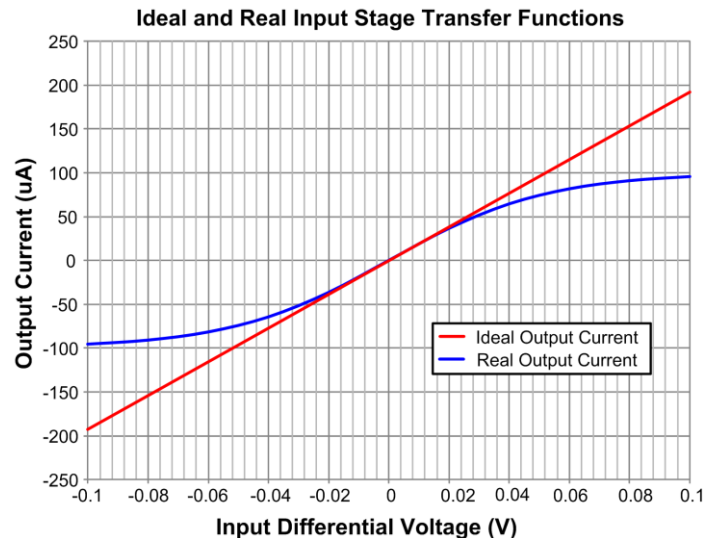
Input Stage Transfer Function

- Ideal output current:

$$I_O \approx \frac{I_T \cdot V_{DIFF}}{2 \cdot V_T}$$

- Real output current:

$$I_O = I_T \cdot \tanh\left(\frac{V_{DIFF}}{2 \cdot V_T}\right)$$



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This slide shows the actual output current versus input differential voltage. The small signal approximation, introduced on the previous slide, is only accurate for small differential input voltages. In this example, you can see that differential input signals in the +/-20mV range are on the linear part of the curve. In the real world, the input differential voltage may not be very small. As we apply larger differential input signals, we will see that the current that the input stage sources and sinks into the compensation capacitor is very nonlinear.

On the right side of the slide, we have a graph with input differential voltage on the x-axis, and output current on the y-axis for a hypothetical op amp input stage with a 100uA tail current source. The red line shows the simple linear approximation that was given on the previous slide, just the tail current times the differential input voltage divided by two times the thermal voltage. We can see near zero differential input voltage that the ideal curve is very close to the real curve. The real curve is shown in blue. The real curve is the tail current times the hyperbolic tangent of the differential voltage divided by two times V_T . This is what the current sourced into the compensation capacitor really is. This should make sense, because we can never source or sink more current into the compensation capacitor than our tail current source. But, you can see that the ideal curve just keeps progressing up well past 100uA, whereas the real curve is limited to a maximum of 100uA.

Input Stage Transfer Function

- Taylor series of the hyperbolic tangent function (tanh):

$$I_O = \frac{I_T}{2V_T} V_{DIFF} - \frac{I_T}{24V_T^3} V_{DIFF}^3 + \frac{I_T}{240V_T^5} V_{DIFF}^5 \dots$$

- Note: Distortion depends on input differential voltage (V_{DIFF})
- More op amp open loop gain (A_{OL}) means less input stage distortion

$$V_{DIFF} = \frac{V_O}{A_{OL}} = \frac{V_{IN}}{1 + A_{OL}\beta}$$

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We know that our input differential pair's transfer function follows the hyperbolic tangent function. If we perform a Taylor series expansion on the input transfer function we get this equation. The first term in the Taylor expansion is the ideal small signal transfer function. In addition to this, we have a series of odd harmonics. The odd harmonics are denoted by odd exponents of 3, and 5. Of course, this series would continue infinitely, only containing odd harmonics. Notice that the harmonics all depend on the input differential voltage, which means that a larger differential input will correspond to larger distortion terms. Thus, for low distortion operation of an op amp, I want the smallest differential input signal possible. Ok, so, how do we do this?

Well, the input differential input of an op amp is equal to the output voltage divided by the open loop voltage gain. The differential input can also be expressed as the input signal divided by one plus A_{OL} times the feedback factor beta. The point here is that op amps with greater open loop gain will have less distortion from their input stage, and that is because their input differential voltage is smaller.

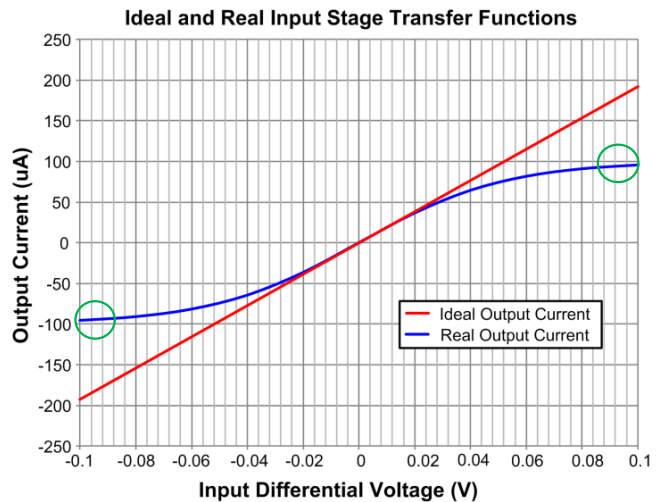
Slew-Induced Distortion?

- **Myth:** Below the slew rate limit, the op amp is distortion free.
- **Reality:** Distortion occurs below slew limit:

$$SR = \frac{i_T}{C_C}$$

- **Example:** $I_T = 100\mu\text{A}$, $C_C = 20\text{pF}$

$$SR = \frac{i_T}{C_C} = \frac{100\mu\text{A}}{20\text{pF}} = 5\text{V} / \mu\text{s}$$



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But what about the concept of slew induced distortion? There is a common myth that below the slew rate limit the op amp is essentially distortion free. However, slewing occurs where 100% of the tail current is diverted into the compensation capacitor. That is, the endpoints of the real output current curve circled in green. Noting that the red curve is the ideal output current, you can see that by the time we reach our slew rate limitation the real output current curve is already very non-linear. So, input stage distortion will happen well below the slew rate limitation of an op amp.

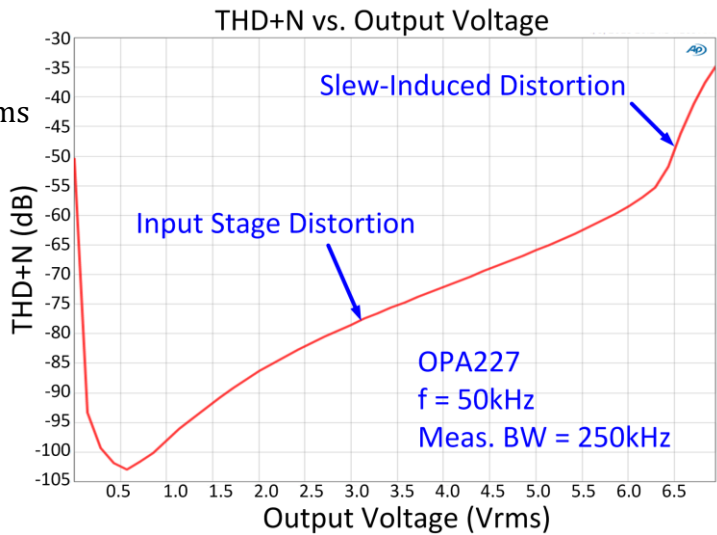
Lets consider an example where the tail current is 100uA and the compensation capacitor is 20pF. In this case, the slew rate can be calculated to be 5V/us. However, that will only happen for input differential voltages of +/-100mV. By the time you apply that level of input differential voltage, the input stage of the amplifier is already extremely non-linear. The slew rate only defines the fastest rate of change in the output of an op amp, it doesn't define a barrier beyond which distortion starts, because distortion will begin well below the slew rate limitation.

Slew-Induced Distortion?

- Slew rate limitation:

$$\frac{SR}{2\pi f} = \frac{2.3 \text{ V}/\mu\text{s}}{2\pi(50\text{kHz})} = 7.32\text{Vpk} = 5.18\text{Vrms}$$

- Input stage distortion always appears before slew rate distortion
- Slew rate limitation does increase distortion at high output levels

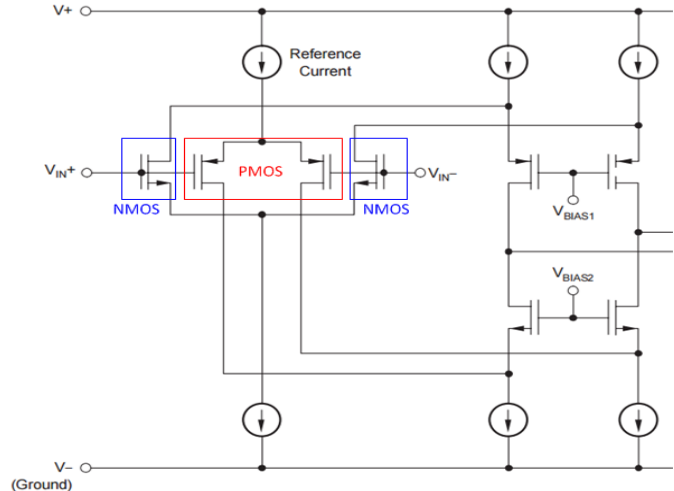


This slide shows an example of measured distortion data for the OPA227. We are plotting the THD+N on the y-axis versus the rms output voltage on the x-axis. This measurement was made with a 50kHz input signal and a 250kHz measurement bandwidth. So, for a 50kHz signal, I can measure up to the 5th harmonic of that signal, because only the 5th harmonic and lower will be inside the measurement bandwidth. All harmonics above the 5th harmonic will be outside the measurement bandwidth and not included in the measurement.

So for a 50kHz signal we can determine what our slew rate limitation will be, that is, we can find the peak output signal without really gross distortion. This is calculated by our slew rate divided by 2-pi times the frequency. For the OPA227 example, the slew rate of 2.3V/us divided by 2-pi times 50kHz, gives us about 7.32Vpk or 5.18Vrms. Let's compare that to the graph. We should notice right away that above about 1Vrms the distortion of the OPA227 is increasing dramatically, but we are still well our slew rate limitation. We calculated the slew rate limitation to be about 5Vrms, but actually shows up near 6Vrms. This is all input stage distortion; primarily 3rd and 5th harmonic. It happens because as we increase our output amplitude, the input differential voltage is getting larger and larger. At higher voltages we reach the slew rate limit and you will see a sharp increase in the level of distortion. However, at that point the THD+N is about -55dB which is unacceptable in most systems. So, if you had relied upon low distortion operation in based on the slew rate limitation, you would be really surprised when you looked at your measured results.

Input Crossover Distortion

- Rail-to-rail inputs 2 differential pairs
 - PMOS for common mode input voltages: V_{EE} to $V_{CC}-1.8V$
 - NMOS for common mode input voltages: $V_{CC}-1.8V$ and above
- “Crossover region” where both inputs are conducting
 - DC offset change
 - Shift in AC parameters
- The offset of the NMOS pair may be untrimmed
 - Causes a sudden change in input offset voltage of the op amp

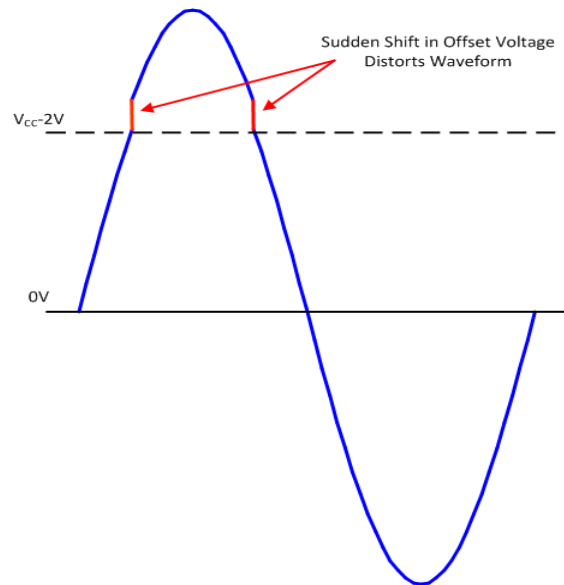
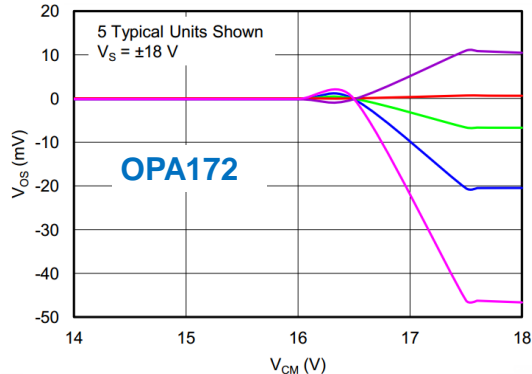


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Moving on to another source of input stage distortion, let's address input crossover distortion. The schematic on the right hand side of the slide is a classic rail-to-rail input CMOS op amp with a double folded cascode. It consists of a PMOS input pair and an NMOS input pair. For common mode input voltages from the negative supply up to 1.8V below the positive supply the PMOS input pair is operating and the NMOS pair is idle. Above that common mode range, so for 1.8V below the positive rail and above, the NMOS input stage takes over and the PMOS pair is idle. There is a crossover region at about 1.8V below the positive rail where both inputs are conducting. In that region, the dc offset can change and there may be a shift in the amplifier's ac parameters. Above that region, the offset of the NMOS pair may be untrimmed and this will cause a sudden change in the input offset voltage of the amplifier. This sudden change in offset voltage will show up as distortion in ac signals.

Input Crossover Distortion

- Non-Inverting Amplifiers
 - Input signal passes through crossover region
 - Additional offset is summed with the input signal
 - Additional offset distorts the signal
 - Typically high-order harmonics



The graph on the lower left hand side shows the offset voltage versus common mode voltage for the OPA172. This graph focus on common mode voltages near the positive supply, that is near the crossover region. The part is operating on $\pm 18V$ supplies, and as the input common mode voltage approaches the positive rail you can see the offset enter a crossover region and then the offset settles to whatever the offset of the NMOS pair is. If we think of this change in offset as a sudden step in input offset voltage, we can see how this will affect the output of a unity gain follower with a sine wave applied to the input. So imagine I have an op amp in a gain of +1 and I'm applying a sine wave to the input. As the sine wave approaches the transition region, the offset voltage shifts. This creates a discontinuity in the sine wave where the sudden increase in the offset is summed with the input signal shifting the signal. These sudden shifts in the signal typically generate higher order distortion terms which will be above the second or third harmonic.

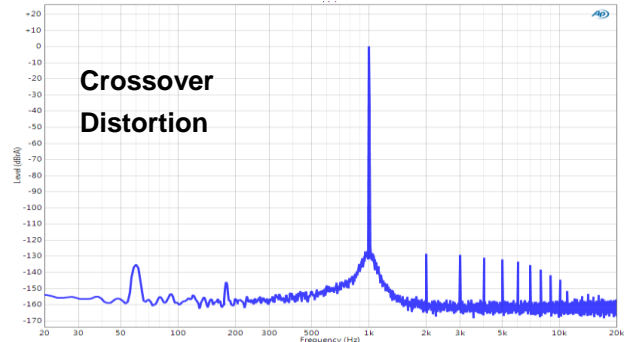
Example of Input Crossover Distortion

OPA2172: Gain +1, $5V_{RMS}(7.07V_{pk})/1kHz$ signal, $100k\Omega$ load

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE					
V_{CM}	Common-mode voltage range ⁽¹⁾	(V-) - 0.1 V		(V+) - 2 V	V



+/-10V Supplies



+/-9V Supplies

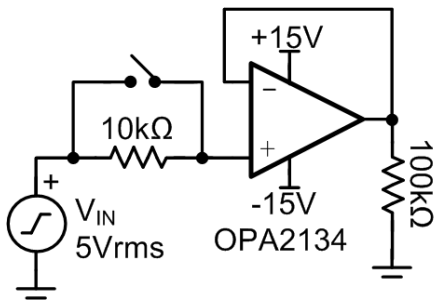
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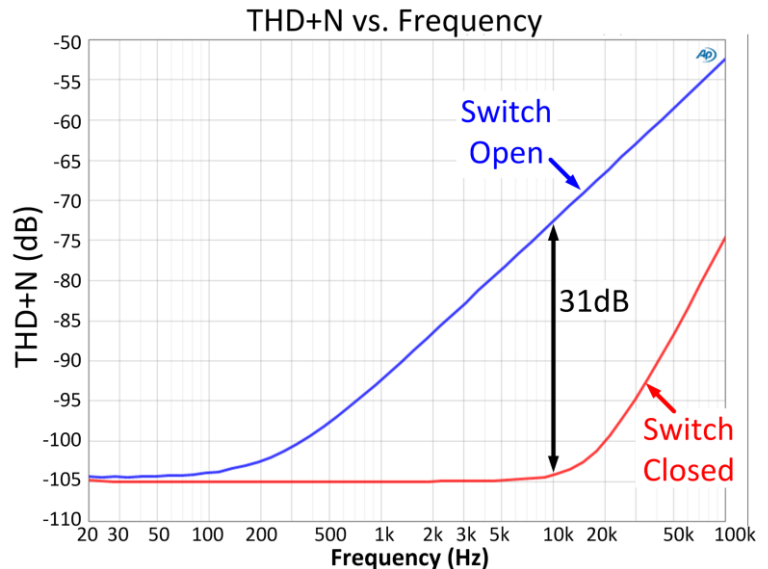
This slide shows measured examples of an amplifier with and without crossover distortion. In this example an OPA2172 amplifier is used in a gain of +1 with a 5Vrms, or 7.07Vpk, input signal is applied. The crossover region for this device happens about 2V from the positive supply. The case on the left, uses +/-10V supplies, and with a 7.07Vpk input the signal is about 3V away from the positive rail. So this case does not enter the crossover region. The distortion is extremely low in this case. The noise floor is about -160dB below the fundamental, and the third harmonic is dominating here at about -146dB.

Just decreasing the power supply voltages to +/-9V, causes all these harmonics to be generated. This happens because now the input sin wave is a little closer than 2V from the positive rail and we are entering the crossover region. The amplitude of the harmonics is still fairly low at about -130dB relative to the fundamental. If we were to decrease the supply voltage further, the distortion would get worse.

Common-Mode Input Impedance Variation



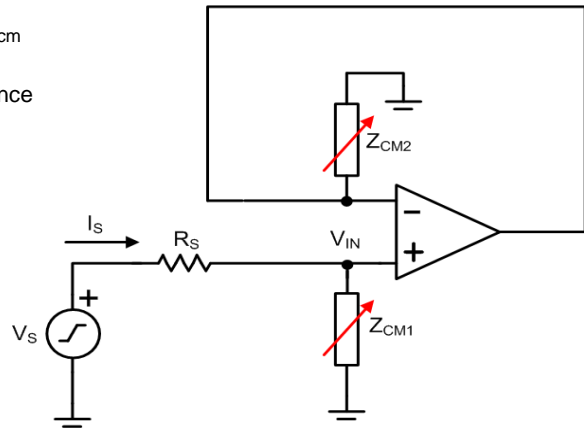
- Meas. Bandwidth = 500kHz
- THD+N Comparison at 10kHz
 - $R_s = 0$, -104dB
 - $R_s = 10k\Omega$, -73dB



Many engineers are familiar with slew rate limitations or input crossover distortion, but common mode input impedance variation is often not understood or neglected. The graph on the right shows the dramatic impact of common mode input impedance variation on distortion. The circuit configuration here is the OPA2134 op amp in a voltage follower configuration with a 5Vrms input source and a 10kΩ source impedance. The switch can be closed or opened to show the distortion with and without the source impedance. With the source impedance shorted, the distortion is very low; see the red line on the plot. However, if I open the switch the source impedance is 10kΩ, and now the distortion is much worse; see the blue line. In fact, comparing the blue and red line you can see that the distortion is actually 31dB worse at 10kHz. So, the question is, why does this happen? Since op amps have very high input impedance, you might expect that the 10kΩ source impedance shouldn't matter. First, you should realize that this change is not because of the noise from the 10kΩ resistor, as noise would just shift the entire curve upward. So the increase in THD+N is from increasing distortion, but what causes this distortion?

CM Impedance Variation

- Common-mode input impedance varies with V_{cm}
 - This distorts the input voltage waveform
 - Worst in non-inverting, low gain, high source impedance
- Input capacitance variation
 - JFET Input Op Amps:
 - Gate-to-substrate capacitance
 - ESD Diodes
 - BJT Input Op Amps:
 - Collector-base junction capacitance
 - ESD Diodes
 - CMOS Input Op Amps
 - ESD Diodes
- Input resistance variation
 - Mismatch in leakage of ESD diodes
 - Beta of input transistors varies with V_{CE} and I_C



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The answer is that the common mode impedance is generally not a constant and it will vary with a change in common mode voltage. Think of my common mode impedance as a lumped element impedance from each op amp input to ground. This impedance will vary depending on the voltage across it. As I apply an input sine wave to the op amp, if this impedance is varying, then the current drawn through the source impedance is no longer sinusoidal. It changes based on what the common mode voltage is, and instantaneously what this impedance is in real time.

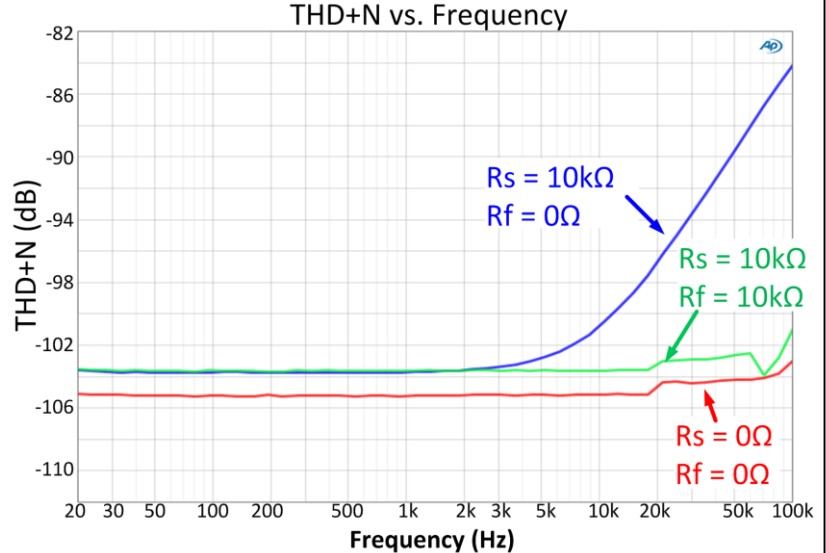
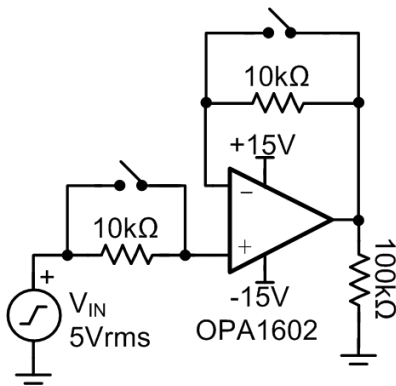
You might wonder what causes the input impedance to vary. Depending on the type of op amp there are a few different mechanisms that cause it. The worst offenders are the classic JFET input op amps. For these op amps, the gate to substrate capacitance on the input devices is the primary cause of the input impedance variation. So, most classic JFET input amplifiers have a very large gate to substrate capacitance that comes from the reversed biased diode created from the input JFET to the substrate of the op amp. As the input common mode voltage changes, the voltage across the reversed bias diode changes. In general, if you change the reverse bias voltage across a diode its capacitance changes. And that is what is happening here. However, even if you don't have a gate to substrate capacitance, we still have reverse biased ESD diodes whose capacitance will change with common mode voltage. On BJT op

amps the main offender is the collector to base junction of the device. Of course, BJT devices also have ESD diodes, and on CMOS devices this effect is entirely from the ESD diodes. On CMOS op amps the input structures are inherently more susceptible to ESD. Therefore, the ESD diodes are normally larger, and consequently, this effect can be greater in a CMOS op amp.

There is also input resistance variation, not just input capacitance variation. This can come from mismatch in the input ESD diode leakage. On bipolar amplifiers, the beta of the input transistors is not constant. Beta varies with changing collector to emitter voltage, and collector current. As the common mode voltage changes the collector to emitter voltage and collector current will change and the beta will be modulated. Variations in beta versus common mode, cause variations in bias current which is effectively a variation in the input resistance of the amplifier.

Improving Performance: Match Impedance at Inputs

- Adds additional noise
- May cause stability problems!



TEXAS INSTRUMENTS

If all op amps have input impedance that varies with common mode voltage how can we improve performance? As we mentioned previously, the varying common mode impedance draws a current through the source impedance. I can put an identical impedance in the feedback loop of the op amp so that the impedance seen by each input of the op amp is matched. Since the common mode impedance at each input of the op amp is varying identically, the nonlinear current drawn by each input will also be identical. This will create a matched distortion signal at each input of the op amp, which will be canceled by the common mode rejection of the amplifier. Unfortunately, placing a resistor in the feedback of the amplifier can create stability problems. So, if you use this technique to reduce distortion, make sure that you simulate to check stability.

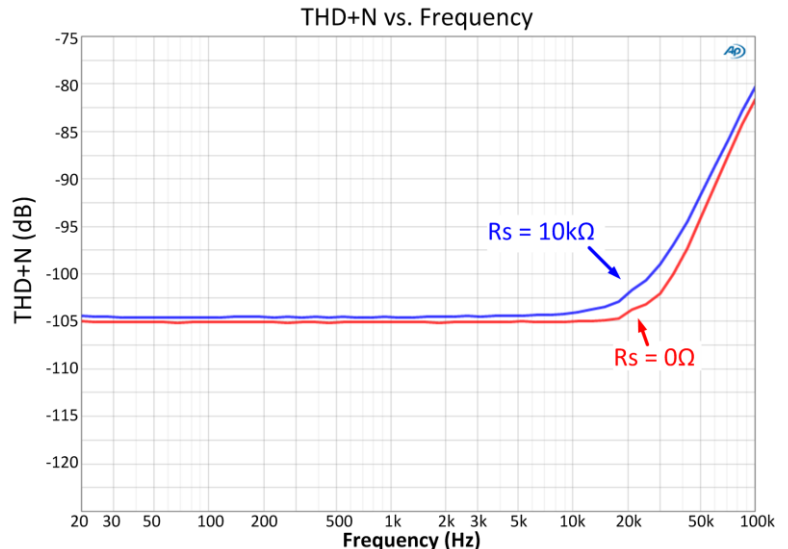
To demonstrate the effectiveness of this technique, we show the measured results for a OPA1602 in three different configurations. First look at the red plot. This is the distortion of the OPA1602 with zero source impedance and zero feedback resistance. The blue curve shows distortion including the 10kΩ source impedance, but the feedback is still 0Ω. The blue curve illustrates the problem with the nonlinear common mode impedance. The green curve shows what happens when you include the 10kΩ matching resistor in the feedback. In the case of the green curve all of the high frequency distortion has been canceled by the common mode rejection of the op amp. However, we do have the additional noise of the 10kΩ resistor, and that is why the green curve is shifted by about 1dB.

Improving Performance

- Best Performance: dielectrically isolated JFET-Input
 - Absolute best:
 - OPA827, OPAx140/x141/164x
 - Very good: “DiFET” op amps: OPA2107, OPA627, etc.

More information:

“Distortion and Source Impedance in JFET Input Op Amps” –Caldwell, 4Q2014AAJ



To minimize noise, part count, or for stability reasons, you may not want to include the matching feedback resistor. Also, in many cases you don't precisely know the source impedance or the source impedance may be varying, so it is not practical to match the source impedance. In this case, a way to improve performance is to use a modern JFET op amp from TI, which would be on a dielectrically isolated process, or to use a Burr-Brown DiFET input op amps. The plot shown here is an OPA1641 with a zero ohm source resistance shown in red, and a 10kΩ source resistance shown in blue. These op amps have in extremely stable input impedance, so the addition of source impedance does not drastically effect the distortion. If you would like to know more about this subject, including some details on the process level, the AAJ paper “Distortion and Source Impedance” by John Caldwell is a good resource.

Rules for Minimizing Input Stage Distortion

- Minimize Op Amp Input Differential Voltage (V_{DIFF})
 - Reduce output voltage (not usually an option)
 - Reduce gain (may not be an option)
 - Maximize A_{OL}
 - High supply voltages
 - Select parts with proper GBW
- Prevent Input Crossover Distortion
 - Observe input CM voltage range in datasheet
 - Use inverting amplifier topology
 - Use zero-crossover distortion op amps: OPA320, OPA322, OPA365
- Prevent Common-Mode Impedance Effects
 - Use inverting amplifier topology
 - For non-inverting amplifiers match impedances at both op amp inputs
 - Select parts with dielectrically isolated JFET inputs:
 - OPAx140/x141/164x, OPA827, BB DiFET OPAs (OPA627, OPA2107, etc)

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This concludes the section on input stage distortion of op amps. In summary, there are several rules that can be followed to minimize input stage distortion. First, we need to minimize our input differential voltage. This can be done by minimizing the output signal amplitude, but this is usually not practical as the end application normally requires a specific amplitude. Another approach would be to reduce the gain. This may or may not be an option depending on the application. In some cases, we might be able to partition our gain into multiple amplifier sections. Perhaps the most practical method is to maximize the open loop gain of the op amp. That means operating the amplifier at the highest specified supply voltage. Operating devices at low supply voltages will degrade A_{OL} . Also, select parts with the proper gain bandwidth for your application. Consider both the open loop gain and the gain bandwidth product. Many engineers make the mistake of assuming that because an op amp has a large gain bandwidth product, that it must have high open loop gain at the frequencies that they care about. But some op amps sacrifice open loop gain in the pursuit of wider bandwidth. Comparing a very high speed op amp to a precision op amp, at audio frequencies for example, the precision amplifier may have higher open loop gain at low frequencies.

Next, prevent input crossover distortion. Observe the common mode voltage range and avoided entering the crossover region if possible. Alternatively, use an inverting amplifier topology which keeps the amplifiers inputs at a fixed common mode voltage. Unfortunately, most inverting amplifier topologies have a low input impedance, so this may not be practical for your application. Or you

can use zero-crossover distortion amplifiers. These op amps have a charge pump on the input stage to prevent the crossover distortion effects.

Finally, prevent the effects of common mode impedance variation. Again, we can use the inverting topology. For non-inverting amplifiers, you can match the impedance on the inverting and non-inverting inputs. Also, we can use amplifiers with dielectrically isolated JFET inputs.

Thanks for your time! Please try the quiz.

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In summary, we explained the sources of input stage distortion. Also, we learned some methods for minimizing this distortion..

Stay tuned for the next video which discusses details on output distortion sources.

Thank you for time! Please try the quiz to check your understanding of this video's content.