

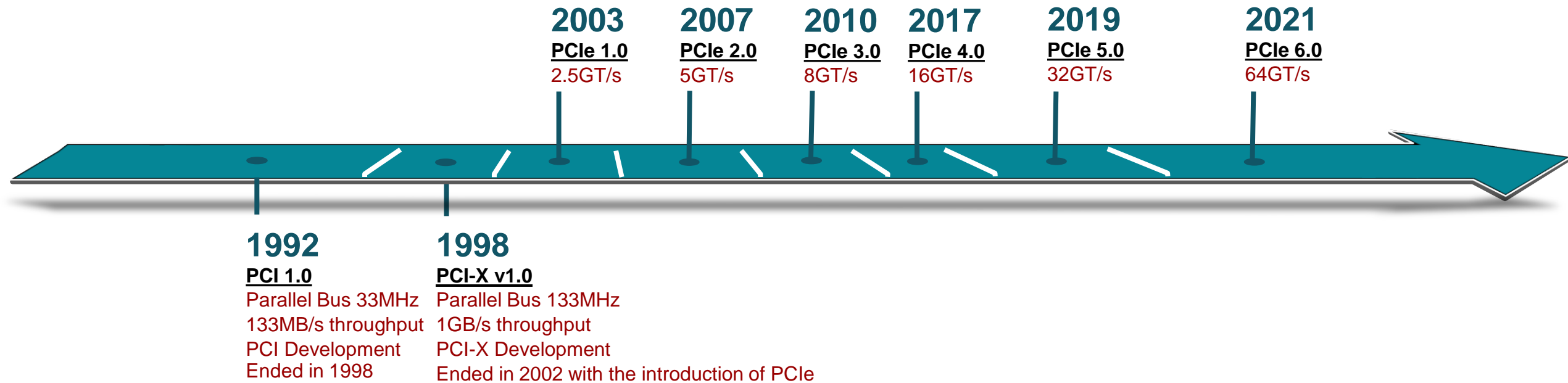
# What is PCIe?

TI Precision Labs – PCIe

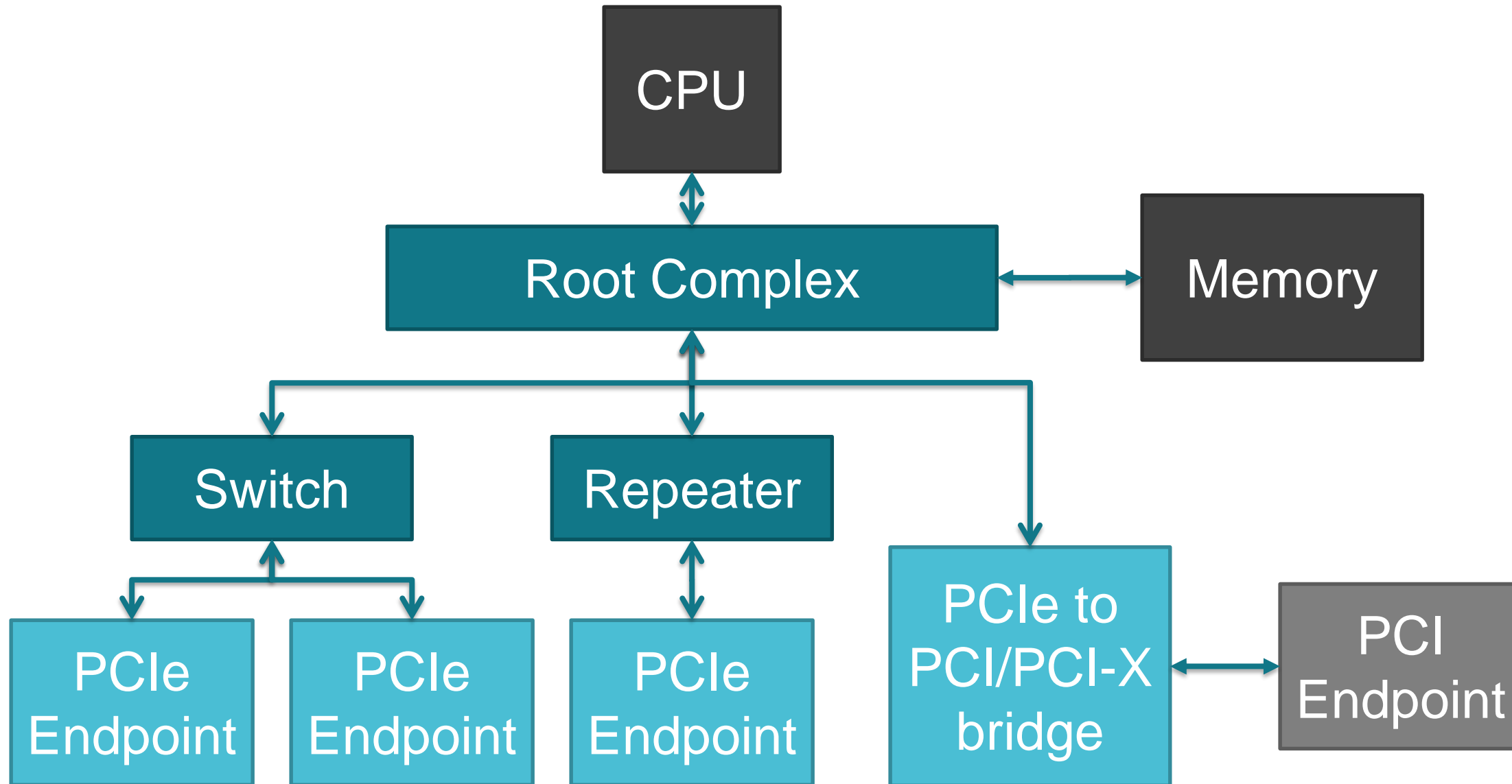
Presented by Nicholas Malone

# What is PCIe?

## Peripheral Component Interconnect Express



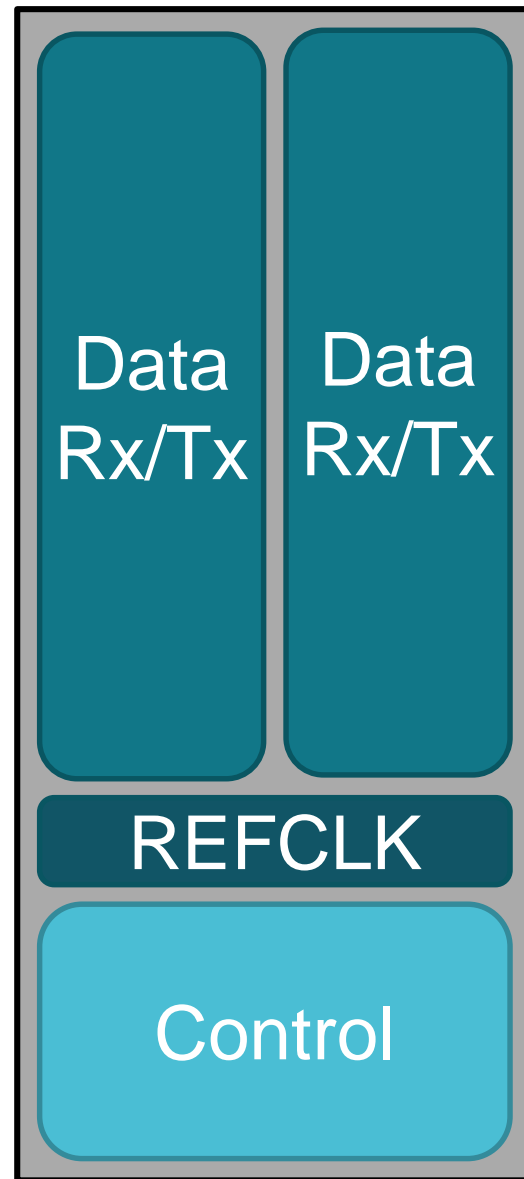
# PCIe topology



# PCIe components



Root Complex

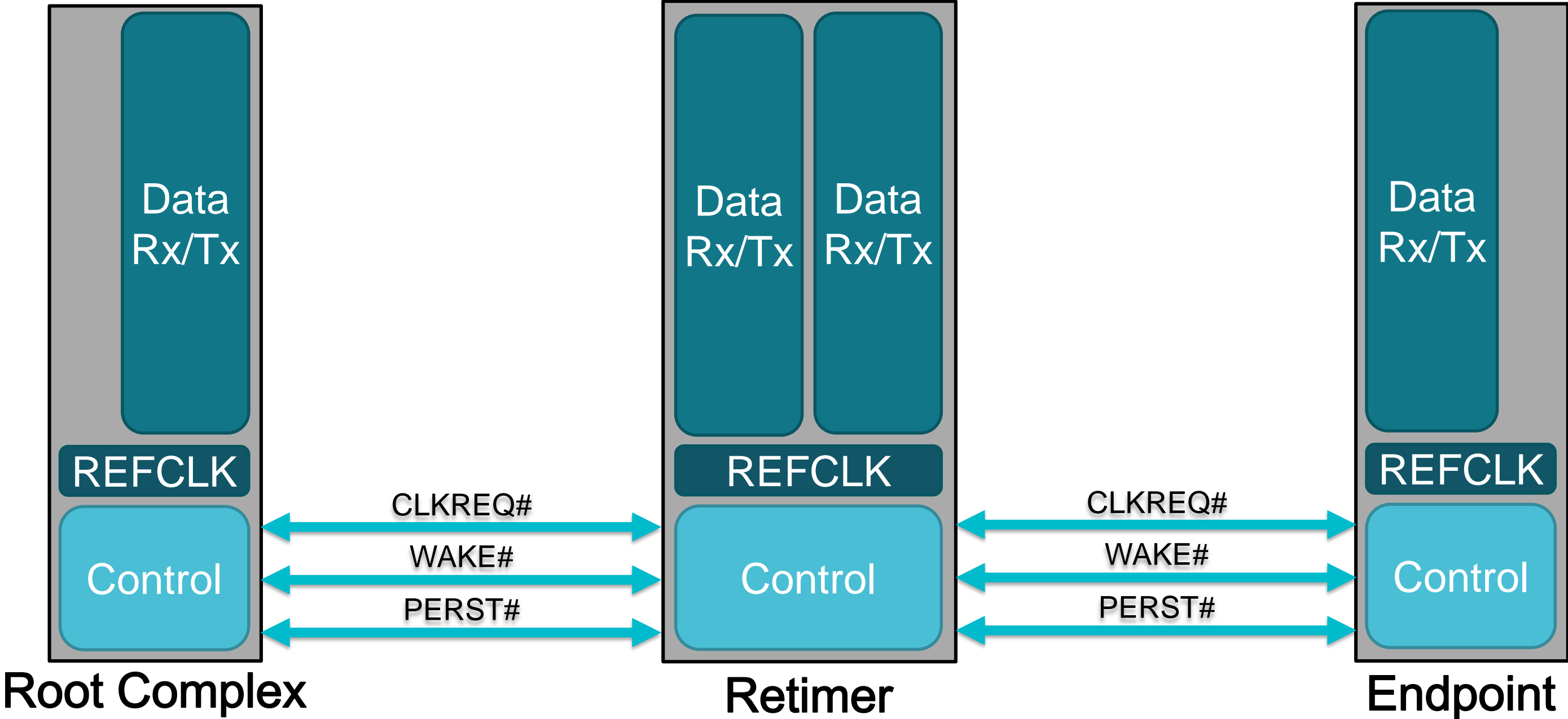


Repeater

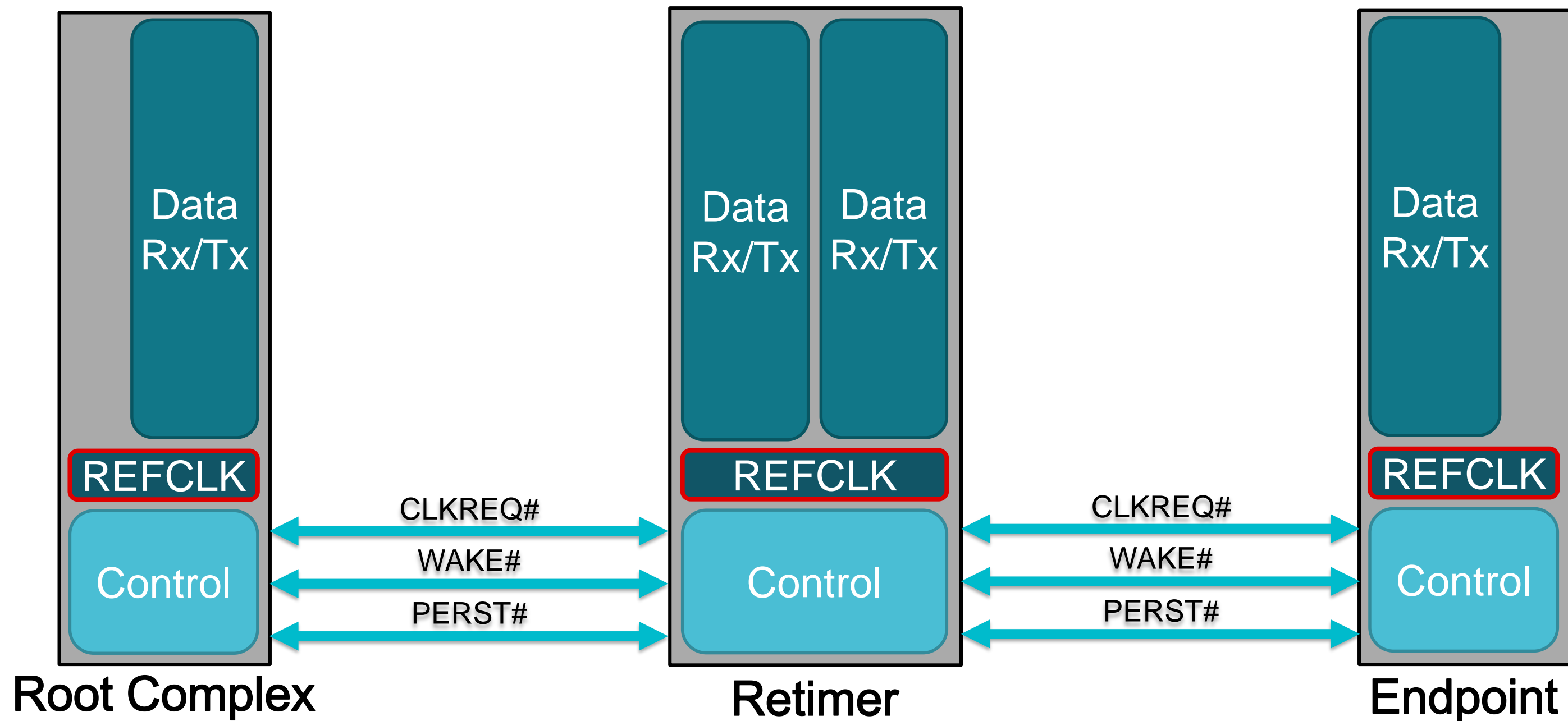


Endpoint

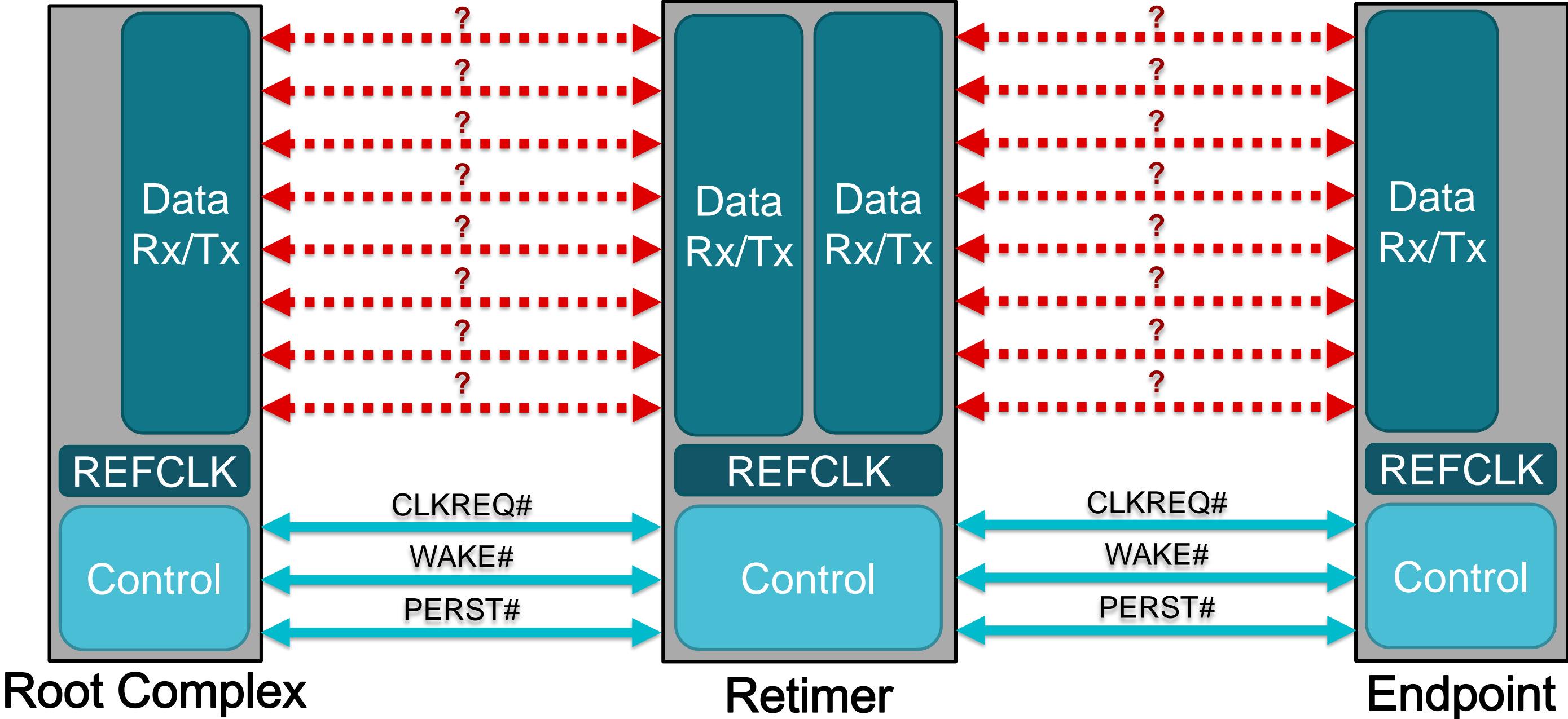
# PCIe signaling – control



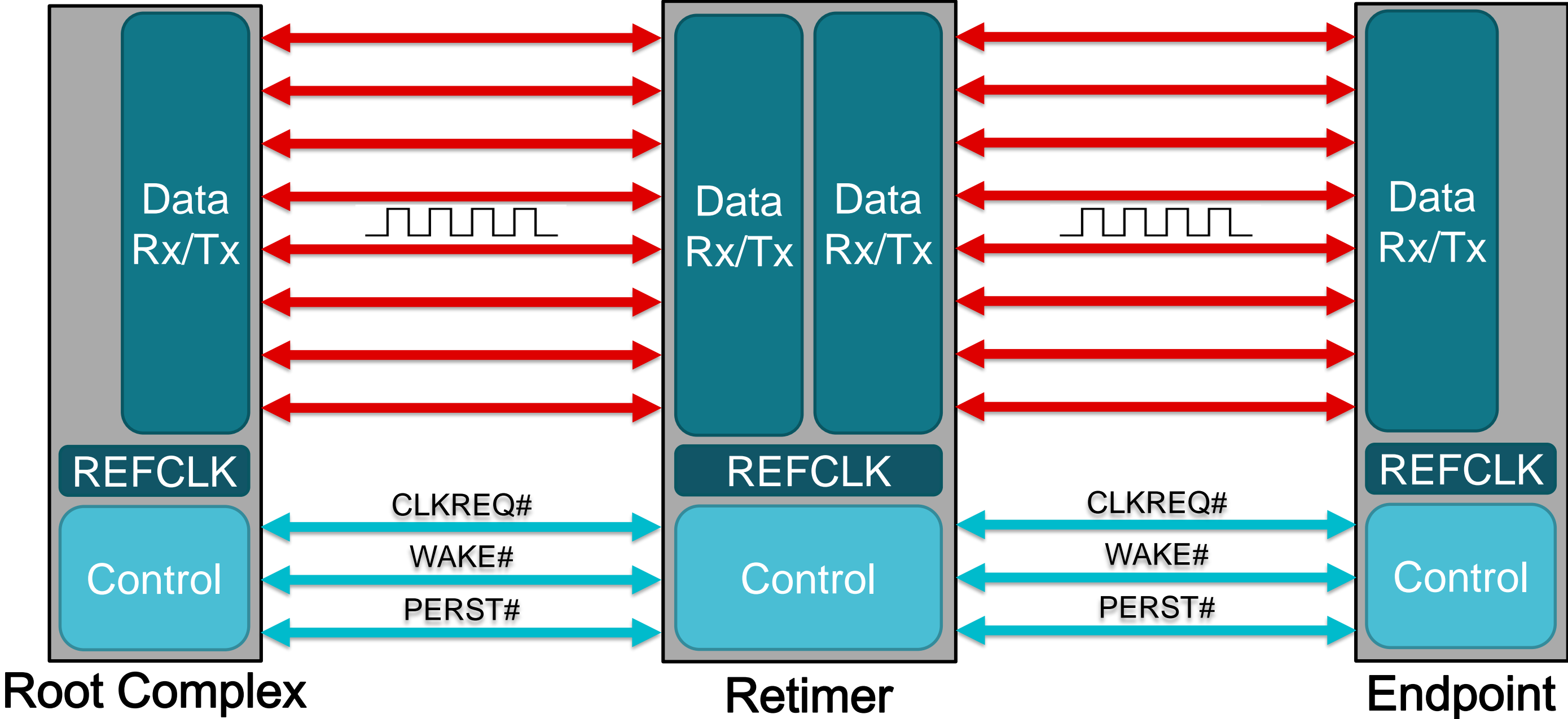
# PCIe signaling – reference clock



# PCIe link initialization – rx detect

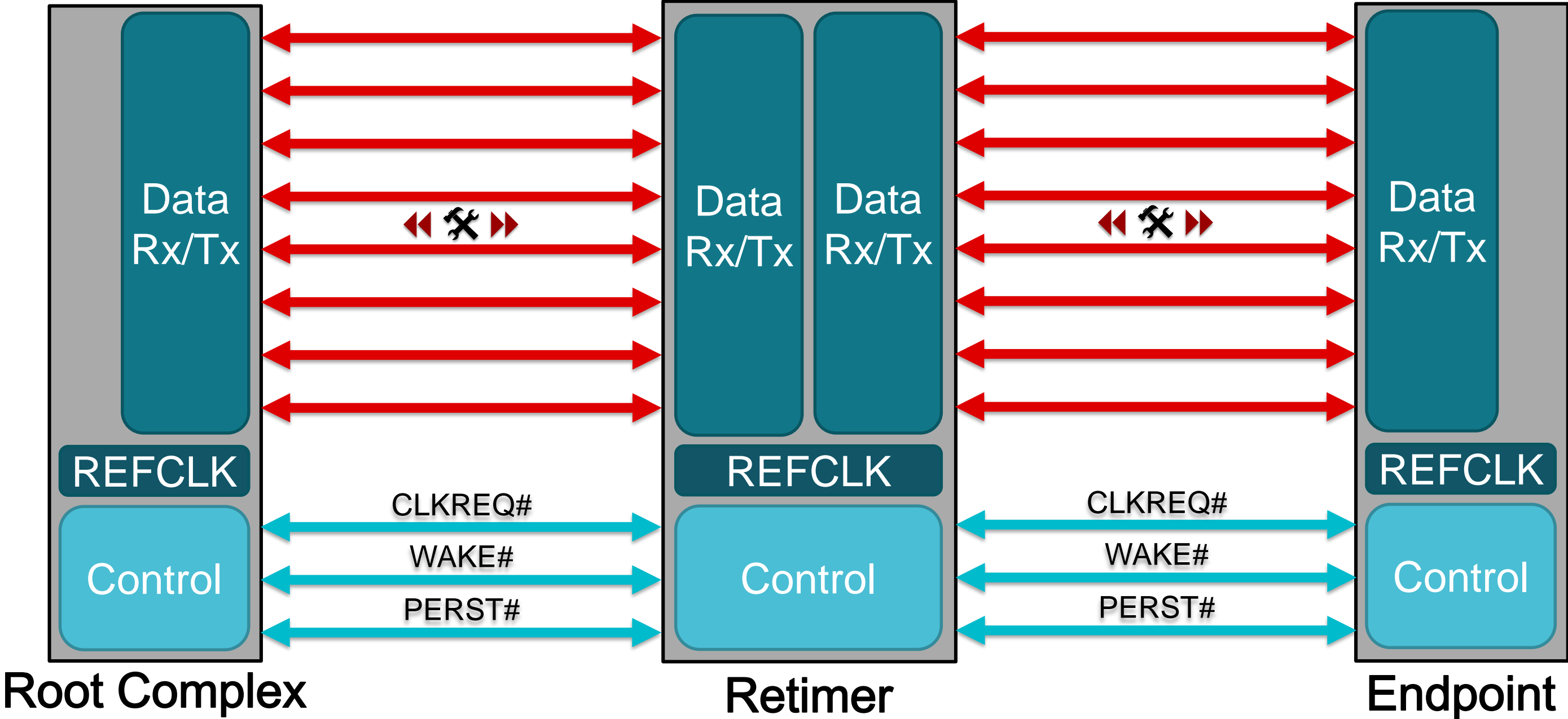


# PCIe link initialization – polling

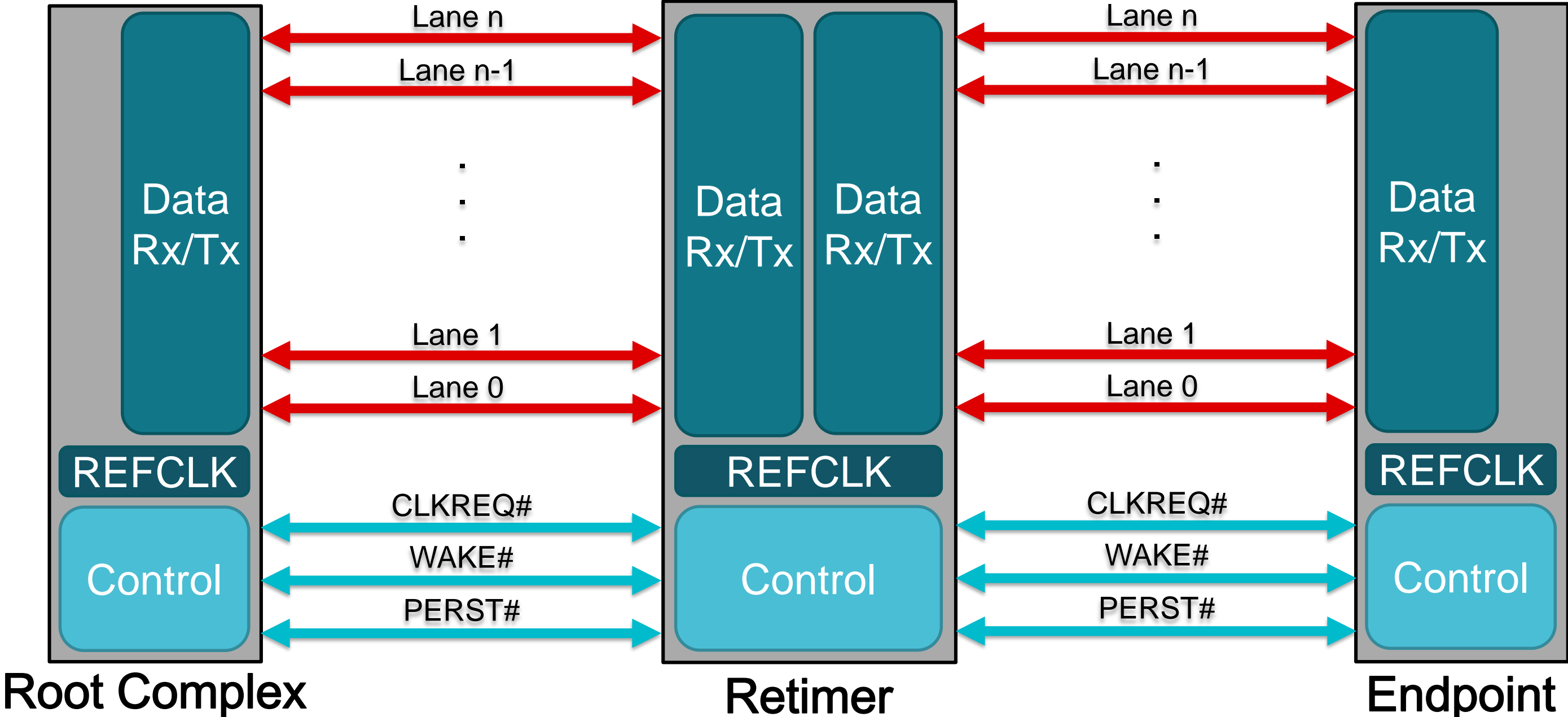




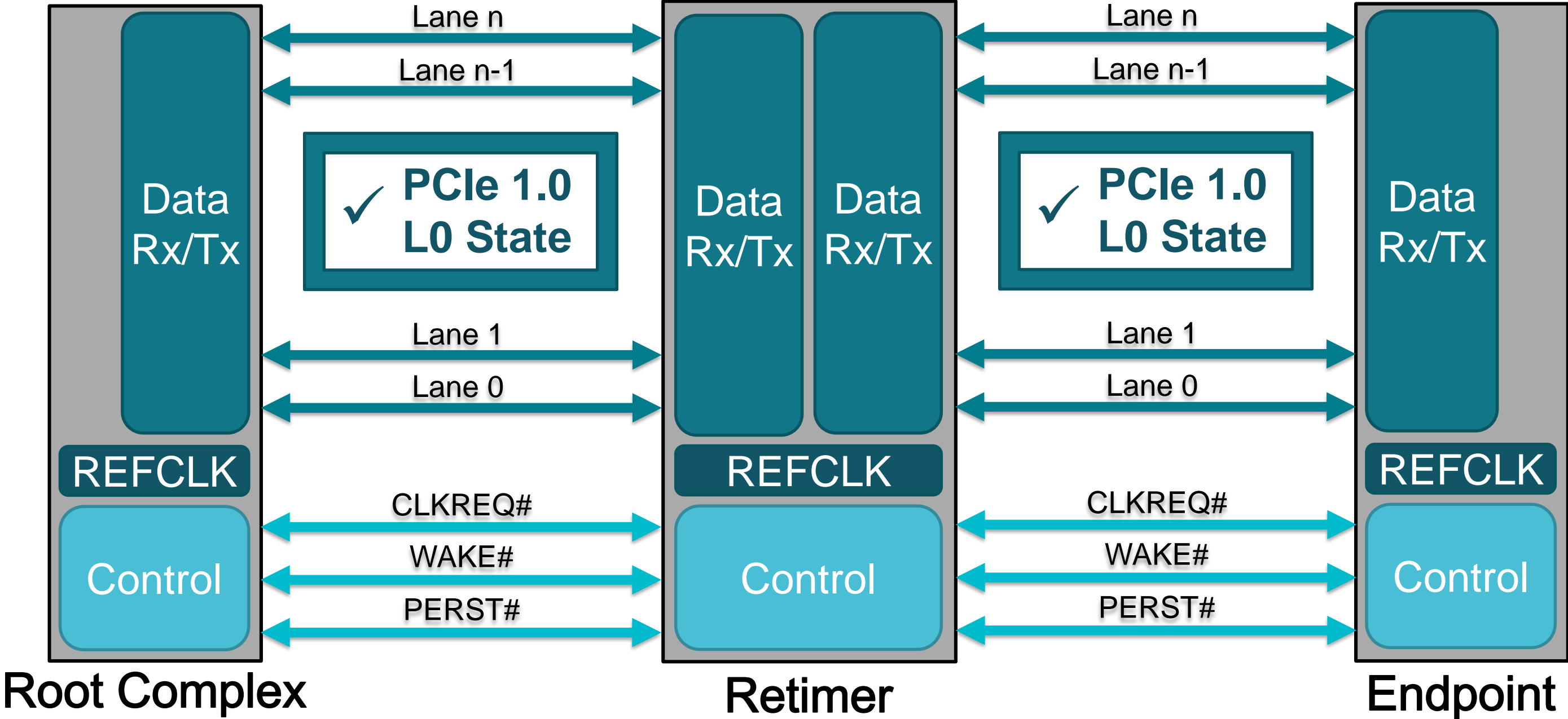
# PCIe link training – configuration



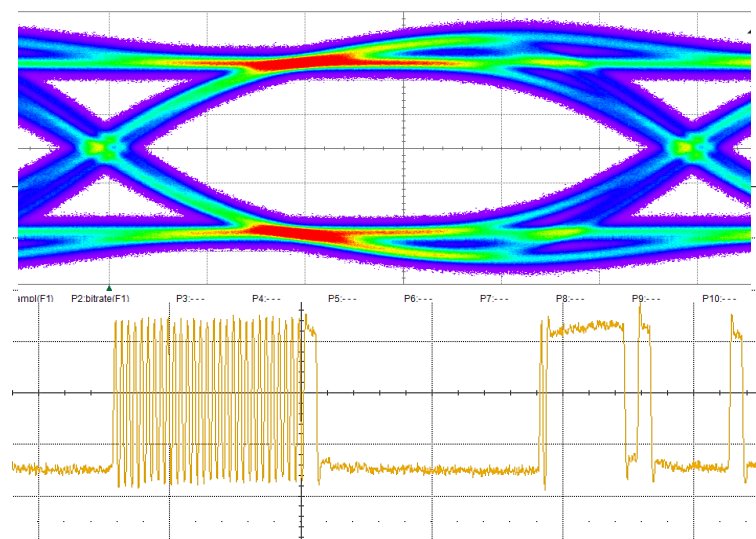
# PCIe link training – configuration



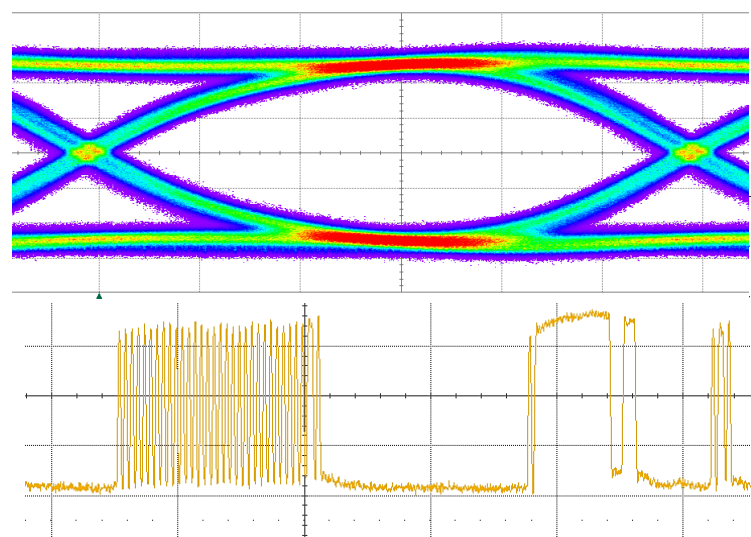
# PCIe communication – gen1



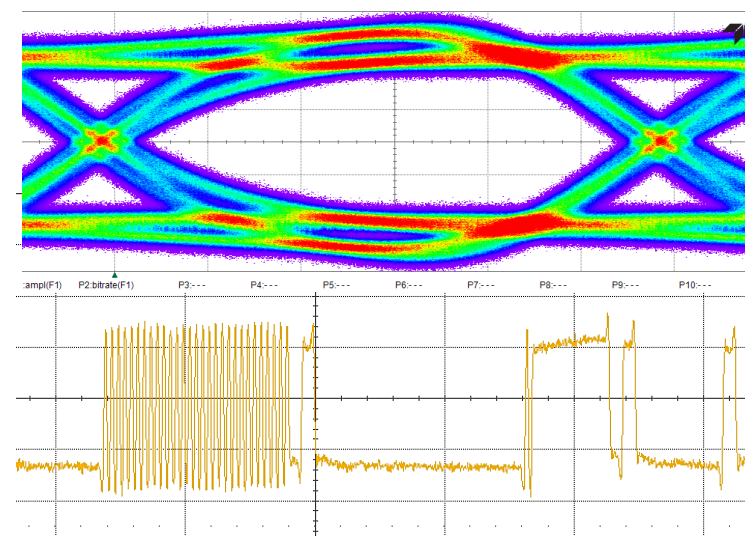
# PCIe link equalization – presets



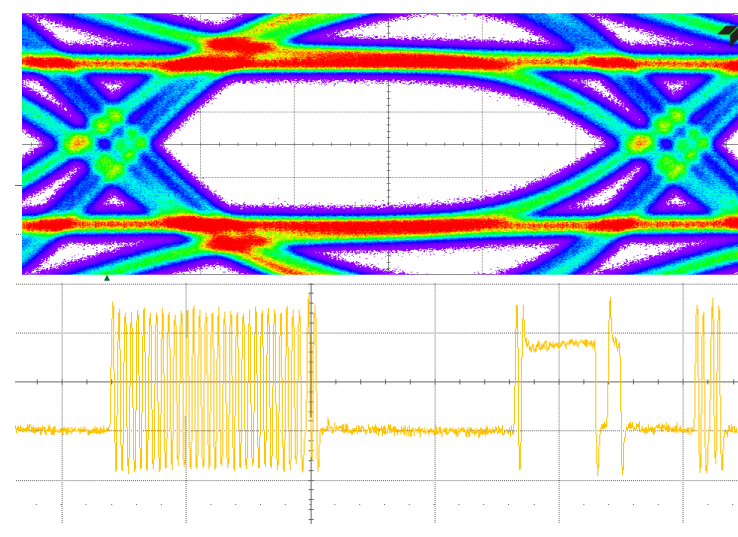
**Preset 0**



**Preset 2**

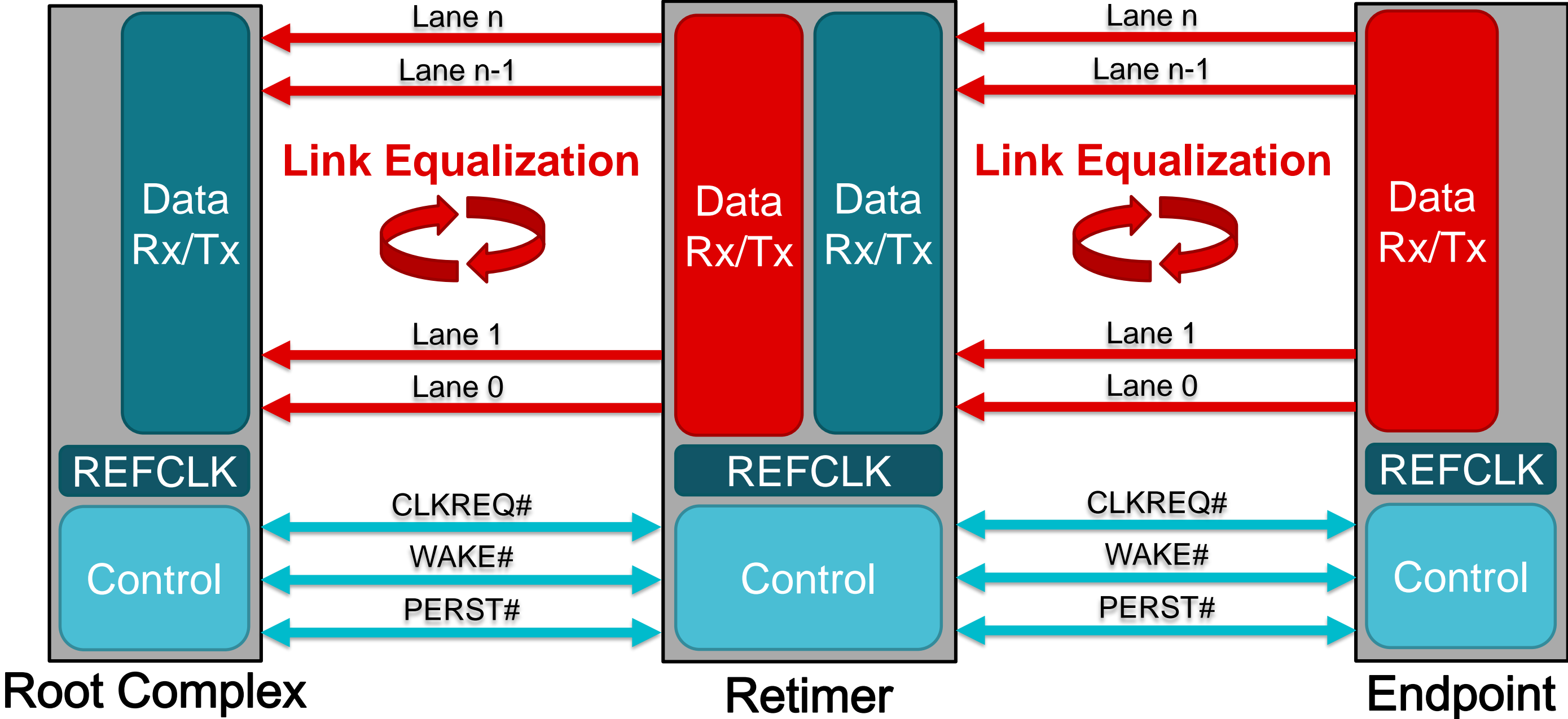


**Preset 7**

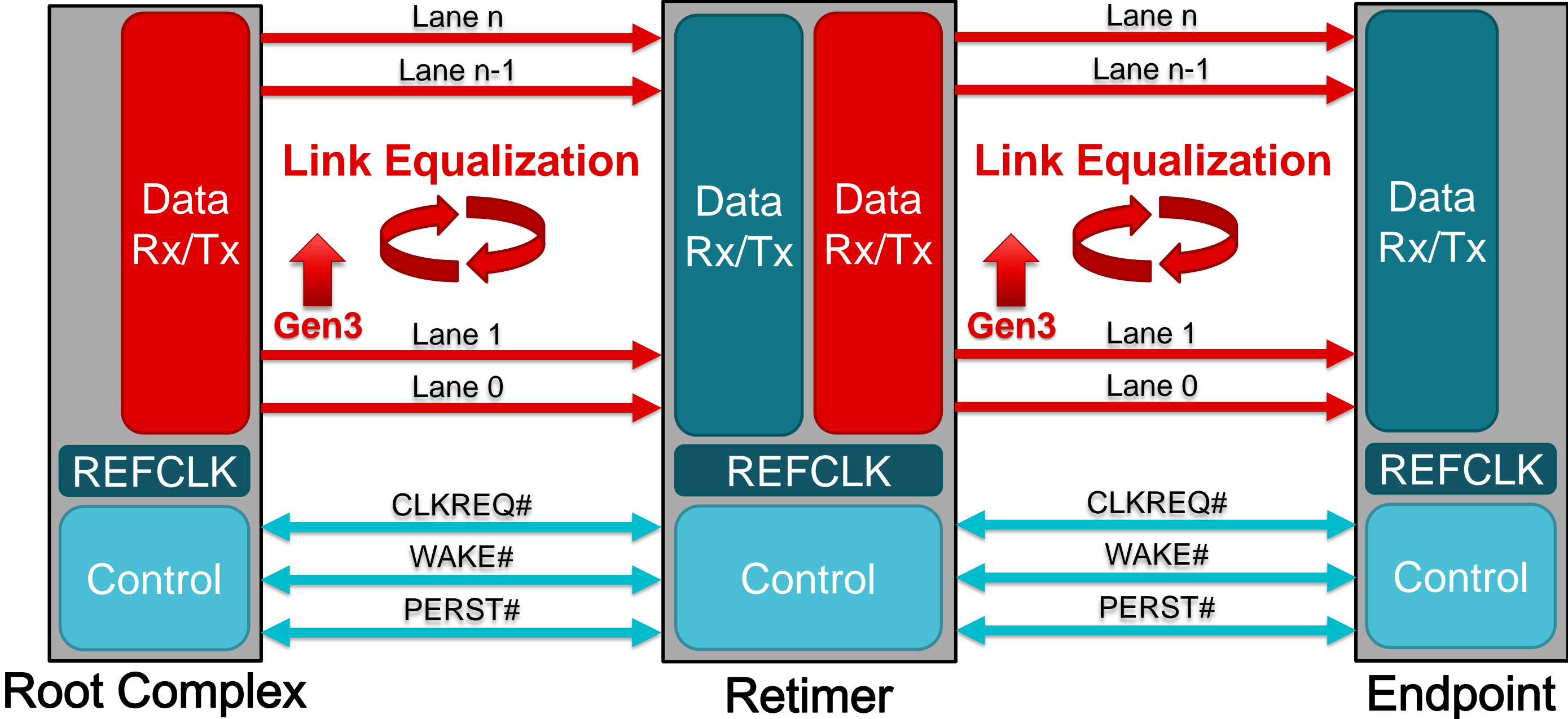


**Preset 10**

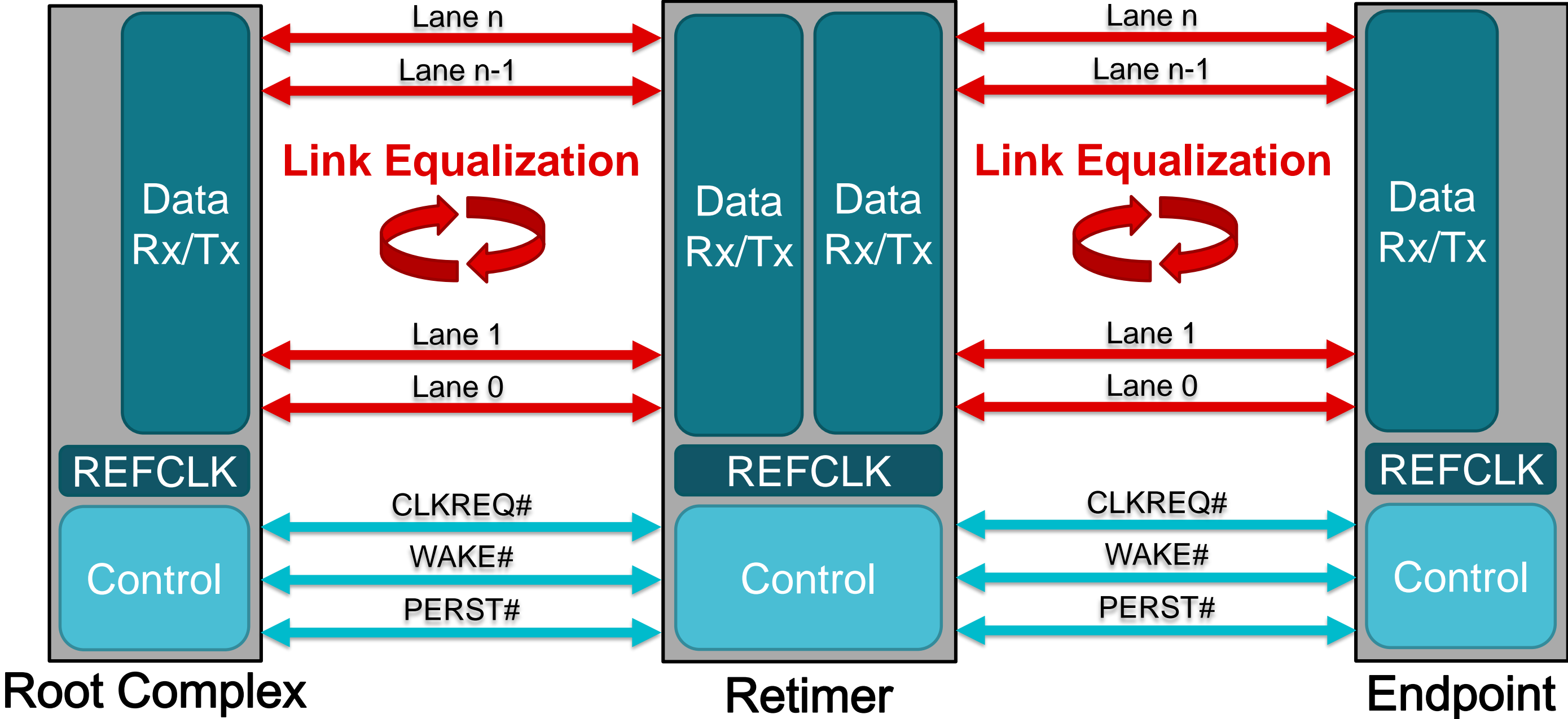
# PCIe link equalization – phase 0



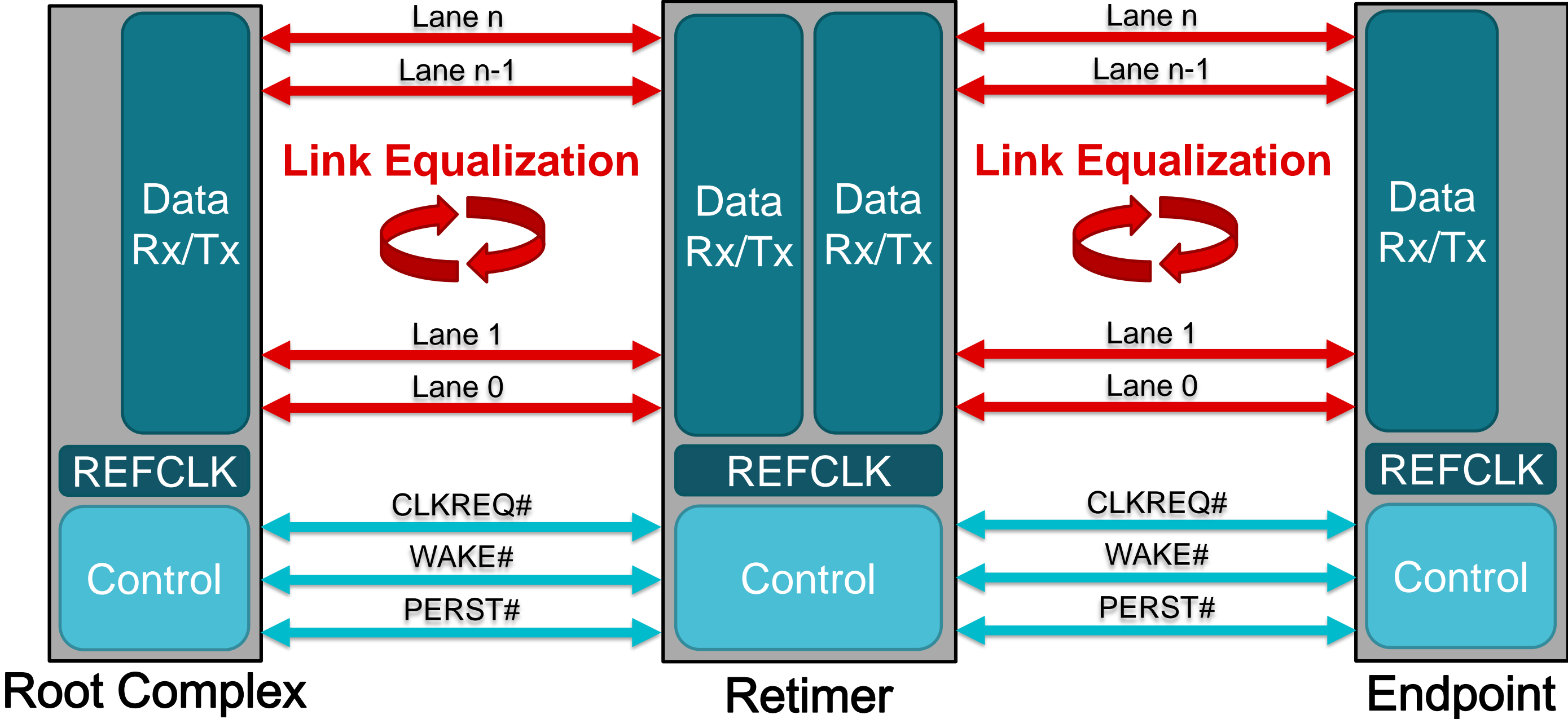
# PCIe link equalization – phase 0



# PCIe link equalization – phase 1

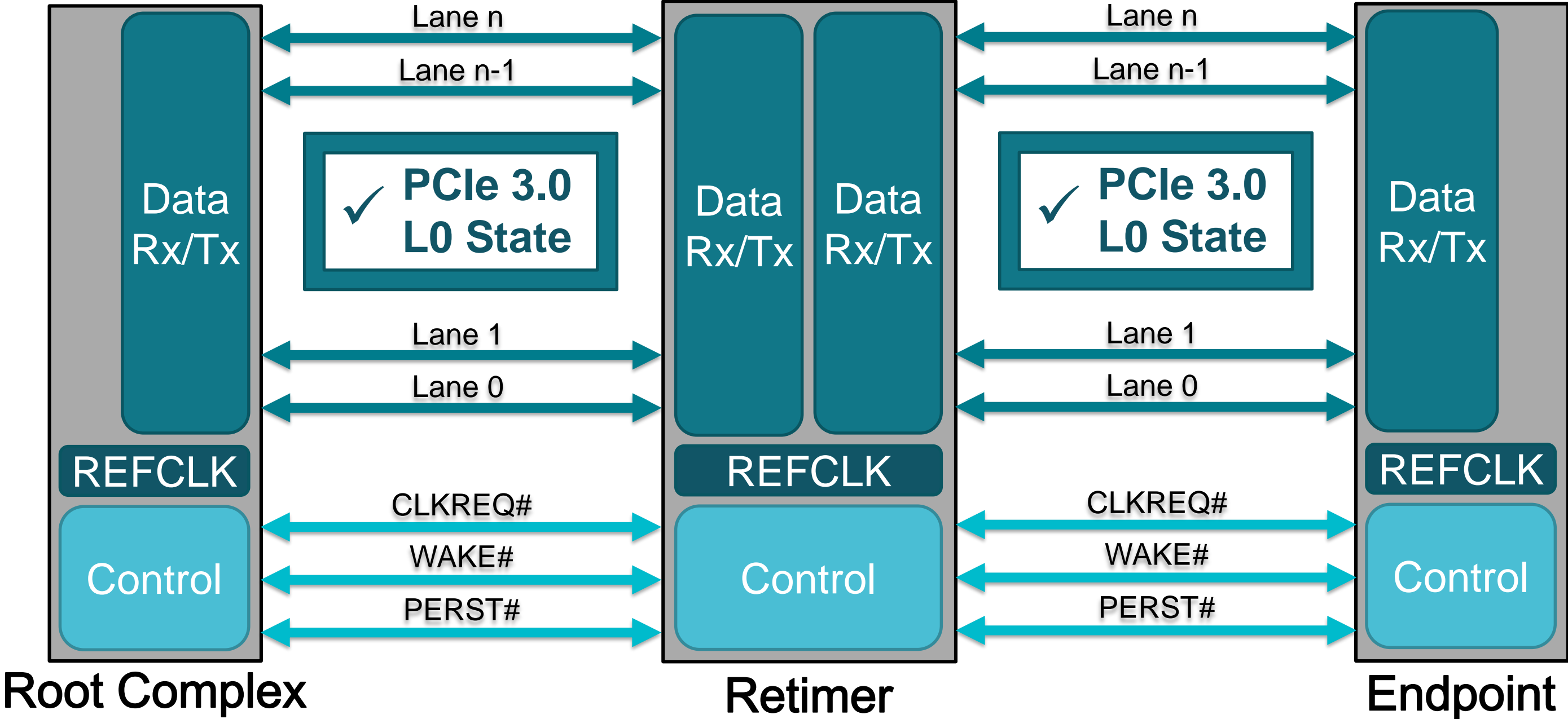


# PCIe link equalization – phase 2 and 3



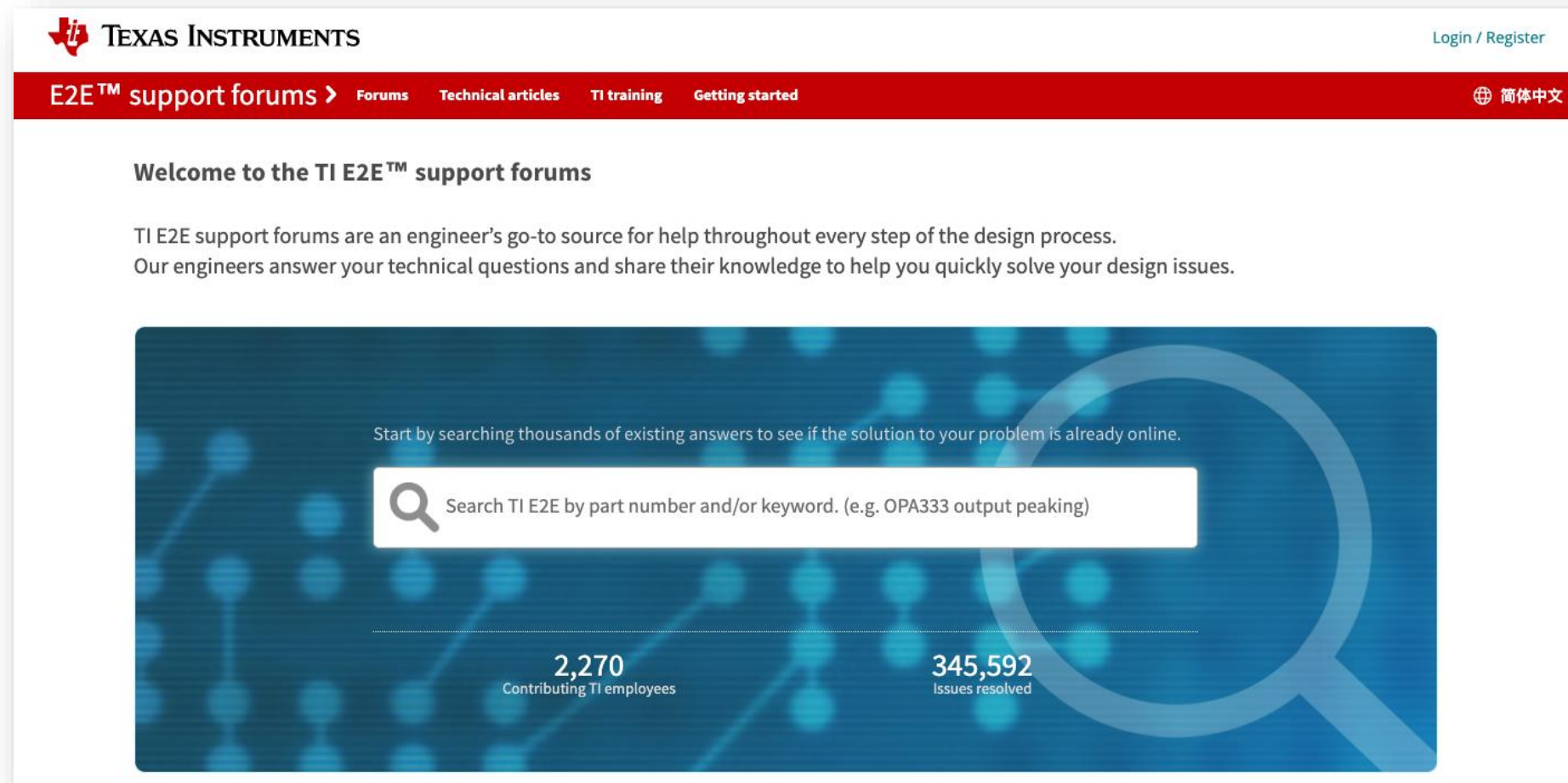


# PCIe communication – gen3



# Thank you

- [TI Precision Labs - What is a Signal Conditioner?](#)



The screenshot shows the TI E2E support forums homepage. At the top left is the Texas Instruments logo. To the right of the logo is the text "TEXAS INSTRUMENTS". In the top right corner, there is a link for "Login / Register". Below the logo is a red navigation bar with the text "E2E™ support forums > Forums Technical articles TI training Getting started". To the right of this bar is a globe icon and the text "简体中文". The main content area has a heading "Welcome to the TI E2E™ support forums" followed by a paragraph: "TI E2E support forums are an engineer's go-to source for help throughout every step of the design process. Our engineers answer your technical questions and share their knowledge to help you quickly solve your design issues." Below this is a large blue banner with a search bar. The search bar contains the text "Search TI E2E by part number and/or keyword. (e.g. OPA333 output peaking)". Below the search bar are two statistics: "2,270 Contributing TI employees" and "345,592 Issues resolved".



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# Quiz

- What describes the function of the PERST# signal in a PCIe link?
  - a) A low pulse on this signal will begin a transition to a low power state.
  - b) A transition from low to high will indicate that power rails are stable and link initialization is ready to begin.
  - c) This signal, held low, will cause the PCIe link to transition into a recovery state.
  - d) This is used to request a clock from the upstream port.

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  - d) This is used to request a clock from the upstream port.

b) A transition from low to high on the PERST# line indicates that the PCIe power rails are stable and that link initialization should begin.

# Quiz

- What is the first step in the PCIe link initialization process?
  - a) Receiver Detect
  - b) Configuration
  - c) Polling
  - d) Link Equalization

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a) Before transmission can begin, the receiver detect circuit in a PCIe device must first confirm that there is a link partner to pair with.

# Quiz

- What is the term for a large PCIe link split into multiple smaller links?
  - a) Segmented
  - b) Bifurcated
  - c) Split
  - d) Reduced Link



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b) A bifurcated PCIe link refers to a larger PCIe link split into multiple smaller links. For example, a 16 lane PCIe link can be divided into 4 links 4 lanes wide.

# Quiz

- At what PCIe data rate(s) does link initialization include a link equalization step?
  - a) PCIe Gen 4
  - b) PCIe Gen 1
  - c) PCIe Gen 3
  - d) PCIe Gen 5

# Quiz

- At what PCIe data rate(s) does link initialization include a link equalization step?

a) PCIe Gen 4

b) PCIe Gen 1

c) PCIe Gen 3

d) PCIe Gen 5

a, c, and d) Link EQ is a required link training step for PCIe communication above Gen3 data rates.

# Quiz

- What is “normal” state for PCIe link that sends and processes packets?
  - a) Loopback
  - b) L0
  - c) L2
  - d) Forwarding

# Quiz

- What is “normal” state for PCIe link that sends and processes packets?
  - a) Loopback
  - b) L0
  - c) L2
  - d) Forwarding

b) L0 describes a PCIe link that is active and able to send on process packets regularly.



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