Op Amp PCB Layout – Trace Parasitic Effects

TI Precision Labs – Op Amps

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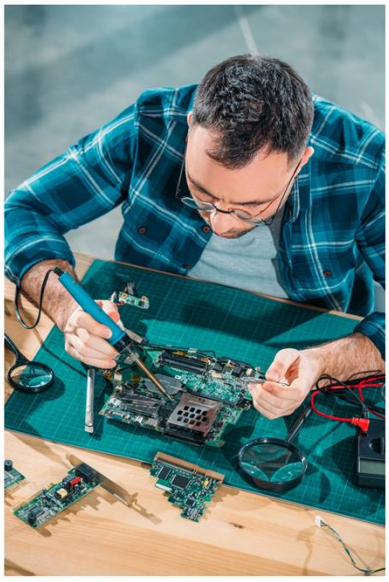
Hello and welcome to the TI precision labs series on PCB layout techniques for op amps. In this lecture, we'll give an introduction to op amp layouts and discuss some of the parasitic effects associated with PCB traces and how to deal with them.

Op amp layout is important



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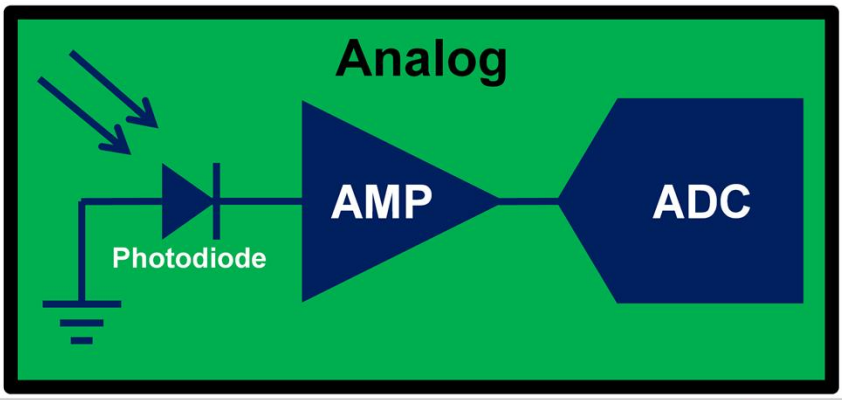
When it comes to analog circuits, the layout phase following the schematic design can feel like an afterthought. Even worse, the temptation to skip the board prototype stage altogether can be strong, especially when deadlines are tight. But it is important to remember that a non-ideal layout can have disastrous consequences for a project and offset many hours of careful circuit design. So it is well worth the time to review good layout techniques and verify one's design with prototypes.

What we will cover

1. Use short traces
2. Avoid parallel traces
3. Avoid capacitance on inverting input



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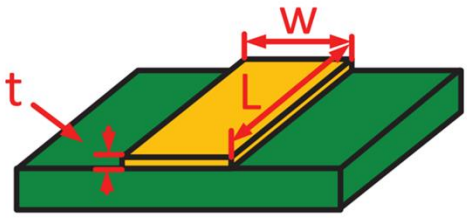
Proper op amp layouts involve many best practices. Fortunately, a lot of these concepts overlap with the more general techniques used in analog board layouts. So learning one typically reinforces the other. In this presentation, we will review the importance of short traces and the reduction of associated parasitic impedances. Then, we'll discuss parallel traces and their potential issues. Finally, we'll cover the sensitivity of the path from the op amp's inverting input to its output node. This is a topic that is particular to op amp layouts and not analog layouts in general. For each technique, we will also examine at least one example layout to see how the theory can be applied in practice.

Use short traces

Analog Engineer's Pocket Reference Guide

1. Avoid parasitic impedance
2. Widen traces for better current-carrying capability



$$R = \rho \frac{L}{t \times W}[1 + \alpha(T - 25°\text{C})]$$

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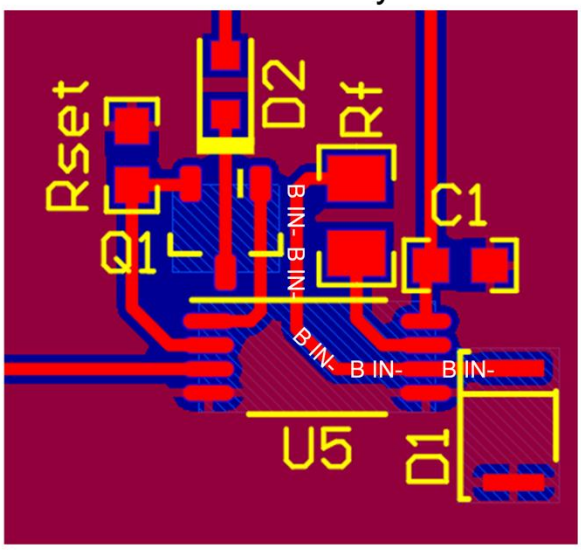
The first piece of advice for op amp layouts is that traces should be kept as short as possible. Longer traces can introduce unwanted parasitic resistance, capacitance, and inductance. These effects are usually undesired and may have negative consequences for signal integrity. Widening a trace will reduce the parasitic resistance, though it may come at the cost of increased parasitic capacitance if there is a trace or metallic pour on an adjacent layer. We'll cover the formulas for parasitic capacitance later in this presentation. For now, note that traces are generally made wider when they are expected to carry greater levels of current.

For PCB traces, the associated parasitic resistance is given by the formula $R = \rho \frac{L}{t \times W}[1 + \alpha(T - 25°\text{C})]$ where "R" is the total resistance, "ρ" is the resistivity of the metal trace, "L" and "W" are the length and width of the trace in that order, "t" is the thickness of the trace, "α" is the temperature coefficient of the trace, and "T" is the temperature in Celsius.

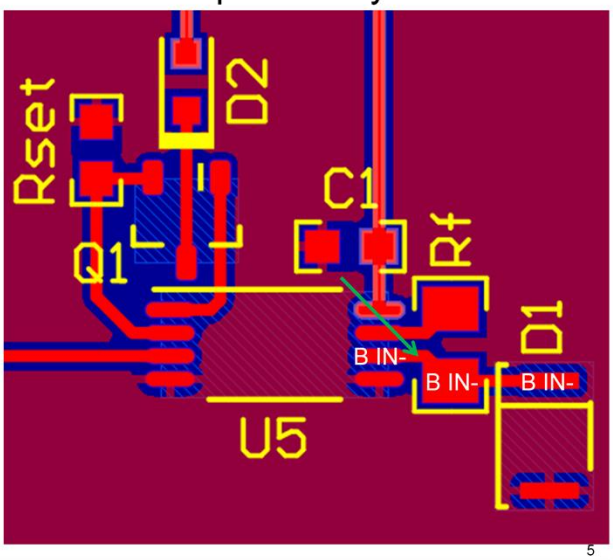
For this and other helpful PCB formulas, check out the online version of TI's Analog Engineer's Pocket Reference Guide.

Use short traces – Example 1

Problematic layout



Improved layout



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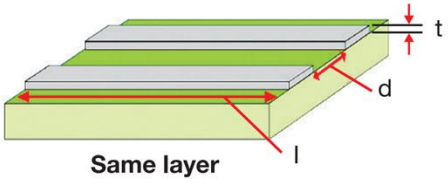
Let's now take a look at a simple example. On the left, there is an 8-pin, dual channel op amp. The area in red is the top metal layer and the area in blue is the bottom metal layer. The purple area shows where these layers overlap with a ground plane on both the first and second layer. The inverting input node of channel B is noted as "B IN-". Can you spot a potential issue here? You may have noticed that this trace is noticeably longer than the other traces and is introducing parasitic impedance into the circuit. Depending on the circuit and the node involved, this may or may not significantly affect the performance of the circuit. However, the inverting input is usually thought of as a sensitive node. So, it's a good idea to shorten this trace if at all possible.

On the right, you can see that the issue of the long trace can be resolved by repositioning the "Rf" component such that the trace now has a shorter path to its pin.

Analog Engineer's Pocket Reference Guide

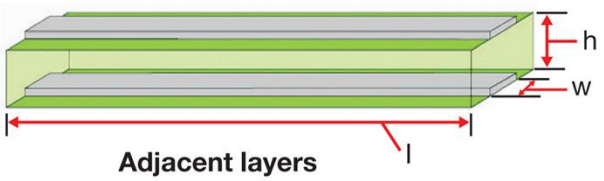
Avoid parallel traces

1. Parallel traces can lead to parasitic capacitance
2. Traces can also be parallel to planes
3. Parallel traces may contribute to inductive coupling



Same layer

$$C = \frac{k \times t \times l}{d}$$



Adjacent layers

$$C = \frac{k \times \varepsilon_r \times w \times l}{h}$$

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Another important layout technique is to avoid parallel traces when possible. Remember that traces on a PCB are metallic and parallel metallic plates with an insulator in between form a capacitor. So when two traces run in parallel, either on the same plane or on adjacent planes, they create a parasitic capacitance. This can lead to the unwanted coupling of signals from one trace into another.

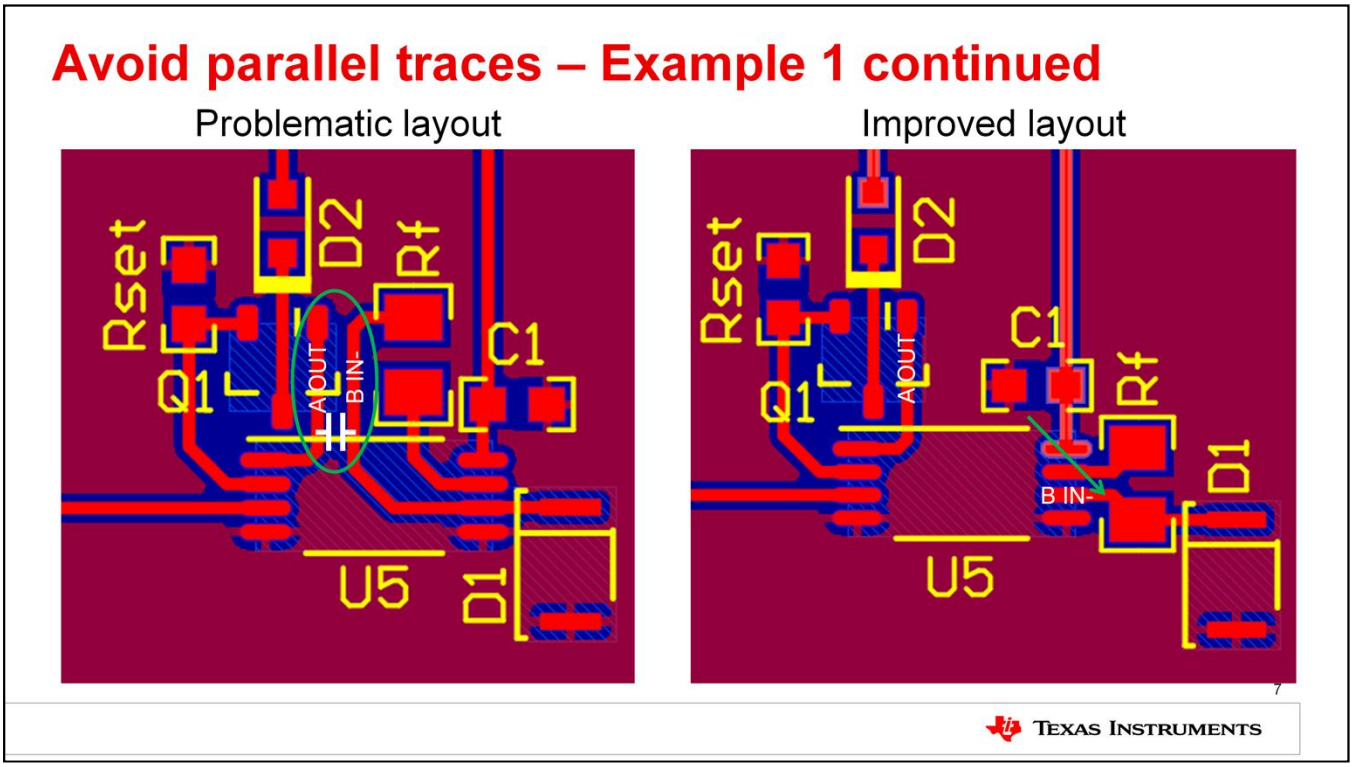
For parallel traces on the same layer, the associated parasitic capacitance is given by the formula $C = \frac{k \times t \times l}{d}$ where "C" is the total capacitance, "k" is the permittivity of free space, "t" and "l" are the thickness and length of the traces, respectively, and d is the distance between the near edges of the traces. Similarly, when two traces are on adjacent layers they form a capacitance described by the formula $C = \frac{k \times \varepsilon_r \times w \times l}{h}$, in which "C" is the total capacitance, "k" is the permittivity of free space, "ε_r" is the dielectric constant of the insulating PCB material (often FR-4), "w" and "l" are the width and length of the traces, respectively, and h is the distance between the planes. These and other formulas on PCB parasitic effects can be found in the Analog Engineer's Pocket Reference Guide.

Similarly, a trace can form a parasitic capacitance with a parallel metallic layer pour on the same layer or on an adjacent layer. For example, if the layer below a signal path is a solid ground plane, then a parasitic capacitance can form from the signal path to ground. Oftentimes, this effect is negligible. But for very long traces or

sensitive nodes it can be an issue.

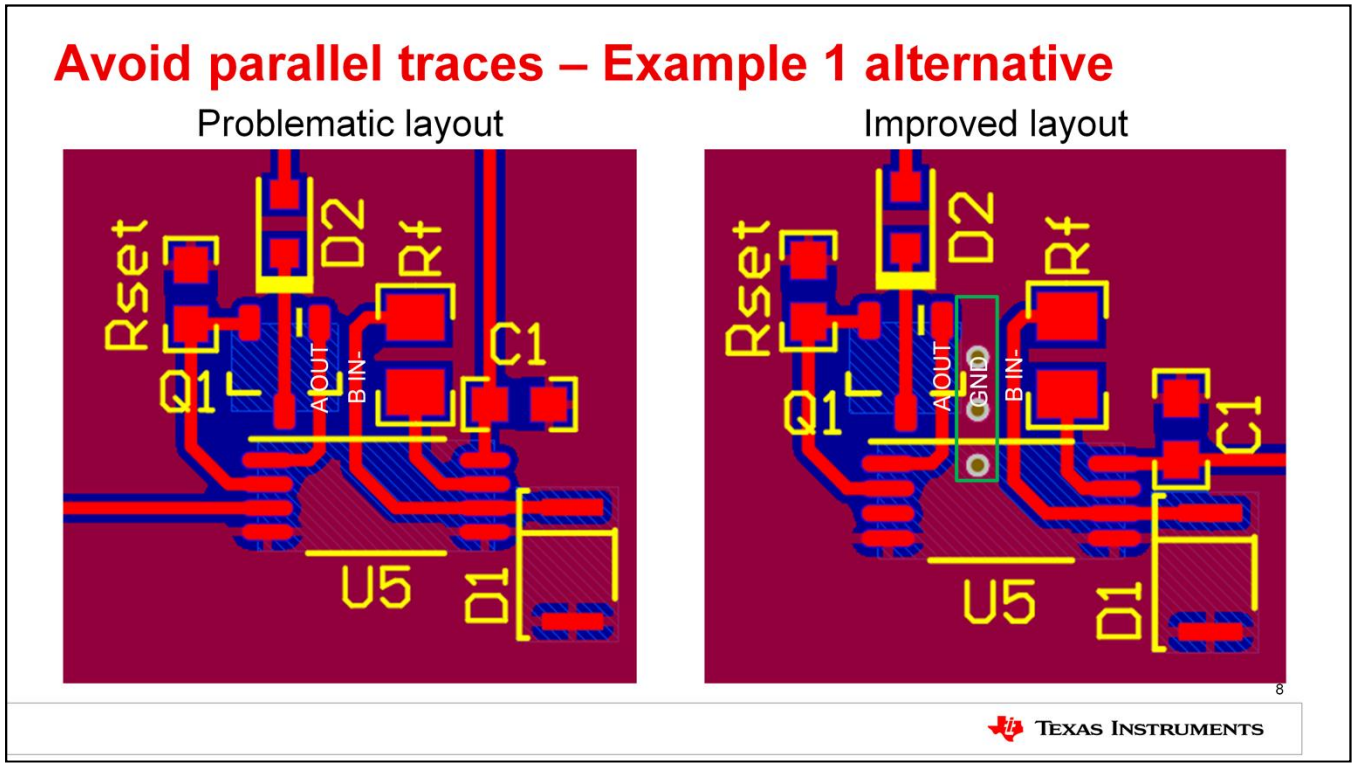
One more thing to note is that parallel traces can experience inductive coupling. A changing current in a wire generates a magnetic field and this magnetic field can in turn generate current in nearby conductive loops. This is a consequence of Faraday's Law and the effect is stronger when the distances involved are shorter meaning that parallel traces may be susceptible to this issue. Note that this is a greater concern with high speed signals. So you need to be careful and avoid placing analog traces near digital traces. This topic will be expanded upon in the presentation titled, "Op Amp PCB Layout – Grounding & Bypass."

Avoid parallel traces – Example 1 continued



Let's now revisit the first example. We initially noted that the inverting input of channel B, also known as the "summing node," has a long path. Knowing what we now know, there is the potential for an additional issue here. You may have noticed that the highlighted traces run in parallel. Since the traces are metallic, they act as capacitive plates and can allow unwanted signal coupling. This is generally bad for any two signals, but it is especially dangerous when the traces go to the IN- and output pins as we will cover in the next topic.

Just as the issue of the long IN- trace was solved by moving the Rf component, so too can it solve the problem of the A OUT and B IN- traces running in parallel.

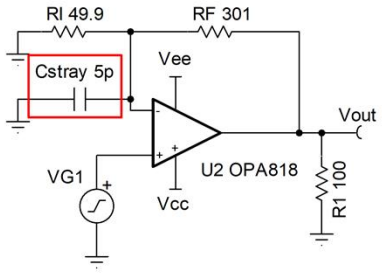


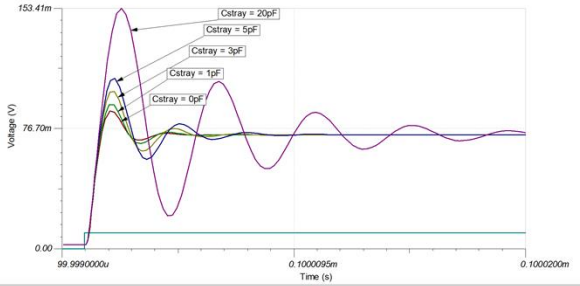
Unfortunately, it may not always be possible or practical to rearrange components in such a manner. Sometimes space constraints make such layout strategies difficult to implement. In cases where parallel traces are somewhat unavoidable, a different approach can be used. Here is an example of an alternative solution. First, the traces are separated as much as possible. Then, the ground pour on the top layer in red is permitted to run between the traces. The ground pour acts as a shield to prevent coupling between the signal traces.

For further protection, ground vias can also be placed here to ensure the voltage at this point of the ground plane is common to the voltage of the ground plane on the bottom layer in blue. Thus, for cases where parallel traces must be used, ground shielding with a ground plane and vias is a viable option.

Avoid capacitance on inverting input

1. Avoid parasitic capacitance
   1. Keep trace(s) to IN- short
   2. Avoid placing vias in this path
2. Place passive components close to the op amp
3. High speed amps are more sensitive and may require removing ground plane from below IN- pin





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As mentioned in the previous example, something that is special to op amp layouts is the importance of the IN- pin. The IN- pin, or the “summing node,” controls the negative feedback for the amplifier. If the signal in the feedback path encounters large impedances, then the phase of the feedback signal will shift excessively. This can be thought of as a delay in the signal path. As the effect becomes worse, the output will show longer and longer response times with greater overshoot. Eventually, the phase shift will be so poor that the amplifier’s feedback will become positive rather than negative and the output will begin to oscillate uncontrollably. This undesirable outcome is referred to as “instability” and is explained in much more detail in the TI Precision Labs series on op amp stability.

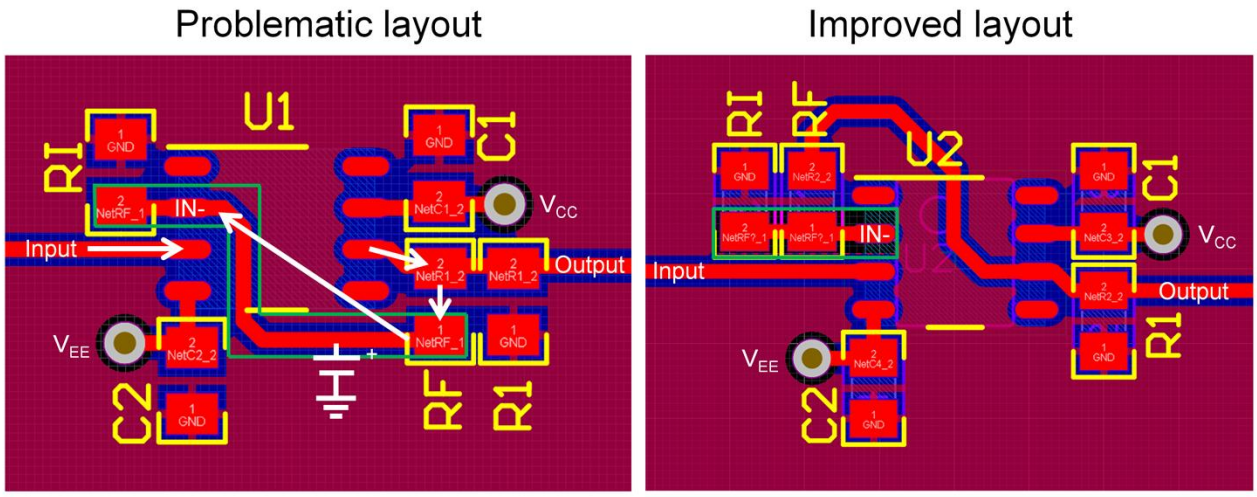
To prevent instability, it is important that the sensitive signal path from the OUT pin to the IN- pin be kept as clean of parasitic effects as possible. The output pin is generally capable of driving some load capacitance, while the input pin has a very low input capacitance by nature. Typically, the amplifier’s input capacitance is on the order of a few pF. So, the IN- pin is more sensitive than the output pin and it is especially important that the parasitic capacitance be kept off the inverting input.

To do this, keep traces to the IN- pin short and avoid placing vias along the path. Also, place any passive, discrete components close to the pin. If necessary, you may choose to remove the ground plane on layers below the IN- pin. Note that,

because of their wide bandwidth, high speed amplifiers are more susceptible to instability from parasitic impedance than most amplifiers.

On this slide, you can see how a small parasitic capacitance on the summing node can create a large overshoot response on the output. Please note, however, that the OPA818 has a very high bandwidth and most amplifiers will not be this sensitive. However, this is a good example to illustrate the importance of keeping this node clean.

Avoid capacitance on inverting input – Example 2



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Let's consider another example with an 8-pin, dual channel op amp. As can be seen, the input arrives from the left to the non-inverting input pin, or IN+, and the output is fed back to the inverting input pin, or IN-. Take a moment to look at the layout. Do you see any signs of potential trouble? You may have noticed that the path from pad 1 of the RF component to the IN- pin is relatively long. The path from OUT to IN- is sensitive and it is important to keep the traces into the IN- pin as short as possible. In this case, the metallic trace interacts with the metal ground plane on the bottom layer to form a capacitance from the trace to GND. This means there is a stray capacitance on the IN- pin. This parasitic capacitance will typically be on the order of pF and is less likely to be a problem on the output pin. However, the IN- pin will have a natural input capacitance on the order of a few pF. So a stray capacitance can be a significant addition. This can lead to stability problems, especially when designing with high-speed op amps.

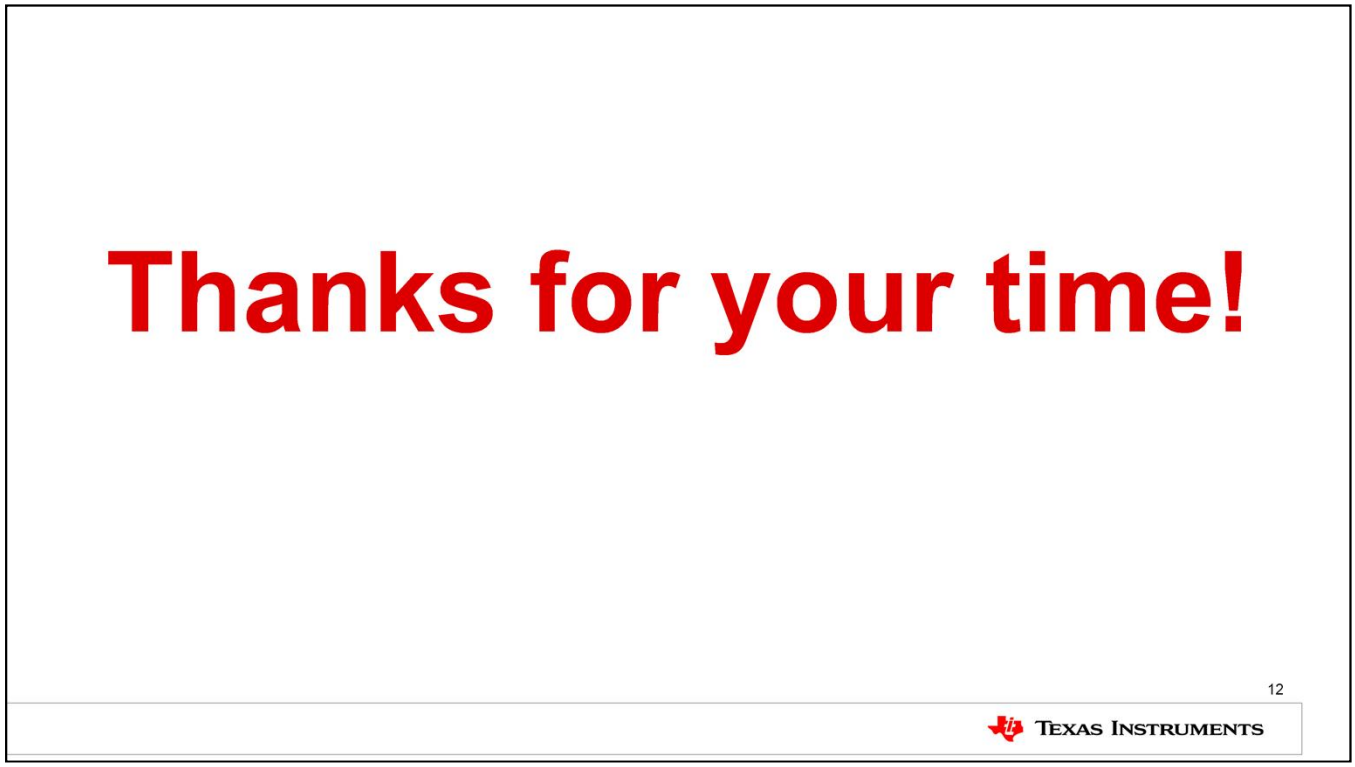
On the right is an improved version of the layout. Notice that the RF component has been moved closer to the inverting input pin. Although the trace from the output pin is longer, the trace going into the IN- pin is now much shorter. This drastically reduces the parasitic capacitance on the IN- pin. Additionally, the GND plane on the second layer has been removed under the IN- trace. This also helps to remove parasitic capacitance on IN-. However, it may only be necessary for very sensitive circuits.

Summary

1. Use short traces
2. Avoid parallel traces
3. Avoid capacitance on inverting input

There are various techniques used in creating good op amps layouts and many of them overlap with good analog layout in general. In this presentation, we covered those having to do with parasitic impedance on signal traces. In summary, make sure to use short traces when possible. Also, avoid placing traces in parallel or shield the traces when putting them in parallel is unavoidable. Lastly, minimize the parasitic capacitance on the op amp summing node, especially as seen by the IN- pin.

We will expand on these ideas in “Op Amp PCB Layout – Grounding & Bypass,” where we will take a look at separating analog and digital signals, grounding, and bypass capacitors.



That’s all for now! Thanks for watching.