

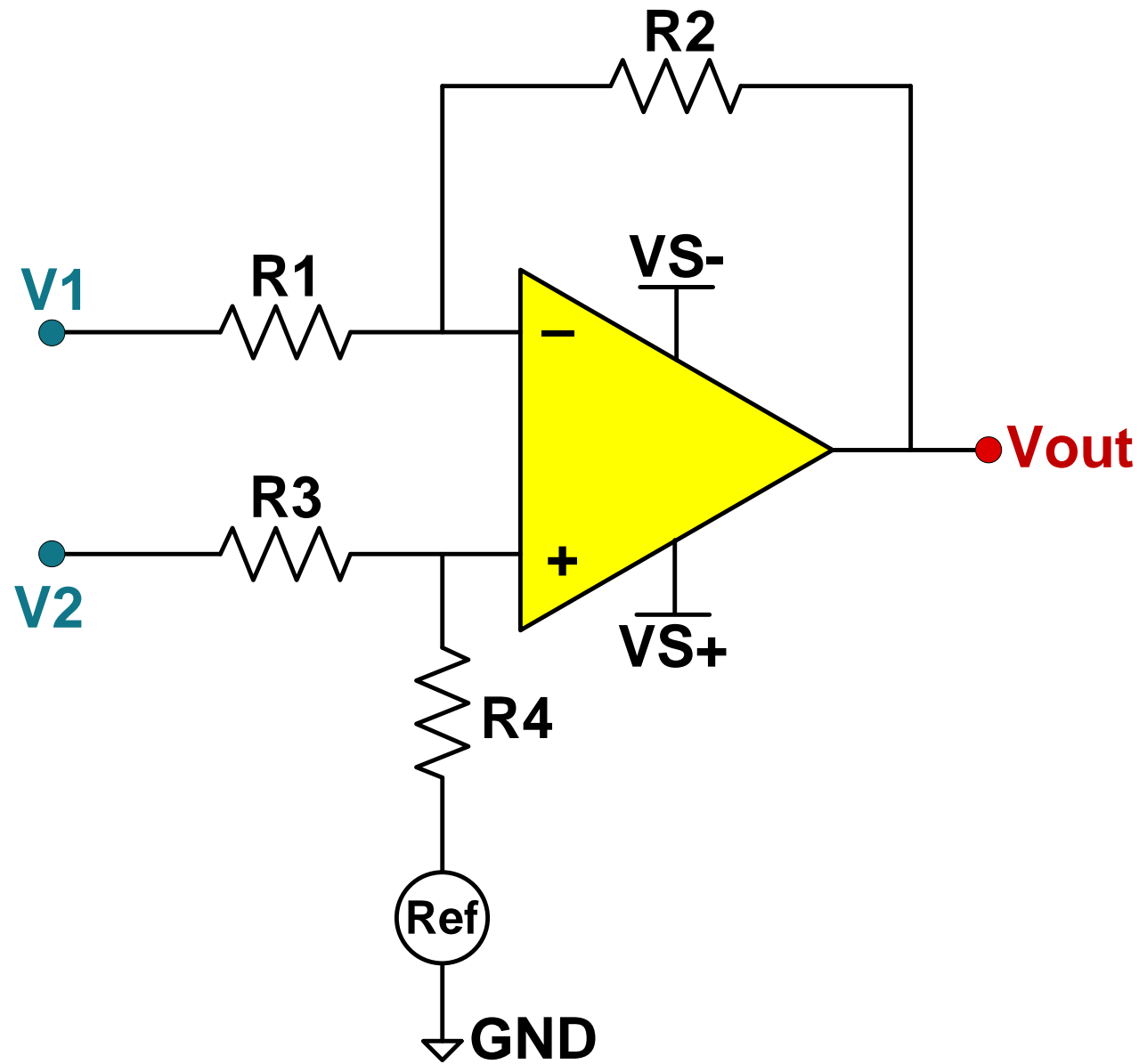
Instrumentation amplifier (IA) topologies: three-amp

TI Precision Labs – Instrumentation Amplifiers

Presented by Tamara Alani

Prepared by Tamara Alani

IA topologies – One amp recap



Difference amplifier output equation:

$$V_{out} = V_d \times A_d + Ref$$

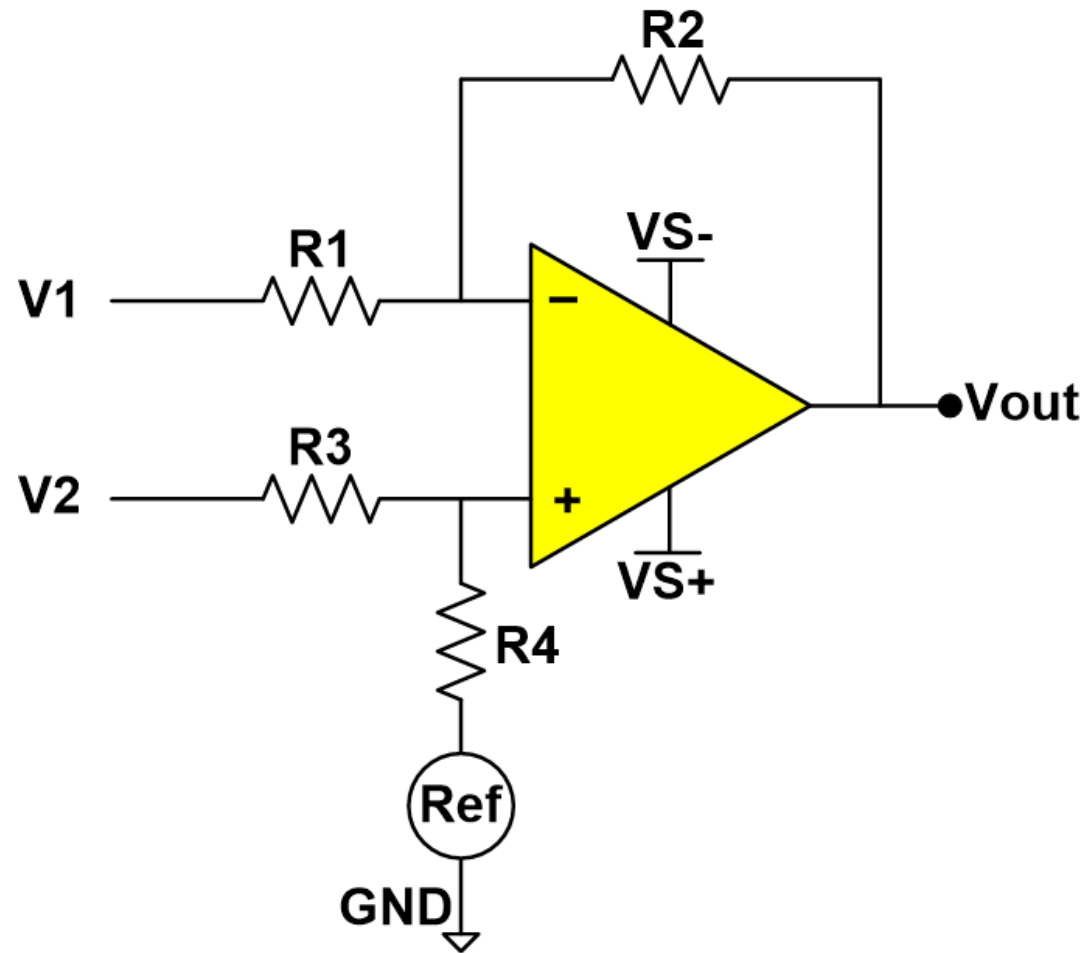
Where A_d is the gain of the circuit

If $R_1 = R_3$, and $R_2 = R_4$, then $A_d = \frac{R_2}{R_1}$

Challenges:

1. Precision relies on matched resistors
2. Low input impedance

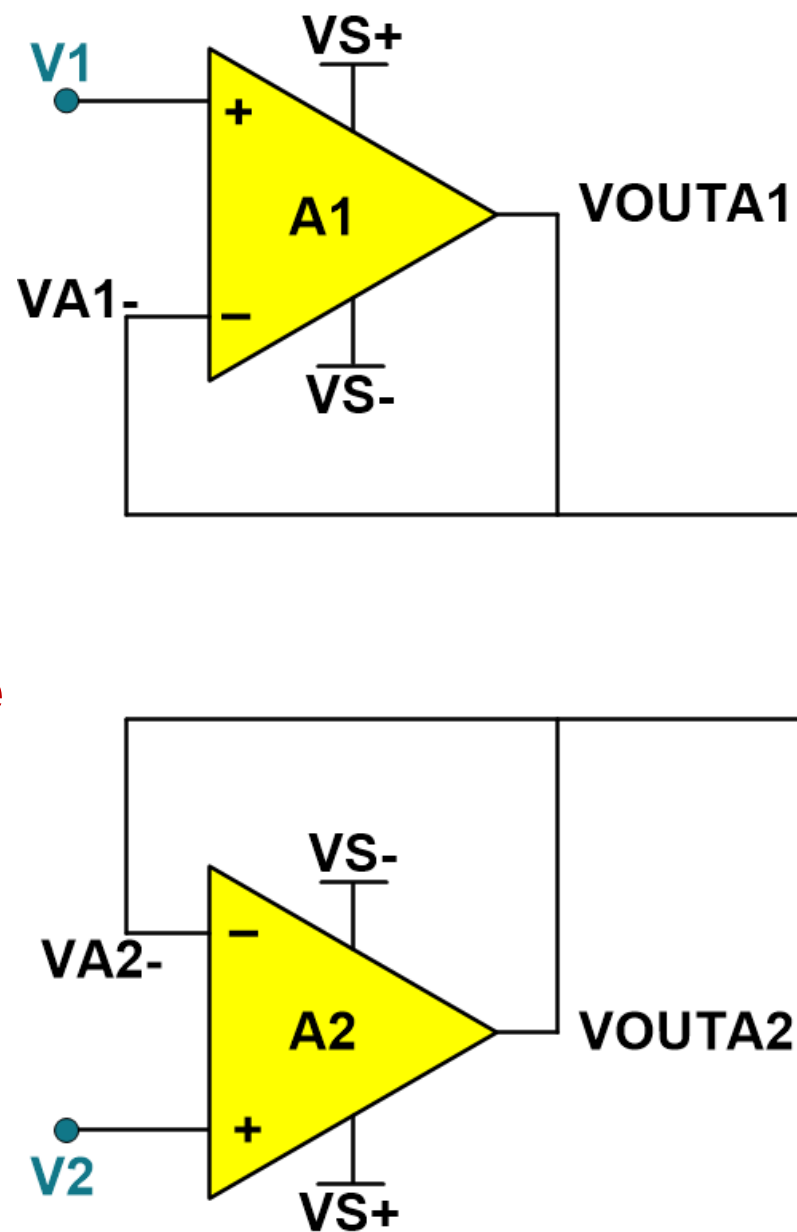
Difference amplifier recap – Input impedance



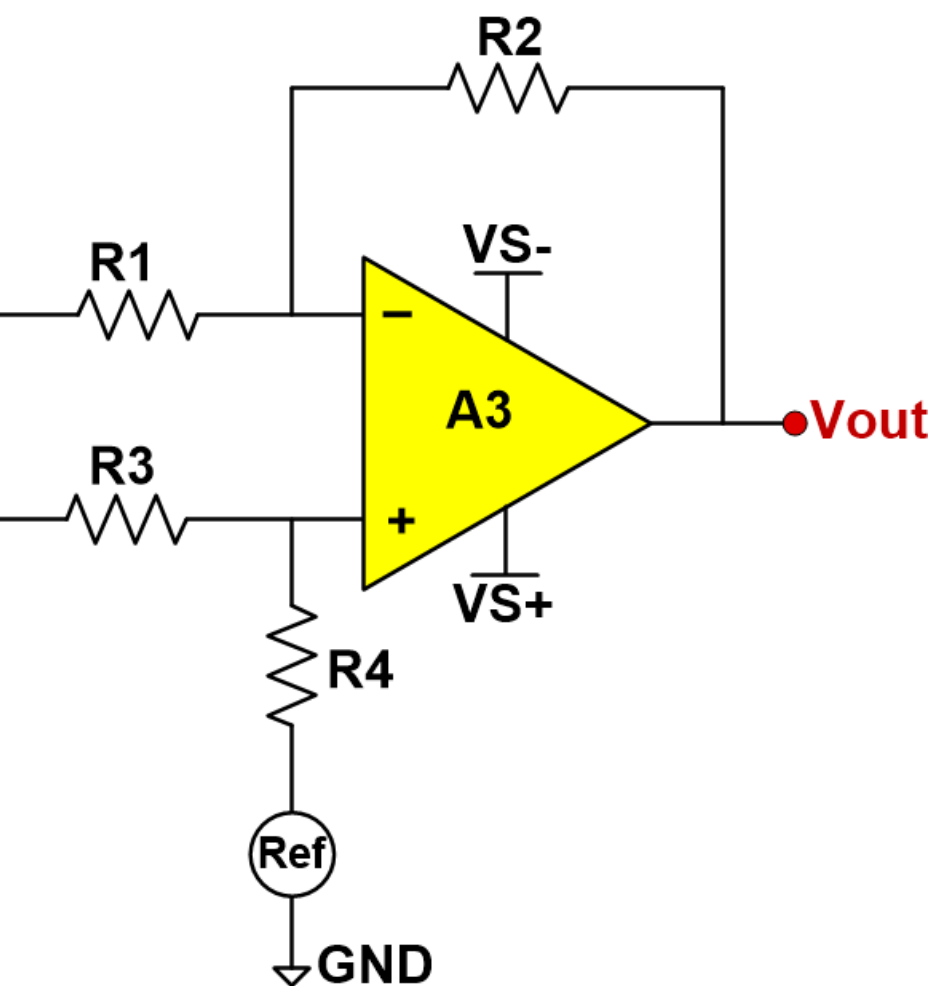
Design challenges:

- ▶ **Low input impedance**
- ▶ Precisely matched resistances
- ▶ This circuit will draw current from the signal source, and if the source's output impedance is not zero, it will degrade accuracy.

IA topologies – Three amp configuration

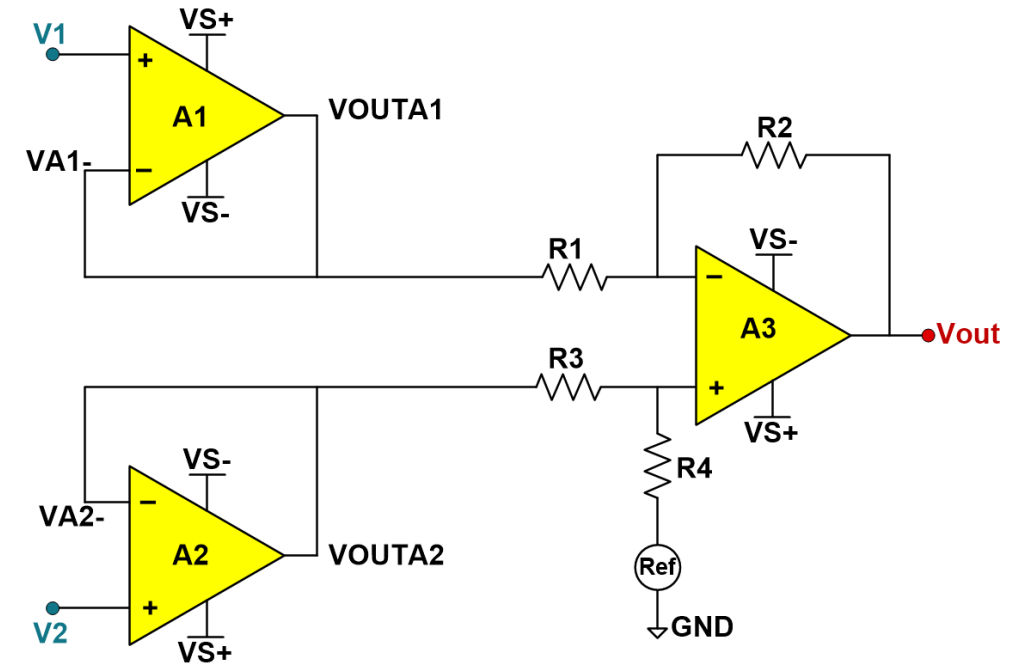
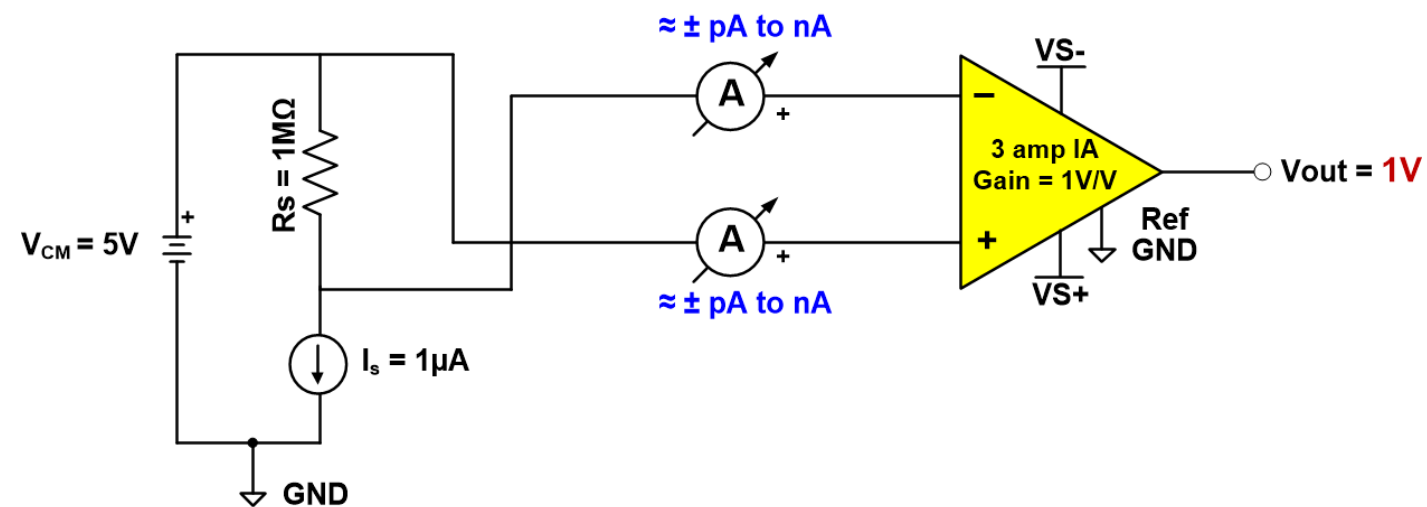
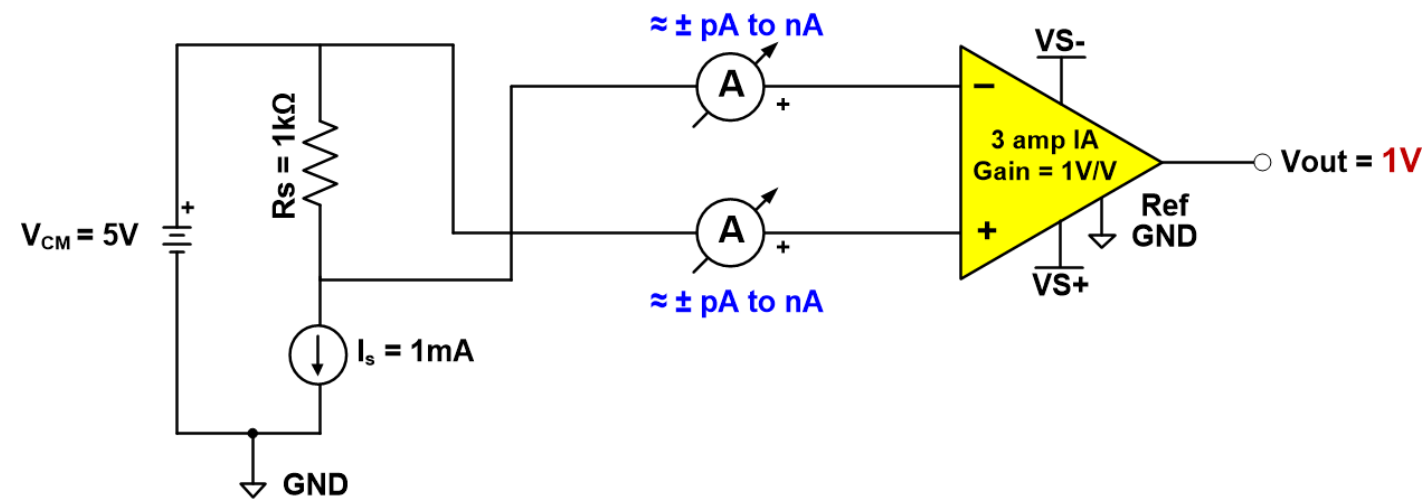


Buffer stage
with high
input impedance



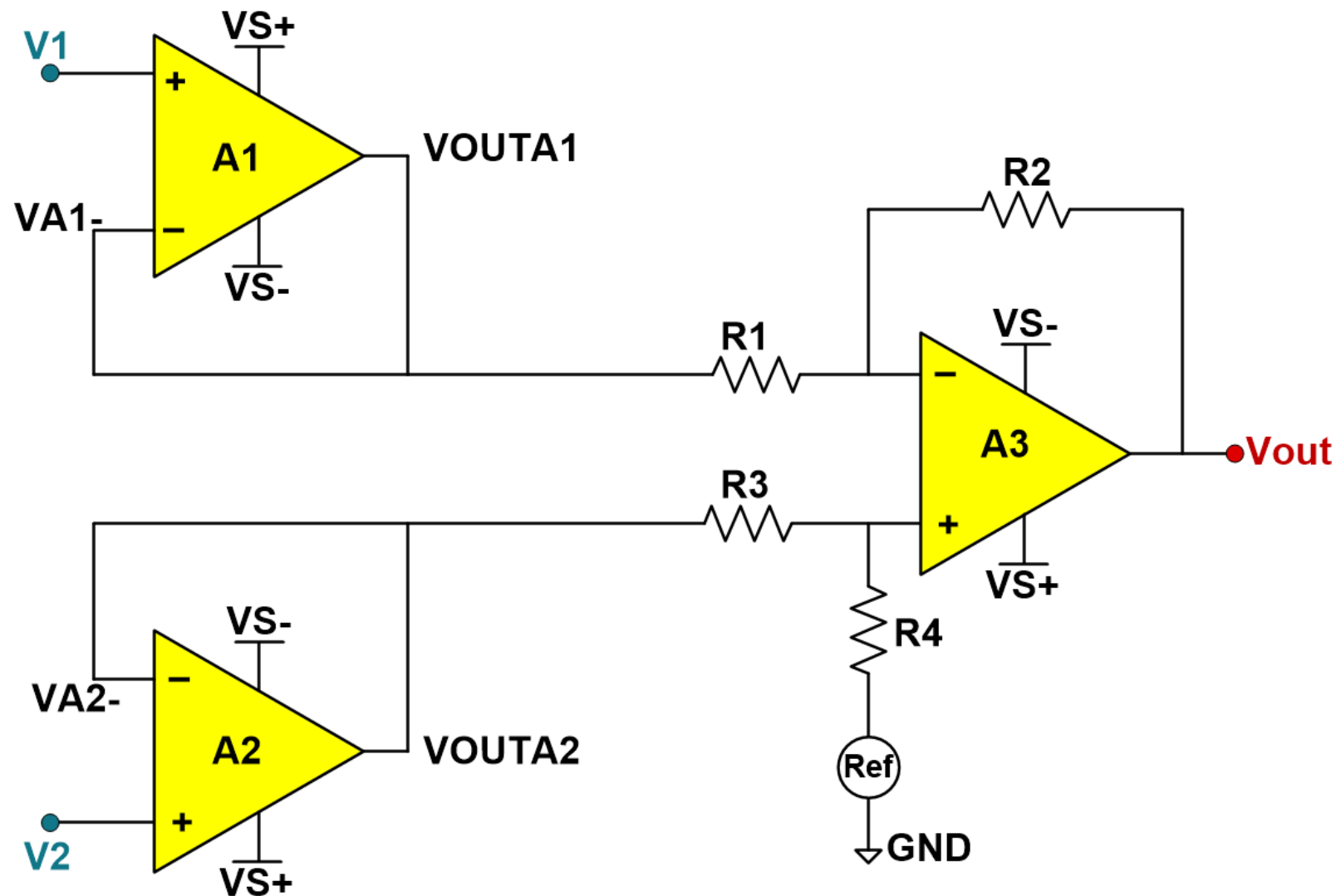
Difference
amplifier
output stage

3 amp IA input impedance – Current sensing



- Input impedance from 10^9 to $10^{12} \Omega$ are typical, due to A1 and A2
- This high input impedance limits the current flowing through the inputs to levels ranging from pA to nA.
- Current draw is still dependent on technology, temperature, common mode voltage, and more.

3 amp IA – Gain control



$$\text{Signal gain, } A_d = \frac{R_2}{R_1}$$

This is assuming:

$$R_1 = R_3 \text{ and } R_2 = R_4$$

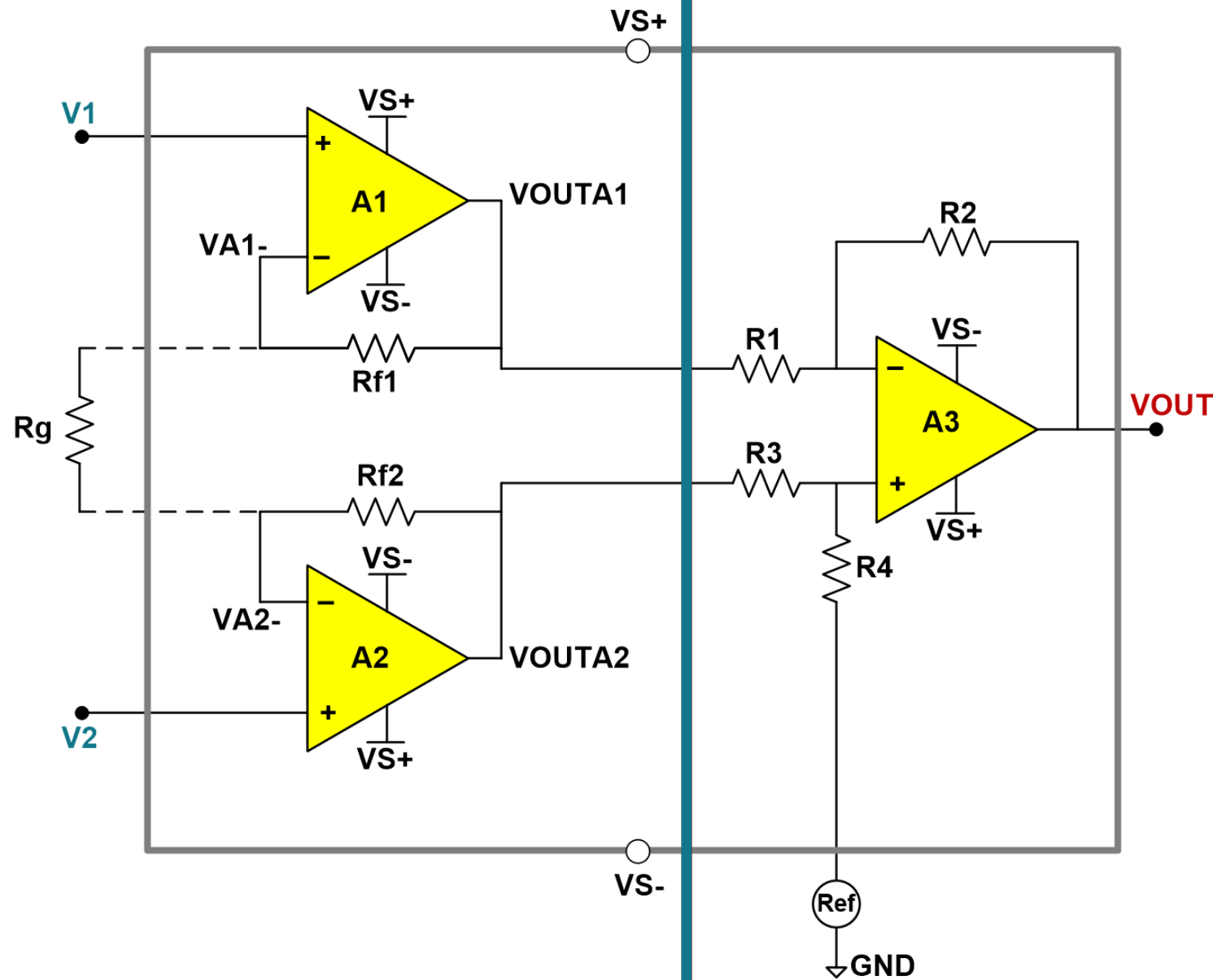
If gain needs to be adjusted, 4 resistors need to be changed and matched for optimal precision.

Want: Easy gain control

Solution: Pull into first stage

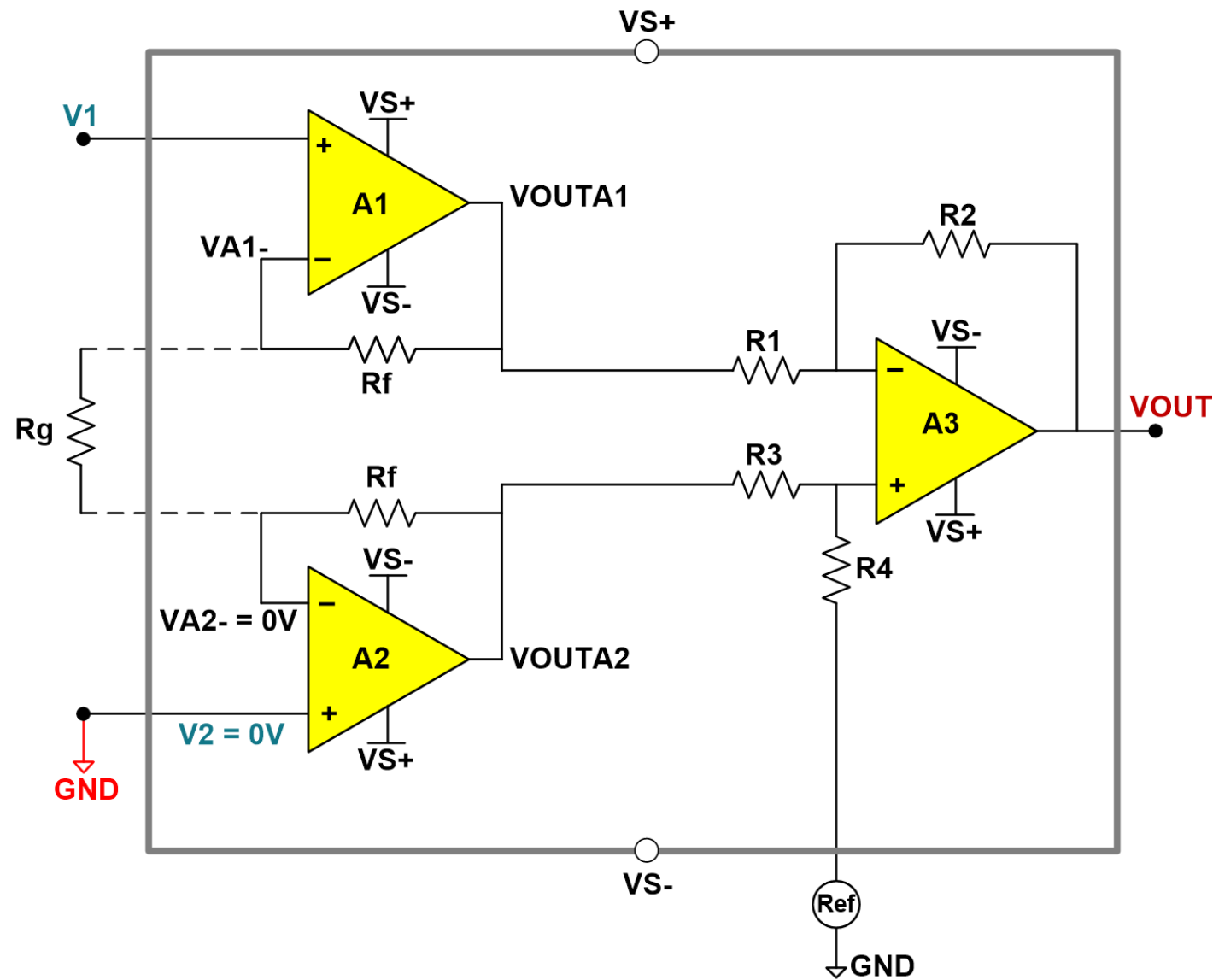
3 amp IA – Two stage breakdown

Buffer stage with gain and high input impedance



Difference amplifier output stage

3 amp IA derivation – First stage



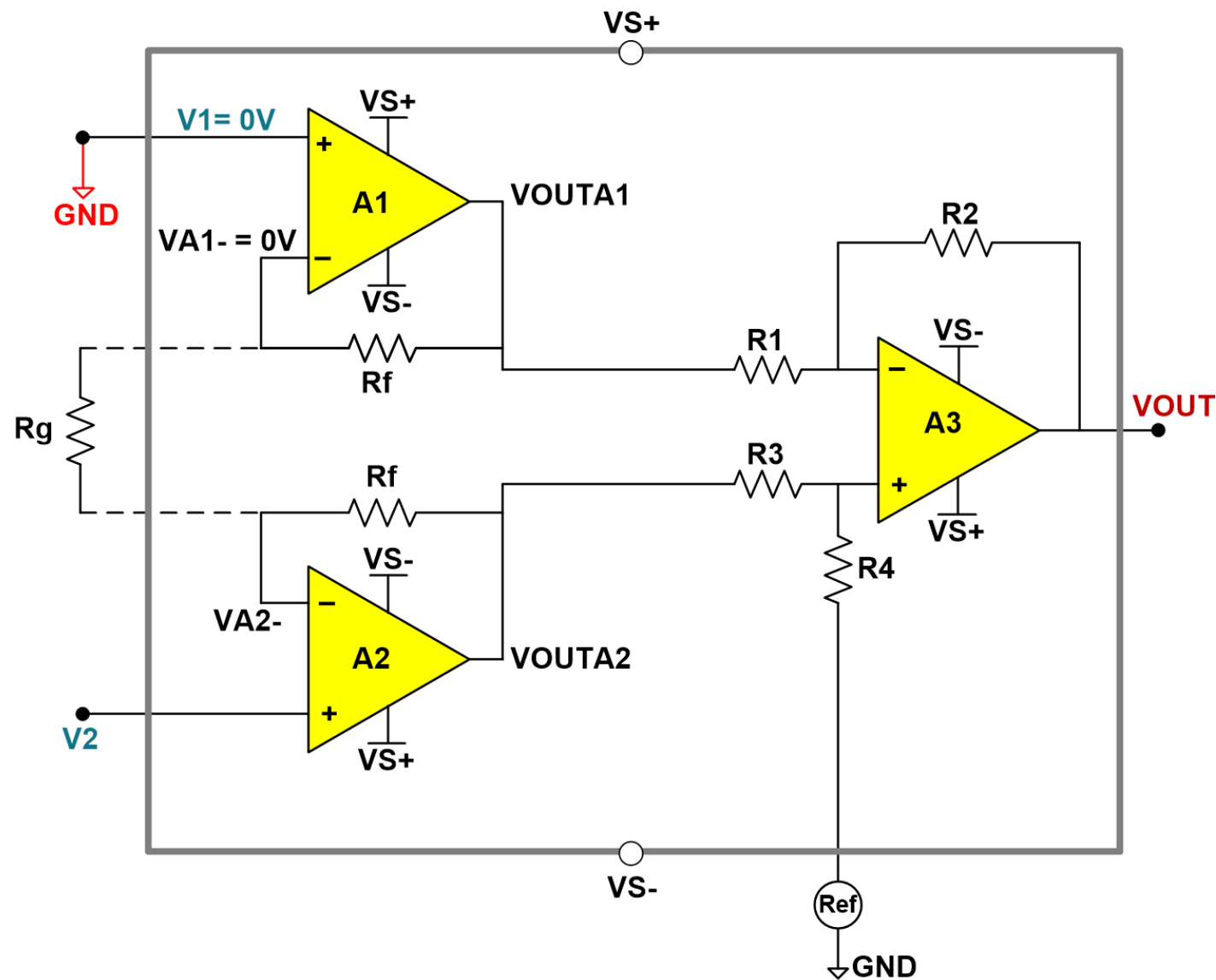
- VOUTA1 consists of two components: voltage due to V1 and V2
- If $V2 = 0V$, then $V_{A2-} = 0V$
- A1 looks like a non-inverting amplifier:

$$A_d = 1 + \frac{R_f}{R_g}, \text{ and}$$

$$V_{outA1} = V1 \times \left(1 + \frac{R_f}{R_g} \right)$$

Equation 1

3 amp IA derivation – Frist stage cont'd



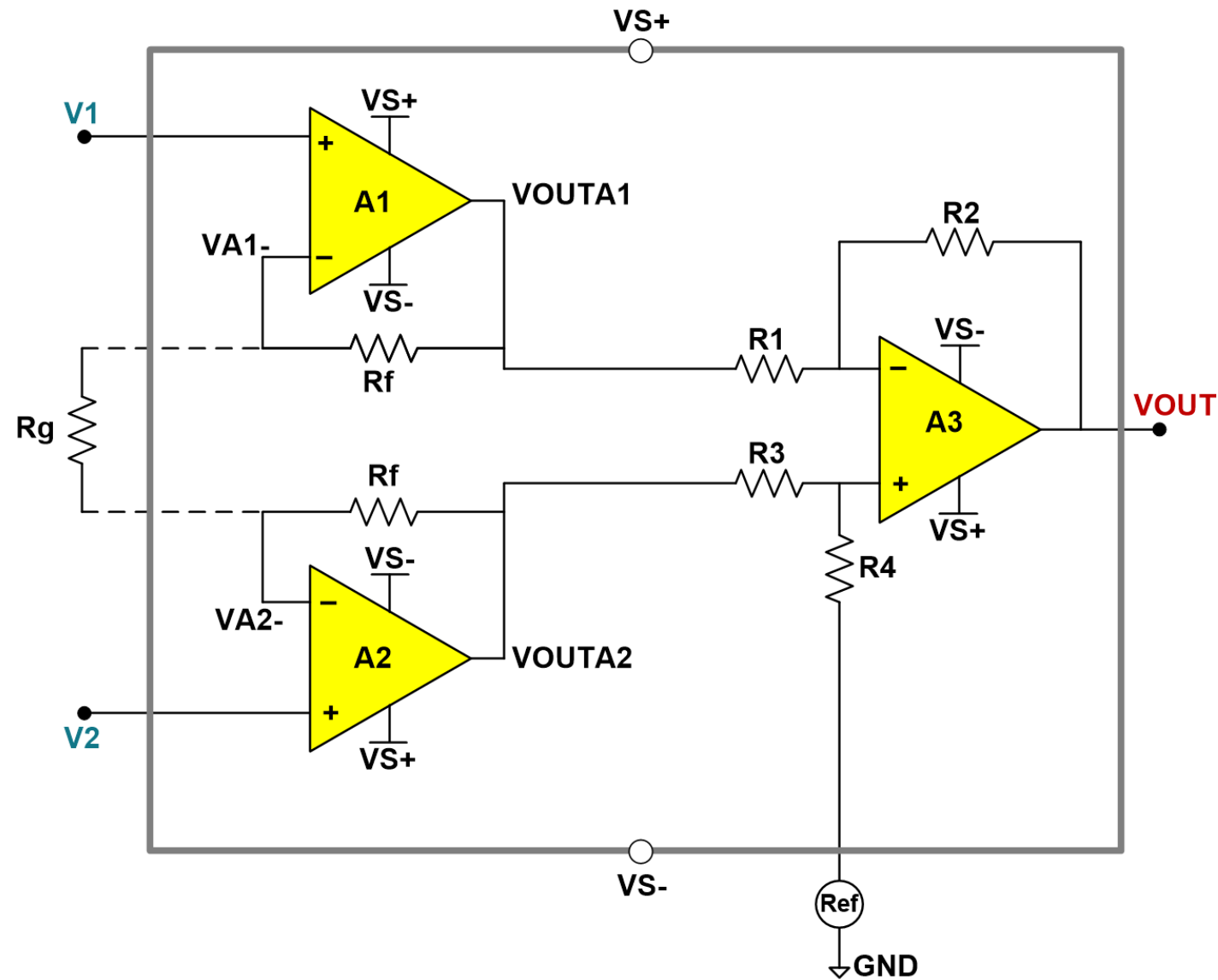
- If $V1 = 0V$, then $VA1- = 0V$
- A1 looks like an inverting amplifier:

$$A_d = -\frac{R_f}{R_g}, \text{ and}$$

$$V_{OUTA1} = V_2 \times \left(\frac{-R_f}{R_g} \right)$$

Equation 2

3 amp IA derivation – Combined



Equation 1: $V_{OUTA1} = V1 \times \left(1 + \frac{Rf}{Rg}\right)$

Equation 2: $V_{OUTA1} = V2 \times \left(\frac{-Rf}{Rg}\right)$

Combing Equations 1 and 2:

$$V_{OUTA1} = \left(1 + \frac{Rf}{Rg}\right) \times V1 - \left(\frac{Rf}{Rg}\right) \times V2$$

$$= \left(\frac{Rf}{Rg}\right) \times (V1 - V2) + V1$$

...Do the same to A2

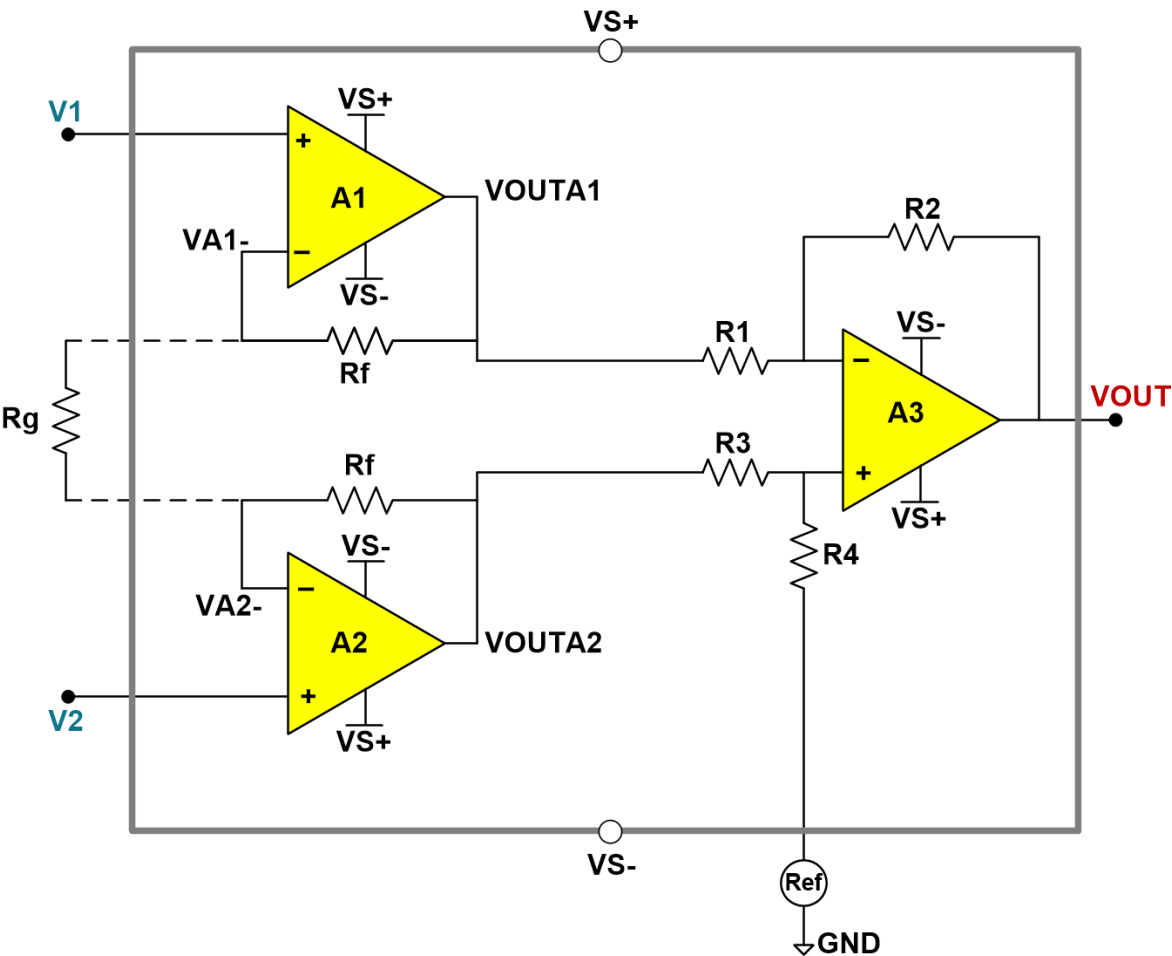
$$V_{OUTA2} = \left(\frac{Rf}{Rg}\right) \times (V2 - V1) + V2$$

VOUTA1 and VOUTA2 feed into A3 (difference amplifier)

Assume R1=R3 and R2=R4, then

$$V_{OUTA3} = \left(\frac{R2}{R1}\right) \times (V_{OUTA2} - V_{OUTA1}) + Ref$$

3 amp IA derivation – Combined



$$VOUTA1 = \frac{Rf}{Rg} \times (V1 - V2) + V1$$

$$VOUTA2 = \frac{Rf}{Rg} \times (V2 - V1) + V2$$

$$VOUTA3 = \frac{R2}{R1} \times (VOUTA2 - VOUTA1) + Ref$$

Substitute the equations for VOUTA1 and VOUTA2 into VOUTA3:

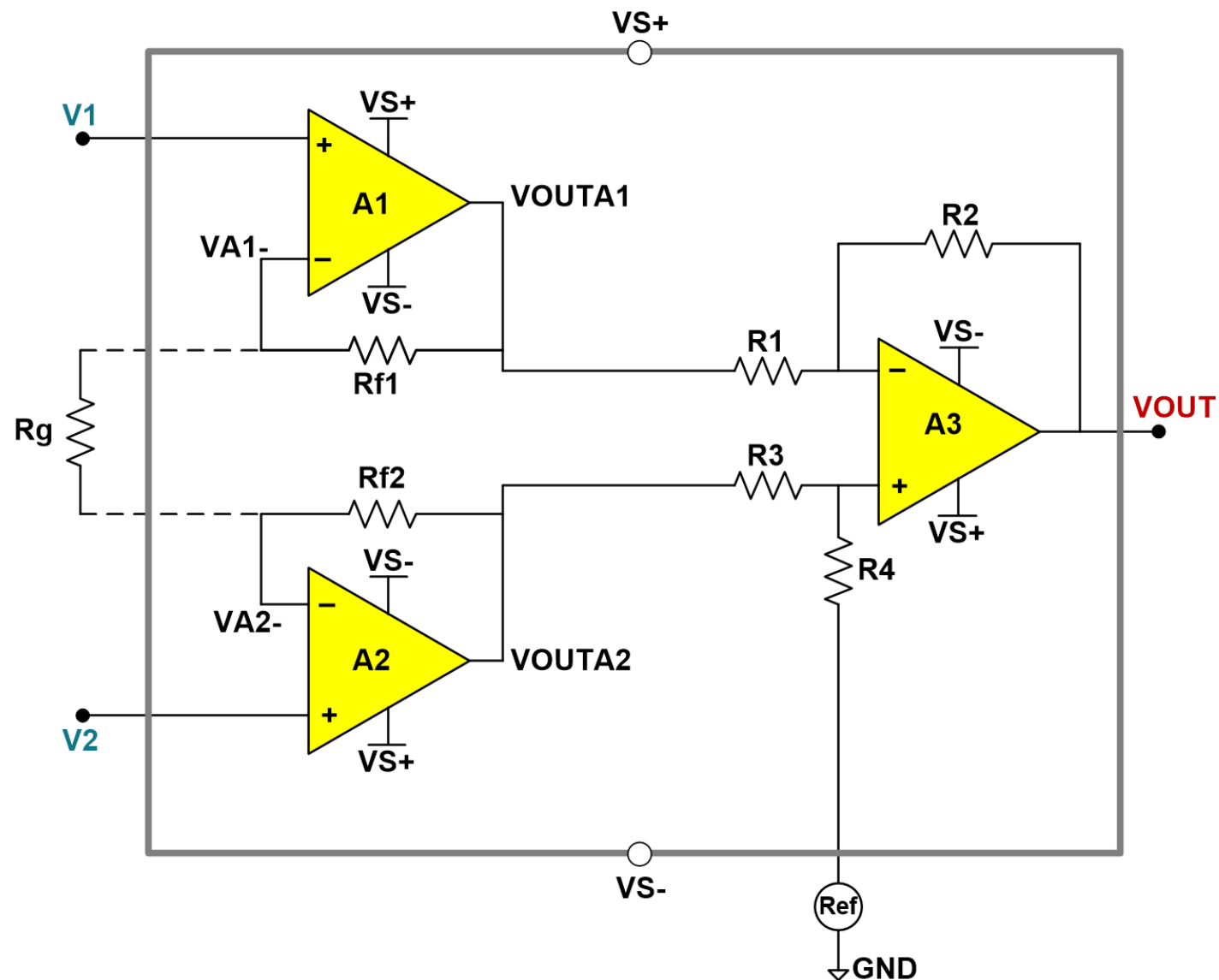
$$VOUT = \frac{R2}{R1} \times \left(\left(\frac{Rf}{Rg} \times (V1 - V2) + V1 \right) - \left(\frac{Rf}{Rg} \times (V2 - V1) + V2 \right) \right) + Ref$$

Simplifying...

$$VOUT = (V2 - V1) \times \frac{R2}{R1} \times \left(1 + \frac{2Rf}{Rg} \right) + Ref$$

Where the differential gain, Ad is $\frac{R2}{R1} \times \left(1 + \frac{2Rf}{Rg} \right)$

3 amp IA – Circuit goal



Circuit component goal:

Match R1 to R2, R3 and R4 to form a unity gain difference amplifier

Match Rf1 and Rf2; feedback resistors which interact with Rg to alter the gain of the input signal (Vd)

Transfer function recap:

$$Ad = \frac{R2}{R1} \times \left(1 + \frac{2Rf}{Rg} \right)$$

$$Vout = Ad \times Vd + Ref, \text{ where } Vd = V2 - V1$$

Amplifier roles:

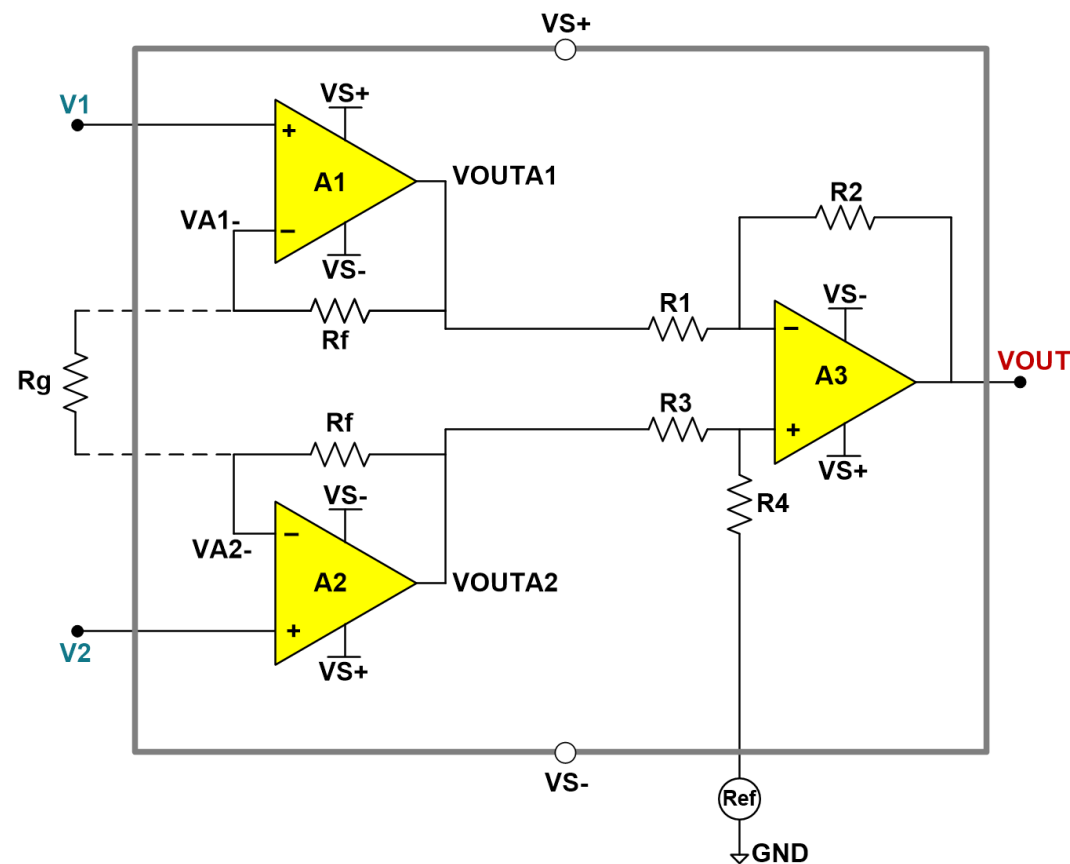
A1 & A2 operate with differential gain to amplify the signal

A3 unity gain difference amplifier

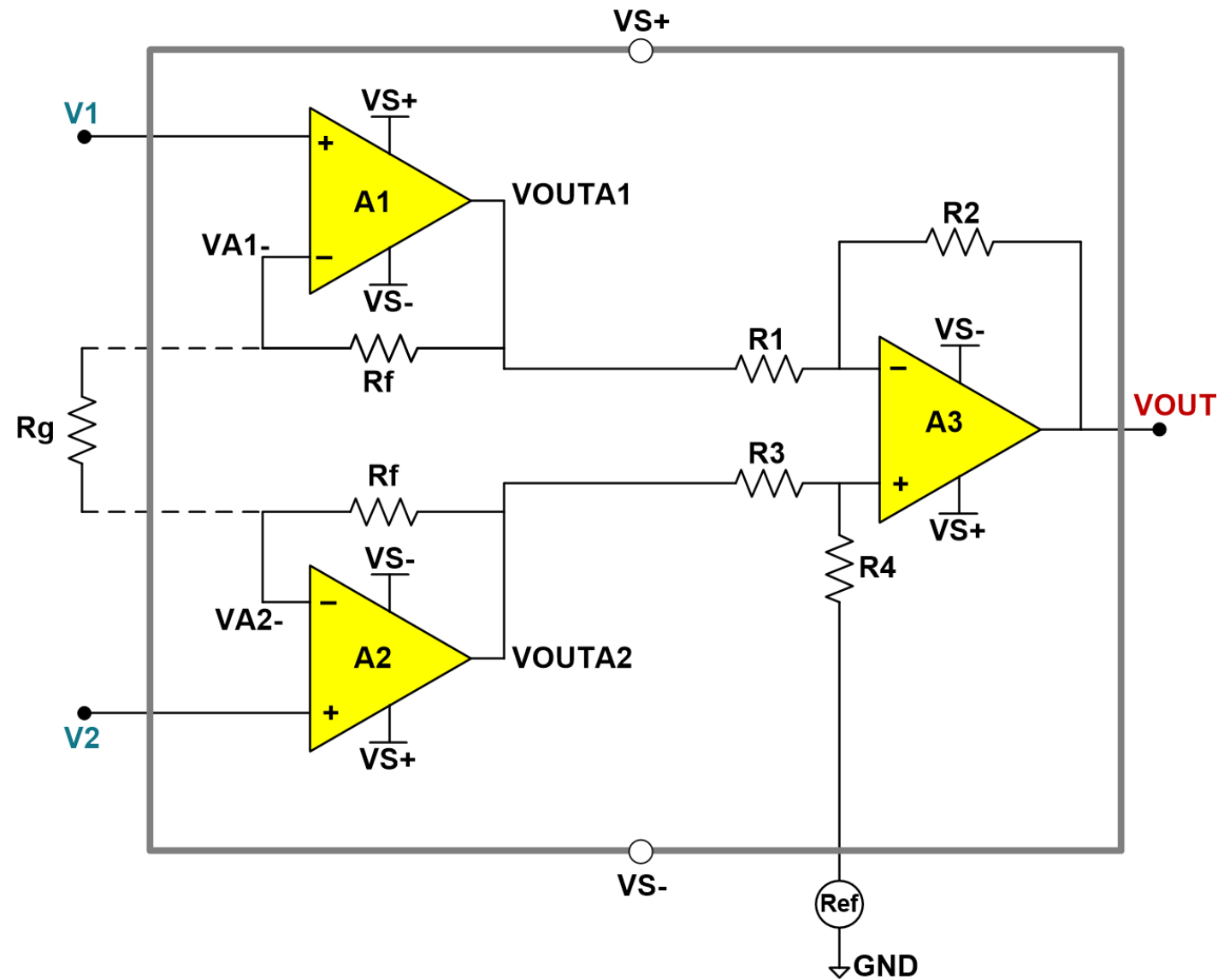
Instrumentation amplifier – Idealized model

Two main characteristics of an instrumentation amplifier:

1. Amplifies the signals that differ between the two inputs
2. Rejects the signals that are the same (common) to both inputs



Idealized model – Common mode voltage analysis



Apply a common mode voltage:

When a common-mode voltage is applied to inputs of A1 and A2, either side of R_g will be equal.

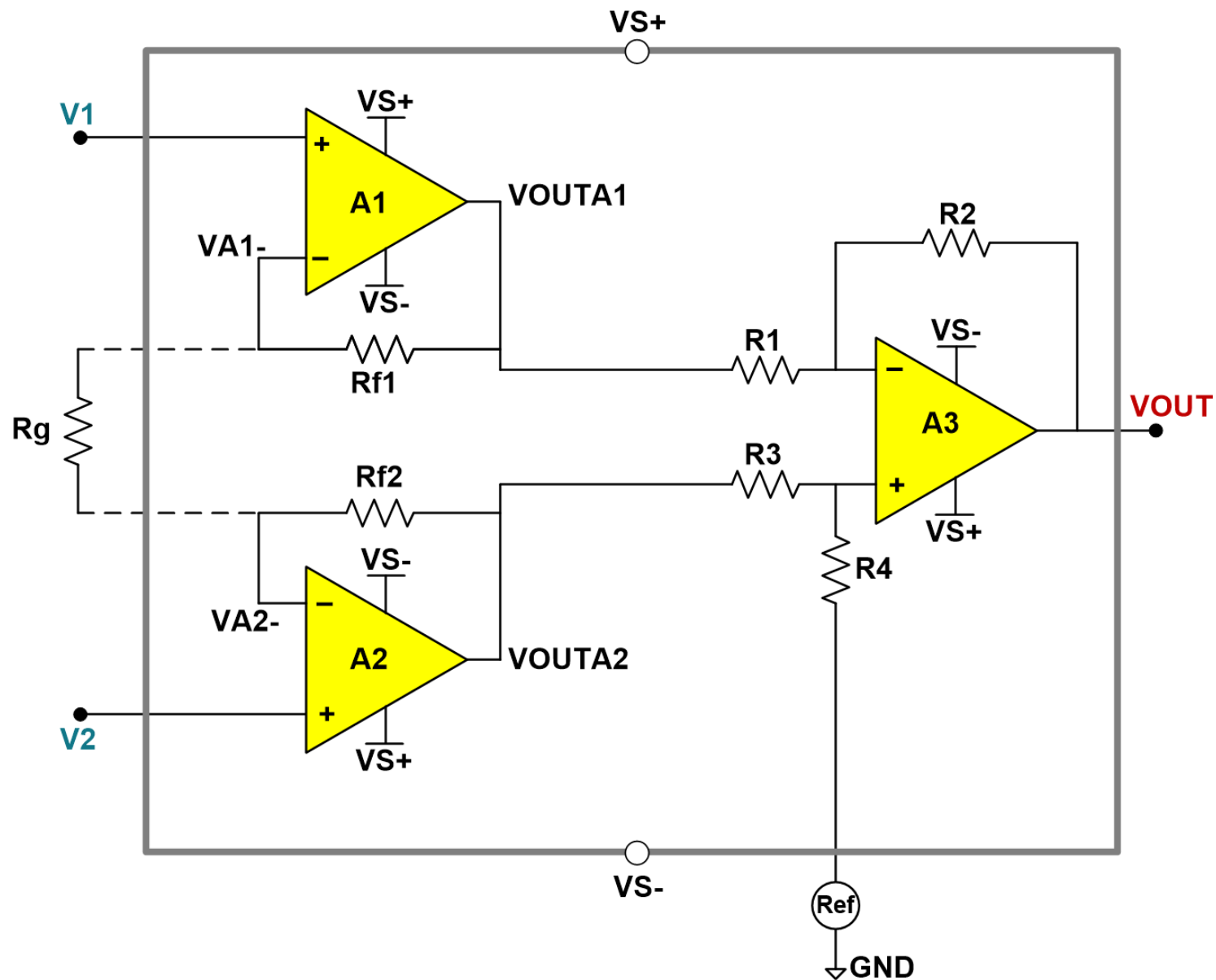
$$IR_g = IR_{f1} = IR_{f2} = 0A$$

Common mode signals will be passed through input buffers A1 and A2 at unity gain, but differential voltages will be amplified by:

$$1 + \frac{2R_f}{R_g}$$

The second stage difference amplifier rejects this common mode voltage and passes only the differential voltage.

CMRR – How gain effects CMRR



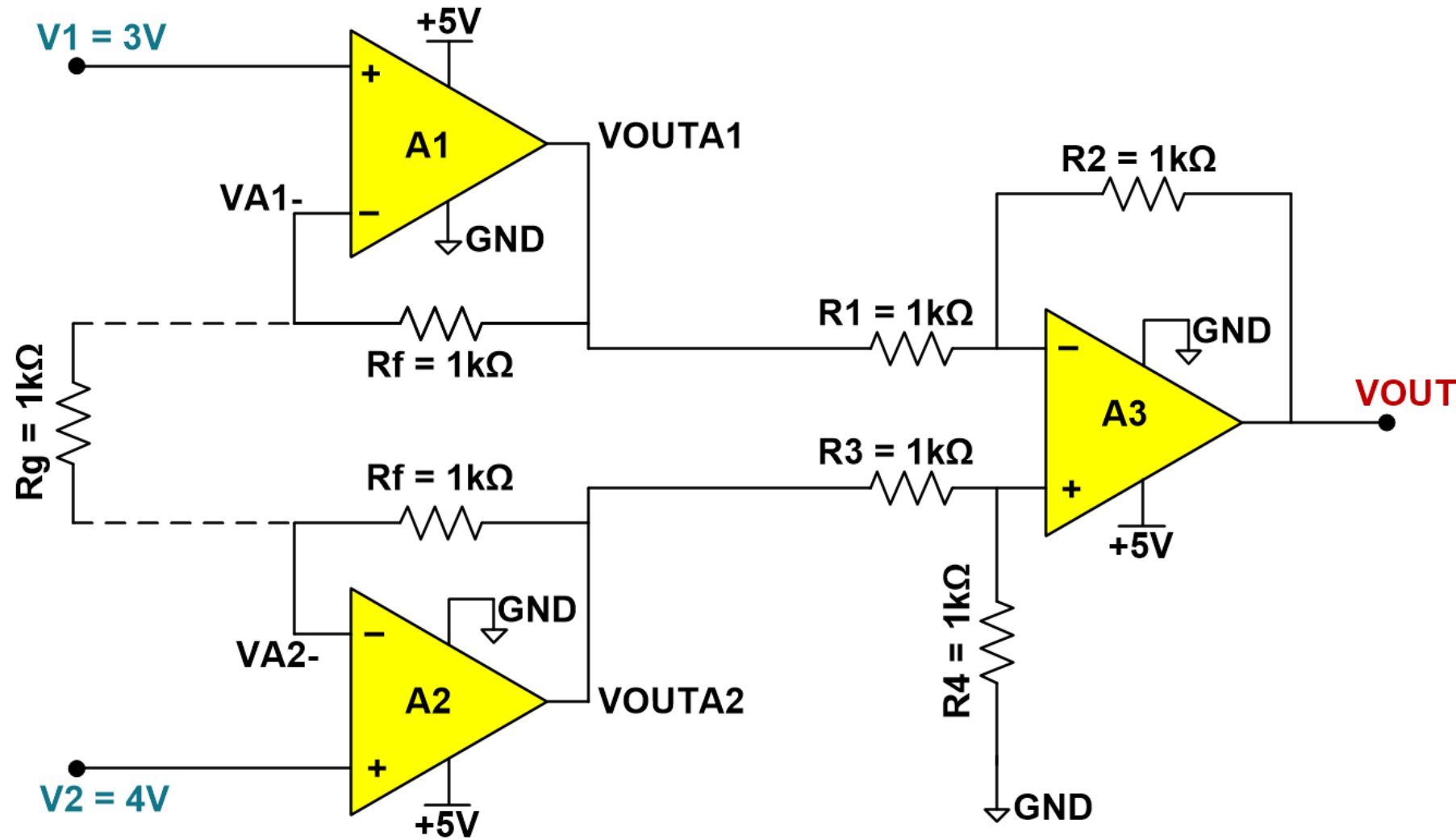
$$CMRR \left(\frac{V}{V} \right) = \frac{\text{differential gain}}{\text{common mode gain}} = \frac{A_d}{A_{CM}}$$

When gain is increased by Rg:

- the differential signal will be increased
- but the common-mode error will not

$\frac{A_d}{A_{CM}}$ will increase so CMRR will theoretically increase in direct proportion to gain

3 amp IA – Linear behavior analysis



3 amp IA with RRIO amps
 $V_s = 5V$ single supply
 $V_2 = 4V, V_1 = 3V$

$$V_d = V_2 - V_1 = 1V$$

$$A_d = \frac{R_2}{R_1} \times \left(1 + \frac{2R_f}{R_g} \right) = \frac{3V}{V}$$

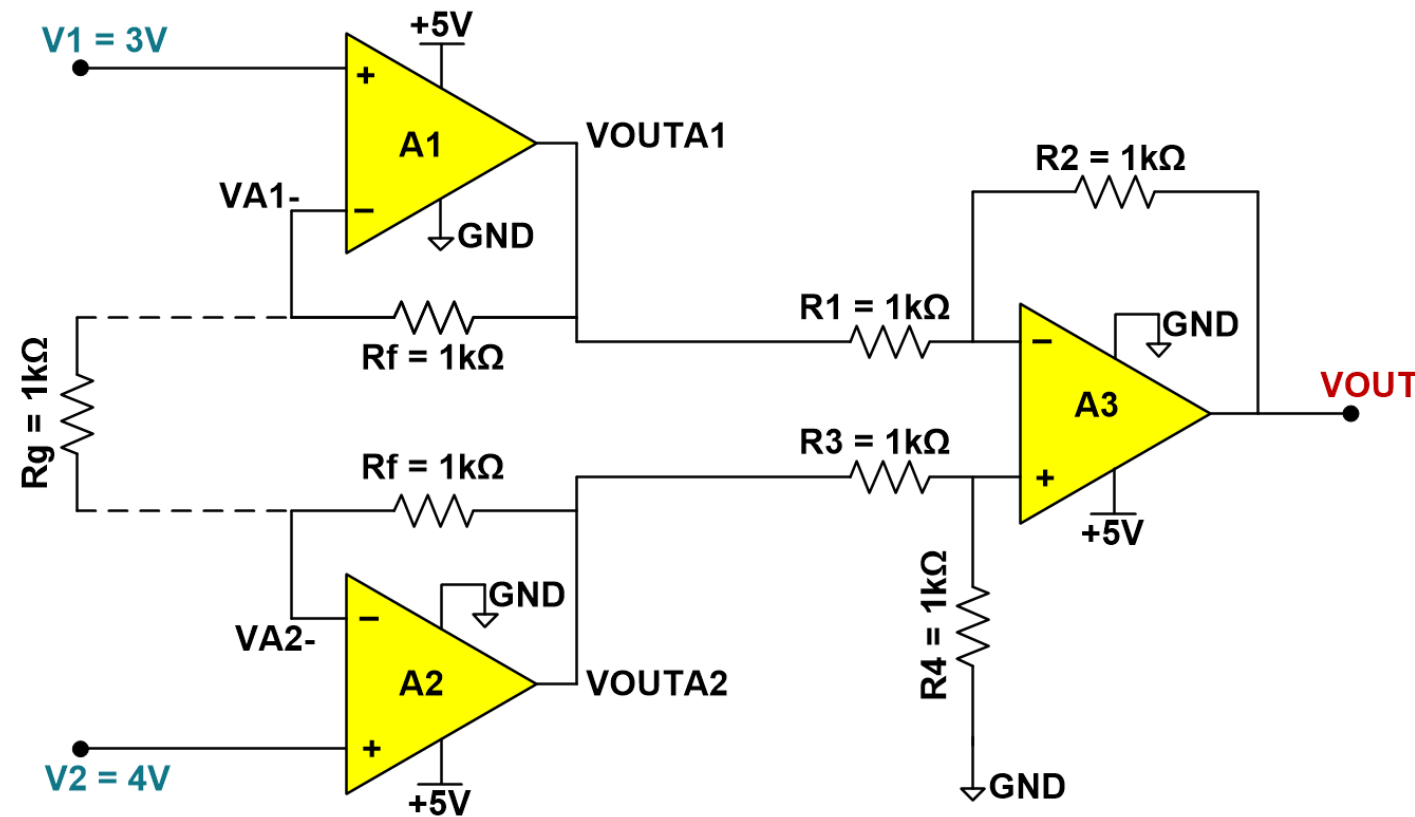
$$R_{ref} = 0V$$

$$V_{out} = V_d \times A_d + R_{ref} = 3V$$

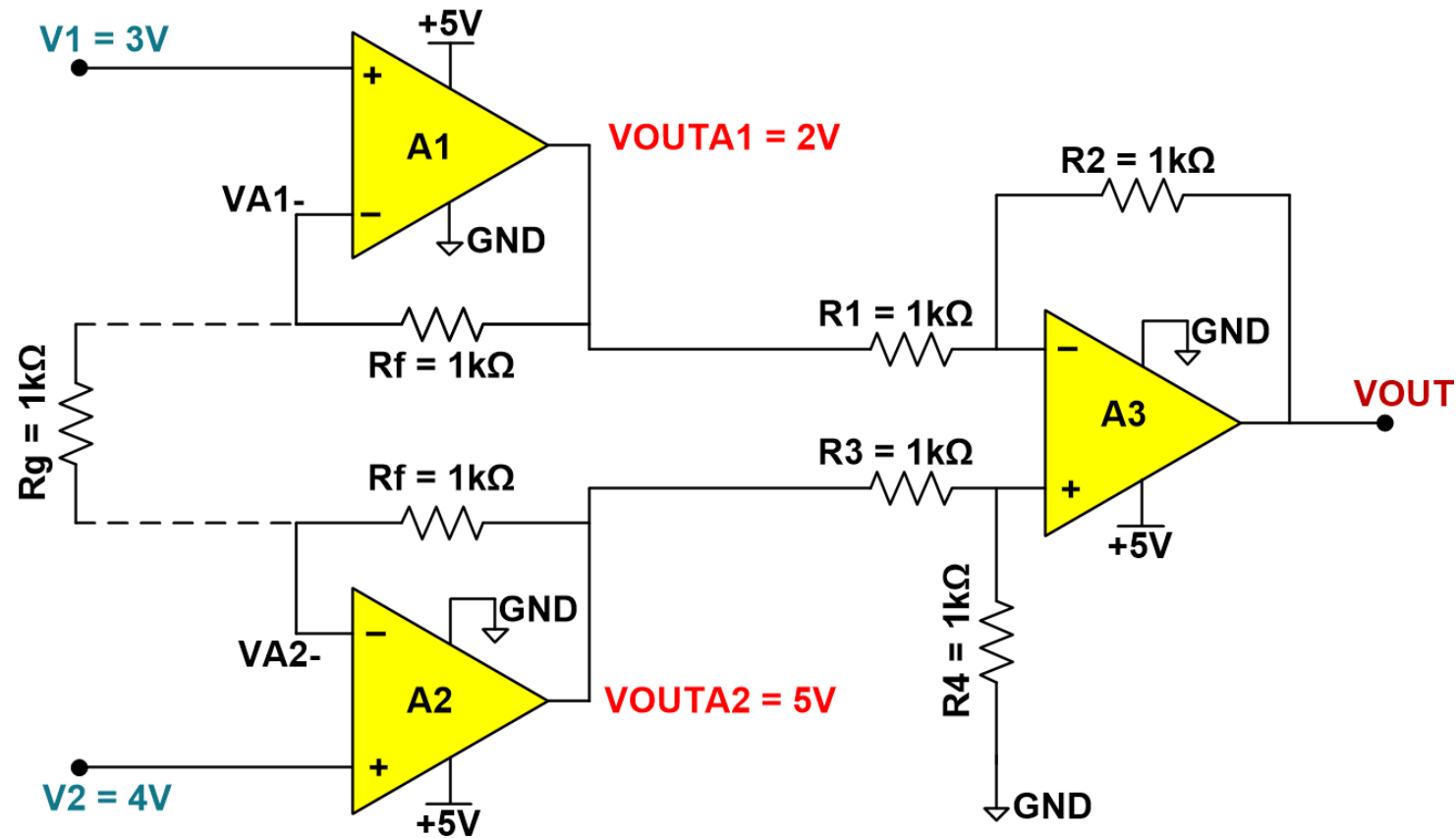
Input and output – RRIO

- **Rail-to-Rail input and output amplifiers**

- Rail-to-Rail input (RRI) amplifiers have input ranges which extend *to* and sometimes *beyond* the rail
- Rail-to-Rail output (RRO) amplifiers have output swings *near* the rails



3 amp IA – Linear behavior analysis



RRI: to and beyond the rail: $0V \leq V_{in} \leq 5V$

RRO: near the rail: $0.1V \leq V_{out} \leq 4.9V$

Let us analyze each amplifier individually:

A1:

- Input = **3V**, this is within $0V \leq V_{in} \leq 5V$
- Output = **2V**, this is within $0.1V \leq V_{out} \leq 4.9V$

A2:

- Input = **4V**, this is within $0V \leq V_{in} \leq 5V$
- Output = **5V**, this is **NOT** within $0.1V \leq V_{out} \leq 4.9V$

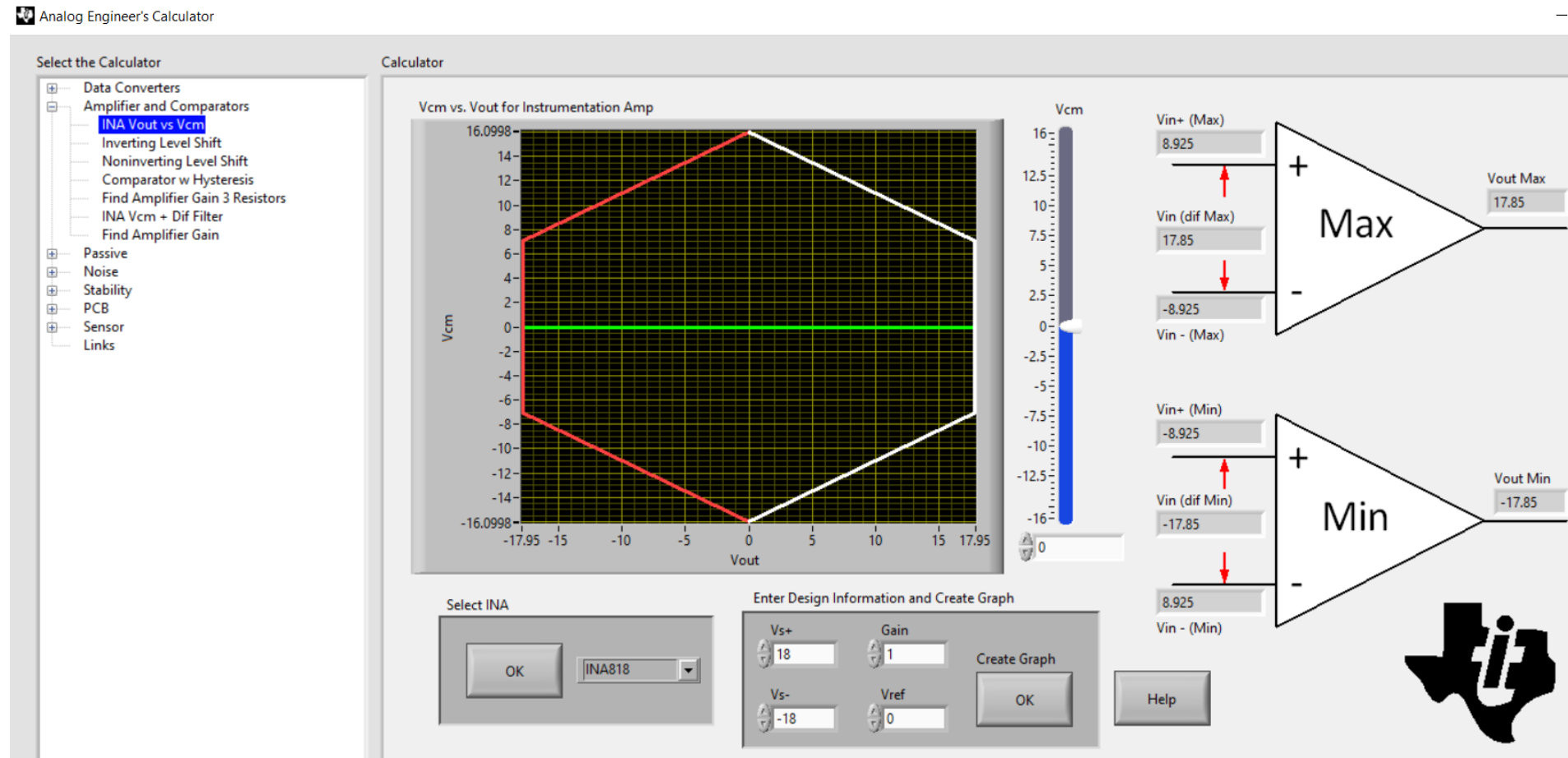
$$V_{OUTA1} = \frac{R_f}{R_g} \times (V_1 - V_2) + V_1$$

$$V_{OUTA2} = \frac{R_f}{R_g} \times (V_2 - V_1) + V_2$$

$$V_{OUTA3} = \frac{R_2}{R_1} \times (V_{OUTA2} - V_{OUTA1}) + V_{ref}$$

3 amp IA – Boundary plot

Boundary plots graphically show a designer the usable range of an IA by analyzing the internal nodes.



Analog engineer's calculator → INA VCM vs Vout

3 amp IA with gain – Example

Assume the following conditions:

Power supply = $\pm 5V$

Reference voltage = $0V$

$V_d = 10mV$, $V_{CM} = 1V$

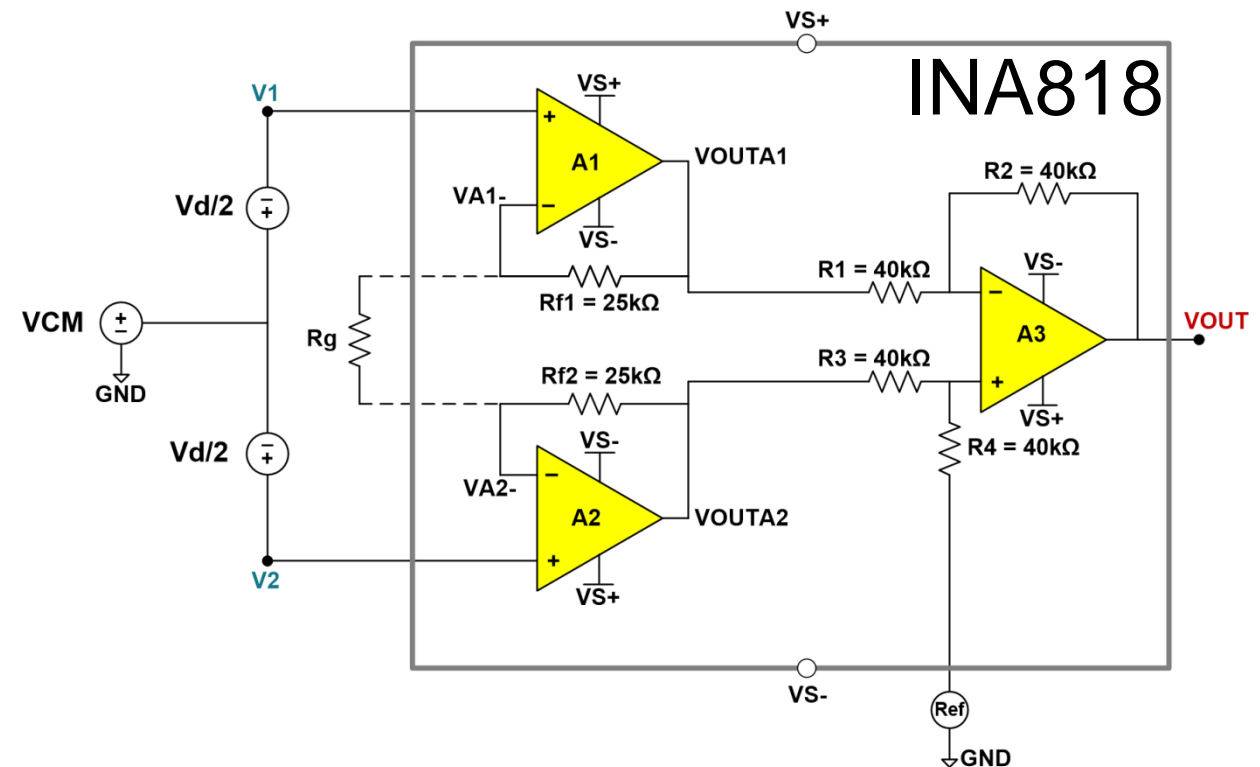
Expected V_{out} is $3V$

Calculate gain: $\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{3V}{10mV} = 300V/V$

Ad for a 3 amp IA:

$$A_d = \frac{R_2}{R_1} \times \left(1 + \frac{2R_f}{R_g} \right)$$
$$300 = \frac{40k}{40k} \times \left(1 + \frac{2 \times 25k}{R_g} \right)$$

Solve for $R_g = 167.2\Omega$



3 amp IA with gain – Example

Assume the following conditions:

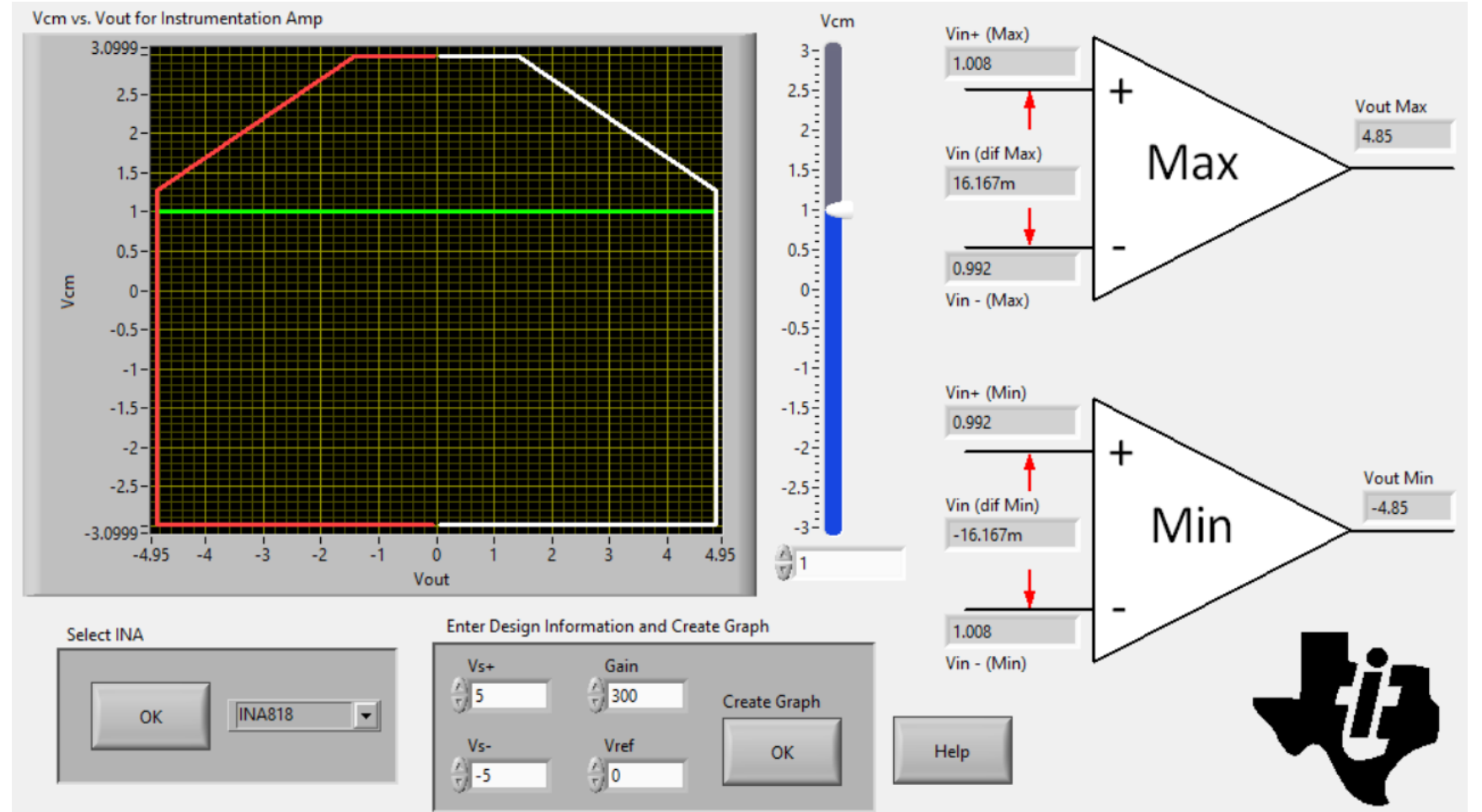
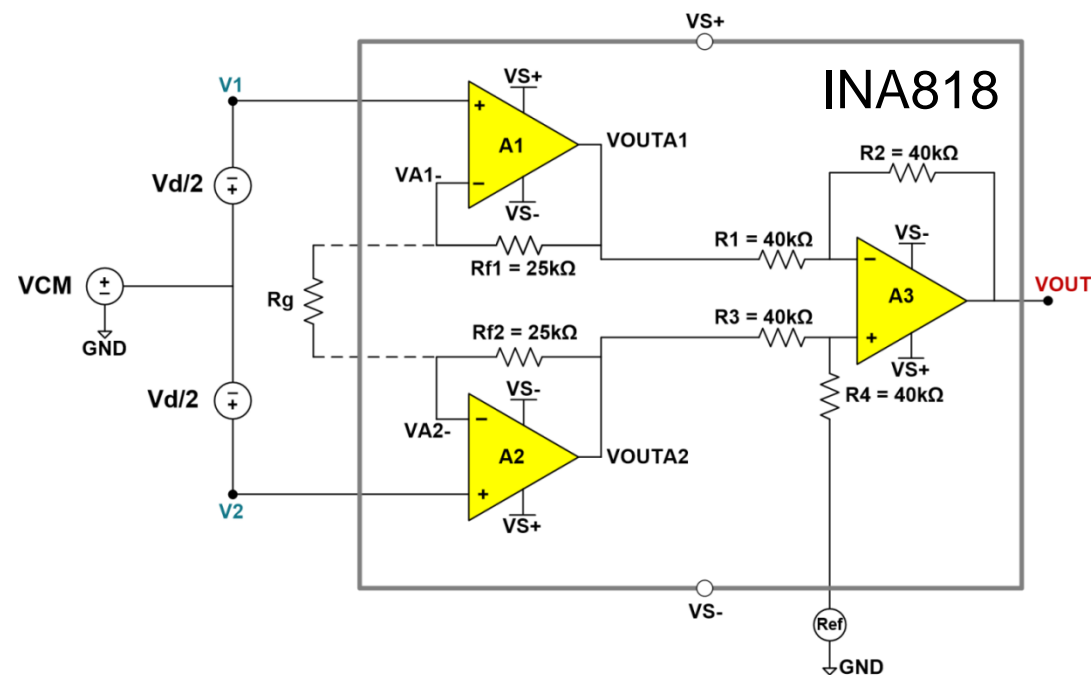
Power supply = $\pm 5V$

Reference voltage = $0V$

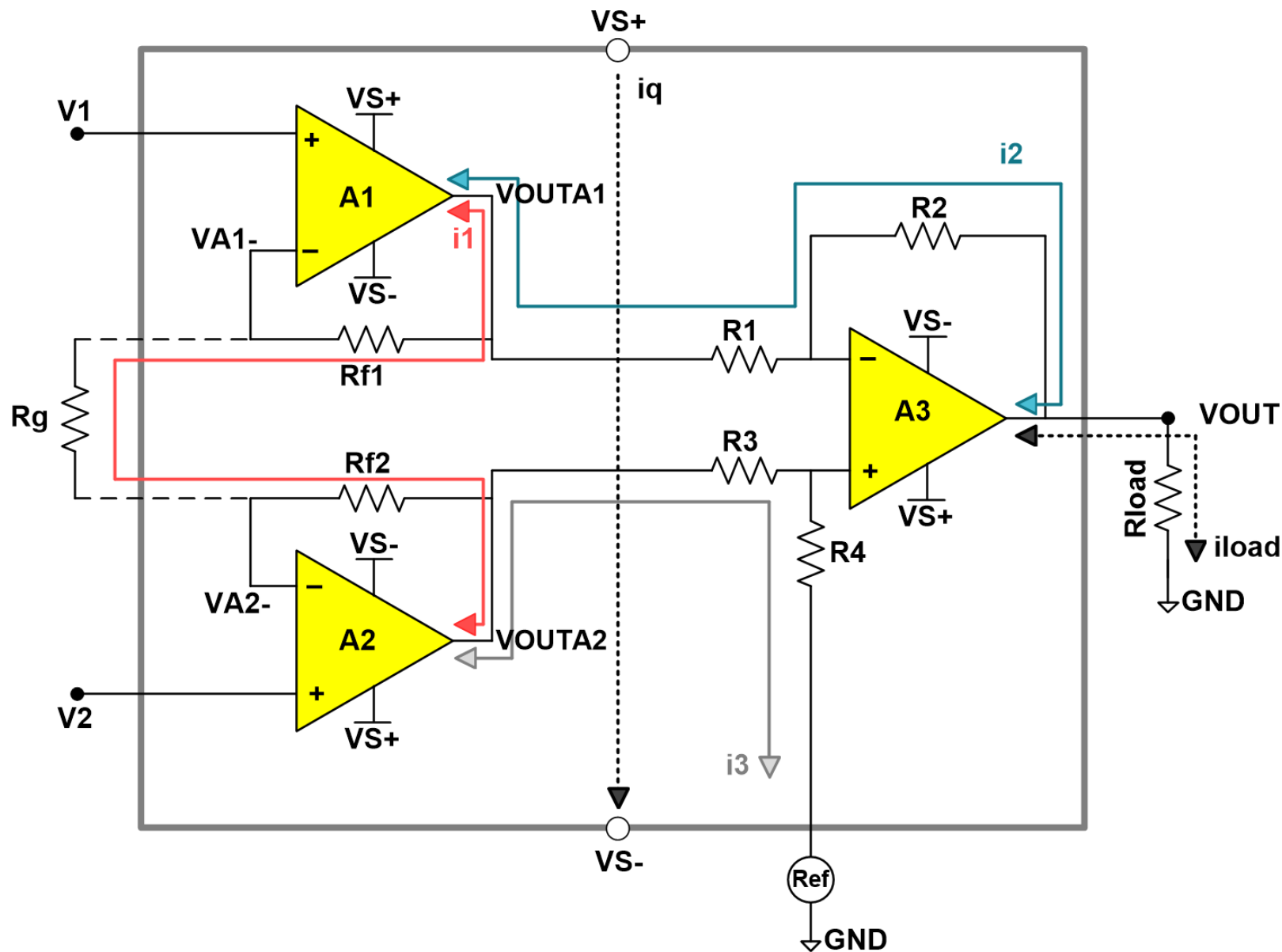
$V_d = 10mV$, $V_{CM} = 1V$

Expected V_{out} is $3V$

Gain = $300V/V$, $R_g = 167.2\Omega$



Common mistakes – Current consumption

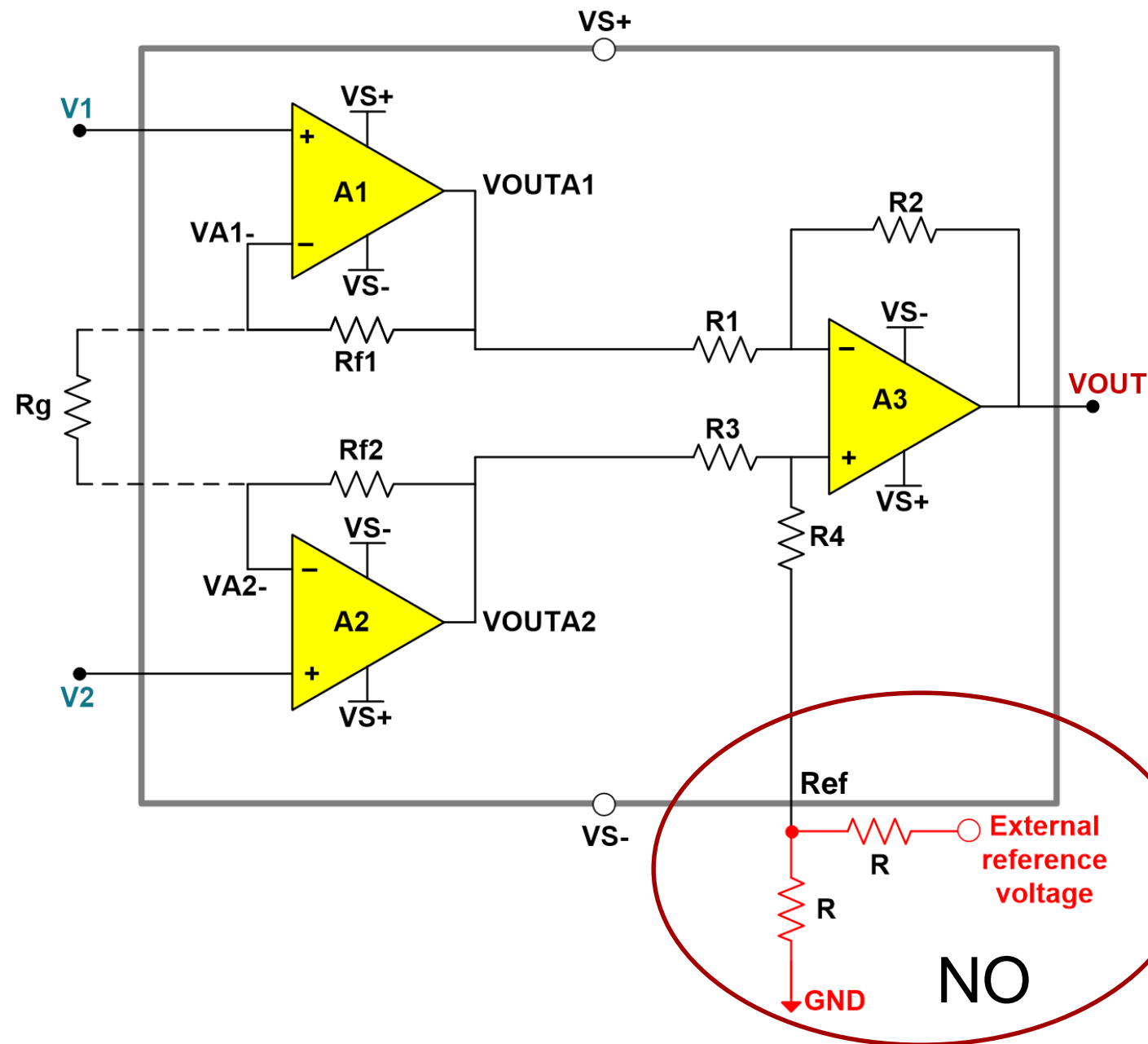


Current consumption of an IA is the sum of all load currents (i_1 , i_2 , and i_3) in addition to the quiescent current and any loading on V_{out} .

- **i_1** : between V_{OUTA1} and V_{OUTA2} through R_{f1} , R_g , and R_{f2} and back through the power supplies.
- **i_2** : between V_{OUT} and V_{OUTA1} through R_2 & R_1 , back through the power supplies.
- **i_3** : between V_{OUTA2} and Ref through R_3 & R_4 and back through the power supplies.

[Analog engineer's calculator → IA Current Consumption](#)

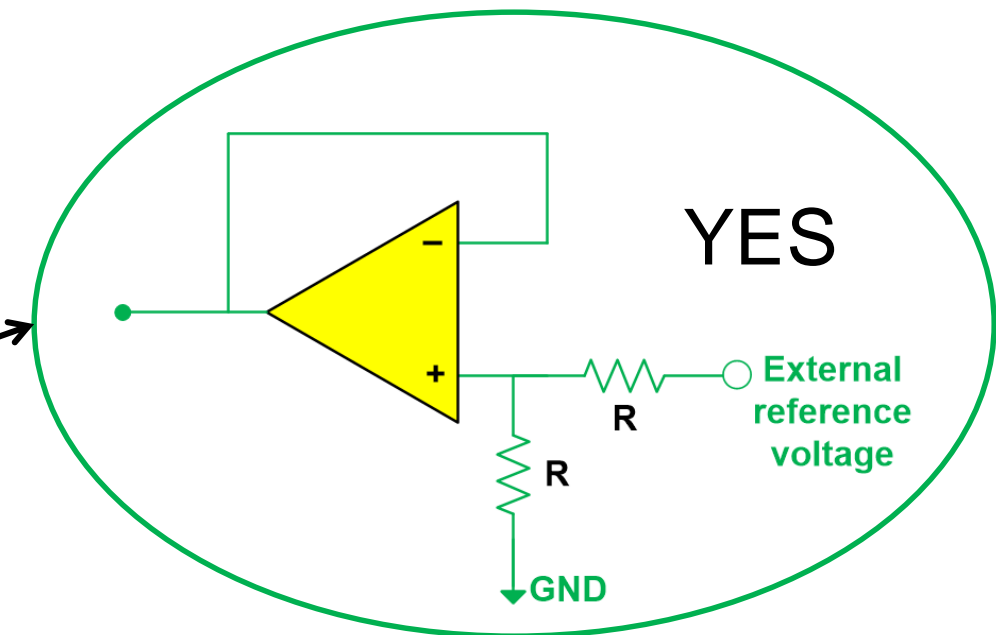
Common mistakes – Driving the Ref pin



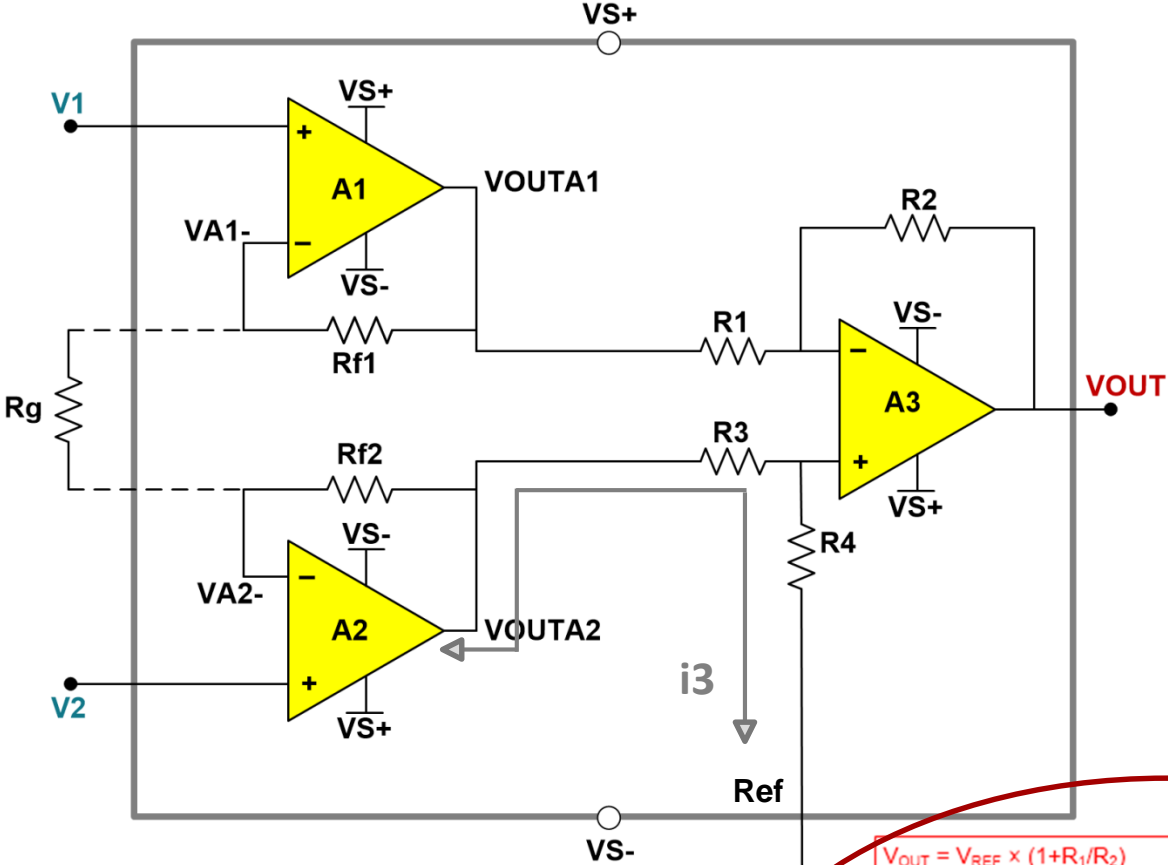
Do **NOT** drive with resistor divider

Assuming A3 is in unity gain ($R_1 = R_2 = R_3 = R_4$), if we add a resistor divider to the Ref pin, this additional resistance combines with R_4 creating a mismatch to R_1 , R_2 and R_3 so A3 is no longer in unity gain! → **CMRR degradation**

Do this



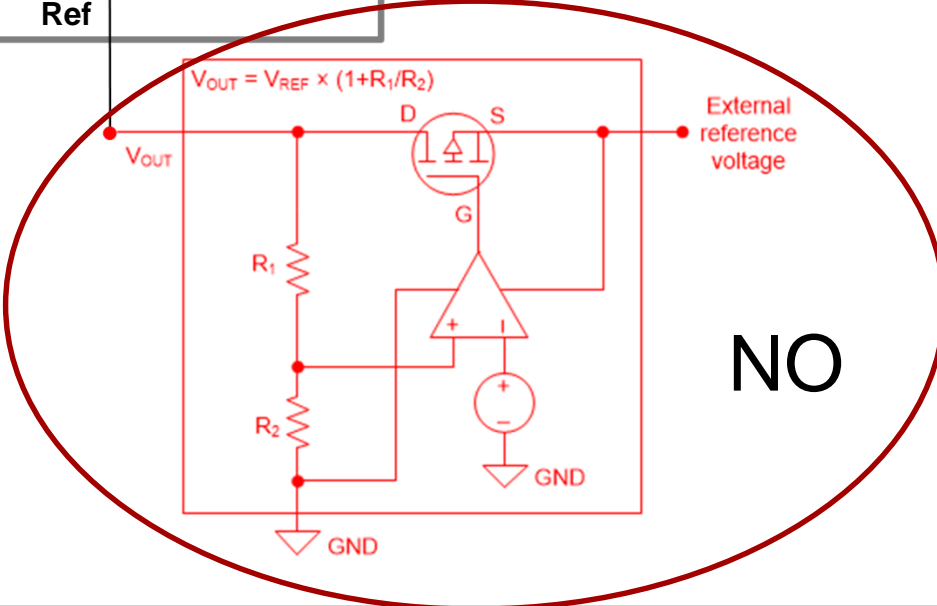
Common mistakes – Driving the Ref pin cont'd



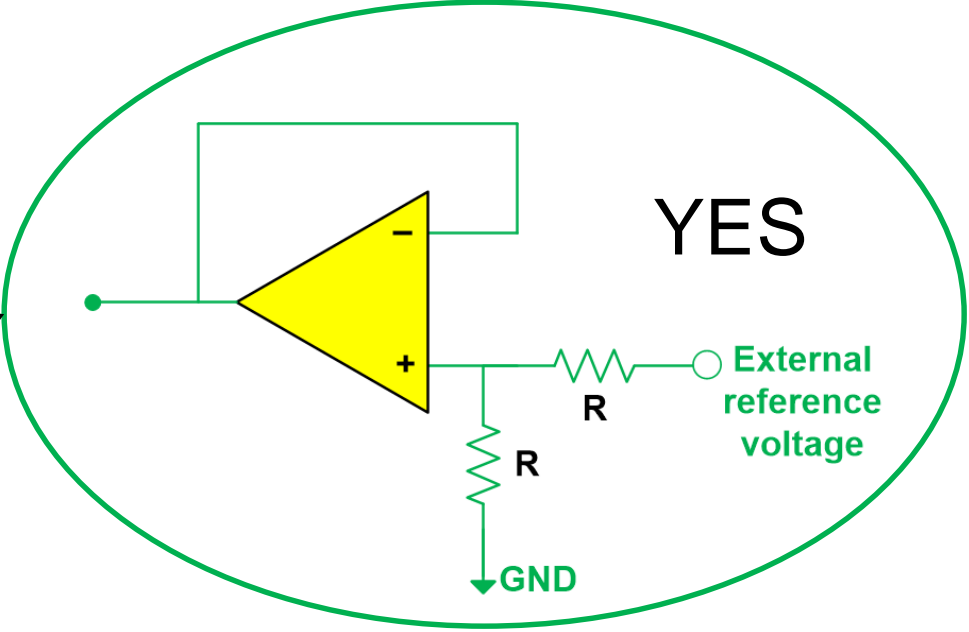
Do **NOT** drive with an LDO

i3: current between VOUTA2 and Ref through R3 & R4 and back through the power supplies.

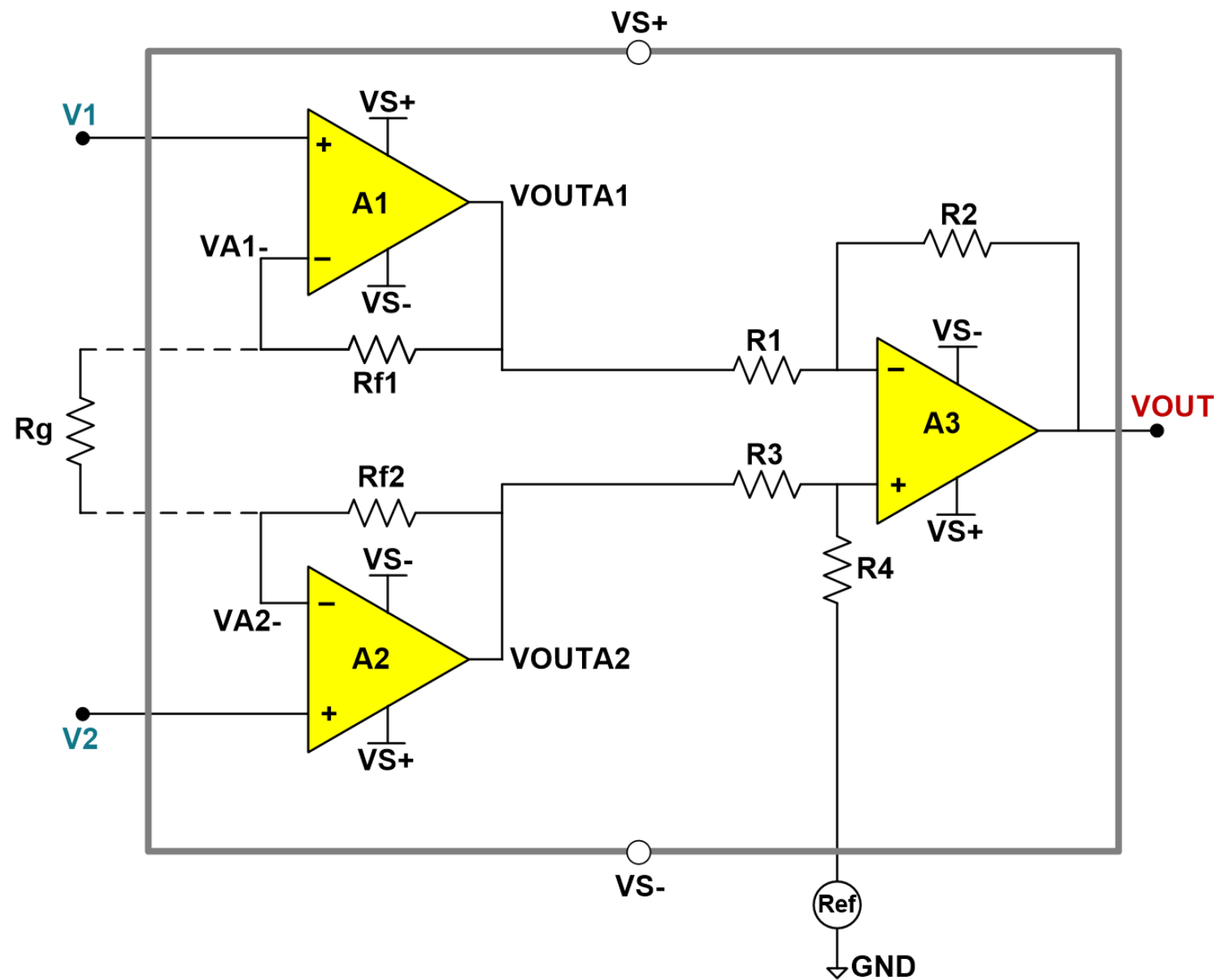
Ref should be able to **sink or source** current depending on the direction of i3



Do this



Instrumentation amplifier topologies – 3 amp summary



Amplifiers A1 and A2:

- balanced input – balanced output stage
- amplifies the differential signal but passes the common mode signal without amplification.
- Responsible for the high input impedance

Amplifier A3:

- forms the second stage of this design as a difference amplifier
- largely removes the common mode signal.

Summary:

If you have an application where you have high impedance sources and high common mode voltages, consider a three-amp IA topology.

Thanks for your time!

To find more Instrumentation Amplifier technical resources and search products, visit [ti.com/inas](https://www.ti.com/inas)

Quiz: Instrumentation Amplifier (IA) topologies: three-amp

TI Precision Labs – Instrumentation Amplifiers

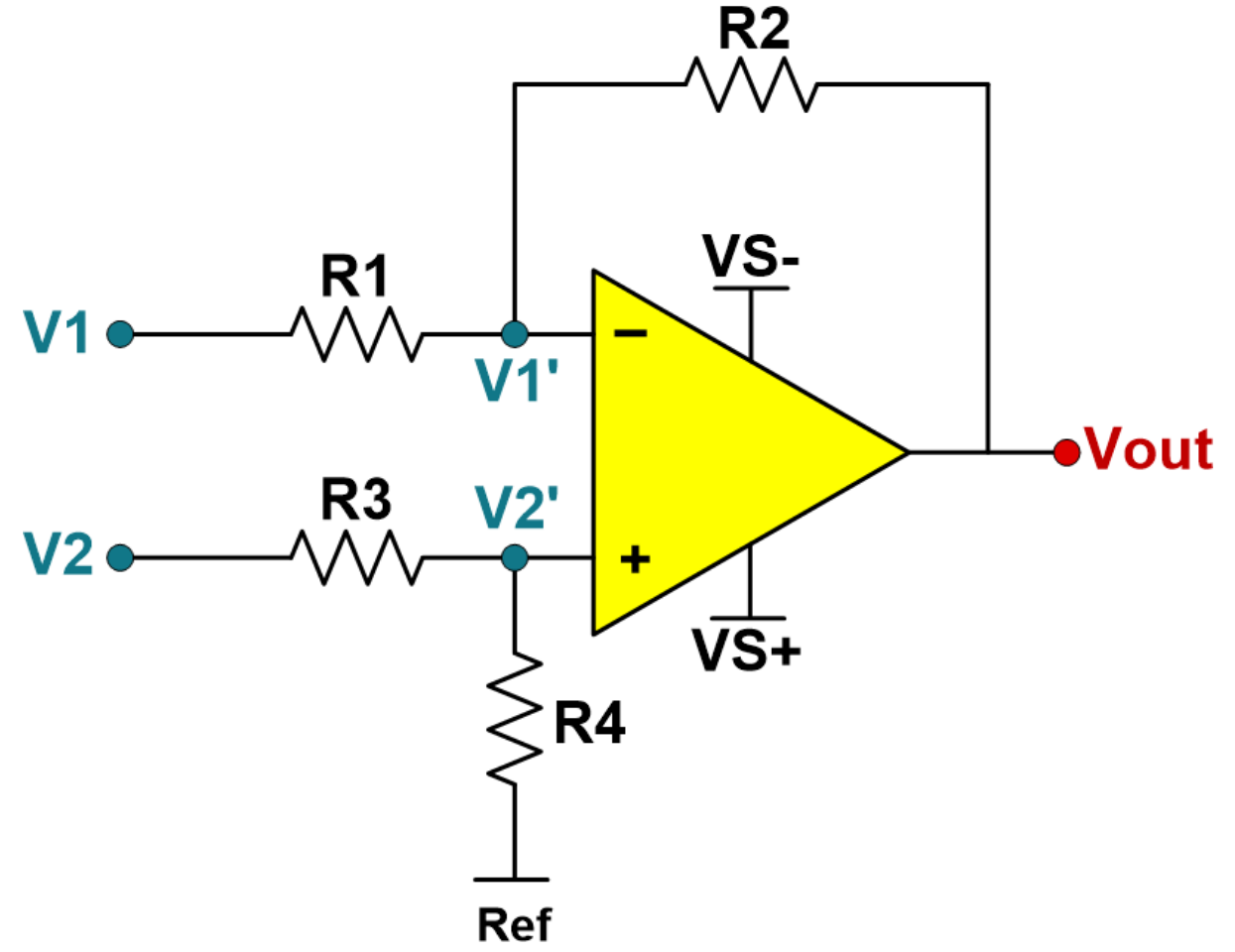
Presented by Tamara Alani

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Quiz: (IA) topologies: three-amp || Question

1. What are two challenges associated with the discrete one-amp IA topology?

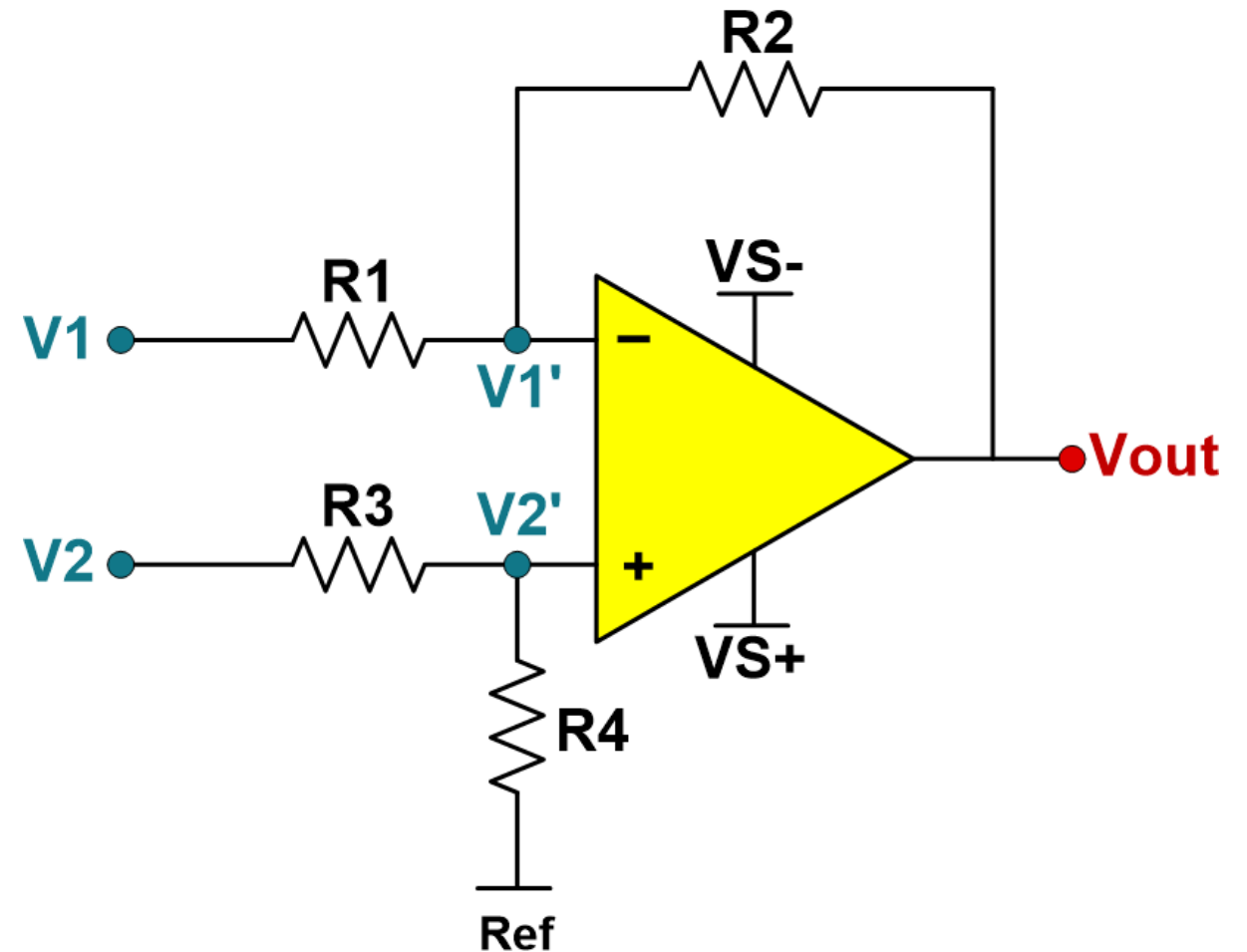
- a) The one-amp IA consumes more power
- b) The one-amp IA has low input impedance
- c) The one-amp IA must have precision-matched resistors for high accuracy
- d) The one-amp IA has fixed gain
- e) The one-amp IA can only be used for mV-level input signals
- f) b & e
- g) c & a
- h) b & c



Quiz: (IA) topologies: three-amp || Answer

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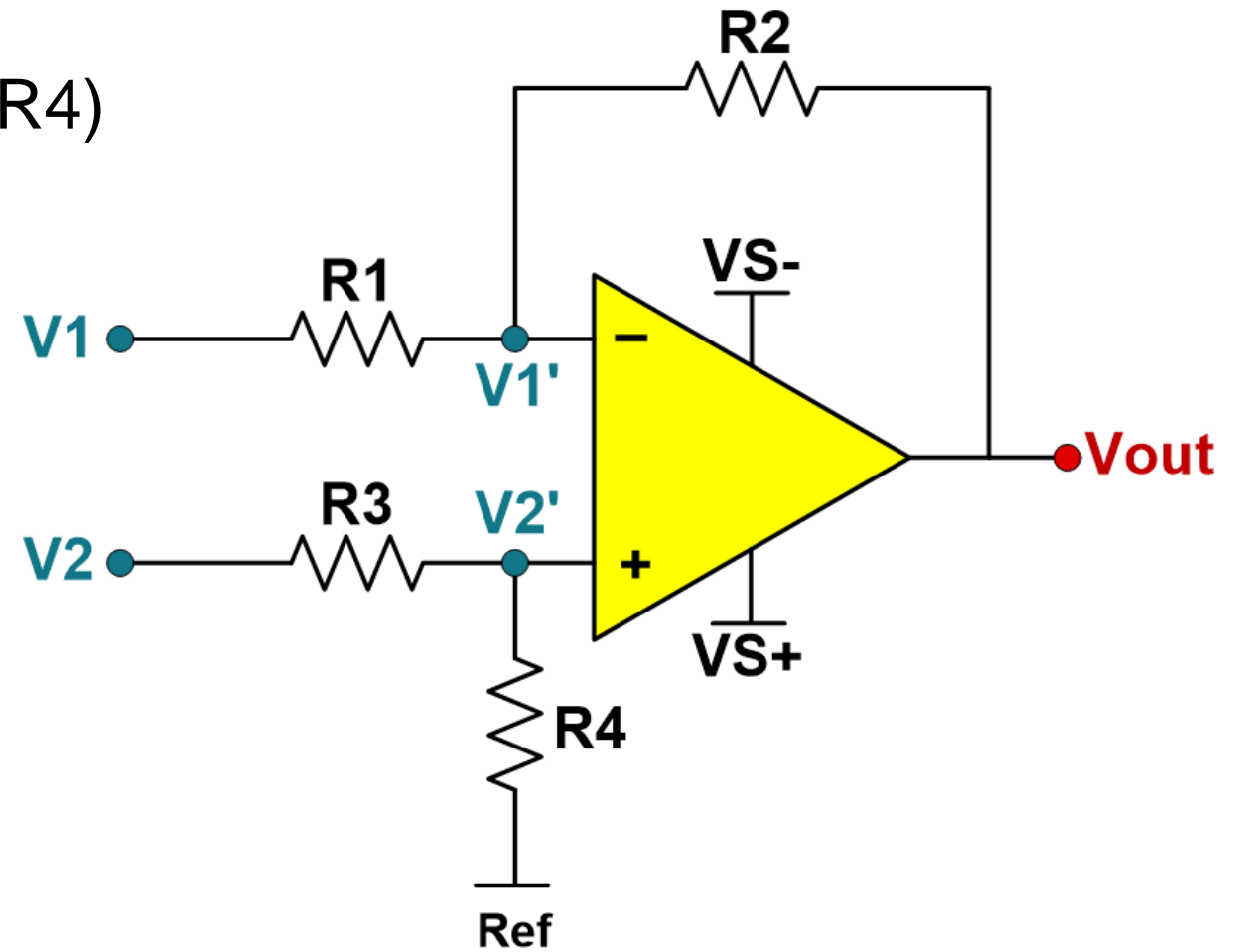
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- f) b & e
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- h) b & c**



Quiz: (IA) topologies: three-amp || Question

2. A one-amp IA has low input impedance. What is best way to resolve this?

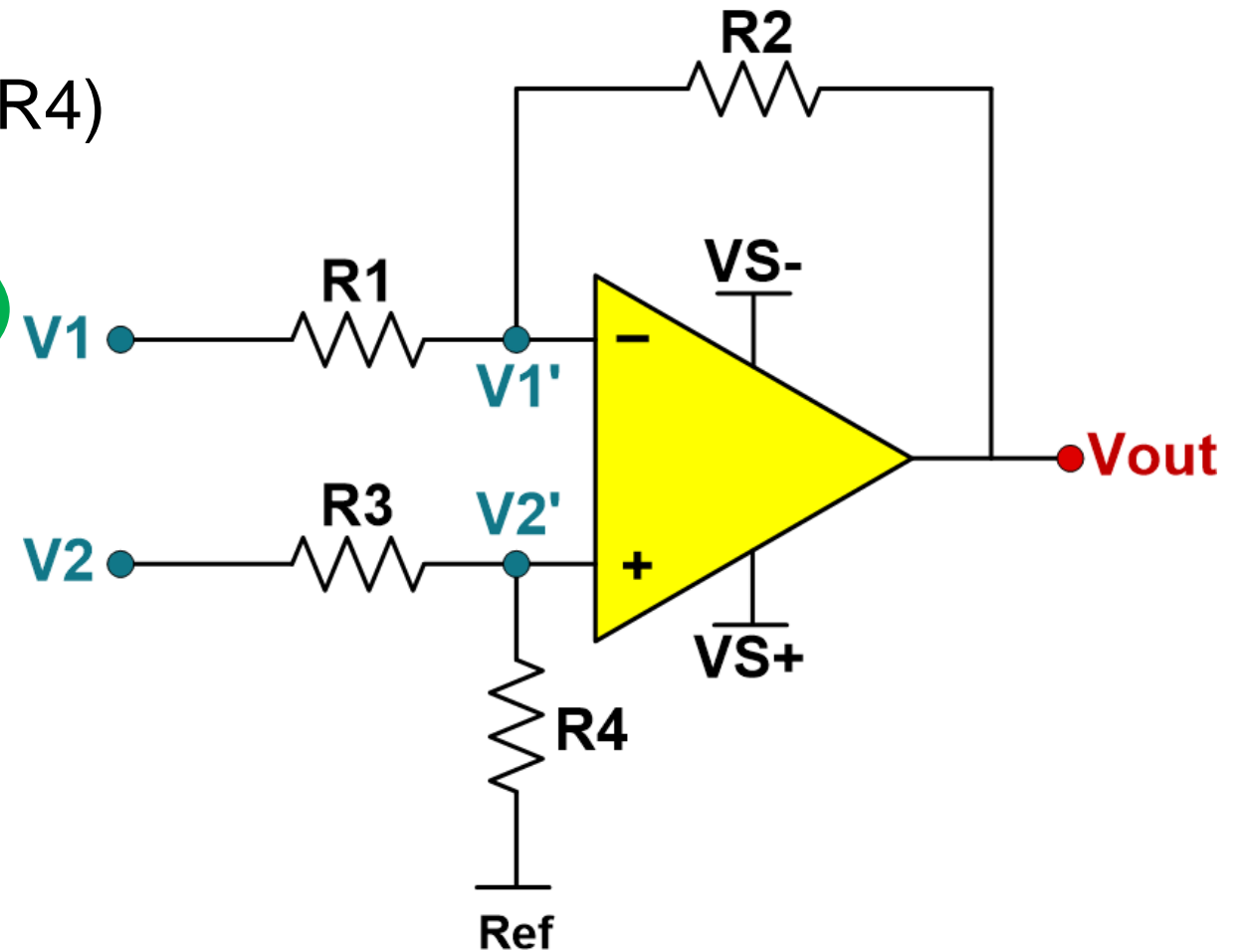
- a) Add really large input resistors (R1 through R4)
- b) Put the amplifier in high gain
- c) Add two buffers at the inputs (V1 and V2)
- d) Find an amplifier with high input impedance



Quiz: (IA) topologies: three-amp || Answer

2. A one-amp IA has low input impedance. What is best way to resolve this?

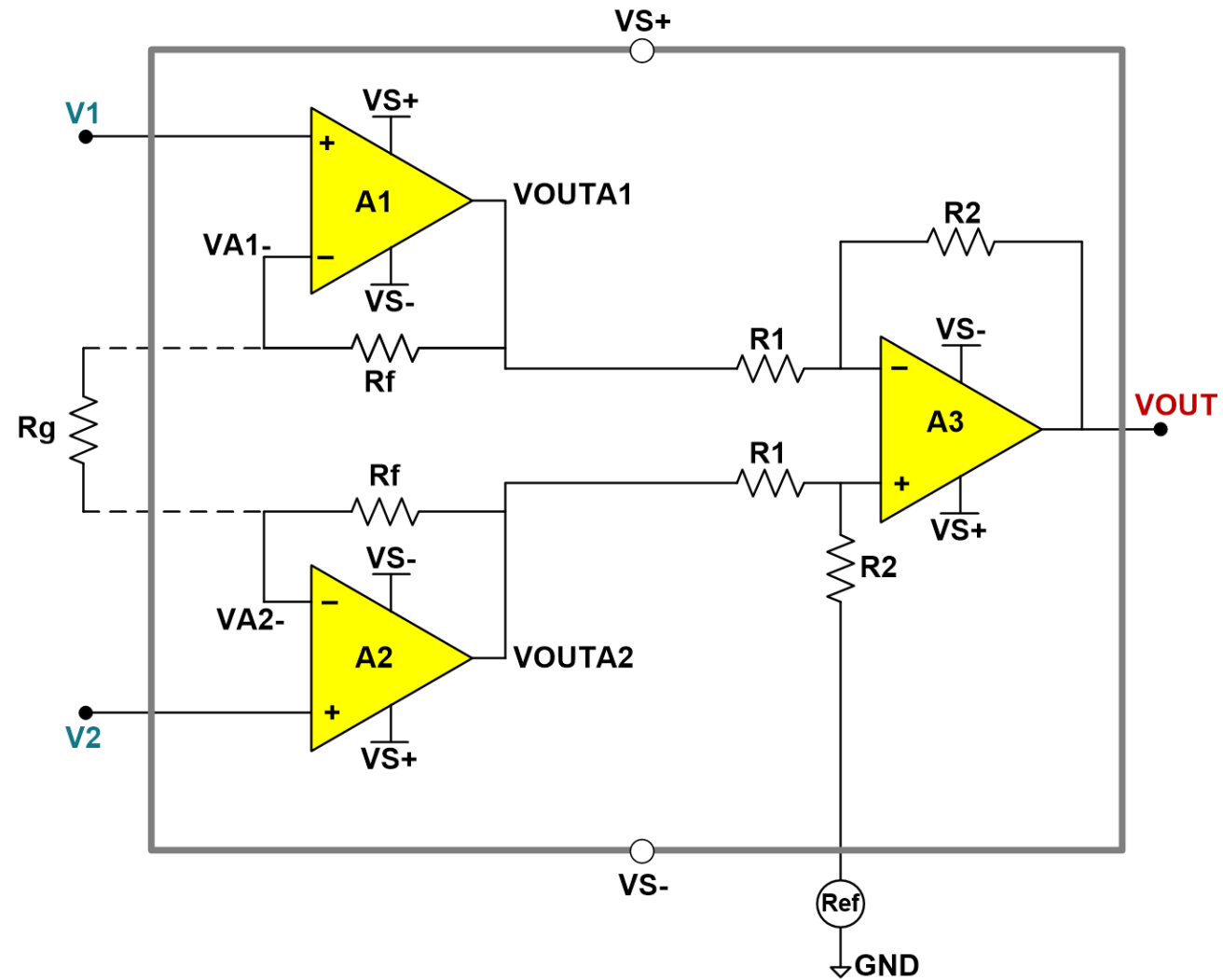
- a) Add really large input resistors (R1 through R4)
- b) Put the amplifier in high gain
- c) Add two buffers at the inputs (V1 and V2)**
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Quiz: (IA) topologies: three-amp || Question

3. What is the gain equation for a three-amp IA?

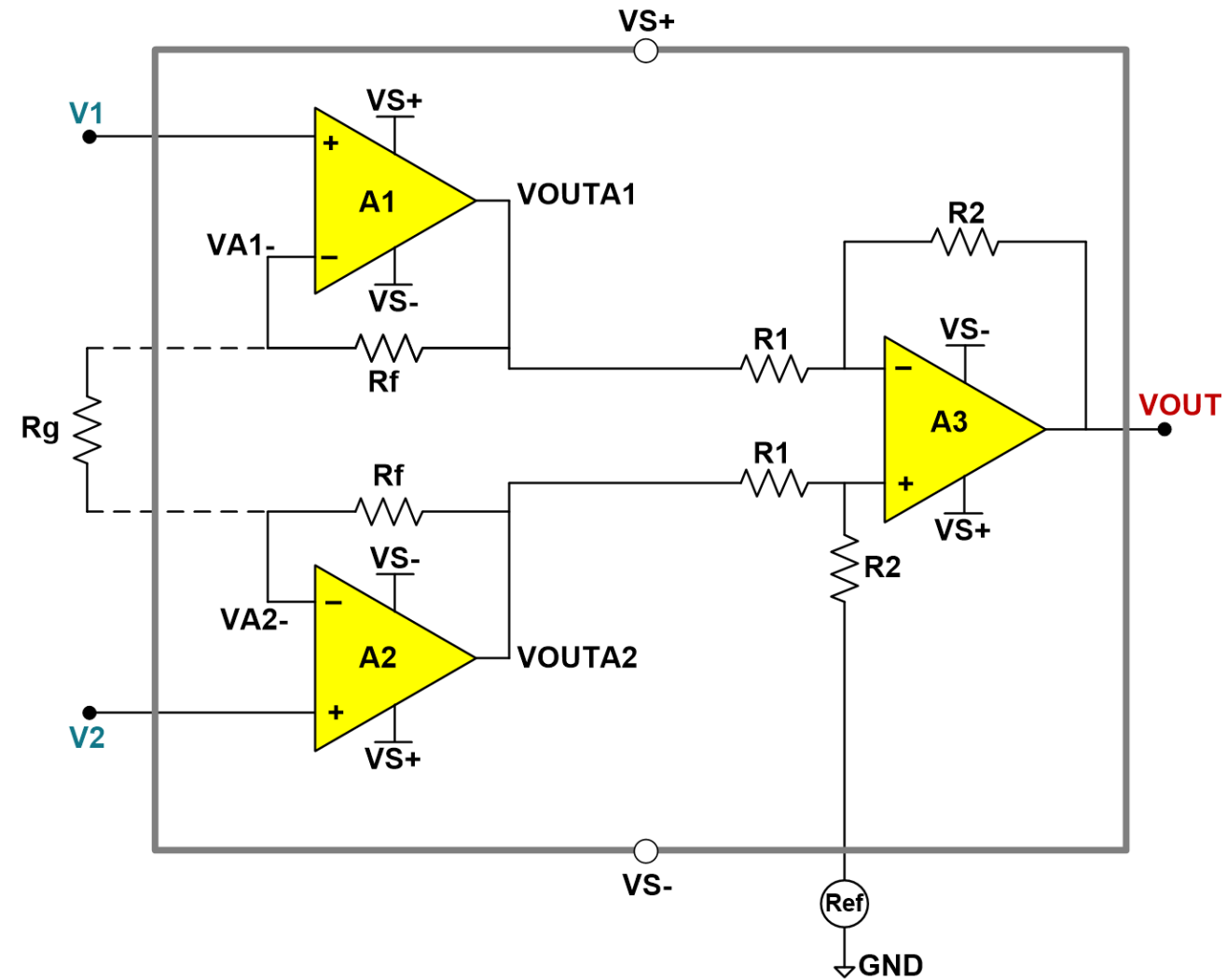
- a) Gain = $\frac{R2}{R1}$
- b) Gain = Rg
- c) Gain = $\frac{R2}{R1} \times (Rg + 2 \times Rf)$
- d) Gain = $\frac{R2}{R1} \times \left(1 + \frac{2 \times Rf}{Rg}\right)$



Quiz: (IA) topologies: three-amp || Answer

3. What is the gain equation for a three-amp IA?

- a) Gain = $\frac{R2}{R1}$
- b) Gain = Rg
- c) Gain = $\frac{R2}{R1} \times (Rg + 2 \times Rf)$
- d) Gain = $\frac{R2}{R1} \times \left(1 + \frac{2 \times Rf}{Rg}\right)$



Quiz: (IA) topologies: three-amp || Question

4. Using the INA333-Q1 (TI's Automotive, Zero-drift, low power IA), what value of R_g do you need to achieve a signal gain of 501V/V?

- a) $R_g = 100\Omega$
- b) $R_g = 200\Omega$
- c) $R_g = 200k\Omega$
- d) $R_g = 501\Omega$

HINT:

Go to the product datasheet:

<https://www.ti.com/lit/ds/symlink/ina333-q1.pdf>

Quiz: (IA) topologies: three-amp || Answer

4. Using the INA333-Q1 (TI's Automotive, Zero-drift, low power IA), what value of R_g do you need to achieve a signal gain of 501V/V?

- a) $R_g = 100\Omega$
- b) $R_g = 200\Omega$**
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- d) $R_g = 501\Omega$

HINT:

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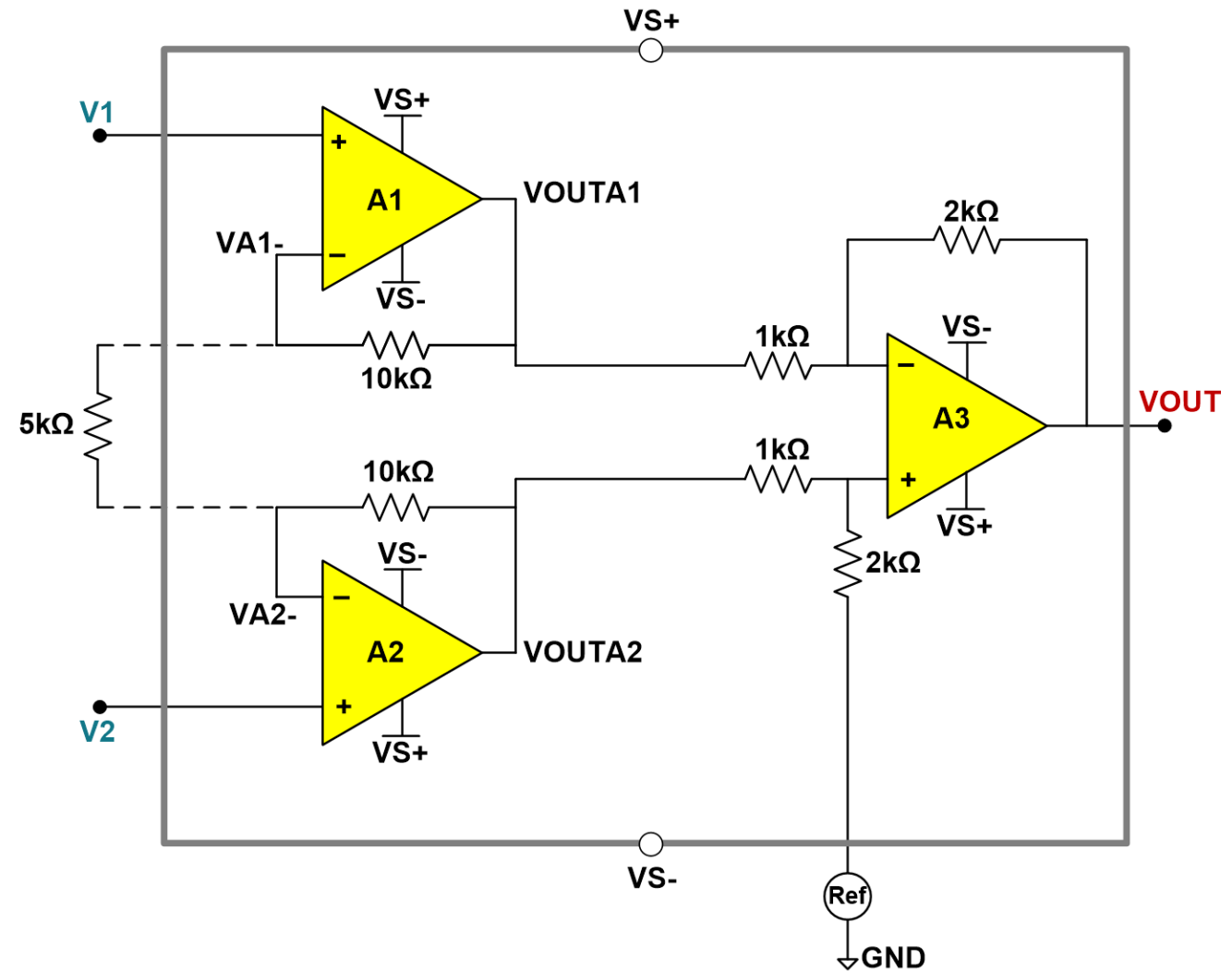
<https://www.ti.com/lit/ds/symlink/ina333-q1.pdf>

$$\text{Gain} = \left(1 + \frac{100k\Omega}{R_g} \right)$$

Quiz: (IA) topologies: three-amp || Question

5. What is the differential gain of the following circuit?

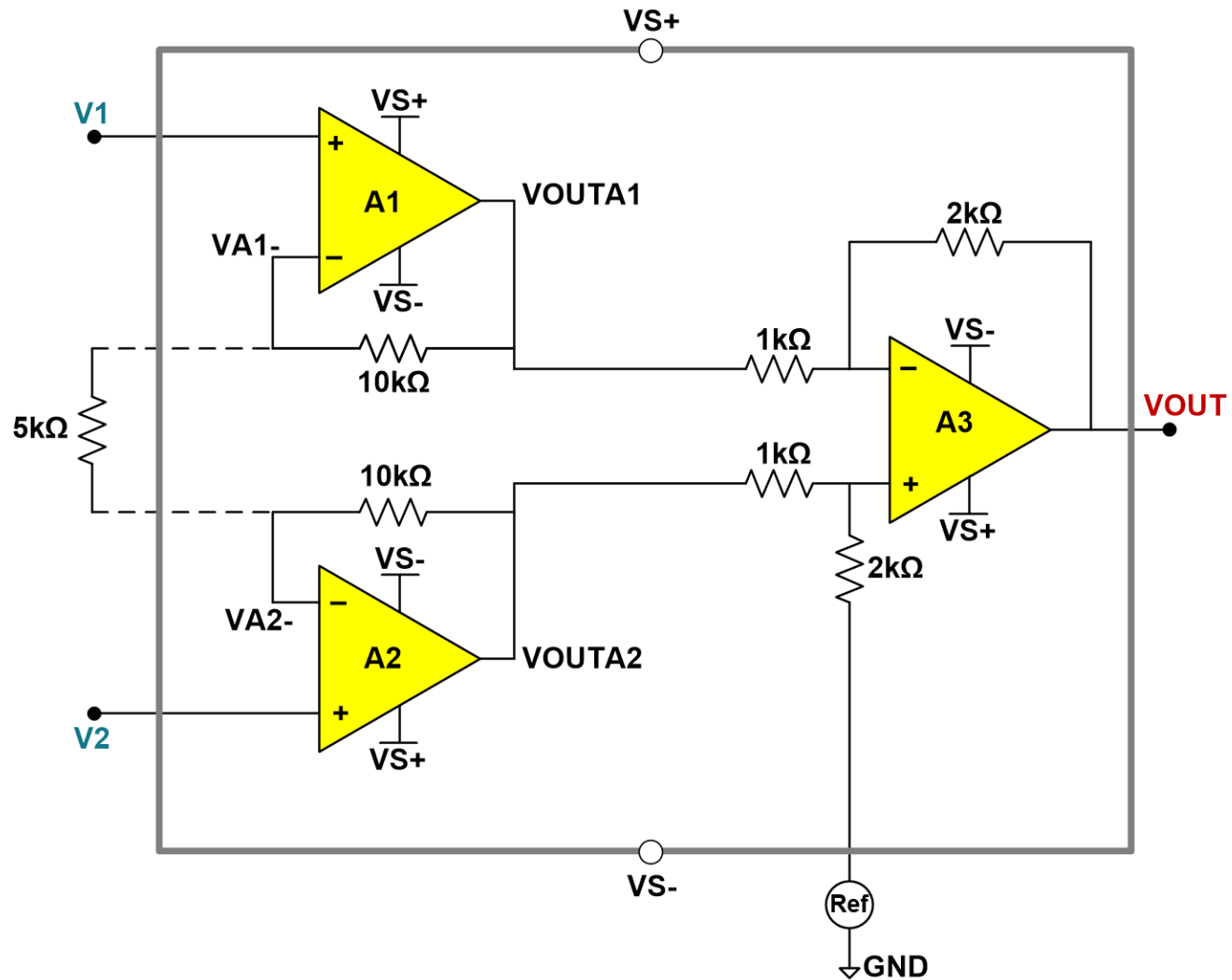
- a) Gain = 5V/V
- b) Gain = 2V/V
- c) Gain = 4V/V
- d) Gain = 10V/V



Quiz: (IA) topologies: three-amp || Answer

5. What is the differential gain of the following circuit?

- a) Gain = 5V/V
- b) Gain = 2V/V
- c) Gain = 4V/V
- d) **Gain = 10V/V**



HINT:

$$A_d = \frac{R_2}{R_1} \times \left(1 + \frac{2R_f}{R_g} \right)$$

Quiz: (IA) topologies: three-amp || Question

6. Using the INA818 (TI's high-precision, low-power IA with over-voltage protection), create a boundary plot for the following conditions:
- Voltage supply = $\pm 15V$
 - Gain = 100V/V
 - Reference = 0V
 - Common mode voltage = 8V

HINT:

Use the INA Boundary Plot calculator in the **Analog Engineer's Calculator**:

<https://www.ti.com/tool/ANALOG-ENGINEER-CALC>

Quiz: (IA) topologies: three-amp || Answer

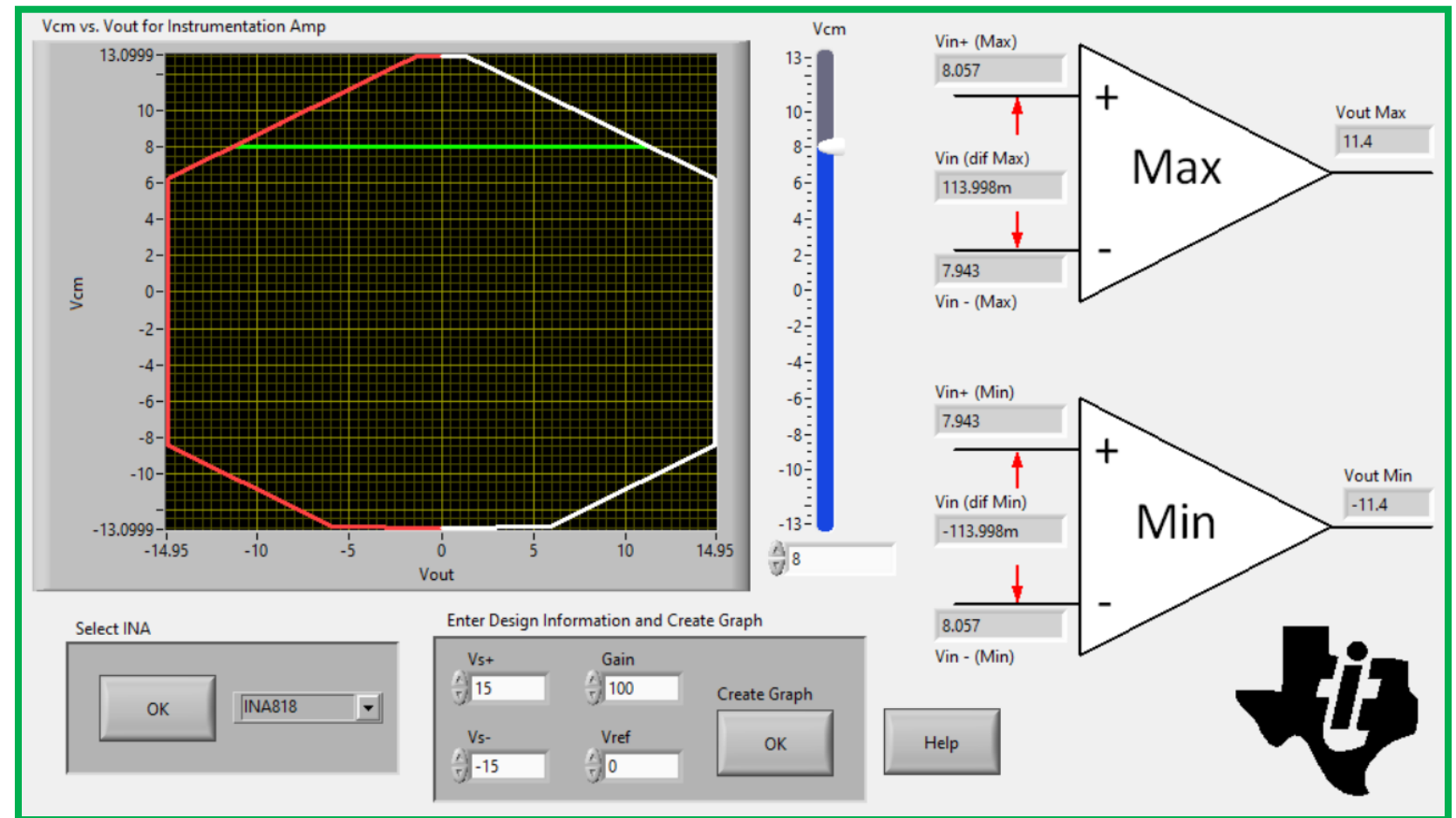
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HINT:

Use the INA Boundary Plot calculator in the **Analog Engineer's Calculator**:

<https://www.ti.com/tool/ANALOG-ENGINEER-CALC>



Quiz: (IA) topologies: three-amp || Question

7. In theory, how does CMRR change with signal differential gain
- a) When signal gain is increased, A_{CM} / A_d will increase so CMRR will double
 - b) When signal gain is decreased, A_{CM} / A_d will increase so CMRR will increase in direct proportion to gain
 - c) When signal gain is increased, A_d / A_{CM} will increase so CMRR will increase by a factor of 1/2
 - d) When signal gain is increased, A_d / A_{CM} will increase so CMRR will increase in direction proportion to gain

Quiz: (IA) topologies: three-amp || Answer

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HINT:

$$CMRR \left(\frac{V}{V} \right) = \frac{\text{differential gain}}{\text{common mode gain}} = \frac{A_d}{A_{CM}}$$

Quiz: (IA) topologies: three-amp || Question

8. What are the typical magnitudes of input impedance for a 3 op amp IA?
- a) $1\ \Omega$ to $1\text{k}\ \Omega$
 - b) $1\text{k}\ \Omega$ to $100\text{k}\ \Omega$
 - c) $100\text{k}\ \Omega$ to $10\text{M}\ \Omega$
 - d) $10^9\ \Omega$ to $10^{12}\ \Omega$

Quiz: (IA) topologies: three-amp || Answer

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- a) 1 Ω to 1k Ω
 - b) 1k Ω to 100k Ω
 - c) 100k Ω to 10M Ω
 - d) **10⁹ Ω to 10¹² Ω**

Quiz: (IA) topologies: three-amp || Question

9. How do you determine the total current consumption of a 3 op amp IA?
- a) Look for the quiescent current specified in the datasheet and multiply it by 3
 - b) (Load currents (i_1 , I_2 , and i_3) + quiescent current) multiplied by 3
 - c) Load currents (i_1 , I_2 , and i_3) + quiescent current + any loading on V_{out}
 - d) (Load currents (i_1 , I_2 , and i_3) + quiescent current)

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