

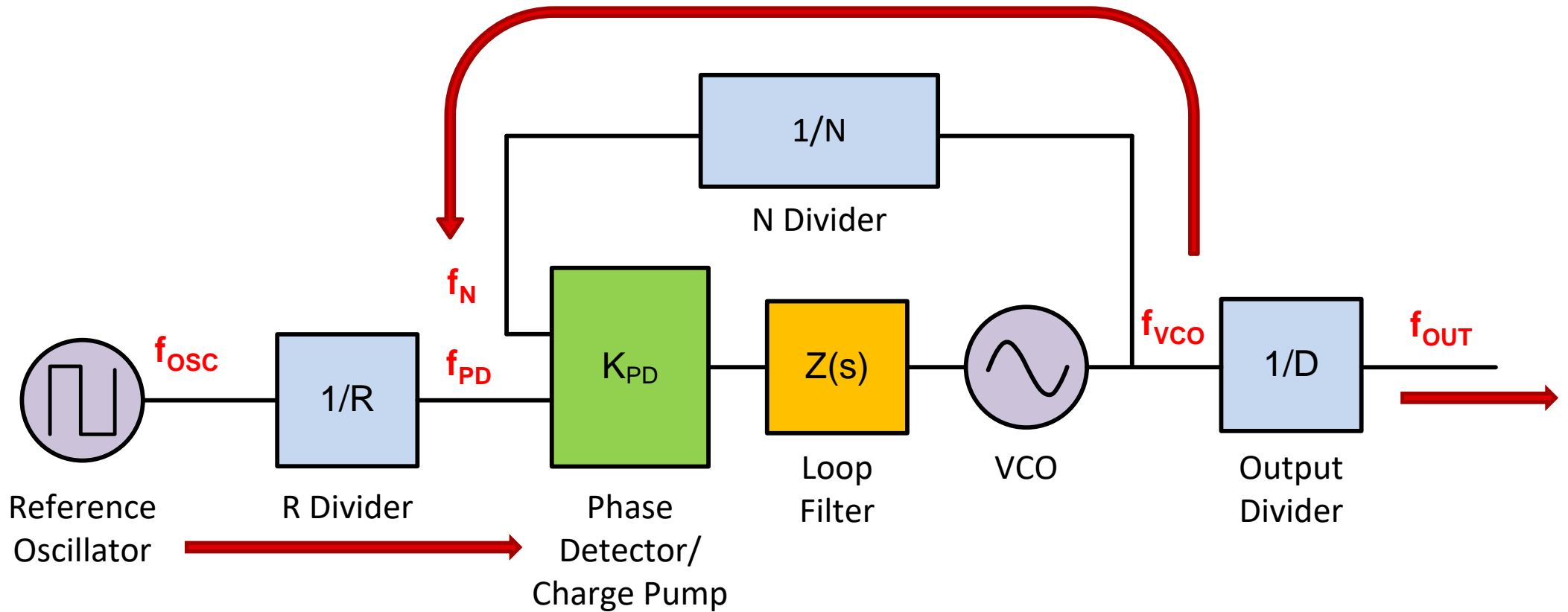
# PLL Transient Response

## TI Precision Labs – Clocks and Timing

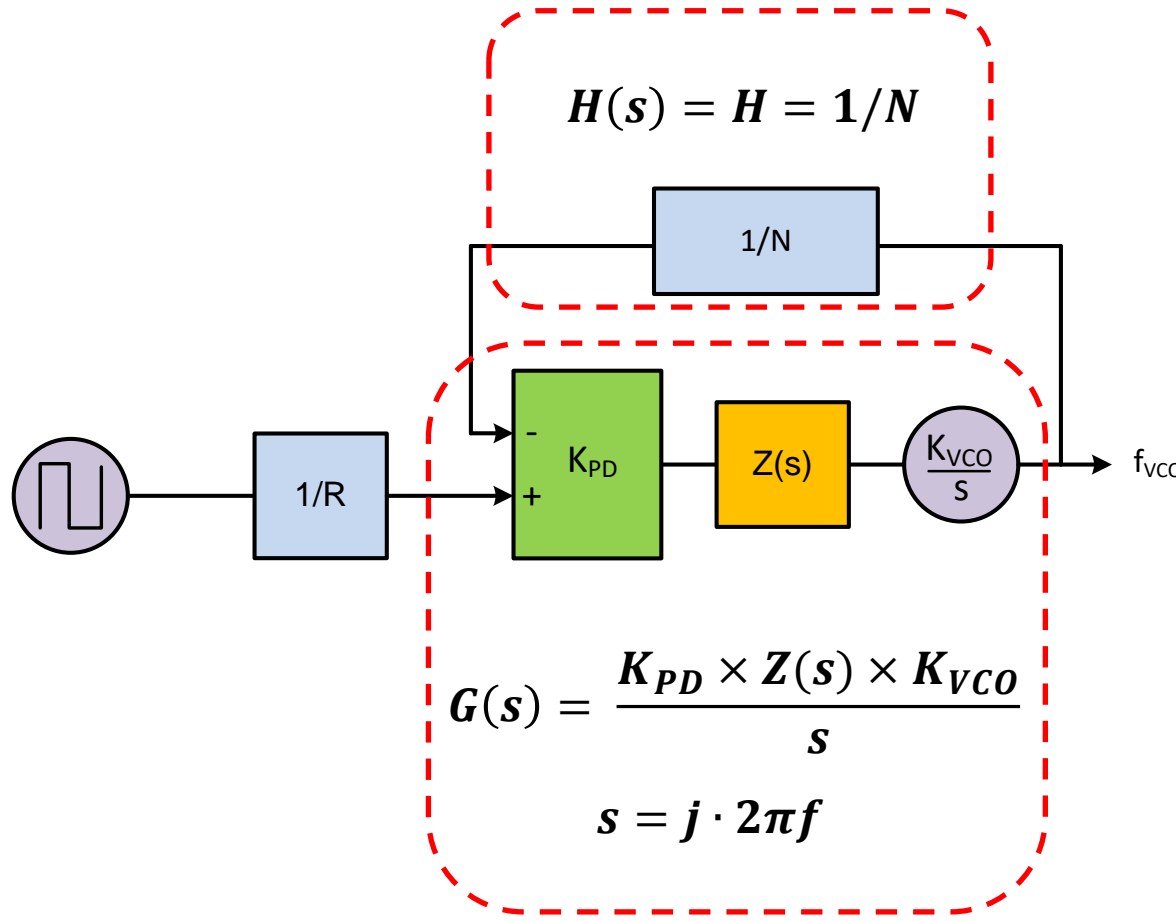
Presented by Dean Banerjee

Prepared by Vibhu Vanjari

# Phase lock loop overview



# PLL loop bandwidth (BW)

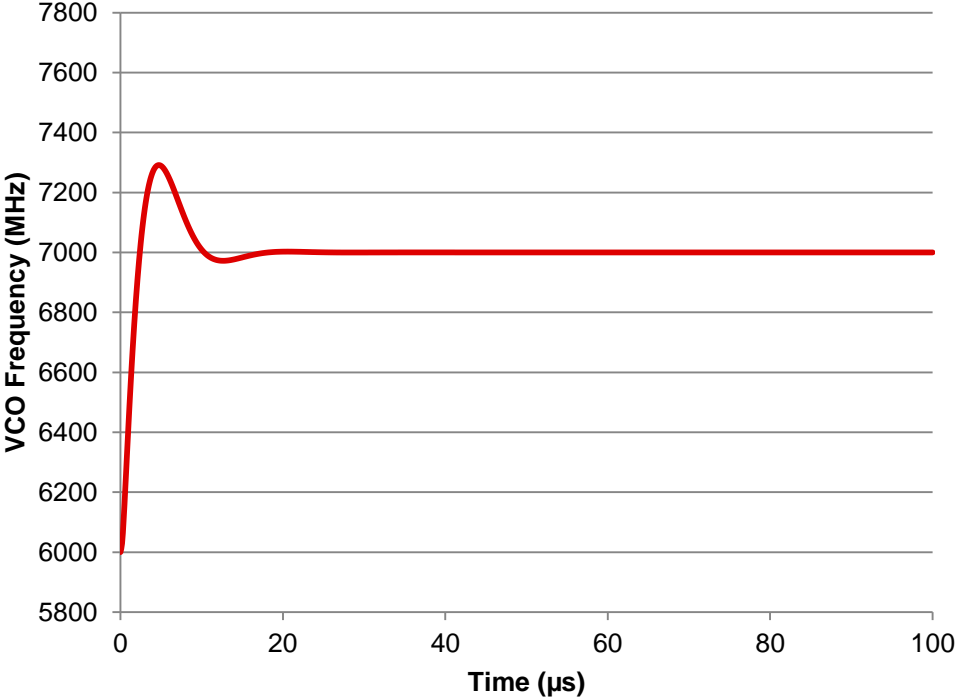


Block	Transfer Function
OSC	$\frac{1}{R} \cdot \frac{G(s)}{1 + G(s) \cdot H}$
R/N Dividers	$\frac{G(s)}{1 + G(s) \cdot H}$
Phase Detector	$\frac{1}{K_{PD}} \cdot \frac{G(s)}{1 + G(s) \cdot H}$
VCO	$\frac{1}{1 + G(s) \cdot H}$

$BW \equiv f : |G(s) \times H| = 1$

# PLL transient response overview

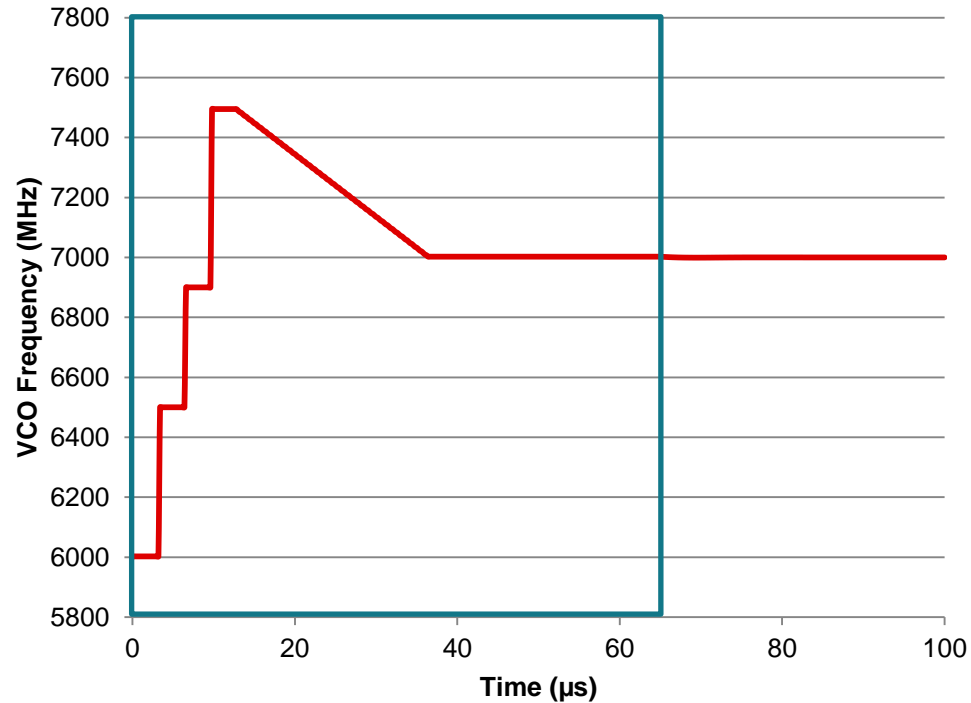
## Analog loop filter transient



Analog lock time = 48 µs  
Total lock time = 48 µs

# PLL transient response overview

## Transient with VCO calibration



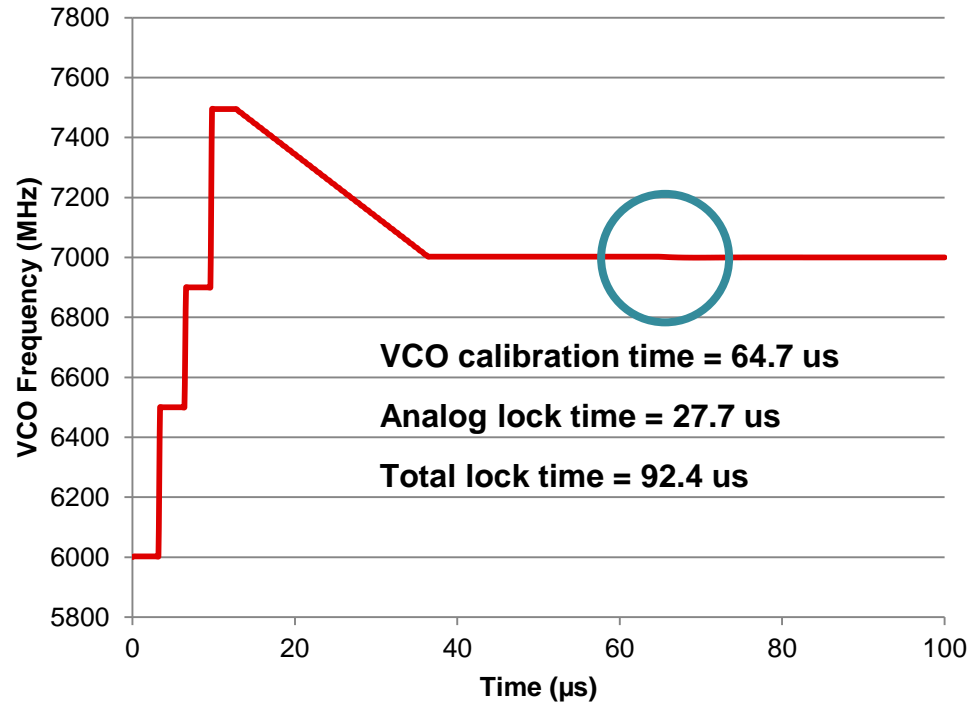
VCO calibration time = 64.7 us

Analog lock time = 27.7 us

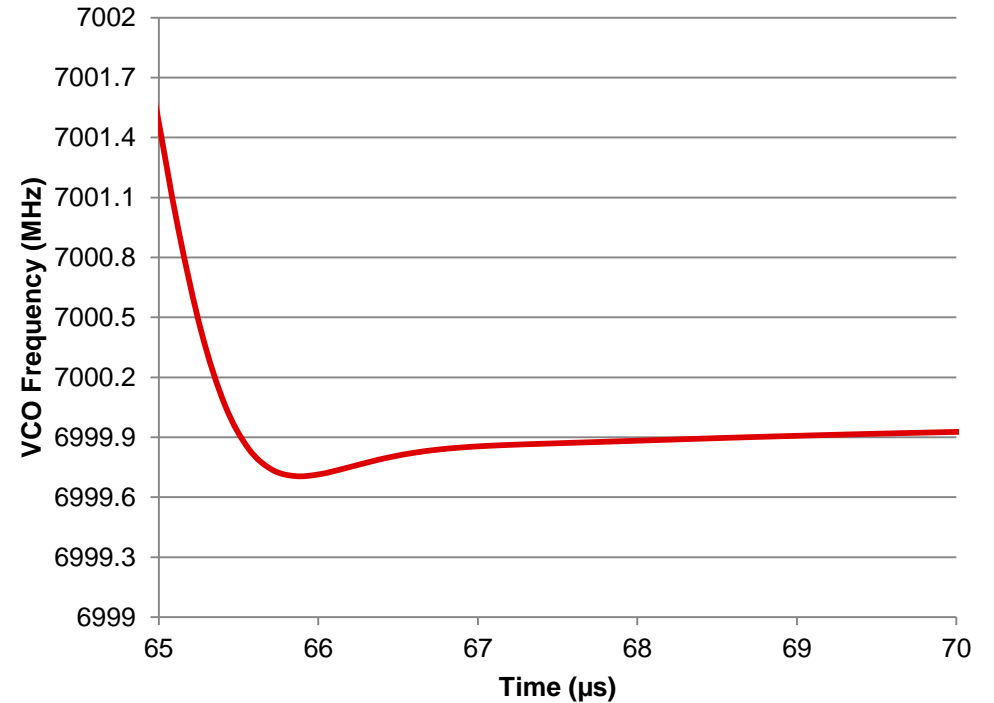
Total lock time = 92.4 us

# PLL transient response overview

## Transient with VCO calibration

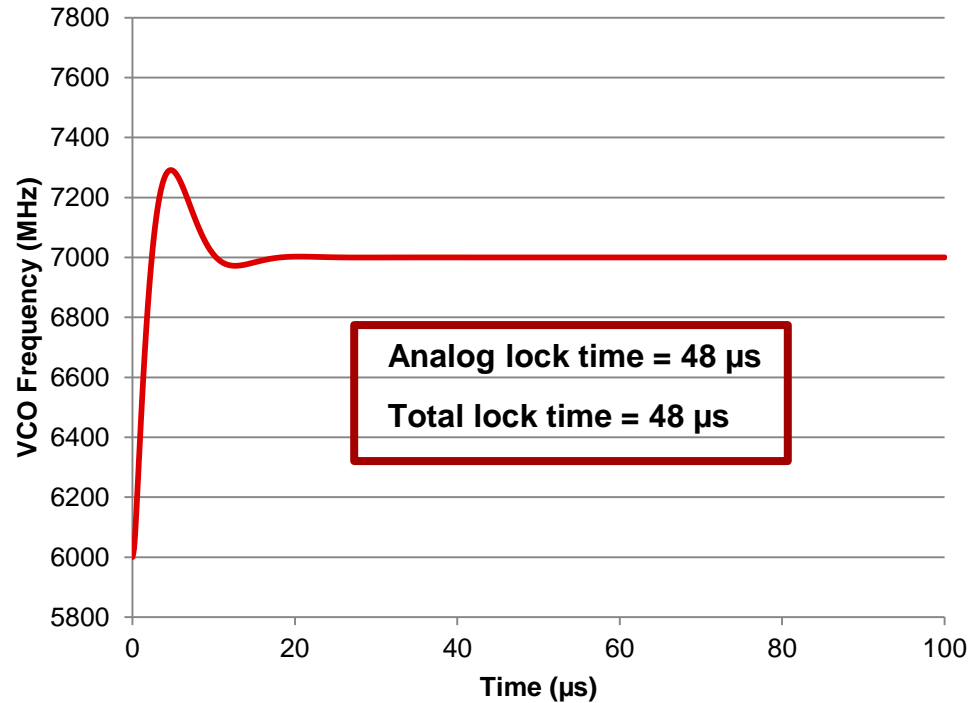


## Zoomed in with VCO calibration

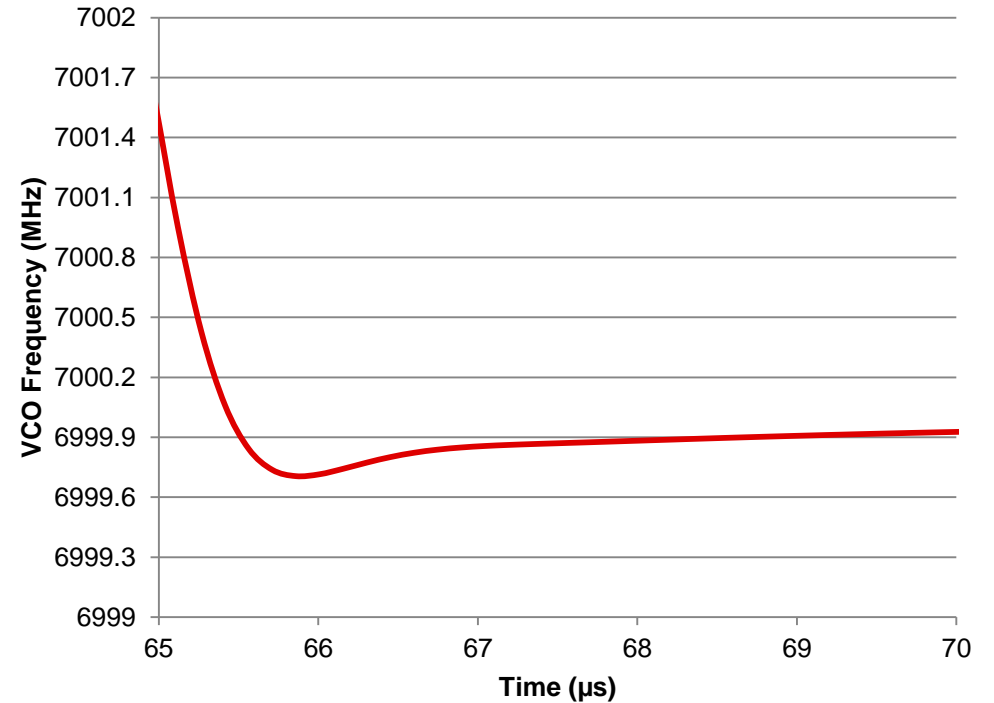


# PLL transient response overview

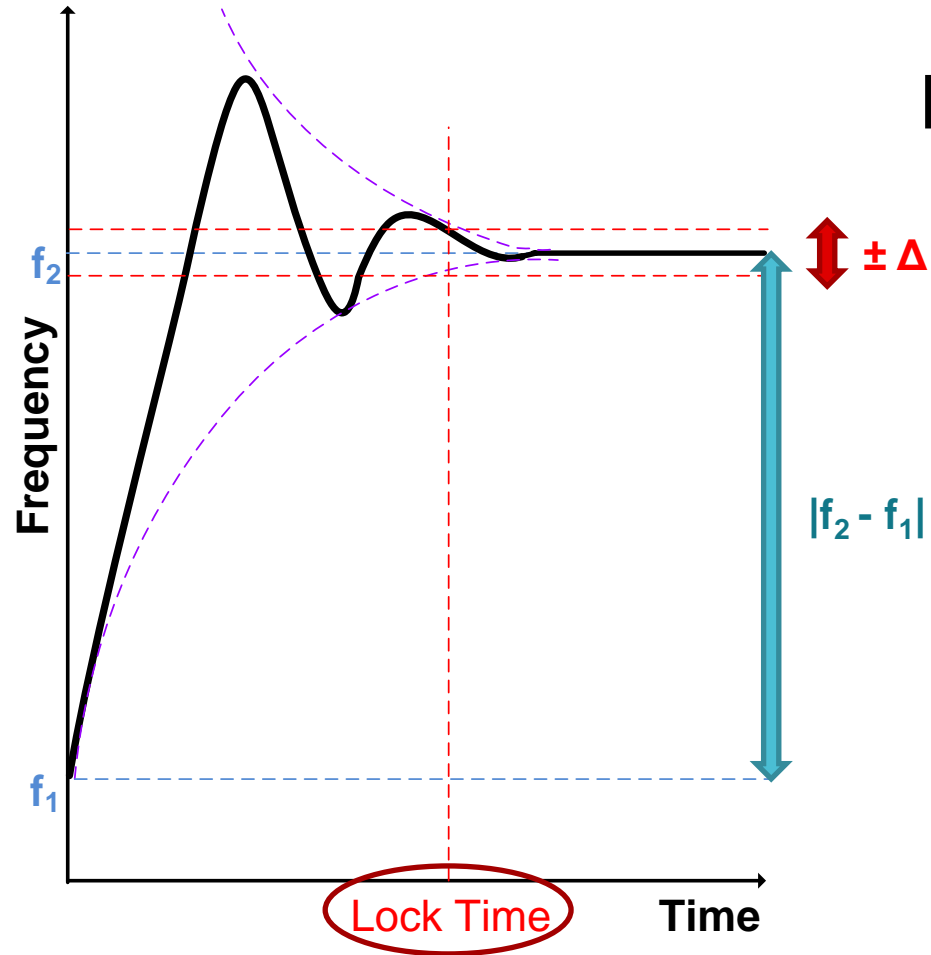
## Analog loop filter transient



## Zoomed in with VCO calibration



# Lock time

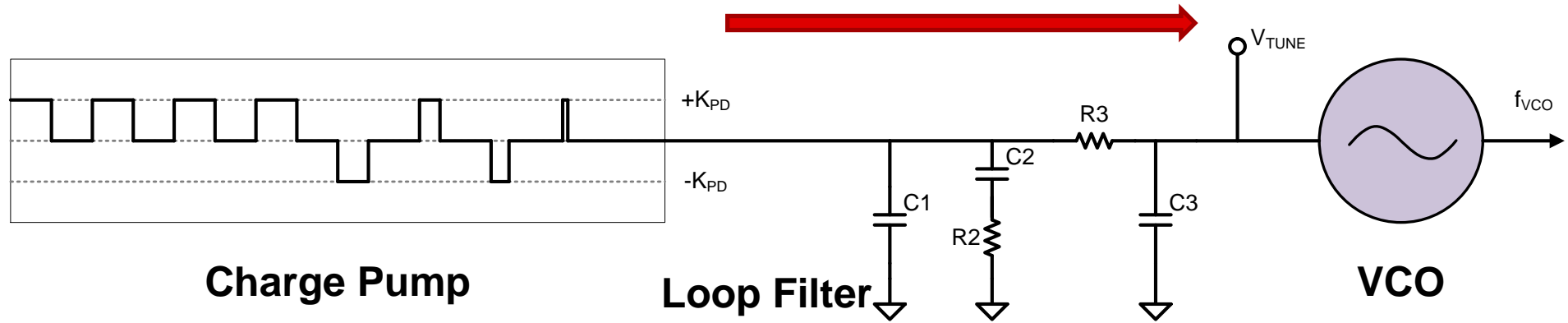


Lock time depends on:

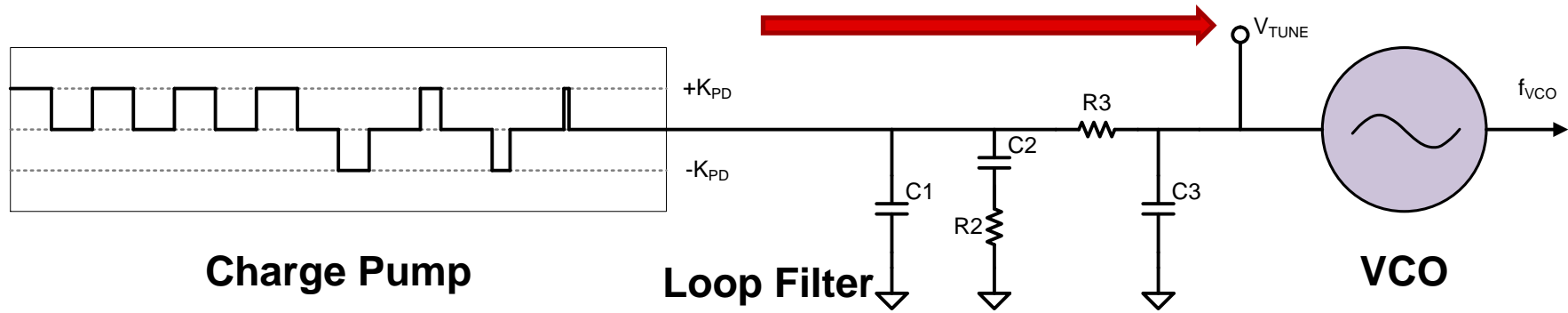
- Frequency jump  $|f_2 - f_1|$
- Tolerance ( $\Delta$ )
- Loop Bandwidth (BW)
- PLL Phase Margin (PM)



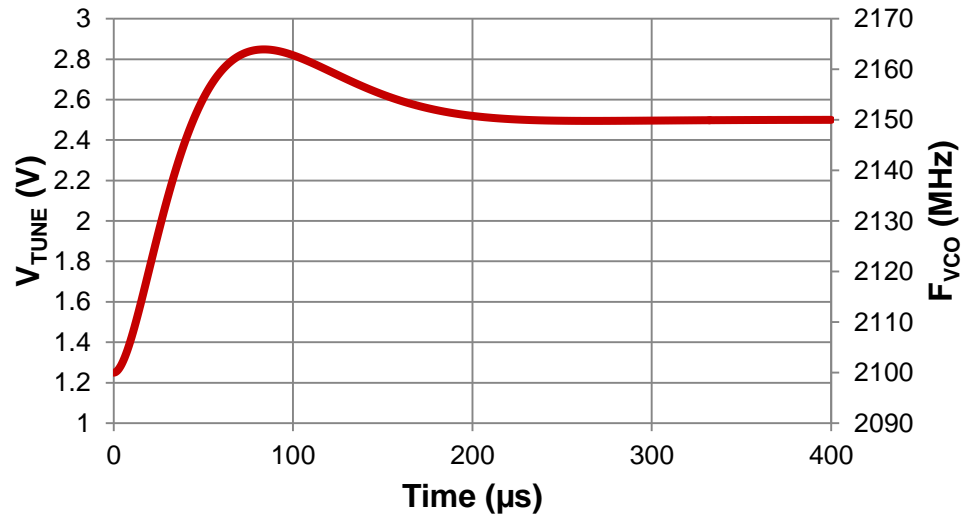
# Transient response



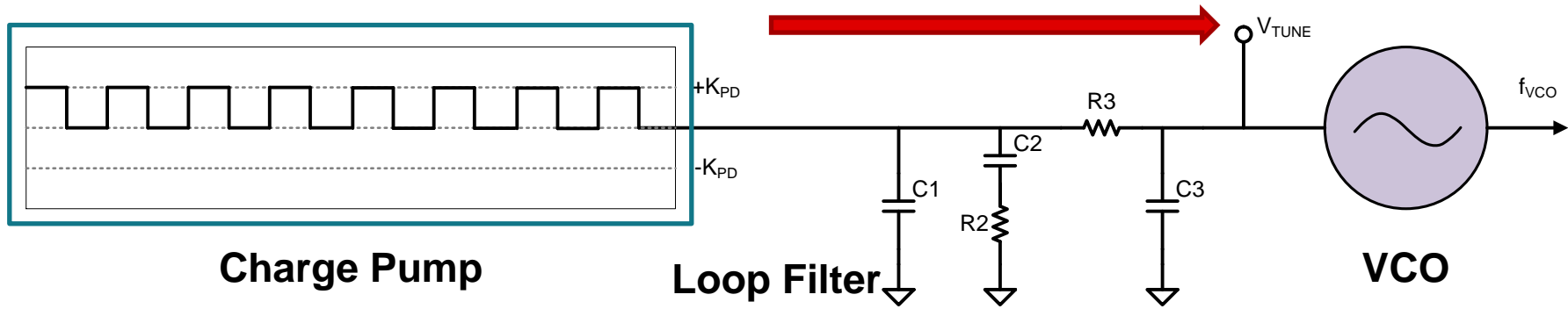
# Transient response



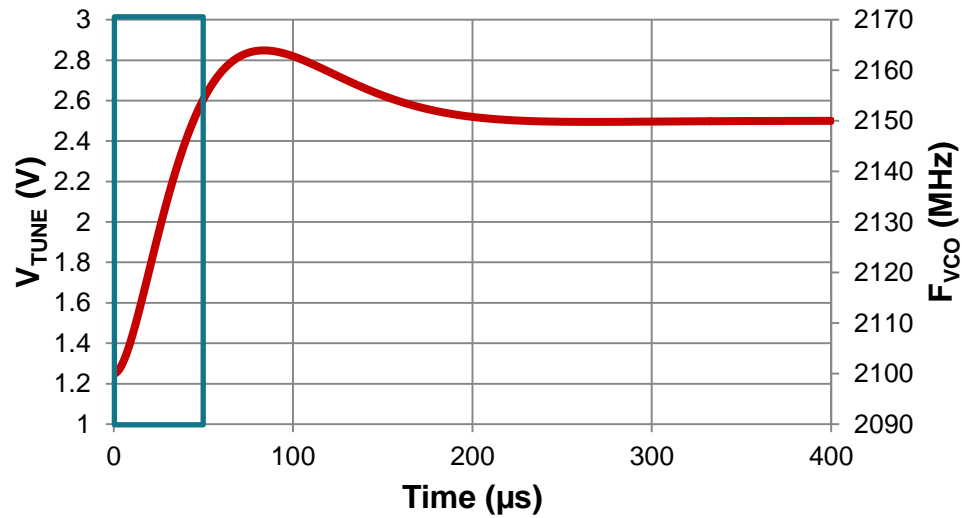
### $F_{VCO}$ and $V_{TUNE}$ transient response



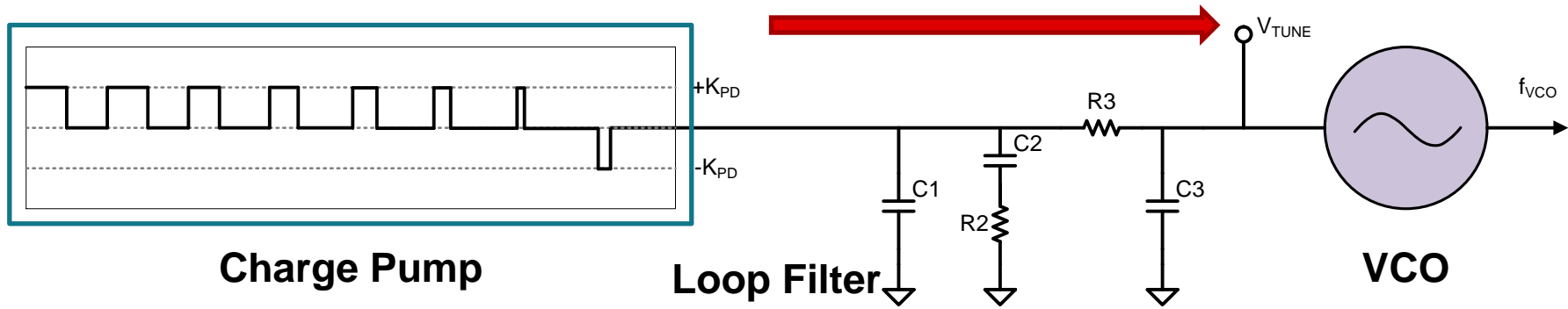
# Transient response



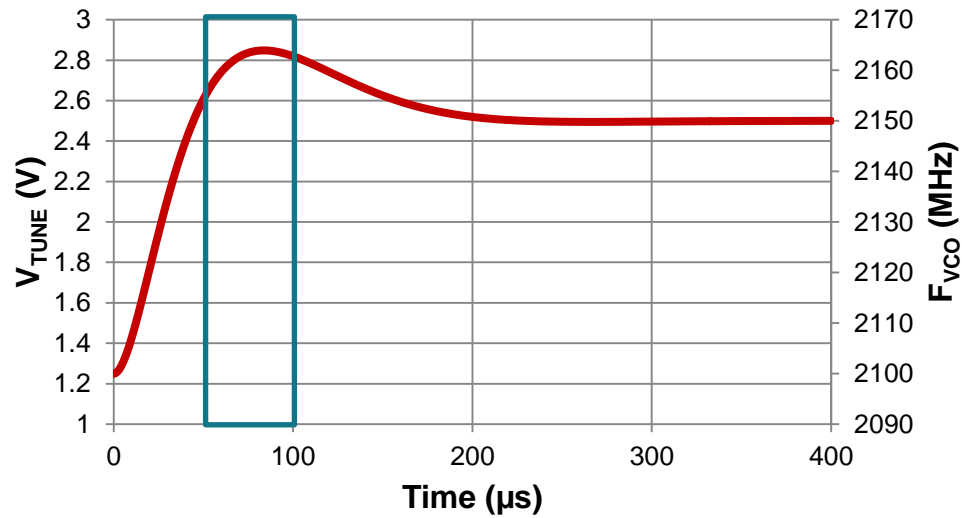
### $F_{VCO}$ and $V_{TUNE}$ transient response



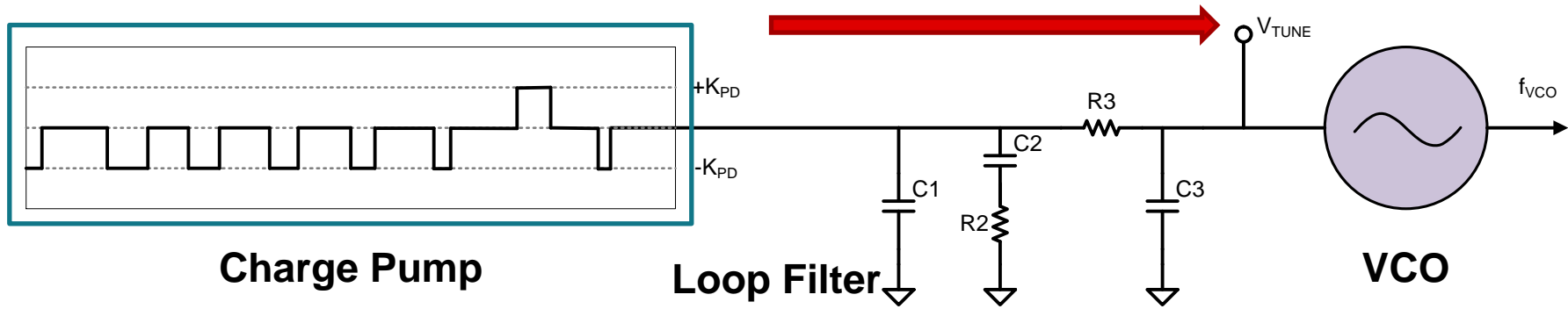
# Transient response



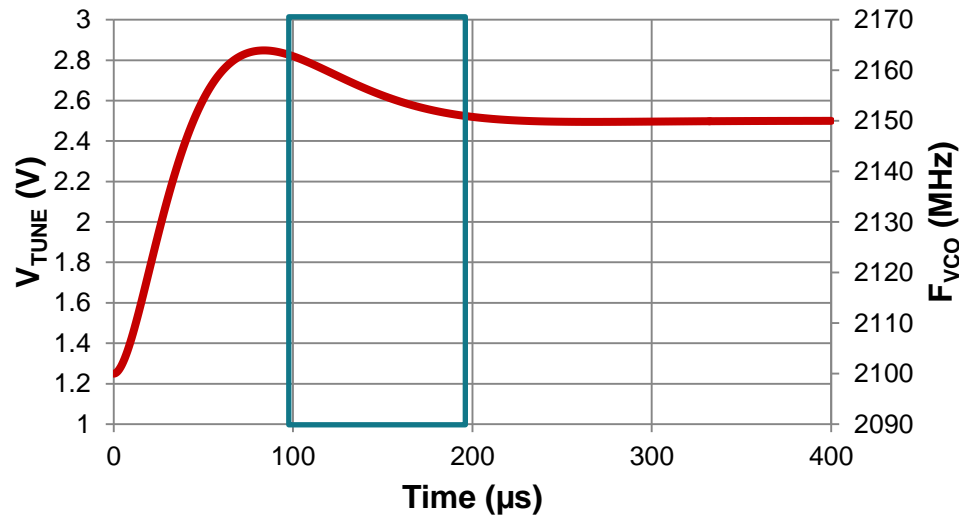
### $F_{VCO}$ and $V_{TUNE}$ transient response



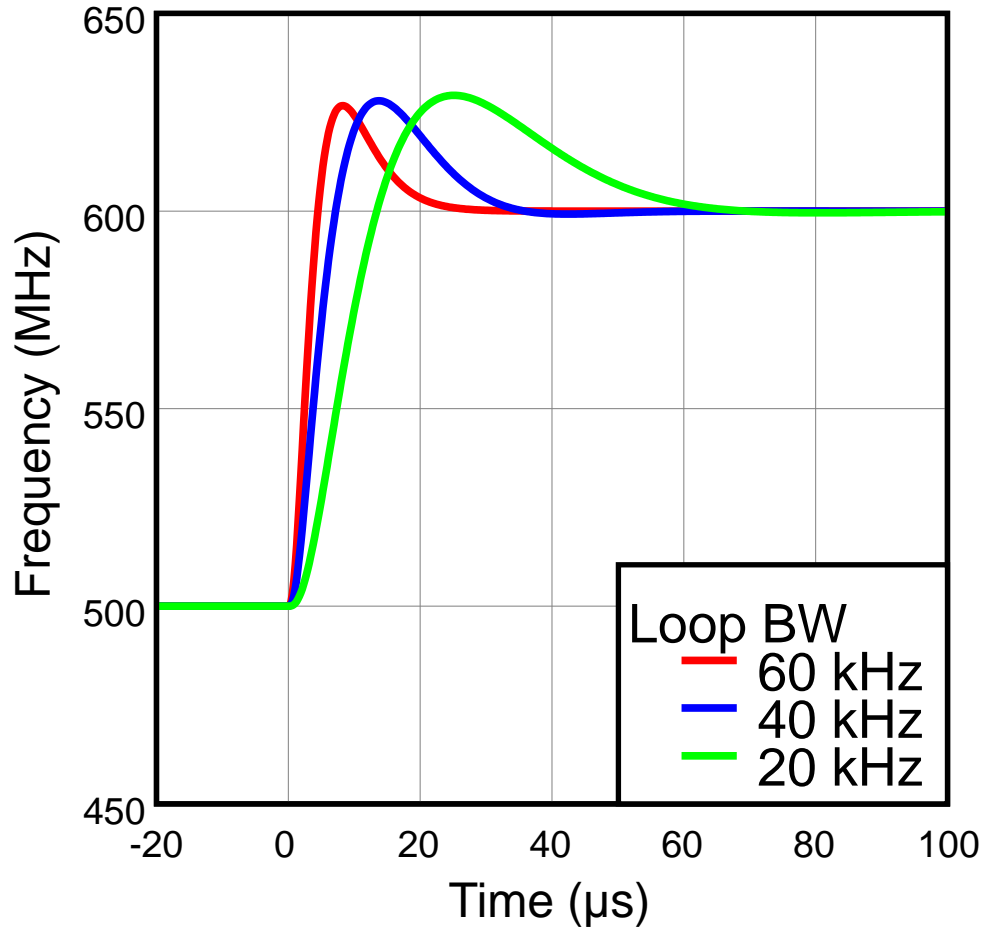
# Transient response



### $F_{VCO}$ and $V_{TUNE}$ transient response



# Bandwidth's impact on lock time

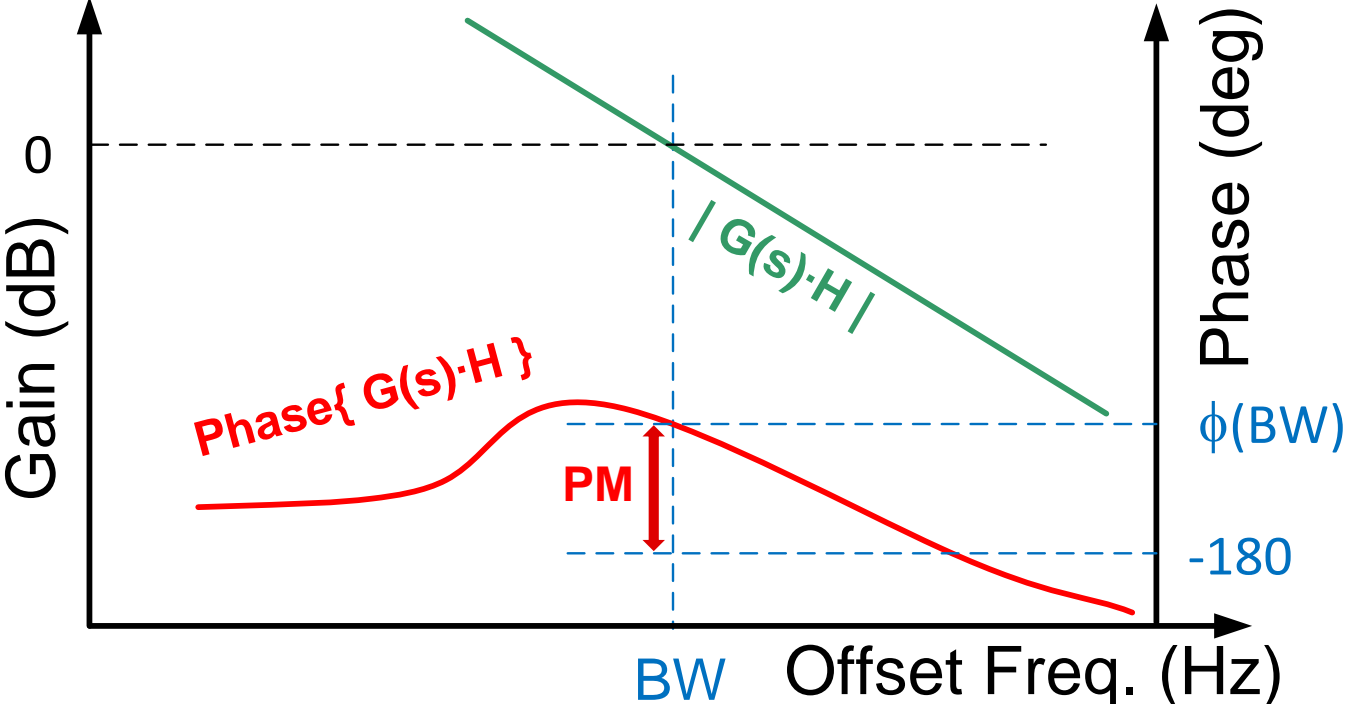


$$BW \equiv f : |G(s) \times H| = 1$$

$$T_{lock} \approx \frac{4}{BW}$$

- Wide loop bandwidth reduces lock time
- Narrow loop bandwidth increase lock time

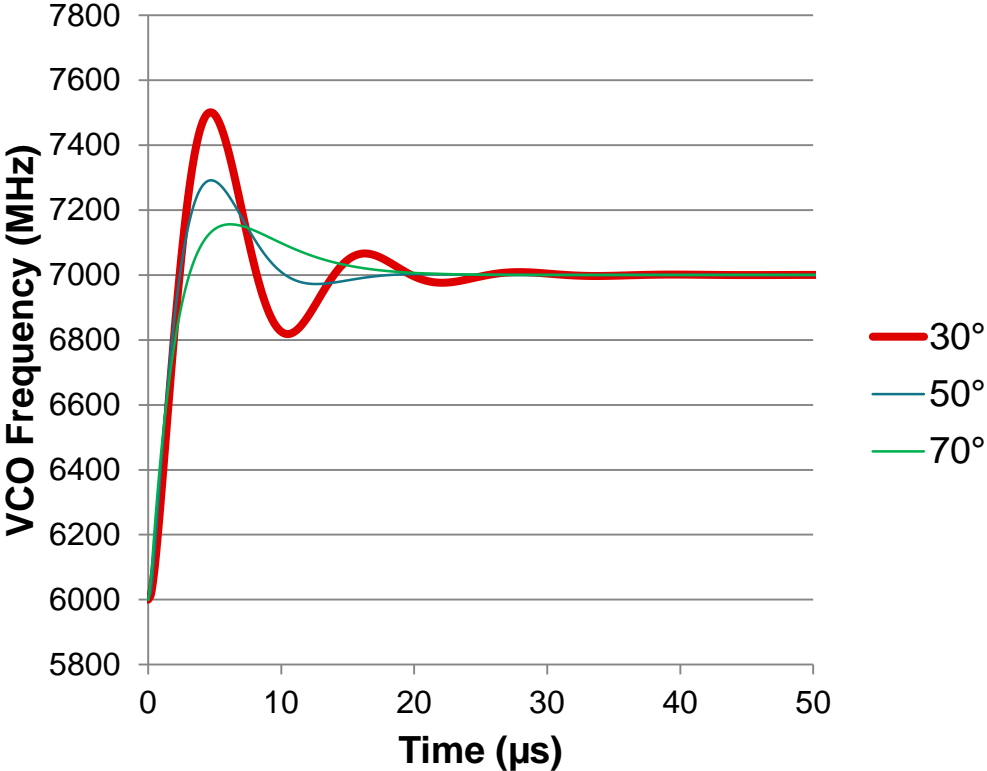
# Phase margin (PM)



$PM = 180 + \text{phase at BW frequency offset}$

# Phase margin's impact on lock time

How does PM impact transient response?

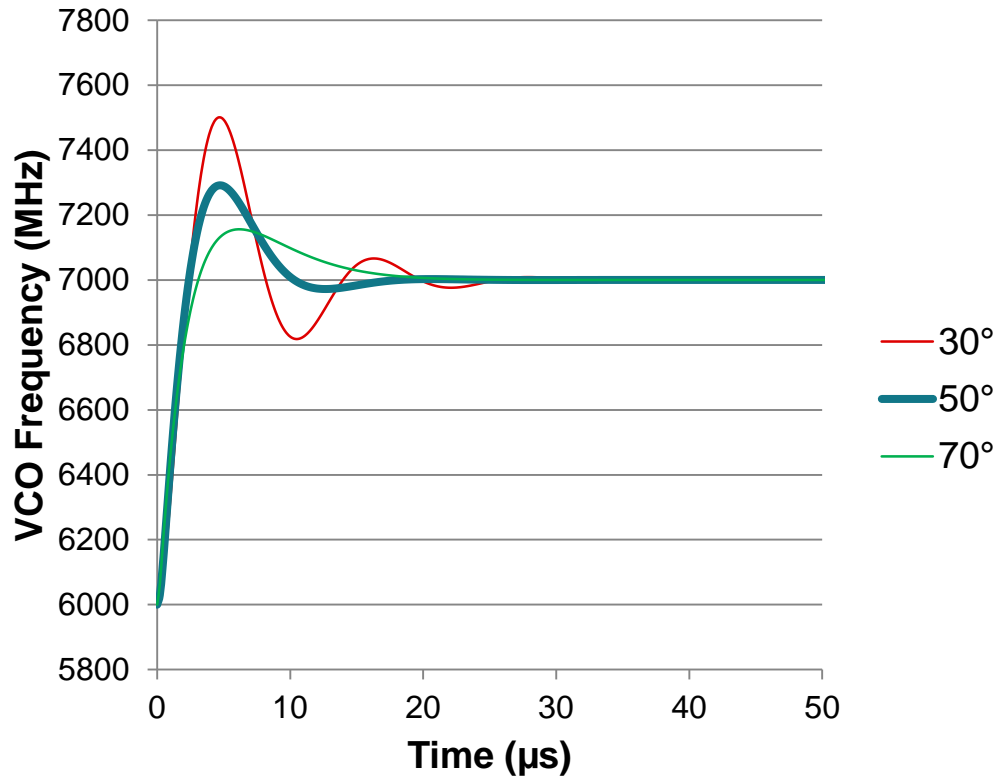


Phase margin	Why choose this?
30° - 45°	Reduce spurs



# Phase margin's impact on lock time

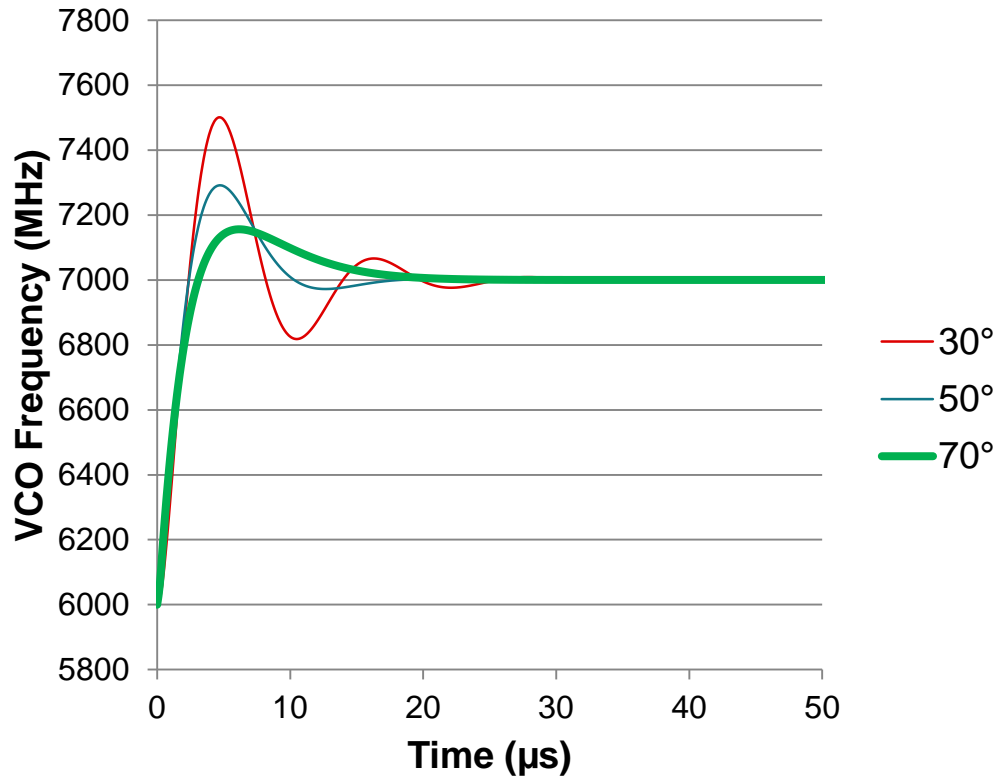
How does PM impact transient response?



Phase margin	Why choose this?
30° - 45°	Reduce spurs
45° - 55°	Balanced lock time, phase noise and spurs

# Phase margin's impact on lock time

How does PM impact transient response?



Phase margin	Why choose this?
30° - 45°	Reduce spurs
45° - 55°	Balanced lock time, phase noise and spurs
55° - 80°	Minimize jitter

# Lock time simulations

PLLatinum Sim

File Options Data Export Resources Help

Select Device Filter Designer Phase Noise Spurs **Lock Time** Bode Plot Database

LMX2594 Lock Time Tips

**Graph Settings**

- Points: 501
- Autoscale Axes:
- X Axis: min 0, max 25 us
- Y Axis: 4700, 7700 MHz
- Load Comparison Trace:
- Include VCO Calibration Time:
- Partial Assist VCO Calibration:
- Show Discrete Model:

**Frequency Response**

Final Frequency	7000 MHz	Analog Model	
Start Frequency	5000 MHz	Analog Lock Time	80.9 us
Settle Tolerance	1 Hz	Total Lock Time	80.9 us
		Peak Time	1.2 us
		Peak Frequency	7236.120 MHz

VCO Calibration Start:

StartCore: VCO4 Calibration VCO Start Frequency: 12000 MHz

**Phase Response**

Phase Disturbance	0 deg	Analog Model	
Settle Tolerance	1 deg	Analog Lock Time	53.5 us
		Total Lock Time	53.5 us
		Peak Time	0.75 us
		Peak Phase	-274532.1 deg

**Transient Response at Fout**

Frequency (MHz) vs Time (us)

Legend: — Analog Model, - - - Envelope+, - - - Envelope-, - - - Comparison

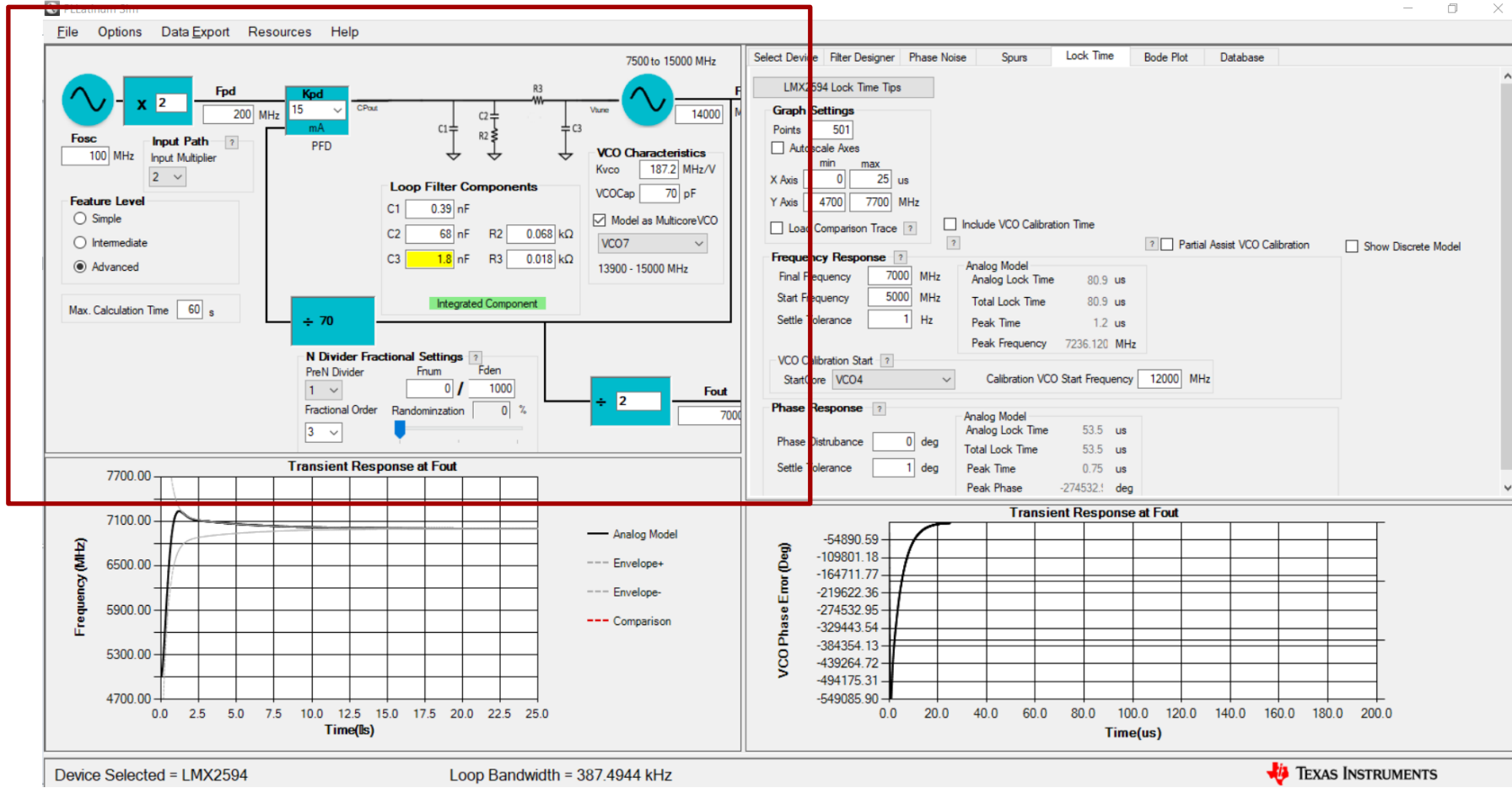
**VCO Phase Error (Deg) vs Time (us)**

Y-axis values: -54890.59, -109801.18, -164711.77, -219622.36, -274532.95, -329443.54, -384354.13, -439264.72, -494175.31, -549085.90

Device Selected = LMX2594 Loop Bandwidth = 387.4944 kHz

TEXAS INSTRUMENTS

# Lock time simulations



# Lock time simulations

The screenshot displays the PLLatinum Sim software interface for an LMX2594 PLL. The main window shows a circuit diagram with the following parameters:

- VCO Characteristics:**  $K_{vco} = 187.2$  MHz/V,  $VCO_{Cap} = 70$  pF, Model as Multicore VCO (checked), VCO7 selected, 13900 - 15000 MHz range.
- Loop Filter Components:**  $C1 = 0.39$  nF,  $C2 = 68$  nF,  $R2 = 0.068$  k $\Omega$ ,  $C3 = 1.8$  nF,  $R3 = 0.018$  k $\Omega$ .
- Dividers:** Input Multiplier = 2, N Divider Fractional Settings: PreN Divider = 1, Fnum = 0, Fden = 1000, Fractional Order = 3, Randomization = 0%.
- Other Settings:** Fosc = 100 MHz, Fpd = 200 MHz, Kpd = 15 mA, Fvune = 14000 MHz, Fout = 7000 MHz.

Two simulation plots are highlighted with red boxes:

- Top Plot: Transient Response at Fout**  
Y-axis: Frequency (MHz) from 4700.00 to 7700.00.  
X-axis: Time (ns) from 0.0 to 25.0.  
Legend: Analog Model (solid line), Envelope+ (dashed line), Envelope- (dotted line), Comparison (dash-dot line).  
The plot shows the frequency settling to approximately 7100 MHz within 2.5 ns.
- Bottom Plot: Transient Response at Fout**  
Y-axis: VCO Phase Error (Deg) from -549085.90 to -54890.59.  
X-axis: Time (us) from 0.0 to 200.0.  
The plot shows the phase error settling to approximately -54900 degrees within 20 us.

At the bottom of the interface, it states: Device Selected = LMX2594, Loop Bandwidth = 387.4944 kHz.



# Lock time simulations

The screenshot displays the PLLatinum Sim software interface for an LMX2594 PLL. The main window shows a circuit diagram with various control parameters and settings.

**Key Parameters and Settings:**

- Fosc:** 100 MHz
- Input Path:** Input Multiplier = 2
- Feature Level:** Advanced
- Max. Calculation Time:** 60 s
- Loop Filter Components:** C1 = 0.39 nF, C2 = 68 nF, C3 = 1.8 nF, R2 = 0.068 kΩ, R3 = 0.018 kΩ
- VCO Characteristics:** Kvco = 187.2 MHz/V, VCOCap = 70 pF, Model as MulticoreVCO (checked), VCO7 (selected), 13900 - 15000 MHz
- N Divider Fractional Settings:** PreN Divider = 1, Fnum = 0, Fden = 1000, Fractional Order = 3, Randomization = 0%
- Other Settings:** Fpd = 200 MHz, Kpd = 15 mA, Fout = 7000 MHz

**Simulation Results:**

**Frequency Response (Highlighted in Red):**

Final Frequency	7000 MHz
Start Frequency	5000 MHz
Settle Tolerance	1 Hz

**Lock Time Metrics:**

Analog Lock Time	80.9 us
Total Lock Time	80.9 us
Peak Time	1.2 us
Peak Frequency	7236.120 MHz

**Phase Response:**

Analog Lock Time	53.5 us
Total Lock Time	53.5 us
Peak Time	0.75 us
Peak Phase	-274532.1 deg

**Transient Response at Fout (Frequency vs Time):**

The graph shows the output frequency (MHz) over time (ns). The frequency starts at approximately 4700 MHz and settles to 7000 MHz within about 2.5 ns. The legend includes Analog Model (solid line), Envelope+ (dashed line), Envelope- (dotted line), and Comparison (dash-dot line).

**Transient Response at Fout (VCO Phase Error vs Time):**

The graph shows the VCO phase error (Deg) over time (us). The phase error starts at approximately -549085.90 degrees and settles to approximately -274532.1 degrees within about 20 us.

Device Selected = LMX2594      Loop Bandwidth = 387.4944 kHz



# Lock time simulations

The screenshot shows the PLLatinum Sim software interface for an LMX2594 PLL. The main window displays a block diagram of the PLL with various components like the PFD, VCO, and loop filter. Key parameters are set, including a 100 MHz reference frequency (Fosc) and a 70x division factor. The right-hand panel is set to the 'Lock Time' tab, showing a table of lock time metrics for the 'Analog Model'.

Metric	Value
Analog Lock Time	80.9 us
Total Lock Time	80.9 us
Peak Time	1.2 us
Peak Frequency	7236.120 MHz

Below the graphs, the software reports: Device Selected = LMX2594 and Loop Bandwidth = 387.4944 kHz.

SNA336: Streamline RF Synthesizer VCO Calibration and Optimize PLL Lock Time

To find more technical resources and search products, visit [ti.com/clocks](https://ti.com/clocks)



# Quiz

- **True or false: The phase margin is the phase of the open loop transfer function when the gain of the PLL is equal to 0 dB.**
- **True or false: Phase margins under  $30^\circ$  should be avoided to enhance the stability of the PLL, and minimize ringing.**
- **True or false: Larger bandwidths lead to shorter lock times.**

# Quiz

- **True or false**: The phase margin is the distance of the phase from -180 degrees when the gain of the PLL is equal to 0 dB.
- **True or false**: Phase margins under  $30^\circ$  should be avoided to enhance the stability of the PLL, and minimize ringing.
- **True or false**: Larger bandwidths lead to shorter lock times, as the PLL can adjust to changes in the output frequency faster.



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## Quiz

- True or false: When designing a loop filter for a tunable frequency range, the filter should be designed to meet a loop gain constant equal to the arithmetic mean of the minimum and maximum values the loop gain constant takes for the range of VCO frequencies selected.
- True or false: The zero of the transfer function,  $T_2$ , is independent of the loop filter order and is always equal to  $R_2$  times  $C_2$  for a passive loop filter.
- True or false: When a device has integrated loop filter components, no external loop filter components need to be added to the schematic.

Please read the following sentences and determine if each statement is true or false. The next page will have the answers.

## Quiz

- True or **false**: When designing a loop filter for a tunable frequency range, the filter should be designed to meet a loop gain constant equal to the arithmetic mean of the minimum and maximum values the loop gain constant takes for the range of VCO frequencies selected.
- **True** or false: The zero of the transfer function,  $T_2$ , is independent of the loop filter order and is always equal to  $R_2$  times  $C_2$  for a passive loop filter.
- True or **false**: When a device has integrated loop filter components, no external loop filter components need to be added to the schematic.

Statement 1:

False – The loop filter should be designed for the **geometric** mean of the minimum and maximum values the loop gain constant takes, not the arithmetic mean.

Statement 2:

True – The zero of the transfer function,  $T_2$ , is independent of the loop filter order and is always equal to  $R_2$  times  $C_2$  for a passive loop filter.

Statement 3:

False – While a fully integrated loop filter is possible, sometimes only part of the loop filter will be integrated in the device. The parts of the loop filter that aren't on-chip will still need to be routed to externally.