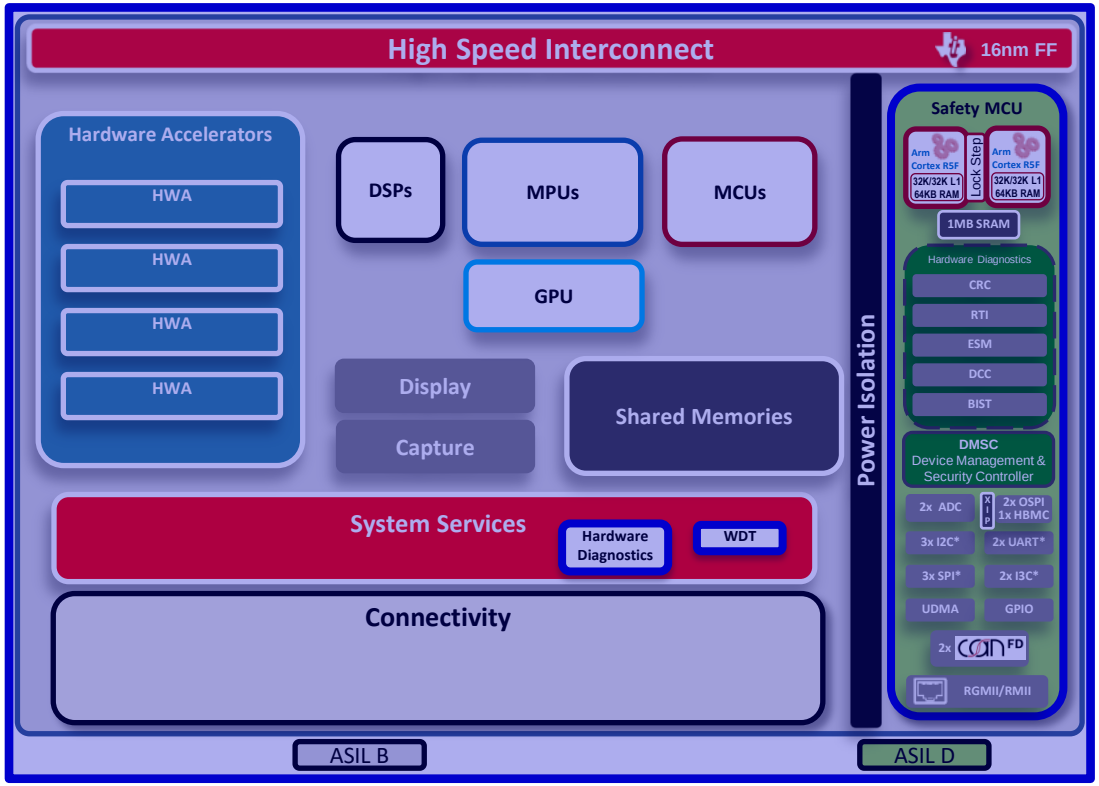
Jacinto™ 7 processors: safety and isolation

Safety and isolation features

- Key features and benefits
- Heterogeneous processing cores
- Application-specific hardware accelerators
- Device management architecture
- Memory architecture and data movement
- **Safety and isolation features**
- Virtualization features
- Security features
- Power management features
- Network connectivity
- Flash and storage
- Serial connectivity

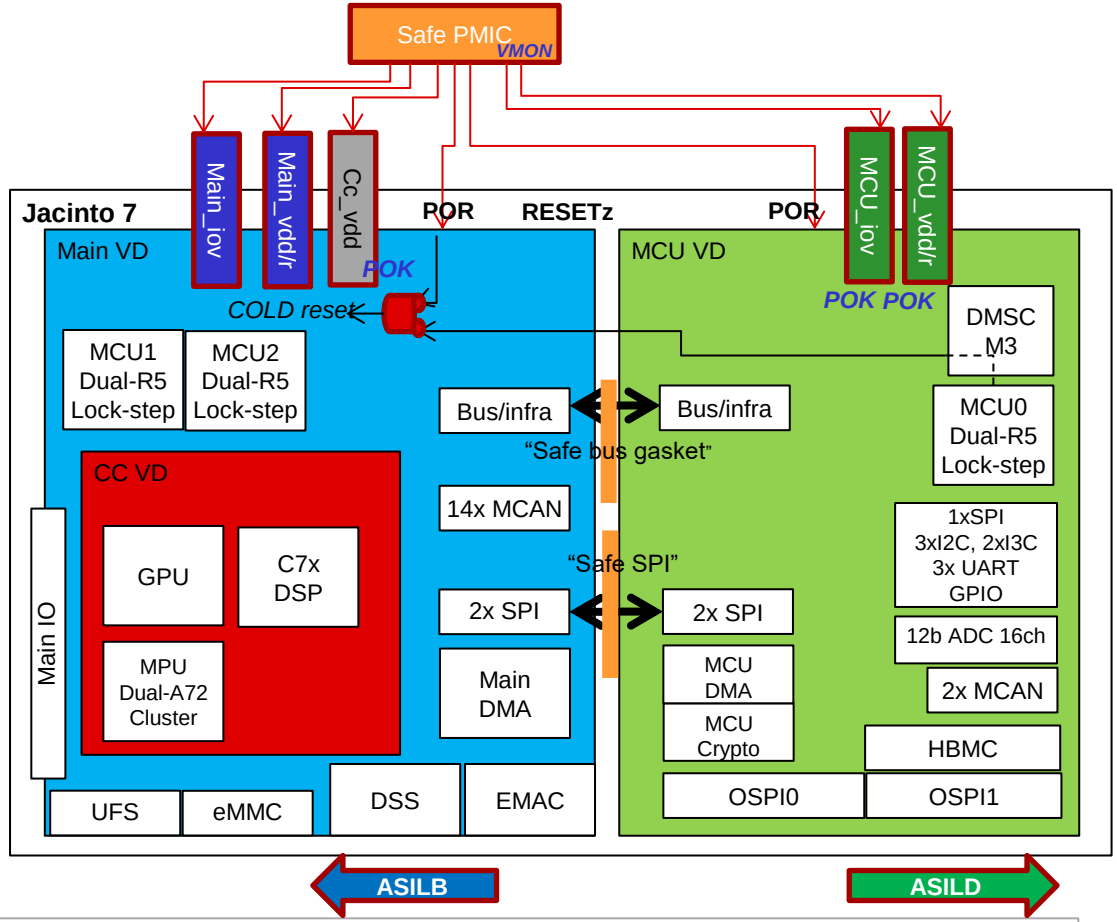


DRA829V/TDA4VM superset device representation

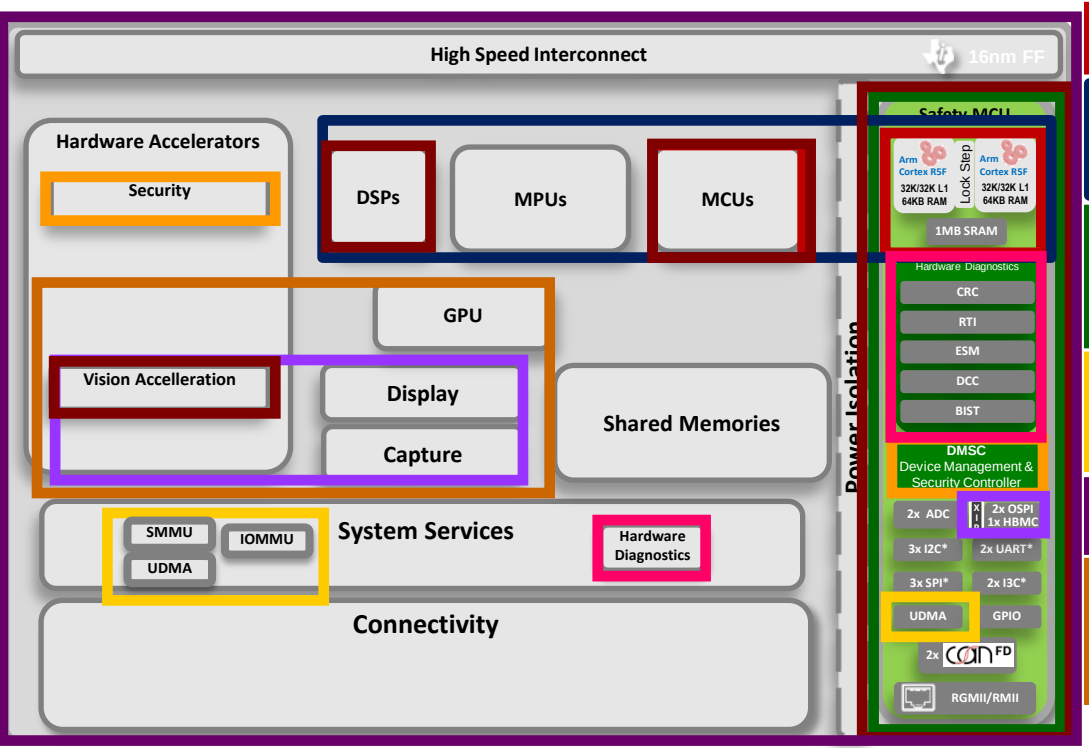
Safety and isolation features

Safety MCU domain is isolated from Main domain:

- Facilitate ASIL-D domain for micro replacement
- Includes lock-step R5 core, DMSC M3, DMA and key peripherals
- Full boot and active operation of Safety MCU without Main domain powered
- Logic and IO voltage isolation with power monitoring (POK)
- Reset clock and bus isolation
- Flexible options for control and data with Main domain:
  - Internal SPI to SPI
  - Full bus with isolation gasket and timeouts
- Works in conjunction with safe PMIC for separate domain



Safety and isolation features



- Hardware lock-step R5 w/ floating point:
  - Boot-time configurable lock-step or split
- CPU coverage:
  - Reciprocal comparison by software
  - Program flow monitoring (WWDT)
  - Asymmetric multi-processing
- Interconnect (Safety MCU):
  - Redundant req/ready
  - Parity on control and attributes
  - SECDED ECC on data
  - Parity protection of critical flops/MMRs
- DMA, virtualization, data movement:
  - Protection of critical control state
  - Redundancy, parity/ECC
  - Address containment / isolation
- Memory ECC (most memories)
- ASIL IP development flow (most IP)
- Graphics, imaging, display & acceleration:
  - Task isolation
  - Memory ECC
  - Image processing
  - Golden frame

- Communication, sensors, flash interfaces:
  - Freeze/hang detection
  - Built-in diagnostics
  - Redundancy
  - Data hash, CRC, authentication
- Security:
  - Authentication
  - Task isolation
- Safety Development Tool Kit (DTK):
  - Voltage & temperature monitors
  - Power monitors (POK)
  - Dual-clock comparators
  - System configuration MMR parity
  - MCRC DMA
  - eFuse chain CRC
  - Error Signaling module (ESM)
- Test
  - Power-On-Self test (Safety MCU)
  - Memory Self Test (PBIST) key IP
  - Logic Self Test (LBIST) key IP
  - IO loopback on interfaces
- External monitoring
  - 16 channel ADC (12b, 4MS/s)
  - External power monitors (POK)

For more information

- For more training on Jacinto 7 processors: http://training.ti.com/jacinto7
- Download Processor SDK Automotive for Jacinto 7 processors: http://www.ti.com/tool/PROCESSOR-SDK-DRA8X-TDA4X
- Order TDA4VM Jacinto Automotive processors for ADAS & autonomous vehicles: http://www.ti.com/product/TDA4VM
- Order the TDA4VMx evaluation module: http://www.ti.com/tool/TDA4VMXEVM
- Order DRA829V Jacinto Automotive processors for gateway & vehicle compute: http://www.ti.com/product/DRA829V
- Order the DRA829Vx evaluation module: http://www.ti.com/tool/DRA829VXEVM
- For questions regarding topics covered in this training, visit the processors support forum at the TI E2E Community website: https://e2e.ti.com