Cosmic radiation effects on electronics and how to pick the right part

Kirby Kruckmeyer,

Radiation Effects and Applications Engineer

Agenda

Taken from TI's "Radiation handbook for electronics"

www.ti.com/radbook

Talk will focus on space radiation effects

- **Destructive radiation effects**
  - TID, SEL, SEGR and Displacement Damage
- **Non-destructive radiation**
  - SET, SEFI and SEU
- **Risks of using COTS for space applications**
- **Radiation misconceptions**
  - SOI, epi, datecode, process control

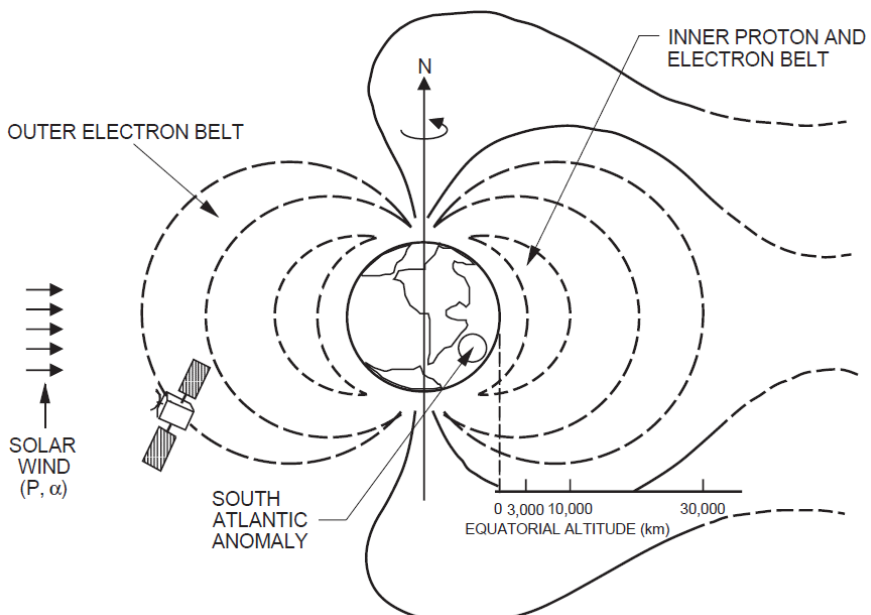
Kirby Kruckmeyer

- **Coauthor of TI's Radiation handbook for electronics**
- **Applications and radiation engineer in TI HiRel group**
- **Experience**
  - Came to TI from National acquisition in 2011
  - Radiation testing and qualification
  - Rad hard wafer processing
  - Mil/aero manufacturing, testing and qualification
- **Previous experience**
  - Bipolar and CMOS wafer processing
  - Automotive Q100 product development and qualification
- **Name etched on wafer floating in space**

Space radiation environment

Natural

- **Sources**
  - Cosmic rays from outside our solar system
  - Solar radiation
  - Particles trapped in the radiation belts
- **Particles**
  - Electrons
  - Low energy protons
  - High energy protons
  - Heavy ions
- **Exposure variables**
  - Orbit
  - Solar activity



Man made

- **Sources**
  - Nuclear detonation
- **Particles**
  - Neutrons
  - Photons

GaAs MMIC Reliability Assurance Guideline for Space Applications

Radiation effects

	TID	SEE	DDD	Prompt Dose
	Total ionizing dose	Single event effects	Displacement damage dose	Prompt dose
Source	Protons and electrons in space; X-rays and gamma rays on earth	High energy protons and heavy ions in space; neutrons on earth	Protons in space	A flash of protons from a nuclear explosion
Effect	Accumulated dose over time charges dielectrics	A single high energy strike causing a transient, upset, latch-up, damage or other effect	Damage to the silicon lattice from many ion strikes	Large photo currents in bulk of die
Subcategories	ELDRS	SEL, SET, SEU, SEFI, SEGR		Dose rate upset, dose rate latch-up
Test method	Gamma rays	Accelerator (cyclotron)	Neutrons	Flash x-ray
Mitigation (other than rad hard IC)	Shielding (adds cost and weight)	Redundancy; detection and reset (adds complexity, cost and down time)	Shielding (adds cost and weight)	Redundancy; detection and reset (adds complexity, cost and down time)

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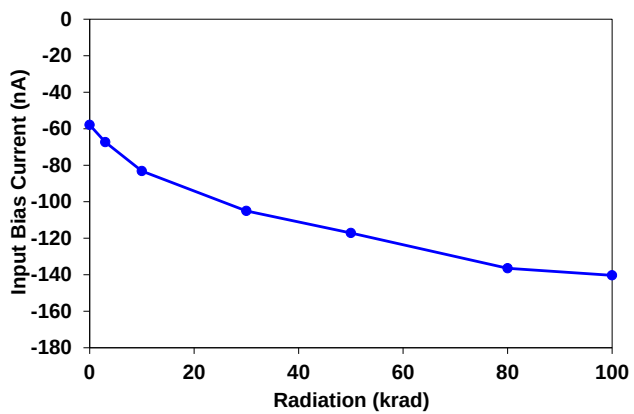
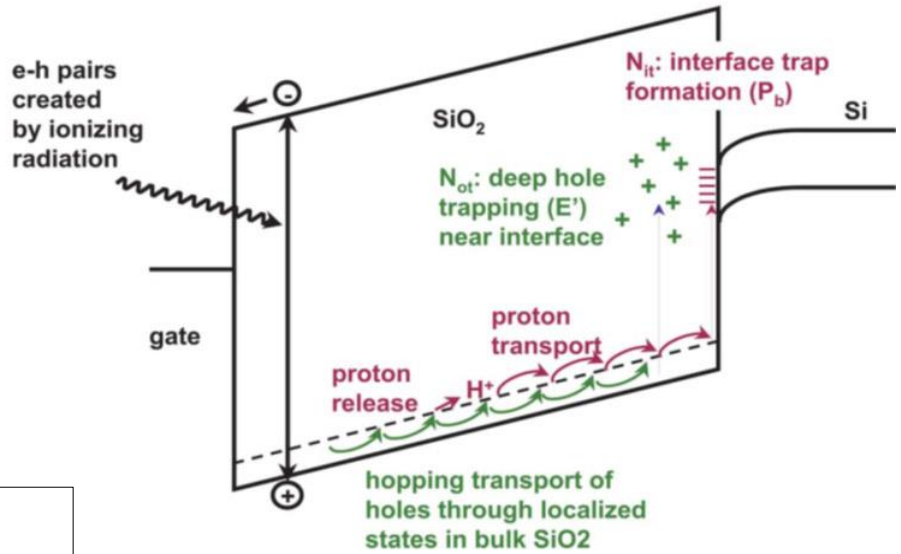
TID – total ionizing dose

- **Dielectric (oxide, nitride, etc.) charging and surface states at oxide/silicon interface**
- **Increased leakages and soft breakdowns; impacts**
  - supply current
  - input parameters (bias current, offset voltage)
  - response time
  - output voltage
  - linearity
  - functionality
- **Can be shielded to some extent**
  - adds weight and cost
  - not 100% mitigation





James R. Schwank et al., "Radiation Effects in MOS Oxides", *IEEE Trans. Nucl. Sci.*, 55(4), Aug. 2008, pp. 1833-1853.

TID units

- **The units for TID are rad**
  - rad(Si) for silicon based products
  - rad = “Radiation Absorbed Dose” (CGS units)
  - dose causing 100 ergs of energy absorbed by 1 g of matter
- **1 krad = 1000 rad**
  - krad(Si) are most common units for electronics
- **1 Gy = 100 rad**
  - Grey are in SI units
  - Gy is most commonly used in medical applications

TID testing

- **Device under test (DUT) electrically tested**
  - per datasheet or SMD
- **DUT exposed to gamma rays**
  - Cobalt-60 source
  - Radioactive decay of Co-60 emits gamma rays
  - DUT powered up while being irradiated
- **Post irradiation:**
  - DUT retested
- **RLAT: radiation lot acceptance testing**
  - Either wafer or wafer lot

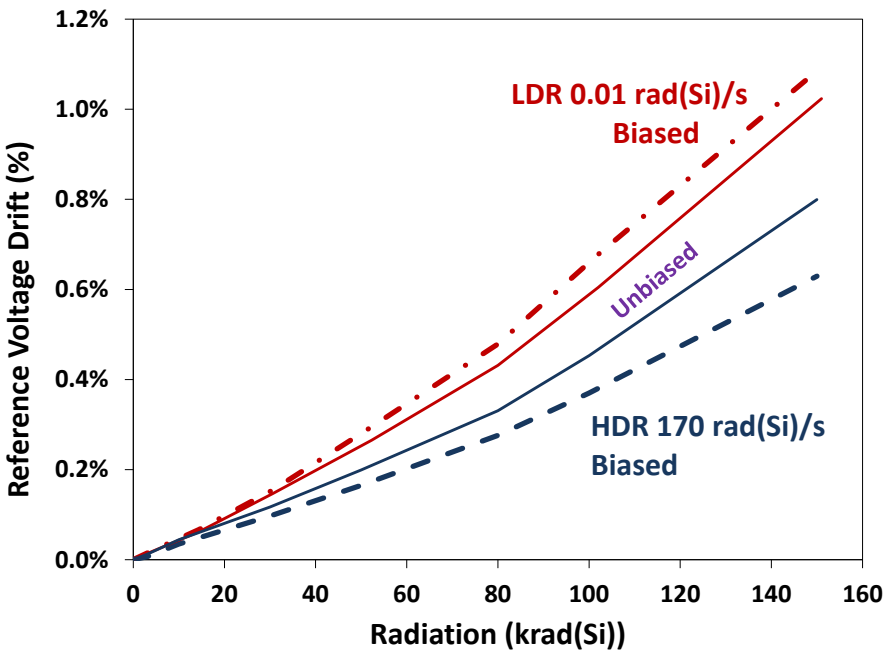
TI's HDR TID test system

ELDRS – enhanced low dose rate sensitivity

- **Standard radiation test is an accelerated test**
  - High dose rate (HDR): 50 to 300 rad/s
  - Less than 6 minutes to reach 100 krad
  - Space systems can take 10 years to reach 100 krad
- **ELDRS discovered in 1990**
  - Some bipolar linear products degraded more when lower dose rate used to attain same TID
  - Sometimes worse case when DUT unbiased during irradiation
  - Old way of testing (HDR biased) not valid for some products going into space environment
- **Risk with classic linear bipolar**
  - Not a risk for CMOS, digital or SiGe

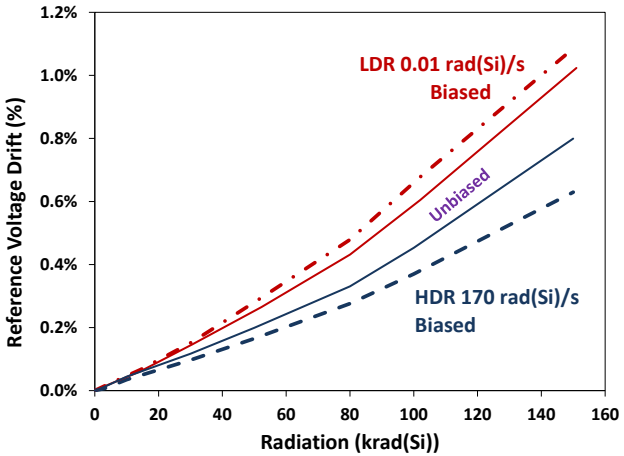
HDR = high dose rate (50 to 300 rad/s)

LDR = low dose rate (0.01 rad/s)



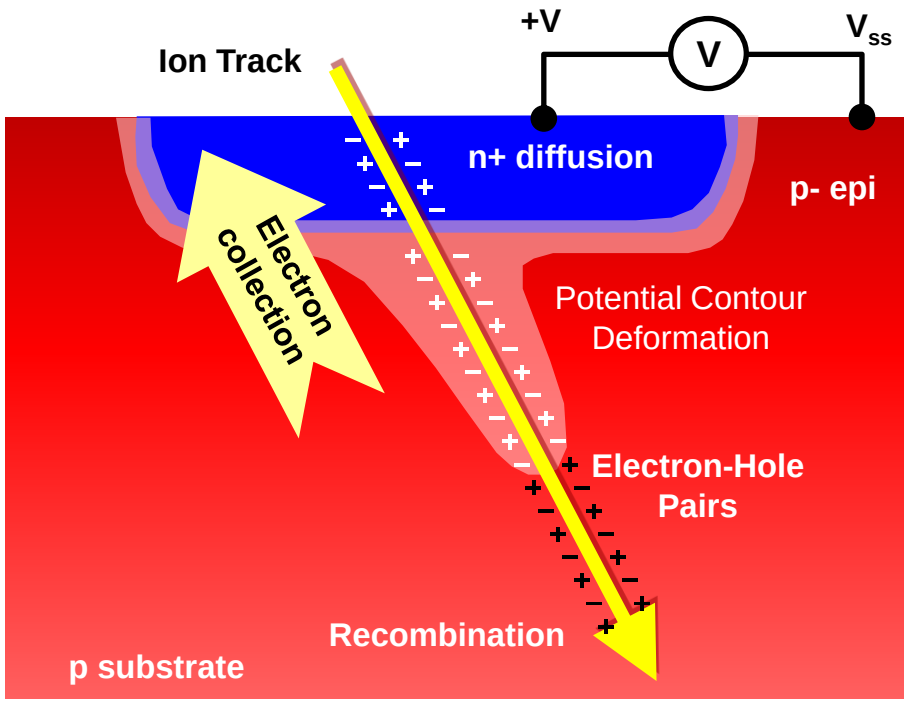
ELDRS characterization and testing

- **Bipolar linear products are now characterized for ELDRS**
  - Some units irradiated at HDR (50 to 300 rad/s)
  - Some units irradiated at LDR (0.01 rad/s)
  - Results compared
  - If more drift at LDR, product is said to have ELDRS
    - RLAT must be done at LDR
  - If product does not show significantly more drift at LDR the part is considered ELDRS-free
    - RLAT done at either LDR or HDR
- **Testing to 100 krad at LDR (0.01 rad/s) takes almost 6 months**
- **TI does RLAT on classic bipolar products (LM124, LM139, LM117, etc) at LDR even though the products are ELDRS-free**



SEE – single event effects

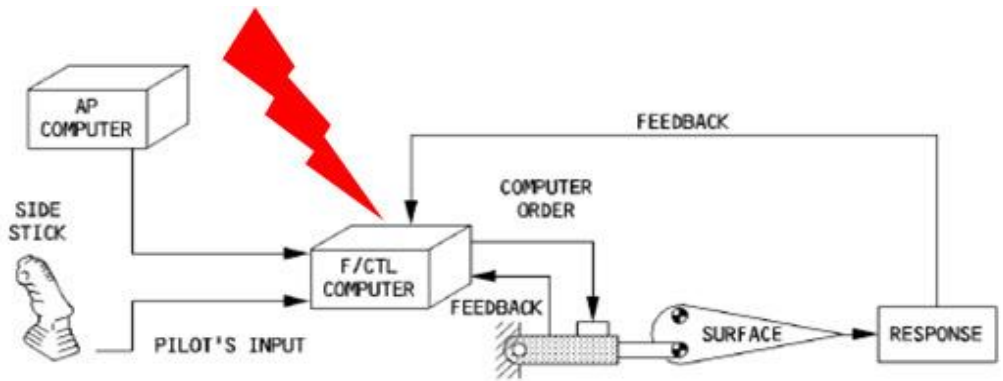
- **In space, a single heavy ion or high energy proton impacts a device**
  - On earth can be caused by neutrons (not covered in this talk)
- **Ion generates electron-hole pairs**
  - Can cause non destructive effects
    - **SEU – single event upset**
    - **SET – single event transient**
    - **SEFI – single event functional interrupt**
  - And destructive effects
    - **SEL – single event latch-up**
    - **SEGR – single event gate rupture**
    - **SEB – single event burnout**
    - **SEDR – single event dielectric rupture**
- **Typically cannot be shielded**

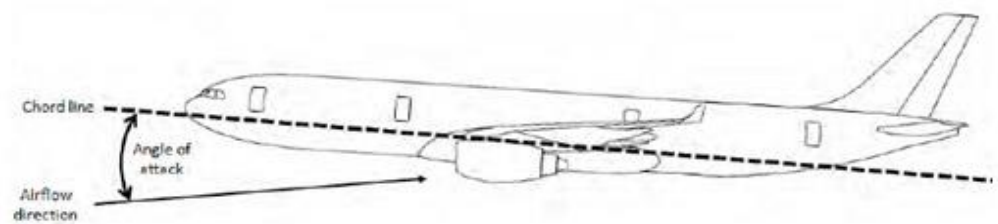


Reverse-biased N+/P junction

Single event on Qantas Flight 72

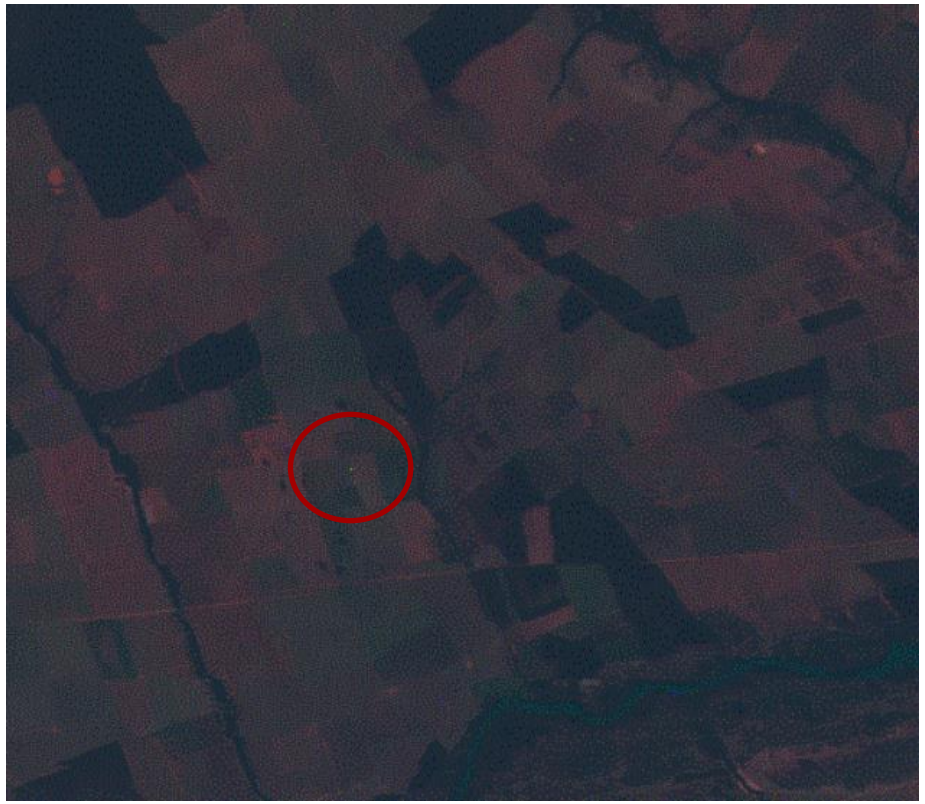
"In-flight upset, 154 km west of Learmonth, WA, 7 Oct. 2008, VH-QPA Airbus A330-303," ATSB Transp. Safety Report - Aviation Occurrence Invest., AO-2008-070, pp. 1 – 313, Dec. 2011.





Single subatomic event has human-scale impact!

Examples of single events in space



Green spot is from an SEU on the Level-0 Landsat 7 Enhanced Thematic Mapper Plus (ETM+)

https://landsat.usgs.gov/single-event-upset-seu

IMAGE Significant Ops History

Failure Review Board Final Presentation

Time		Event
2000	3/25	Launch from VAFB on Delta II.
	3/25	In Orbit Checkout largely nominal, except for Nutation Damper, MMM overwrite bug, Clock drift greater than expected. AST retry default increased. RPI deployment completed 2000/05/11, and full instrument checkout begins immediately after.
	5/16	RPI Y-axis transmitter fails. RPI s/w 'fuse' uploaded on 2000/06/12.
	6/17	CIDP TAS safes payload due to spin-rate oscillations. TAS Patch 1 on Dec 13.
	10/03	Loss of approximately 130m of RPI -X causes loss of spin balance.
2001	1/11	CIDP reboot due to multiple uncorrectable bit errors during large CME.
	9/18	Lost approximately 25m of RPI -Y axis antenna.
	10/11	CIDP TAS safes payload due to sun-cross error due to extreme sun angle.
02	8/09	Lost RPI +Y tip mass and negligible length of wire. Believed to be caused by orbital debris.
2003	2/1[illegible]	CIDP reboot due to SEU.
	3/30	Begin 2003 Mega-Eclipse season. Eclipses in excess of IMAGEs prime mission design. Payload power-safed by S/C FDC macro's. 2003/04/08 SCU reboot due to S/C FDC power macros. Stored command brought heaters online too soon after eclipse exit.
2004	9/30	Lost most/all of RPI +Y antenna
	11/25	SCU warm reboot due to PDU FDC. SCU Power Supply switched from A to B.
2005	2/01	SCU warm reboot. Cause TBD. SCU Power Supply still on B side.
	8/09	CIDP reboot, believed cause by SEU.
	12/18	Loss of IMAGE RF signal.

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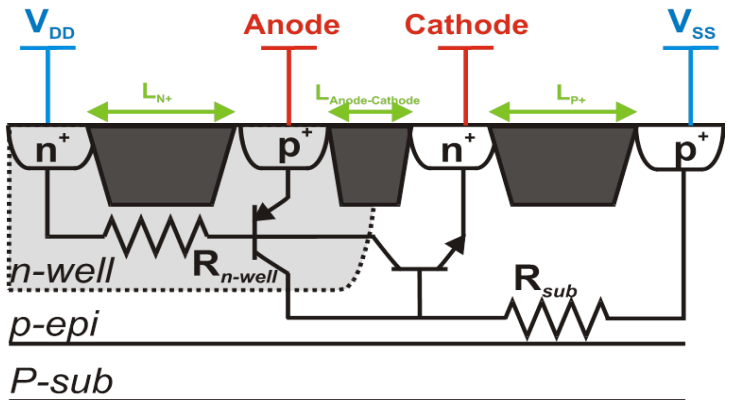
SEUs on Image magnetosphere imaging satellite. It is believed that the satellite lost signal due to an SEU.

https://image.gsfc.nasa.gov/

SEL – single event latch-up

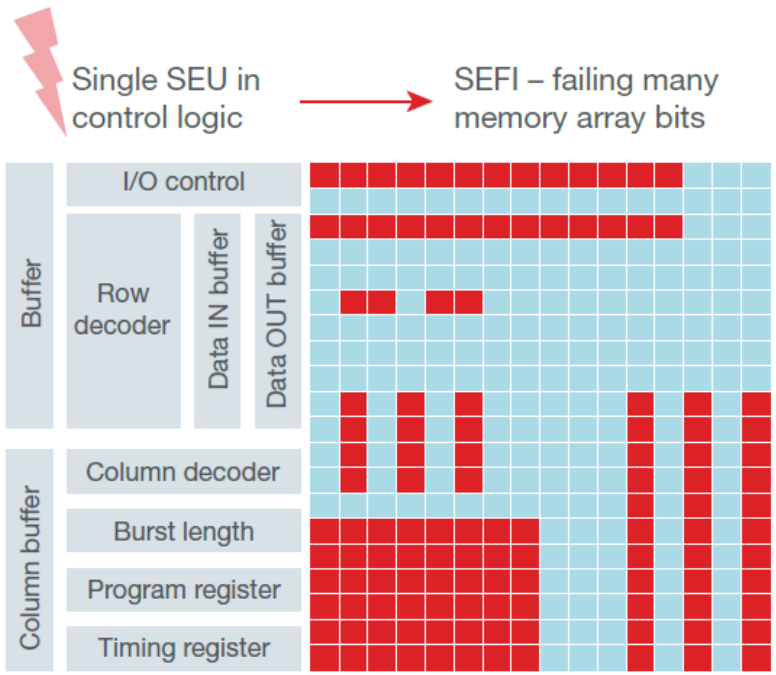
- **Perhaps, SEE of most concern**
  - Most CMOS products at risk and it can be destructive
- **An ion strike turns on parasitic PNPN structure like a silicon controlled rectifier (SCR)**
  - SCR will stay turned on until part is powered down
  - Draws more current than circuit design
  - Can cause product to malfunction
  - Can impact product life
  - Eventually will destroy device (can be less than one second)



- **Some CMOS products inherently immune**
  - Depends on design and/or technology node
  - Won't know without testing or an intimate knowledge of design and process
- **Unlikely in bipolar products (junction isolated)**
  - TI will test new products anyway
- **Mitigation for non rad hard ICs: redundancy and/or detect and reset circuits**
  - Adds complexity, weight, and system downtime

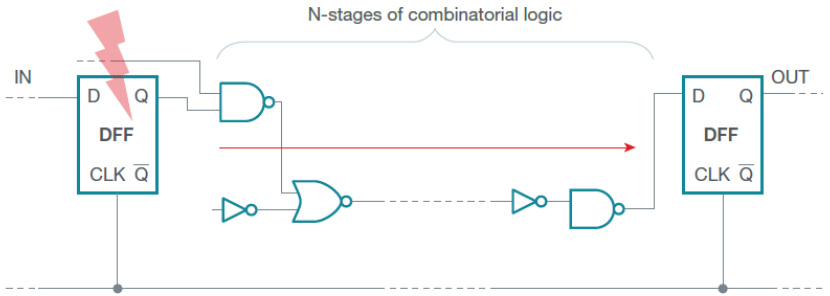
SEFI – single event functional interrupt

- **An ion strike causes a part to go into a different state**
  - different effects
- **Product that is programmed:**
  - control register bit can flip causing the part to go into a different configuration
  - may be necessary to reprogram the part
- **Product with a reset circuit:**
  - ion strike may cause the part to go into reset
  - some will recover on their own,
  - some may need to be reconfigured after reset
- **Product with an off pin:**
  - part could go into the off state
- **Mitigation: periodic register scrub**
  - Additional resources needed; system downtime

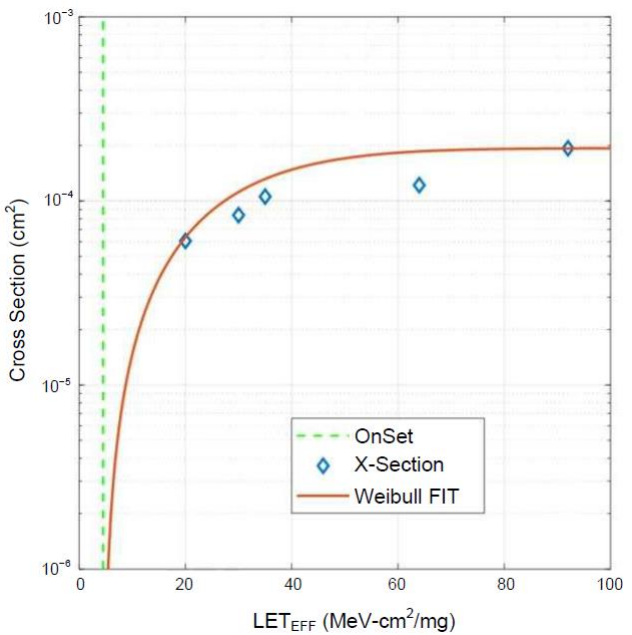


SEU – single event upset

- **Flipping of a digital bit from 1 to 0 or 0 to 1**
  - At one time, SEU was used to describe any nondestructive SEE, such as transients or SEFI
    - Still may see this confusion

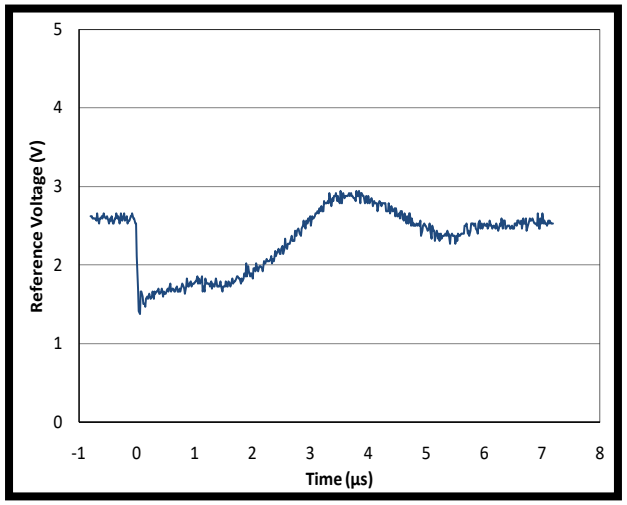


- **Almost all products with a digital outputs will have SEUs under heavy ion testing**
  - Need to determine probability of it occurring and energy required
  - Some products might not have SEUs with lower energy ions or with protons
  - Some products could be SEU immune for certain orbits



SET – single event transient

- **An ion strike causes a transient on a analog output**
  - This is called SEU in older papers
- **Almost all analog products will have SETs under the right (wrong) operating conditions**
- **SETs highly dependent upon the operating conditions**
  - Regulator: input voltage and output voltage, current and capacitance
  - Opamp: configuration, supply voltage, differential input, feedback loop, etc.
- **Mitigation: operating and application conditions**



LM4050-2.5 SET amplitudes and duration with different output capacitor values[25]

Output	Cross-section	Maximum SET positive	Amplitude negative	Maximum SET duration
Capacitor	(cm2)	(V)	(V)	(µs)
No Cap	1.0E-03	1.76	-1.72	7.2+
30µF	1.4E-05	0.33	-0.44	0.06
60µF	None	None	None	None

Destructive SEEs

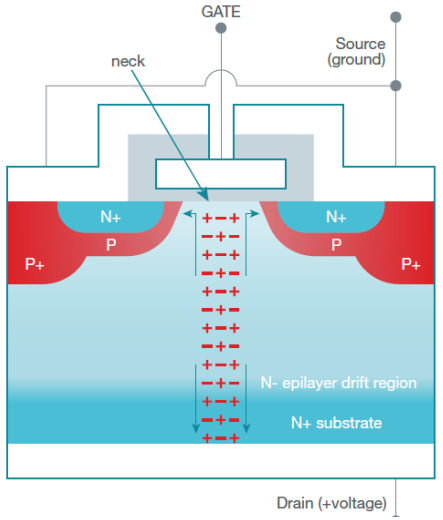
SEB – single event burnout

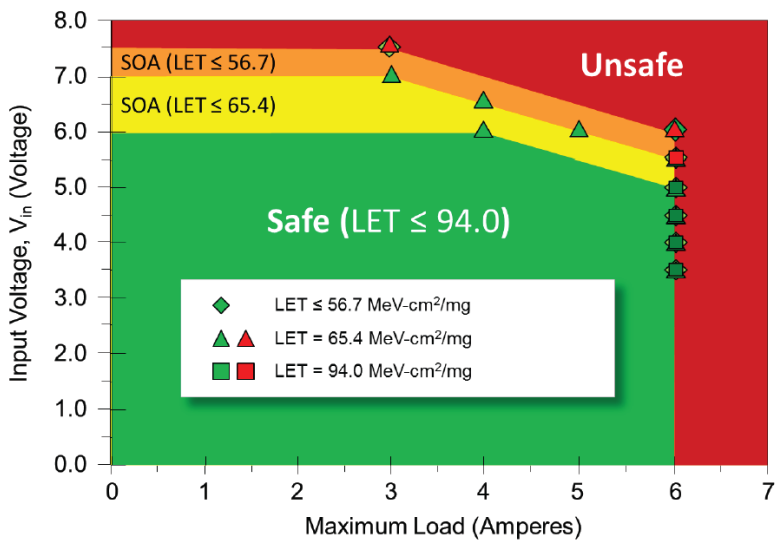
SEGR – single event gate rupture

- SEB and SEGR are two different mechanisms but difficult to distinguish from one another
- Concern for power MOSFETs
- Gate oxide can be damaged from an ion strike
- Voltage and current dependent
  - Commercial products must be derated for space missions
  - TI space products already characterized; derating not needed

SEDR – single event dielectric rupture

- Similar to SEGR but on non power devices such as capacitor oxides

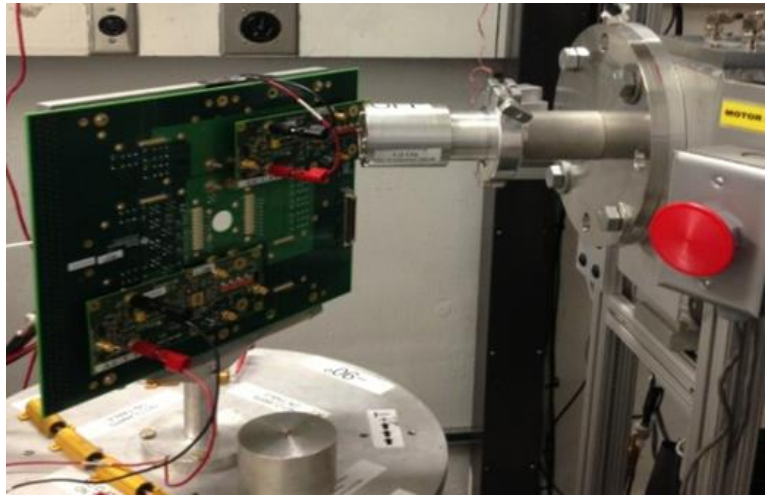




Safe operating range of TI's TPS50601-SP space grade point of load regulator

SEE testing

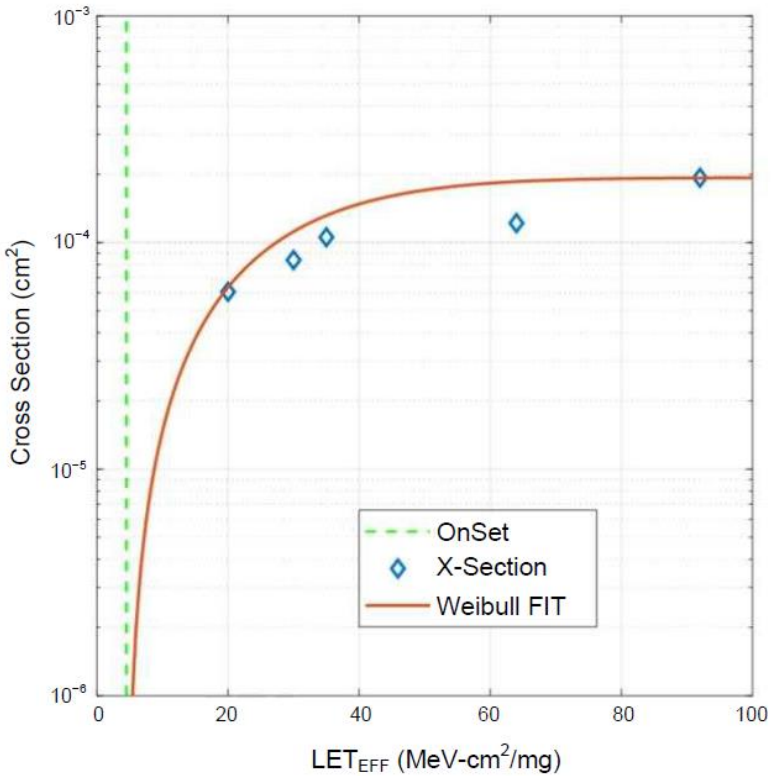
- **Heavy ion testing conducted at a cyclotron**
  - Only a few facilities in the US and in Europe; beam time can be hard to get
  - Cost: $1000 to $4000 per hour of beam time
  - Testing a product takes between 4 to 24 hours or more of beam time
  - Additional costs/time for test setup and analyzing data
- **Proton testing done at similar facilities but other accelerators may be used**
- **DUT delidded to expose die to beam**
  - Most facilities beams cannot penetrate packaging
  - Challenge for flipchips
- **DUT powered up and operating during testing**
- **Monitor part performance during beam run**
  - Supply current for SEL
  - Output for SEU or SET
  - Part functionality for SEFI



TI PXI SEE test board at TAMU cyclotron

SEE test results

- **LET = linear energy transfer**
  - amount of energy deposited in silicon by an ion
  - will be different for different ions
  - Units: MeV-cm^2/mg (sometimes shortened to MeV)
- **Record**
  - Fluence = number of ions shot at DUT during beam run
    - Units: #ions/cm^2
  - Number of errors during beam run
- **Calculate cross section**
  - Number of errors/fluence
    - Units: cm^2
- **Plot cross section vs LET**
- **If LETs below 14 MeV-cm^2/mg it may be necessary to do proton testing**



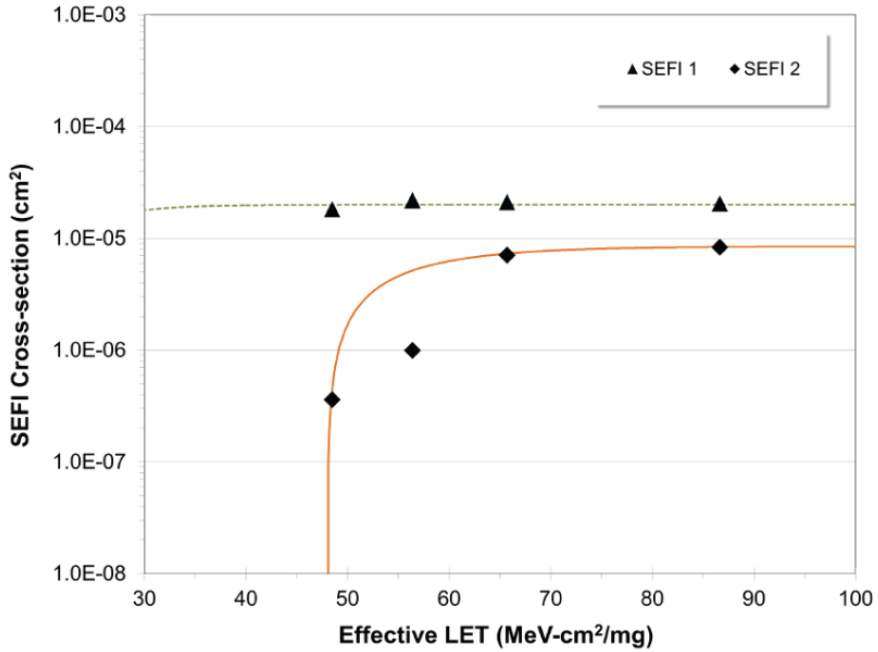
SEE data analysis

- **Fit Weibull curve to data**

$$F(L) = A\left(1 - \exp\left\{-\left[\frac{L - L_0}{W}\right]^s\right\}\right); L > L_0$$

$$F(L) = 0; L < L_0$$

Symbol	Parameter	SEFI 2
A	Saturated cross section	8.7E-06
L_o	Onset LET	48
W	Width	9
s	Fit	1



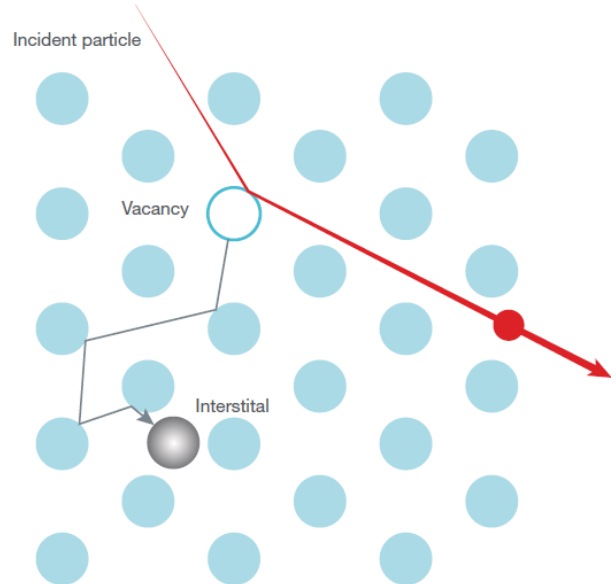
- **Weibull fit parameters used to determine probability of SEE for a certain orbit**

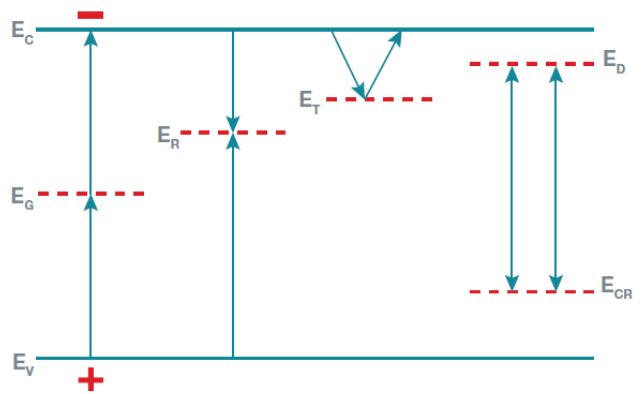
ORBIT TYPE	ONSET LET (MeV-cm²/mg)	CREME96 INTEGRAL FLUX (/day–cm²)	σ_{sat} (cm²)	EVENT RATE (/day)	EVENT RATE (FIT)	MTBE (years)
LEO(ISS)	48.0	4.5E–04	8.7E–06	3.9E–09	0.16	7.0E+05
GEO		1.5E–03		1.3E–08	0.53	2.1E+05

MTBE –
Mean time between event

DDD – displacement damage dose

- **Protons in space can cause damage to the silicon lattice**
  - This can cause traps that tie up carriers (electrons and holes)
  - Can also cause leakages
- **Dependent upon feature size and active junction depths**
  - Some bipolar parts fail below $1X10^{12}$ n/cm^2
  - CMOS tend to survive greater than $1x10^{13}$ n/cm^2
  - Many programs with DDD requirements do not bother to test CMOS products
- **Test method**
  - Stick bag of parts in neutron reactor
  - Wait to cool down
  - Electrically test units
  - Neutrons used instead of protons as protons also have TID effects



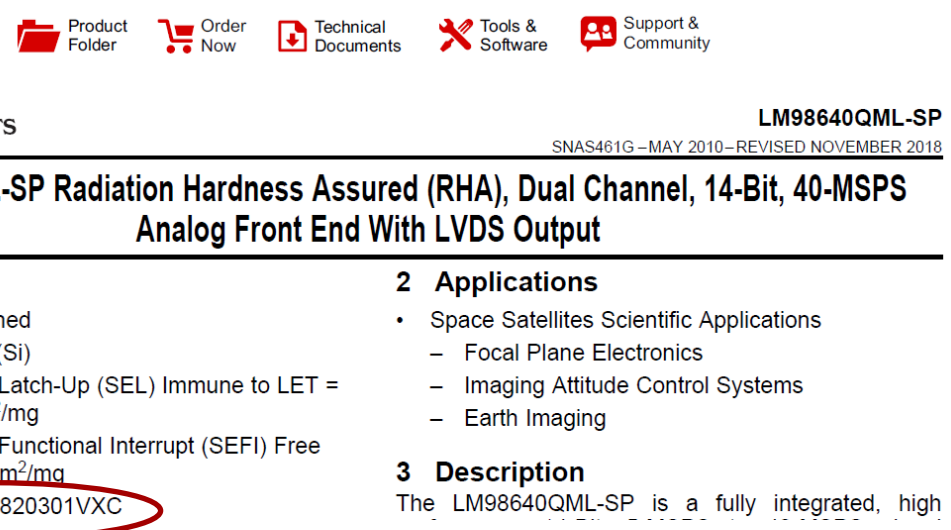


Prompt dose – flash x-ray

- **Nuclear detonation can cause flash of high energy photons**
  - The dose rate many orders of magnitude higher than used for TID testing
- **Flash can cause photocurrents within a device**
- **The photocurrents cause effects similar to SEEs**
  - Multiple effects can occur at once
- **Also known as “dose rate” testing**
  - Not to be confused with LDR/HDR TID testing
- **Testing similar to heavy ion testing**
  - DUT is powered up and operating and monitored
  - DUT is exposed to a flash x-ray
- **Results highly dependent upon the operating conditions at the time of the flash**
- **Suppliers typically do not test**
  - Dose rate and operating conditions usually classified

RHA - radiation hardness assurance

- **RHA products tested and qualified to specific TID level**
- **Each lot goes through TID radiation lot acceptance testing (RLAT)**
  - RLAT can be done on a wafer lot or a single wafer
  - RLAT either LDR or HDR depending upon the technology
  - TID report available for each lot
- **RHA is TID only and does not cover the other radiation effects**
  - Per mil standard definition
  - TI goes beyond the definition and tests for other radiation effects
- **TID level shown in the SMD (5962) number**



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TEXAS INSTRUMENTS

LM98640QML-SP

SNAS461G – MAY 2010 – REVISED NOVEMBER 2018

LM98640QML-SP Radiation Hardness Assured (RHA), Dual Channel, 14-Bit, 40-MSPS Analog Front End With LVDS Output

1 Features

- Radiation Hardened
  - TID 100 krad(Si)
  - Single Event Latch-Up (SEL) Immune to LET = 120 MeV-cm^2/mg
  - Single Event Functional Interrupt (SEFI) Free to 120 MeV-cm^2/mg
  - SMD 5962R1820301VXC

2 Applications

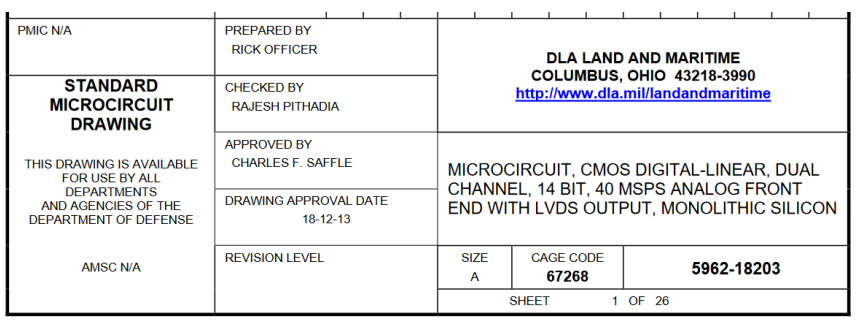
- Space Satellites Scientific Applications
  - Focal Plane Electronics
  - Imaging Attitude Control Systems
  - Earth Imaging

3 Description

The LM98640QML-SP is a fully integrated, high

Test and mil standards, SMDs and DLA

- **MIL-PRF-38535 – how to manufacture, quality and test mil and space products**
  - Replaced MIL-I-38510
- **MIL-STD-883 – test methods for meeting MIL-PRF-38535**
  - TM1019 – TID test method
- **SMD – standard microcircuit drawing**
  - DOD datasheet
  - Contains electrical specifications; no app info (see TI datasheet)



PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.dla.mil/landandmaritime		
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY RAJESH PITHADIA			
	APPROVED BY CHARLES F. SAFFLE	MICROCIRCUIT, CMOS DIGITAL-LINEAR, DUAL CHANNEL, 14 BIT, 40 MSPS ANALOG FRONT END WITH LVDS OUTPUT, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 18-12-13			
AMSC N/A	REVISION LEVEL	SIZE A	CAGE CODE 67268	5962-18203
		SHEET 1 OF 26		

- **DLA – Defense Logistics Agency – Land and Maritime**
  - Formally known as DSCC and DESC
  - Owner of SMDs and mil standards

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962L9950401VCA	3/	LM124AJLQMLV
5962L9950401VDA	3/	LM124AWLQMLV
5962L9950401VZA	3/	LM124AWGLQMLV
5962R9950401QCA	3/	LM124AJRQML
5962R9950401QDA	3/	LM124AWRQML
5962R9950401QZA	3/	LM124AWGRQML
5962R9950401VCA	27014	LM124AJRQMLV
5962R9950401VDA	27014	LM124AWRQMLV
5962R9950401VZA	27014	LM124AWGRQMLV
5962R9950401V9A	27014	LM124 MDR
5962R9950402VCA	27014	LM124AJRLQMLV
5962R9950402VDA	27014	LM124AWRLQMLV
5962R9950402VZA	27014	LM124AWGRLQMLV
5962R9950402V9A	27014	LM124 MDE

SMD PIN – Part identification number

5962R9950402VCA

Radiation rating

R = 100 krad
\- = No rad guarantee
P = 30 krad
L = 50 krad
F = 300 krad

Year SMD started

99 = 1999

Device number

02 = device ID 02
To distinguish part from other variants
In this SMD, 02 indicates ELDRS-free

Grade

V = Space
Q = Mil
Y = Space in non-hermetic ceramic package
S = Space; B = Mil in old 38510 system

Package

C = CDIP
D = CFP
Z = gullwing
Letter is not universal
9 = die

Lead finish

A = SnPb
C = Au

TI's space grade product family (-SP)

- **Manufactured, tested and qualified per QML-V flow of MIL-PRF-38535**
  - Tri-temp tested
  - 100% burn-in
- **Hermetic packaging with no matte Sn lead finish**
- **Mil temp range of -55°C to +125°C**
- **RHA – Radiation hardened**
  - RHA and RLAT to the specified level (30, 50, 100 or 300 krad)
  - ELDRS-free or characterized
  - SEL immune to the specified level (>60 MeV-cm^2/mg)
  - Other SEE characterized; reports available
  - DDD testing on new products
  - All new space products and most older products
    - some older space releases might not be RHA

TI's Range of Solutions

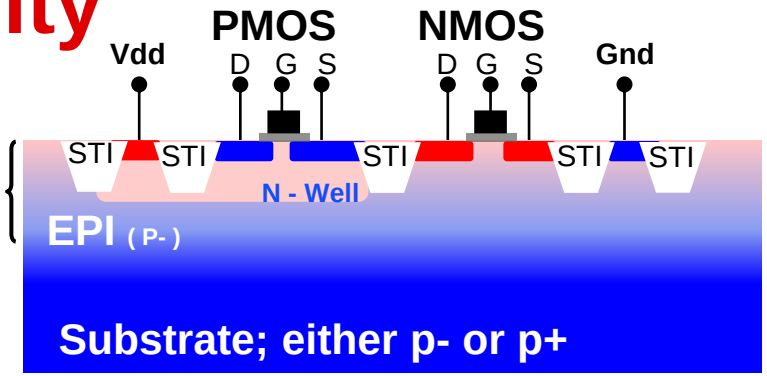
Quality / Reliability / Cost

	Commercial	Q100	EP	QMLQ	SEP	QMLV	
						QMLV	QMLV-RHA
Packaging	Plastic	Plastic	Plastic	Ceramic	Plastic	Ceramic	Ceramic
Single Controlled Baseline	No	No	Yes	Yes	Yes	Yes	Yes
Bond Wires	Au/Cu	Au/Cu	Au	Al	Au	Al	Al
Is Pure Sn used?	Yes	Yes	No	No	No	No	No
Production Burnin	No	No	No	No	No	Yes	Yes
Typical Temperature Range	-40°C - 85°C	-40°C - 125°C	-55°C - 125°C (majority)	-55°C - 125°C	-55°C - 125°C (majority)	-55°C - 125°C	-55°C - 125°C
Radiation (SEL/SEE)	No	No	No	No	Yes	Yes	Yes
Radiation (TID) Lot Acceptance (RLAT)	No	No	No	No	Yes	No	Yes
Lot Level Temp Cycle	No	No	No	Group D	Lot Level	Group D	Group D
Lot Level HAST	No	No	No	N/A	Yes	N/A	N/A
Life Test Per Wafer Lot	No	No	No	No	No	Yes	Yes

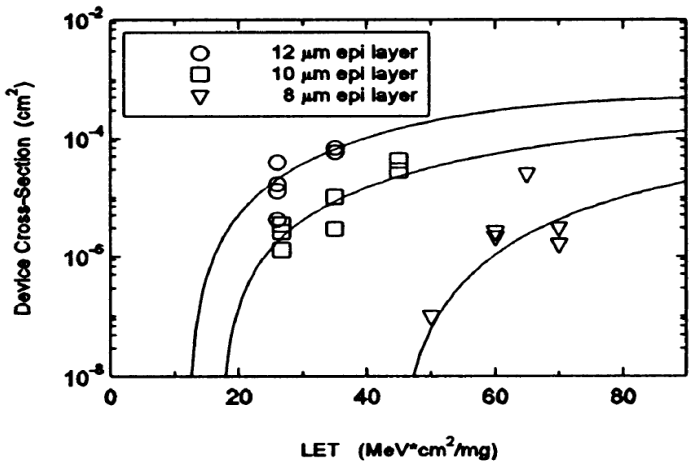
Radiation risks for commercial (COTS) and Q100

- **Most CMOS products at risk for SEL**
- **Power products can have SEGR or SEB and may need derating**
- **TID levels are unknown for most products and technologies**
- **Bipolar linear products might have ELDRS, making HDR test results invalid for space**
- **Radiation sensitivity can be highly dependent upon design**
  - Two products on the same process can have different rad responses
- **Semiconductor suppliers cannot share intimate details about process or design**
  - Proprietary information that gives supplier competitive advantage
- **Lot to lot variations can impact rad response**
- **Radiation testing is costly and time consuming**
- **Myths are out there**
  - Epi or SOI does not mean SEL immunity
  - Datecode does not provide useful lot information

Epi does not guarantee SEL immunity



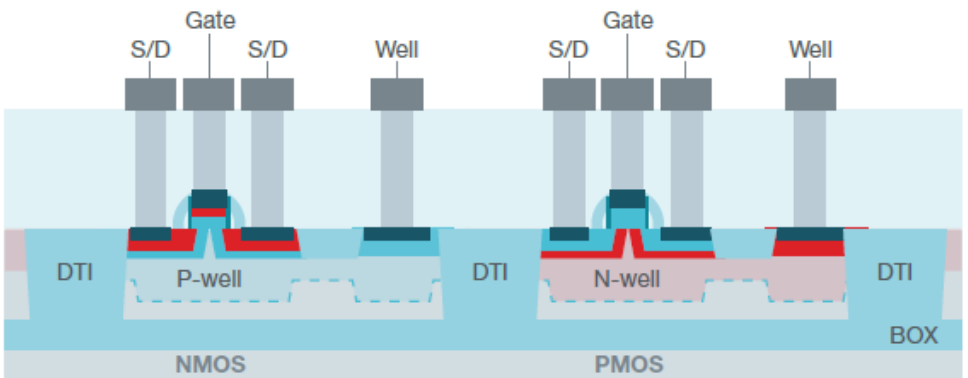
- **One method of radiation hardness involves using an epi substrate**
  - This is a highly engineered process and epi is just a part
  - Most commercial CMOS processes use epi but still have SEL
- **Most CMOS processes use a p- substrate with p- epi grown on top**
  - For SEL hardening to work, substrate must be p+
  - Using to a p+ substrate can impact the performance of some products
- **epi must be thin enough to prevent SCR from turning on**
  - Required epi thinness is typically thinner than standard substrates
  - Thinning the epi can cause performance problems such as lowering the well breakdown voltage
  - Much engineering work goes into developing the rad hard process



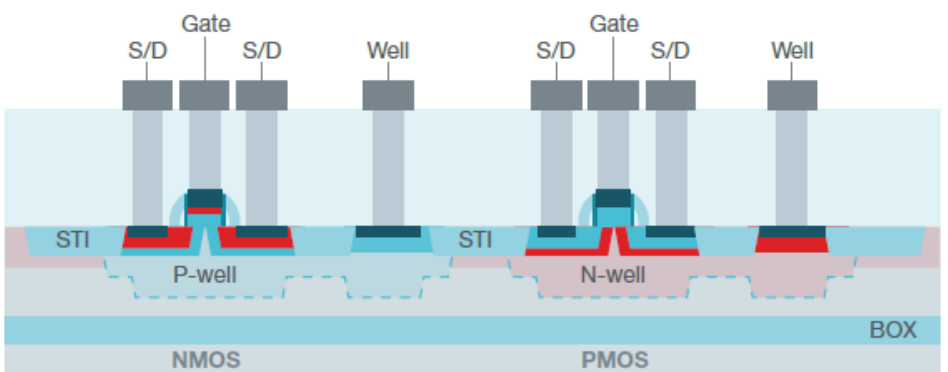
K. LaBel, et al., "Single event effect characteristics of CMOS devices employing various epi-layer thicknesses", RADECS, Sept. 1995., pp. 258- 262

SOI does not guarantee SEL immunity

- **SOI – Silicon on insulator**
  - The active area of device sits on a buried oxide layer (BOX)
- **Deep trench isolation (DTI)**
  - If isolation trench is deep enough to reach down to the BOX, structure cannot have SEL
- **Shallow trench isolation (STI)**
  - If isolation trench does not reach BOX, SEL is still a risk
  - Common in BiCMOS to use DTI for bipolar and STI for CMOS



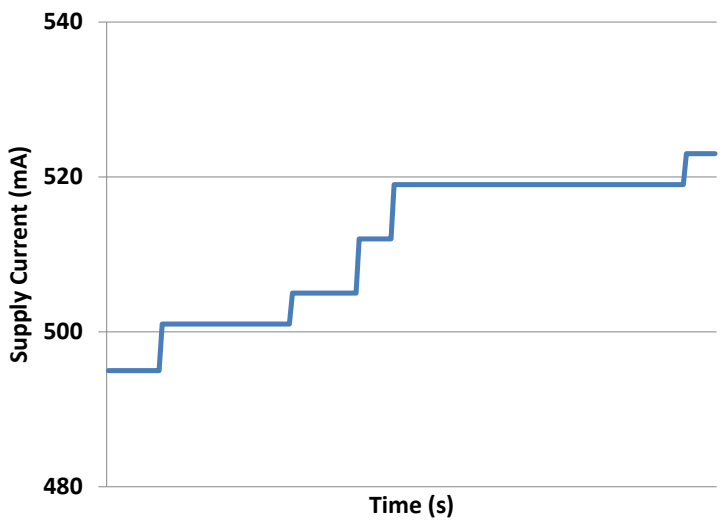
DTI completely isolating N and P wells, preventing SEL



STI not deep to isolate N and P wells; SEL still a risk

Micro SELs are not safe

- **Modern, complex CMOS products can have micro SELs**
  - A latch-up event causes a small rise in current
  - Current is limited either by power supply to latched circuit or size of the SCR
  - Part remains mostly functional
  - Part runs several minutes until power reset without apparent damage
  - Common to see multiple small rises in current
- **Product life risk**
  - Area that is latched can draw more current than designed for
  - Latched circuit will eventually fail after repeated events



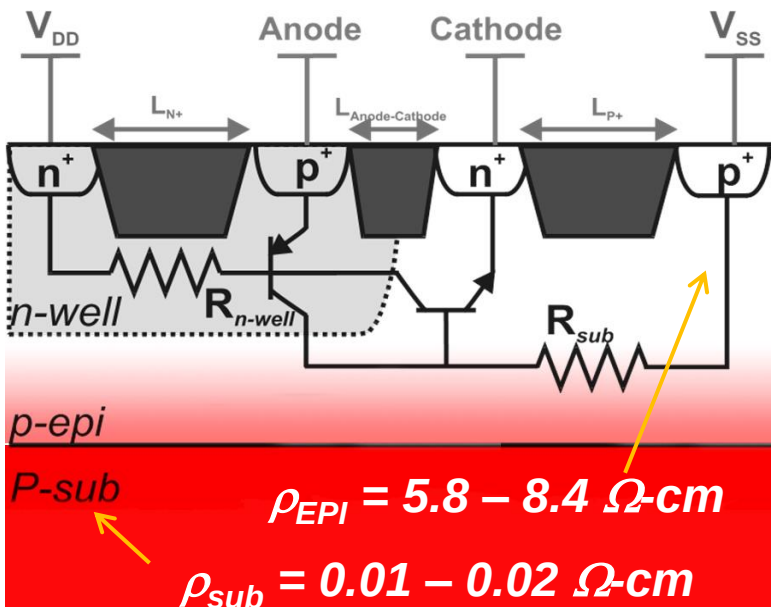
Process variation vs. radiation

- **Wafer fab controls are to maintain consistent electrical performance and quality**
  - Different variables impact radiation performance
- **Variables impacting TID**
  - Passivation stack and stoichiometry
  - Field oxide processes
  - Metal alignment
  - Surface doping levels
- **Variables impacting SEE**
  - Substrate parameters
  - Epi thickness
  - Junction profiles
  - Die layout

Process variation impact on SEL

Typical process control

- EPI thickness (±20%)
- EPI doping (±20%)
- Substrate doping (±33%)
- EPI and substrate doping impact effective EPI thickness



CAN Exhibits SEL based on 0.5um variation

EPI (um)	Temp	LET	SEL
9.5	25	85	No
9.5	125	85	No
10	25	85	Yes
10	125	60	Yes

To ensure SEL immunity of SN65HVD233-SP EPI process must be controlled tighter than typical commercial process

LM108 TID variations

LM108	HDR TID (krad)	Status
Lot #1	100	Pass
Lot #2	30	Pass
Lot #3	10	Fail

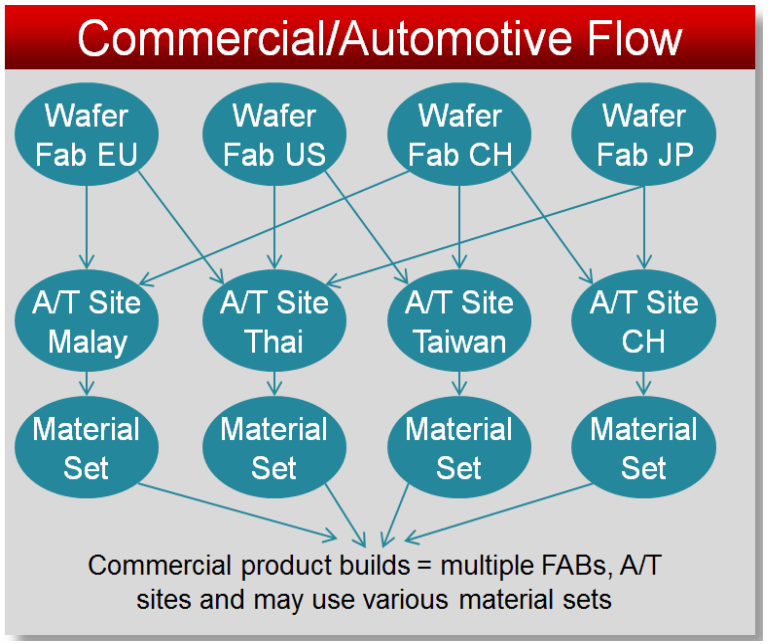
Lot #1 and #3 processed one month apart

LM108	LDR TID (krad)	Status
Wafer #2	80	Pass
Wafer #3	50	Pass
Wafer #15	30	Pass

Three wafers from the same lot

Commercial/automotive manufacturing flow

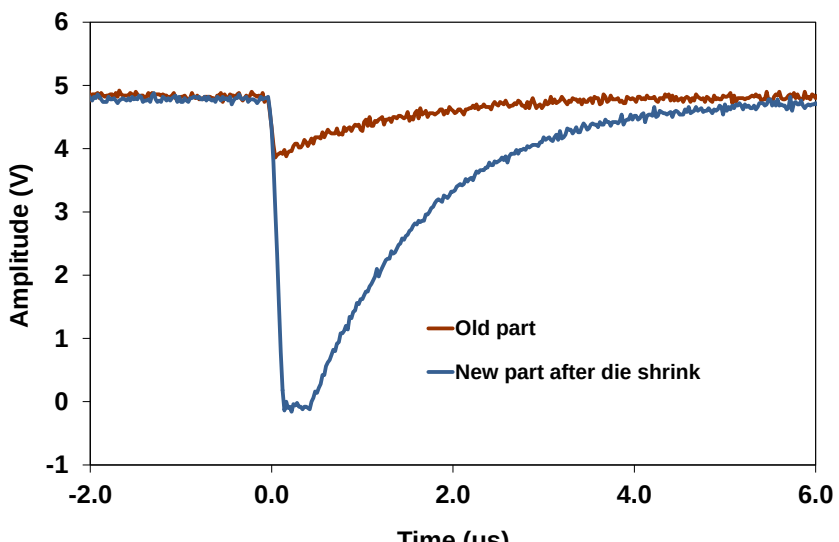
- **Many products manufactured in multiple wafer fabs**
  - Allows manufacturing flexibility
  - Fab transfers and closures
- **Equipment and processing not the same in each fab**
- **Sometimes radical changes during fab transfers**
  - Die shrink
  - Process topography
- **Differences can impact rad performance**
  - Different passivation tools have different TID response
  - Junction profiles changes will impact SEE response



Process changes and transfer impacts

- **Unitrode (UC18xx-SP) fab transfer**
  - 50 krad → 5 krad
- **Introduction of nitride**
  - Excellent moisture barrier for improved quality on plastic packaged parts
  - 100 krad → 10 krad and causes ELDRS
- **LM139 quad comparator transfer and die shrink**
  - Output transient impact
  - TID impact

    Channel 1 10 krad
    Channel 2 80 krad
    Channel 3 100 krad
    Channel 4 80 krad



Commercial Flow (real example: SN74HC138)

3-Line To 8-Line Decoders/Demux

Commercial Process Variables

3 active wafer fabs

- TI SFAB in Sherman, Texas
- ATC (subcontractor) in Hsinchu, Taiwan
- ASMC (subcontractor) in Shanghai, China

Each wafer fab runs a similar BUT NOT identical baseline

- Glassivation (protective overcoat)
- Base silicon wafers (vendor and doping spec)
- EPI versus non-EPI (doping profile/yield)
- Diffusion and metal profiles
- Process equipment
- Process recipes
- Process control limits

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Commercial Assembly Baseline Flows

3 assembly/test sites

- TI Mexico
- TI Taiwan
- ALP (subcontractor) in Thailand

Each assembly site runs a similar BUT NOT identical baseline

- Lead-frame source and geometries
- Mold compound (encapsulant)
- Mount compound (die attach)
- Wire bonder type and profile
- Wire type and other materials
- Injection mold press type and profile

Datecode tells you nothing

- **Four digit datecode is the date product was assembled**
  - Encapsulated in plastic for commercial products
  - Lid sealed for hermetic packages
- **Datecode has no wafer lot information for commercial/automotive products**
  - Wafers can be stored for years before being assembled
  - One datecode is likely to be assembled from more than one wafer
  - One datecode can include different wafer lots
  - One datecode could have units that came from different wafer fabs

Summary

- **Many radiation effects in space that can impact product's life and performance**
- **Predicting a product's radiation response requires intimate knowledge of design and process**
  - Usually not available to customers
- **Choosing and testing parts can be expensive and time consuming**
- **Standard commercial/automotive fab variations can impact product rad performance**
- **Customer has no insight into lot variations**
  - Datecode does not provide meaningful wafer lot information
- **No guarantee that product used will have same performance as units tested**
- **TI space products are tested and qualified up front**
  - We do the testing and verification so you don't have to

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