The McASP Primer

Fundamentals

What is McASP?

McASP is TI's Multichannel Audio Serial Port. It was designed specifically to support use cases requiring multichannel, multi-zone audio:

- McASP can have up to 16 data pins. More data pins = higher possible channel count.
- McASP has a very flexible clocking scheme. This is helpful for multi-zone applications.

McASP fundamentals: Data pins

- McASP supports up to 16 serializers, depending on the device. Each serializer is connected to a data pin, referred to as an AXR pin.
  - Any AXR pin can be configured to either transmit or receive.
- What can we do with 16 AXR pins?
  - If configured for I2S, 16 AXR pins allow for up to 32 channels (2 ch * 16 AXR pins).
  - If configured for multi-slot TDM, 16 AXR pins allow for up to (n slots * 16 AXR pins).

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  7.1.4 = 12 channels. I want to run I2S. So that means that I need 12 / 2 = 6 AXR pins.

McASP fundamentals: Mute pins

McASP may have up to two mute pins:

- AMUTEIN – This is an input. Some external devices have a mute output pin; such a signal may be connected to AMUTEIN. McASP may be configured to mute output under this condition.

- AMUTE – This is an output which McASP may be configured to drive under specific error conditions. Please see the Technical Reference Manual for your device for more details.

McASP fundamentals: Clock pins

McASP may have up to six clock pins. Each clock pin may be sourced externally or generated internally:

- AHCLKX and AHCLKR – These are high-frequency clocks pins, sometimes referred to as master clocks. McASP uses a master clock for one purpose: to divide it down and generate a bit clock.

- ACLKX and ACLKR – These are bit clocks, often referred to as BCK. Data is clocked in and out with respect to bit clock edges. Much of McASP's internal logic runs off of the bit clock, so a bit clock is ALWAYS required.

- AFSX and AFSR – These are the frame sync clocks, often referred to as word clocks, or more commonly as left-right clocks (LRCK). The frame sync clocks run at the sample rate of the audio stream.

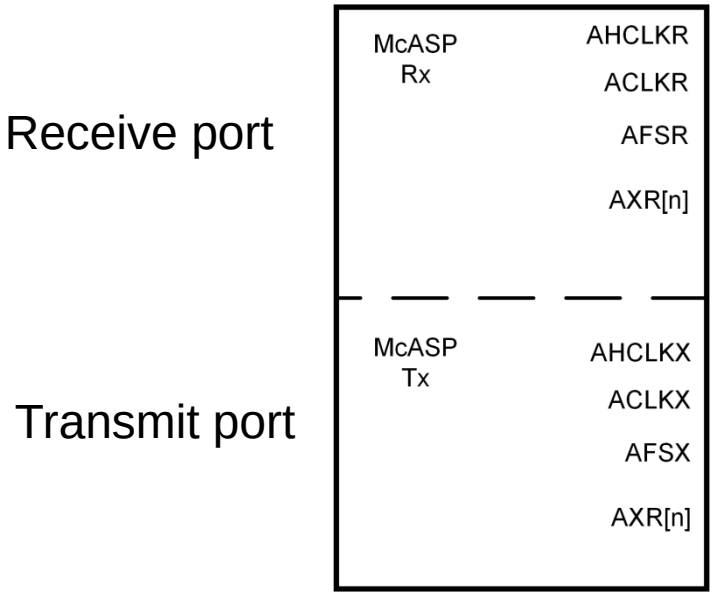
McASP fundamentals: Clock zones

Every McASP has a receive clocking section and a transmit clocking section:

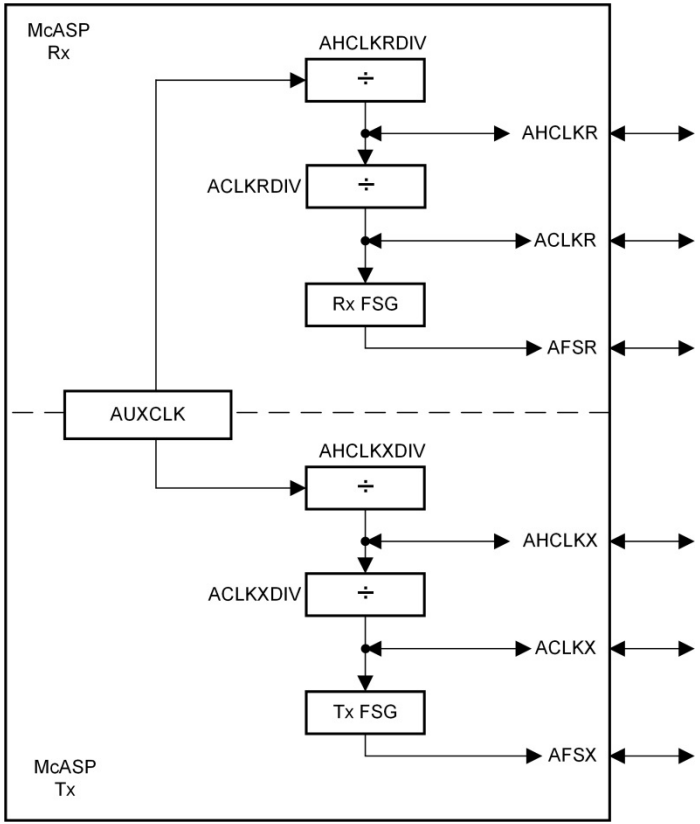
- These are sometimes referred to as the receive port and the transmit port.
- Each clock port constitutes a clock zone. Therefore, each McASP has two potential clock zones (Rx and Tx).
- The Rx and Tx clock zones may be run asynchronously with respect to each other. But in some cases, synchronous operation is appropriate.

McASP external signals

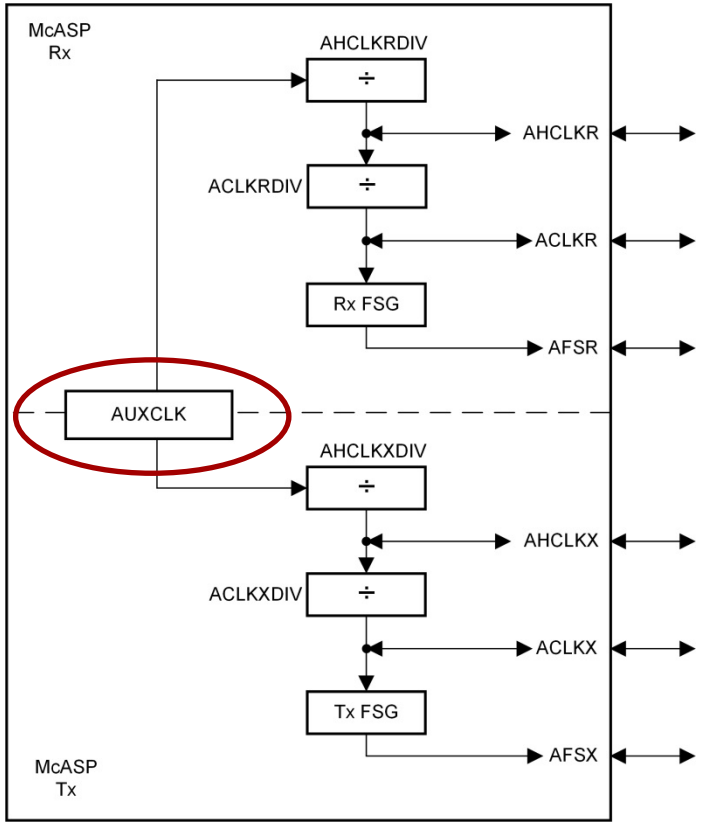
This is a simplified diagram of the McASP pins. Mute pins are not shown, as we won't discuss them further.



McASP clock generation architecture



McASP clock generation architecture



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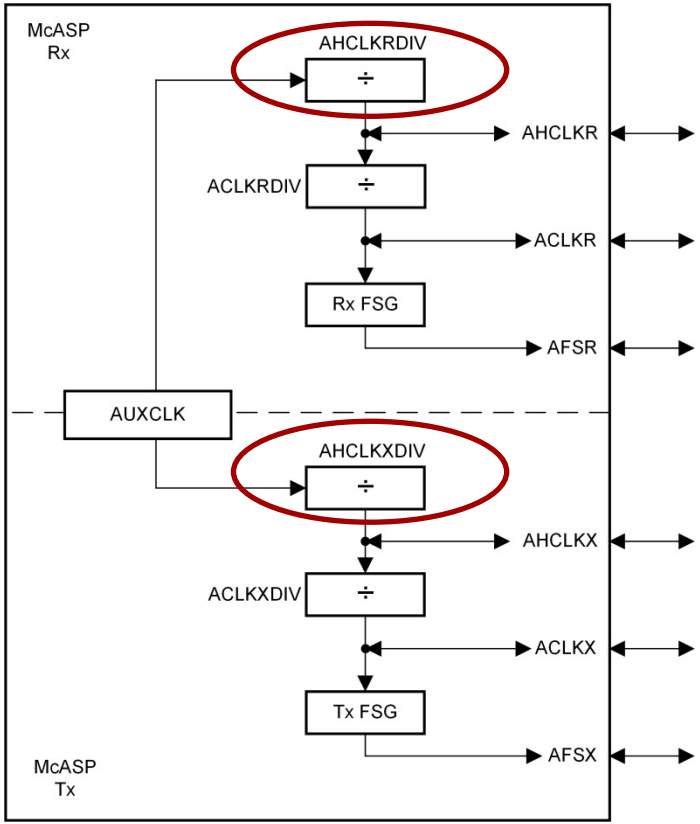
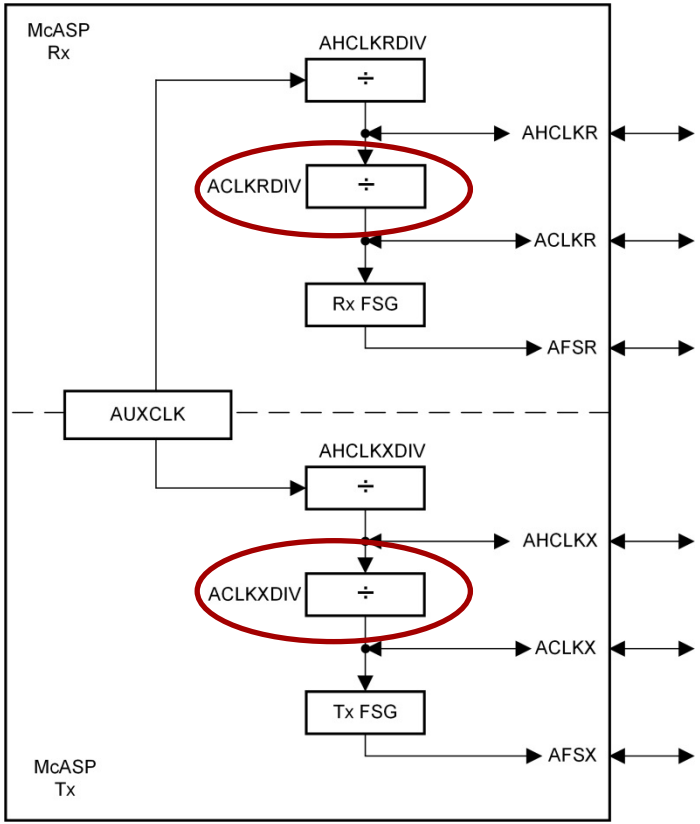


McASP clock generation architecture



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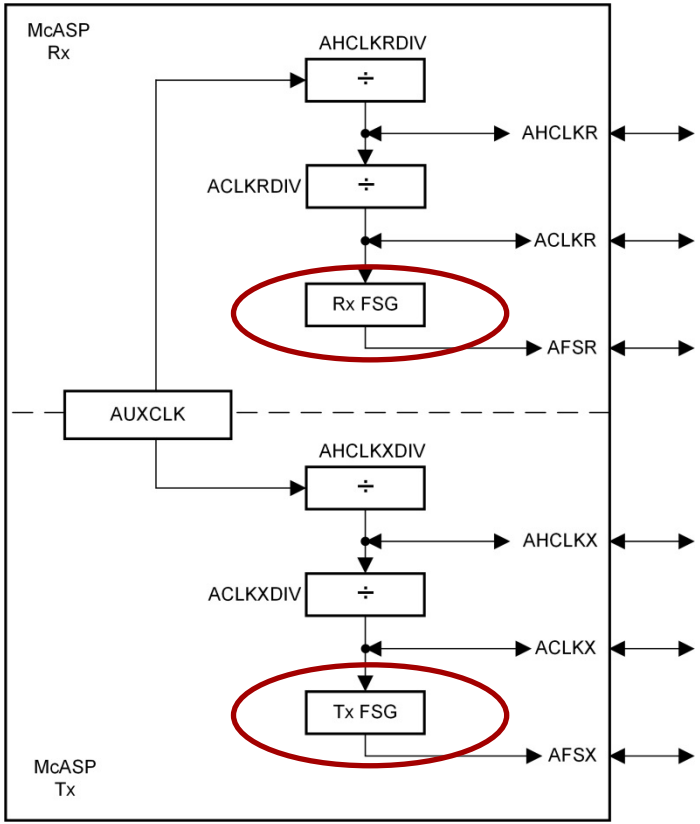
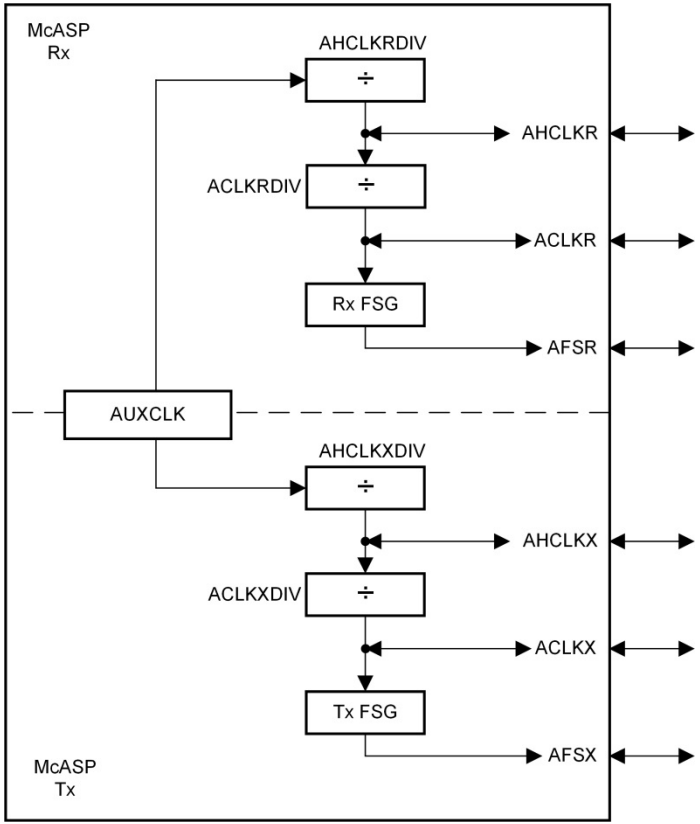


McASP clock generation architecture

All McASP dividers are integer dividers!



For more information

- McASP Design Guide: Tips, Tricks, and Practical Examples
  http://www.ti.com/lit/sprack0

- For questions about this training, refer to the E2E Community Forums at
  http://e2e.ti.com