Texas Instruments

Tools for system-level challenges

A live demo of the top tools to help you navigate your design journey

Jason Clark // Aerospace & Defense Systems

Agenda

- TI industrial systems team overview
- Live demo to find products and reference designs for your application
- Overview of select high speed reference designs

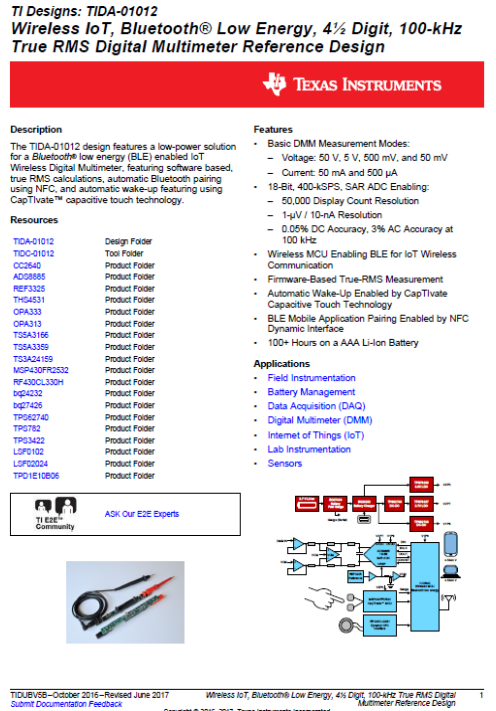
Aerospace & Defense Systems Team Overview

- **Organizational Goals**
  - Solve our customer's system-level challenges
  - Work across TI's product lines and businesses to develop system solutions maximizing signal chain, interface and power performance
  - Demonstrate individual product(s) performance within the system environment → Beyond the EVM (e.g. how does TI's Pwr, ISO, Protection, etc. impact performance)
  - Bring an End Equipment perspective to product roadmap definition

- **Aerospace & Defense Team**
  - Initiated in 2015, now at 5 System Engineers, 1 AFEs and (average YoE >15yrs)
  - Twenty six reference designs released, 9 in development!

What's included in a reference design?

- **Design Files:**
  - Complete **design guide** outlining design features, specifications, block diagram, system design theory, hardware/software, and measured results
  - **Schematics** and **Altium or CAD files**
  - **Bill of Materials**
  - **Gerber Files**
  - **Assembly Drawings**


TI Designs: TIDA-01012
Wireless IoT, Bluetooth® Low Energy, 4½ Digit, 100-kHz True RMS Digital Multimeter Reference Design

Texas Instruments

Description

The TIDA-01012 design features a low-power solution for a Bluetooth® low energy (BLE) enabled IoT Wireless Digital Multimeter, featuring software based, true RMS calculations, automatic Bluetooth pairing using NFC, and automatic wake-up featuring using CapTivate™ capacitive touch technology.

Resources

TIDA-01012	Design Folder
TIDC-01012	Tool Folder
CC2640	Product Folder
ADS8885	Product Folder
REF3325	Product Folder
THS4531	Product Folder
OPA333	Product Folder
OPA313	Product Folder
TSSA3166	Product Folder
TSSA3359	Product Folder
TSSA24159	Product Folder
MSP430FR2532	Product Folder
RF430CL330H	Product Folder
bq24232	Product Folder
bq27426	Product Folder
TPS62740	Product Folder
TPS782	Product Folder
TPS3422	Product Folder
LSF0102	Product Folder
LSF02024	Product Folder
TPD1E10B06	Product Folder

TI E2E™ Community — Ask Our E2E Experts

Features

- Basic DMM Measurement Modes:
  - Voltage: 50 V, 5 V, 500 mV, and 50 mV
  - Current: 50 mA and 500 µA
- 18-Bit, 400-kSPS, SAR ADC Enabling:
  - 50,000 Display Count Resolution
  - 1-µV / 10-nA Resolution
  - 0.05% DC Accuracy, 3% AC Accuracy at 100 kHz
- Wireless MCU Enabling BLE for IoT Wireless Communication
- Firmware-Based True-RMS Measurement
- Automatic Wake-Up Enabled by CapTivate Capacitive Touch Technology
- BLE Mobile Application Pairing Enabled by NFC Dynamic Interface
- 100+ Hours on a AAA Li-Ion Battery

Applications

- Field Instrumentation
- Battery Management
- Data Acquisition (DAQ)
- Digital Multimeter (DMM)
- Internet of Things (IoT)
- Lab Instrumentation
- Sensors

TIDUBV5B–October 2016–Revised June 2017 — Wireless IoT, Bluetooth® Low Energy, 4½ Digit, 100-kHz True RMS Digital Multimeter Reference Design — 1
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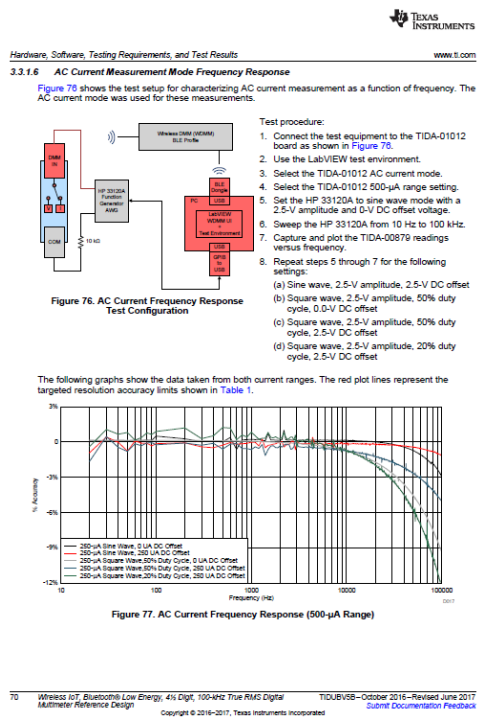
Hardware, Software, Testing Requirements, and Test Results — www.ti.com

3.3.1.6 AC Current Measurement Mode Frequency Response

Figure 76 shows the test setup for characterizing AC current measurement as a function of frequency. The AC current mode was used for these measurements.

Figure 76. AC Current Frequency Response Test Configuration

Test procedure:

1. Connect the test equipment to the TIDA-01012 board as shown in Figure 76.
2. Use the LabVIEW test environment.
3. Select the TIDA-01012 AC current mode.
4. Select the TIDA-01012 500-µA range setting.
5. Set the HP 33120A to sine wave mode with a 2.5-V amplitude and 0-V DC offset voltage.
6. Sweep the HP 33120A from 10 Hz to 100 kHz.
7. Capture and plot the TIDA-00879 readings versus frequency.
8. Repeat steps 5 through 7 for the following settings:
   (a) Sine wave, 2.5-V amplitude, 2.5-V DC offset
   (b) Square wave, 2.5-V amplitude, 50% duty cycle, 0.0-V DC offset
   (c) Square wave, 2.5-V amplitude, 50% duty cycle, 2.5-V DC offset
   (d) Square wave, 2.5-V amplitude, 20% duty cycle, 2.5-V DC offset

The following graphs show the data taken from both current ranges. The red plot lines represent the targeted resolution accuracy limits shown in Table 1.

Figure 77. AC Current Frequency Response (500-µA Range)

70 — Wireless IoT, Bluetooth® Low Energy, 4½ Digit, 100-kHz True RMS Digital Multimeter Reference Design — TIDUBV5B–October 2016–Revised June 2017
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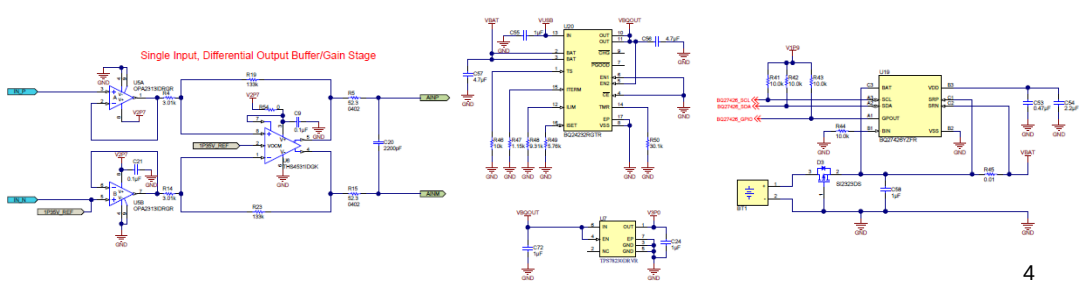
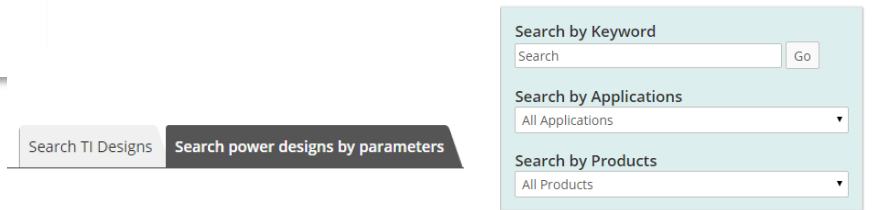


Where to find reference designs?

Main Library

- Located at: www.ti.com/tidesigns
- Search by keyword, application, or products

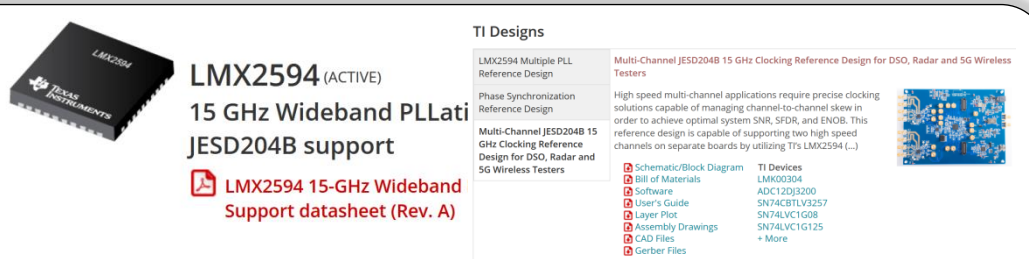


Find through Application Folders

- Located at: www.ti.com/applications
- Search by market, sector or application

Find through Product Folders

- Located at individual product pages
- Find TI Designs under the Tools & Software tab



Reference Designs for High Speed Systems

Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers - TIDA-01021

Features

- 15 GHz Multi-channel JESD204B complaint clocking solution,
  - Device clock frequency – LMX2594 (max – 15 GHz)
  - SYSREF provided for JESD204B interface – LMX2594
- Scalable clocking solution, which can generate various DEVCLK by LMX2594 / LMK04828
- FMC connector adaptor boards to interface with TI high speed analog front end EVMs
- Low power and highly integrated multi-channel clocking solution with JESD204B complaint

Target Applications

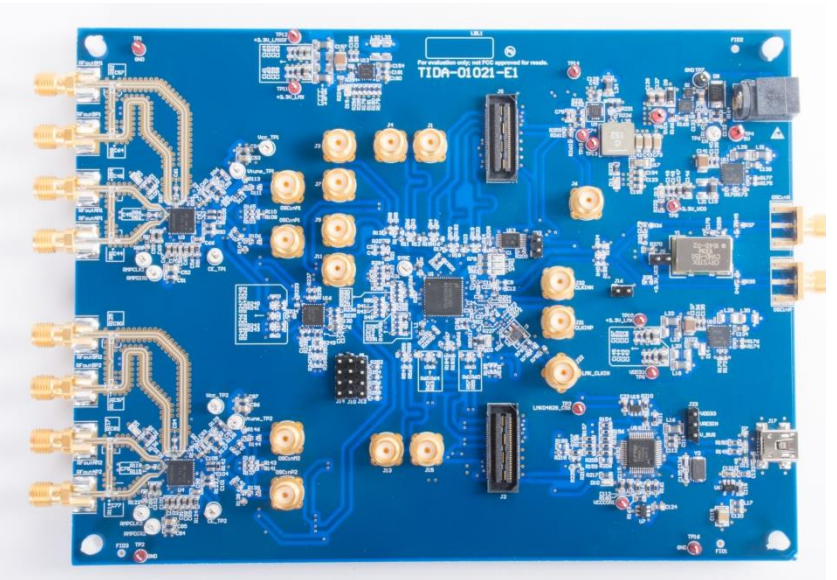
- Oscilloscope
- Wireless Communication Tester
- Software Defined Radio
- Phased Array Radar

Tools & Resources

- Synchronization of JESD204B Giga-Sample ADCs using Xilinx Platform for Phased Array Radar Systems
- LMX2594 – Expected RTM (Q1'17)

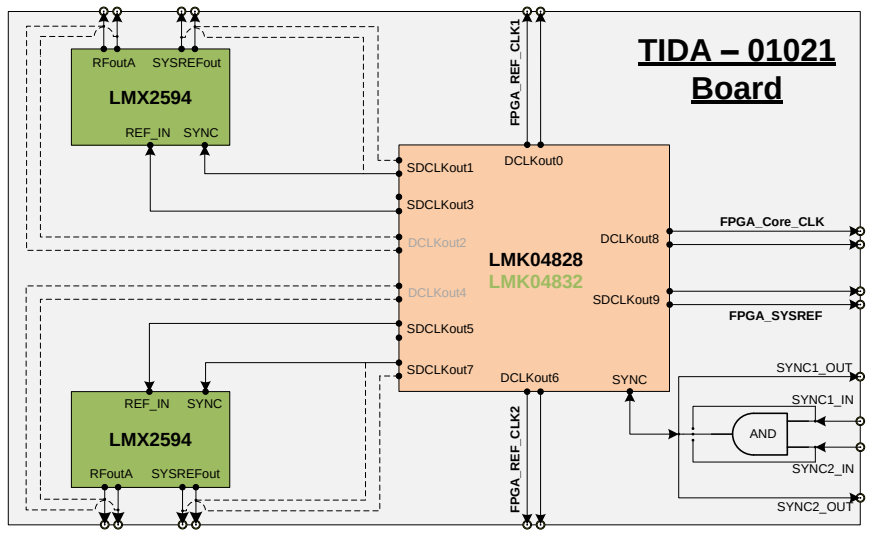
Benefits

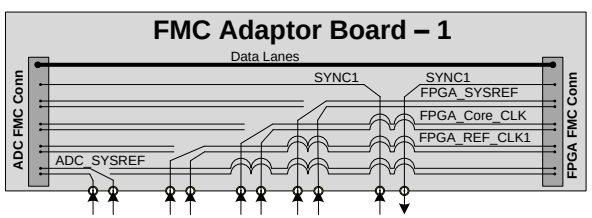
- JESD204B compatible clocking solution for high dynamic range and high SNR multi-channel AFE signal chain
- Configurable phase synchronization to achieve low skew
- 15 GHz clocking solution can be used in multiple end equipments (DSO, Radar, Wireless Test, etc.)
- Supports low latency signal measurement and signal generation systems

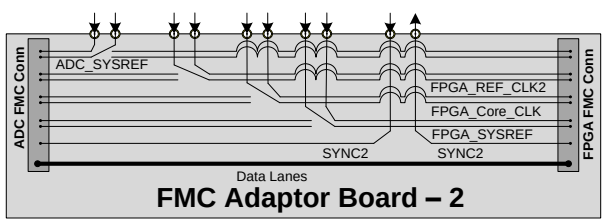


Subsystem block diagram

Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers

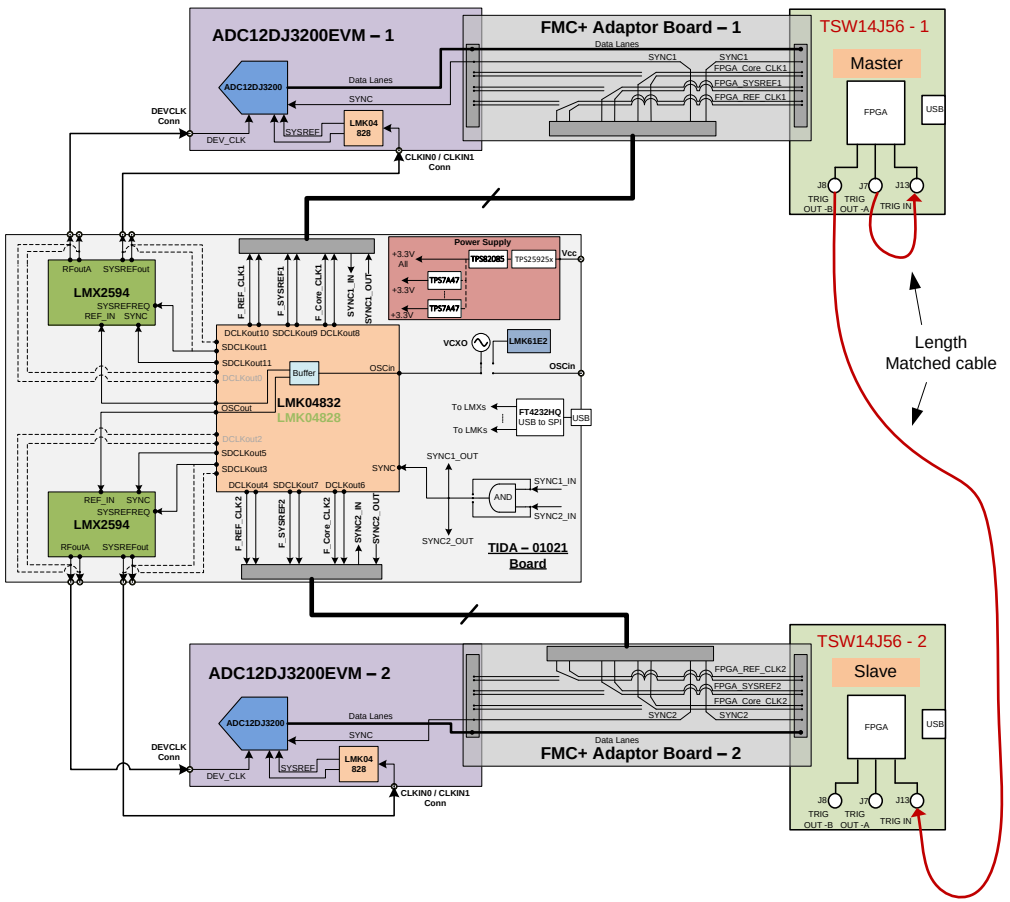




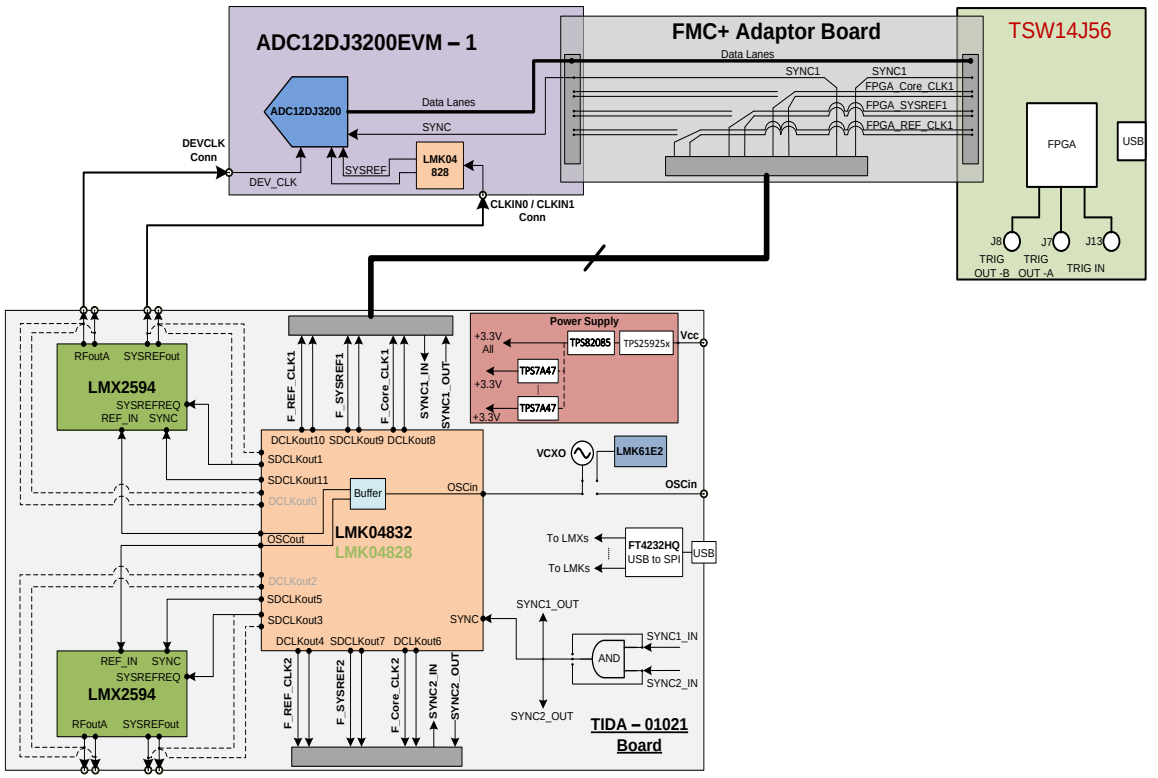


Subsystem test setup block diagram

Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers



* Test setup block diagram for channel-to-channel skew measurement



* Test setup block diagram for SNR measurement

Reference design results

Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers

Table 3. Measured Phase Noise

OUTPUT FREQUENCY (GHz)	CONDITION	EXPECTED PHASE NOISE (dBc/Hz)	MEASURED PHASE NOISE (dBc/Hz)
3.5	10-kHz offset	–117.0	–116.0
	100-kHz offset	–119.7	–118.3
	1-MHz offset	–130.5	–128.7
	10-MHz offset	–149.5	–151.5
9.0	10-kHz offset	–108.8	–108.1
	100-kHz offset	–111.4	–110.1
	1-MHz offset	–123.1	–122.9
	10-MHz offset	–147.4	–147.5
15.0	10-kHz offset	–104.7	–103.8
	100-kHz offset	–107.5	–105.9
	1-MHz offset	–114.7	–115.1
	10-MHz offset	–141.7	–140.8

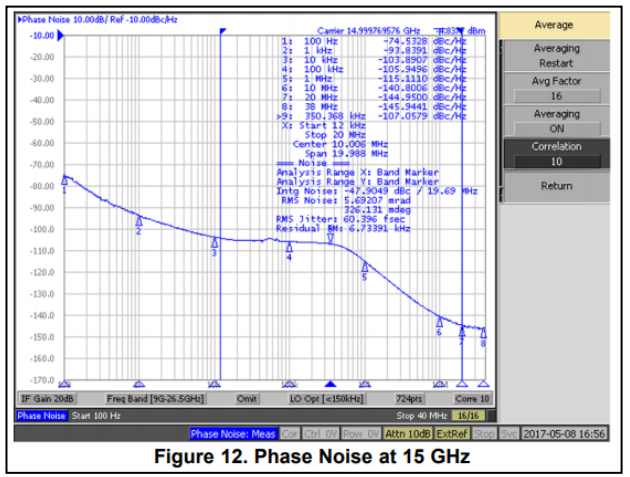


Figure 12. Phase Noise at 15 GHz

Input Freq (MHz)	ADC Datasheet SNR (dBFS)	Measured SNR on ADC12DJ3200 EVM with on board clock (dBFS)	Measured SNR on ADC12DJ3200 EVM with TIDA-01021 clocks (dBFS)
997	56.3	55.25	55.72
2482	55.2	52.71	53.94
5250*	52.6	50.34	49.6*

INPUT FREQUENCY (MHz)	MEASURED TIME SKEW (ps)
997	9.23
2482	9.35

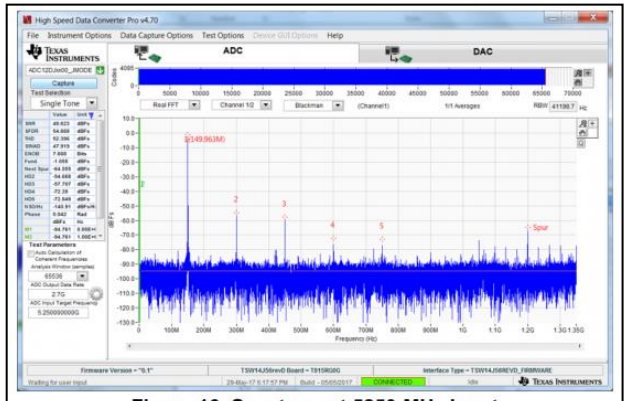


Figure 16. Spectrum at 5250-MHz Input

High Channel Count JESD204B Clock Generation Reference Design for DSO, Radar and 5G Wireless Testers - TIDA-01023

Features

- Scalable 15 GHz Multi-channel JESD204B complaint clocking solution,
  - Device clock frequency – LMX2594 (max – 15 GHz)
  - SYSREF provided for JESD204B interface – LMX2594
- Scalable clocking solution, which can generate various DEVCLK by LMX2594 / LMK04828
- FMC connector adaptor boards to interface with TI high speed analog front end EVMs
- Low power and highly integrated multi-channel clocking solution with JESD204B complaint

Benefits

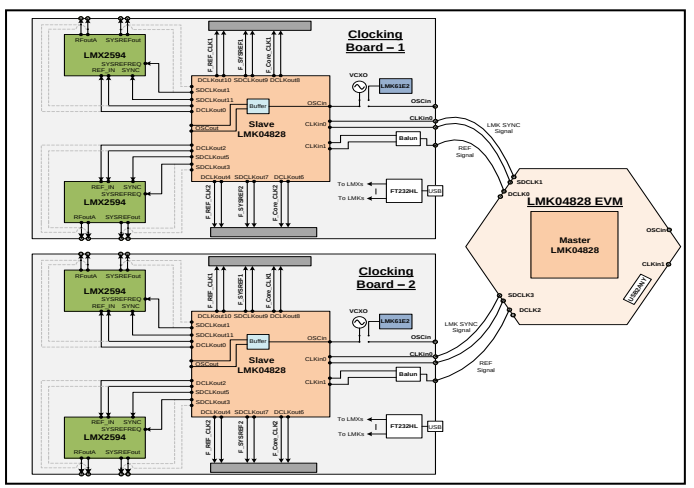
- JESD204B compatible clocking solution for high dynamic range and high SNR multi-channel AFE signal chain
- Configurable phase synchronization to achieve low skew
- Scalable 15 GHz clocking solution can be used in multiple end equipments (DSO, Radar, Wireless Test, etc.)
- Supports low latency signal measurement and signal generation systems

Target Applications

- Oscilloscope
- Wireless Communication Tester
- Software Defined Radio
- Phased Array Radar

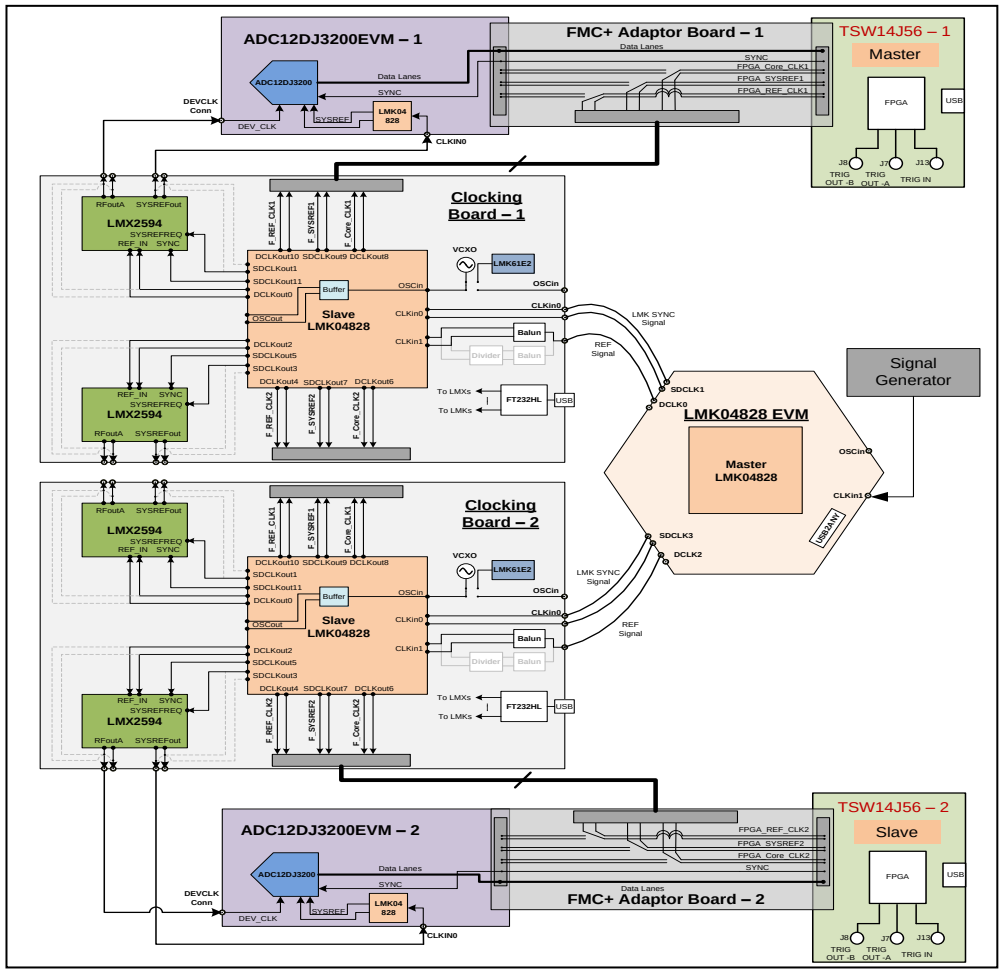
Tools & Resources

- TIDA-01021
- LMK04828EVM
- ADC12DJ3200EVM
- TSW14J56/57



Subsystem block diagram

High Channel Count JESD204B Clock Generation Reference Design for DSO, Radar and 5G Wireless Testers

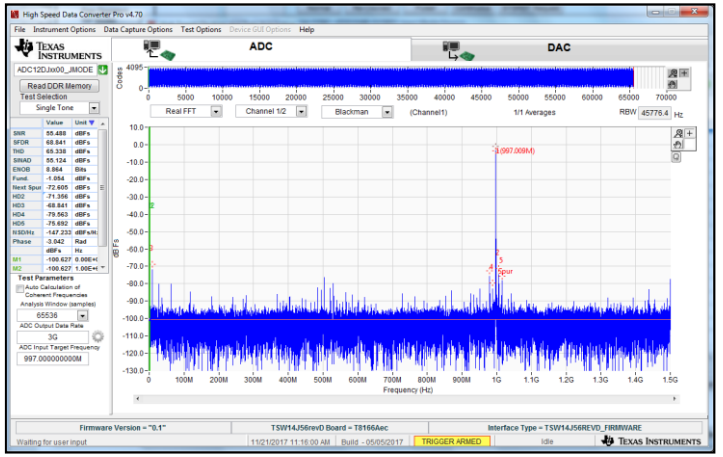


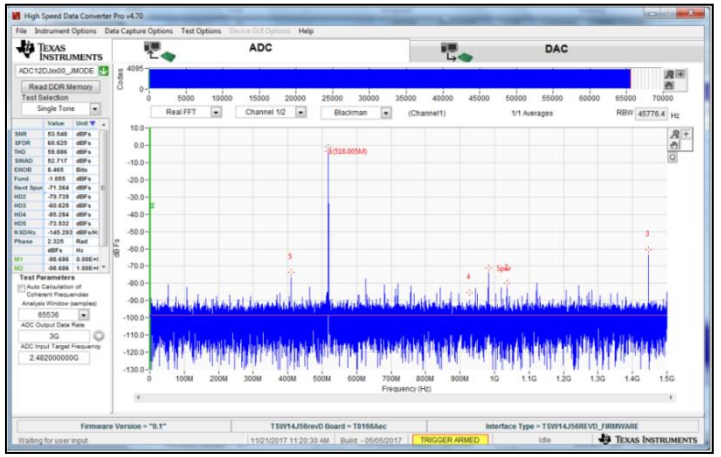
- Designed multi channel clocking board 1 & 2 provides the synchronized JESD204B complained clocks using the Master LMK04828, which provides the reference signals and sync signals to both clocking boards.
- Designed FMC+ adaptor boards provides the interface between TI existing HS ADC EVMs and capture cards
- Multi channel clocking board further scalable up to 7 boards, with the remaining ports of master LMK04828
- Scaling can be more by using the tree topology
- No propagation delay shift over temperature

Clock demonstration with ADC12DJ3200

High Channel Count JESD204B Clock Generation Reference Design for DSO, Radar and 5G Wireless Testers

- ADC12DJ3200 EVM on-board clocks are replaced with TIDA-01023 clocks
- TIDA-01023 on-board LMX2594 generates DEV_CLK – 3GHz and SYSREF – 37.5MHz
- FPGA Clocks are distributed by TIDA-01023 on-board LMK04828 (Slave)
- LMX2594 PLL Synthesizer settings are:
  - REFin – 37.5MHz
  - PD freq – 37.5MHz
- Measured system SNR is improved by the 0.2 to 0.5 dB to the ADC12DJ3200EVM performance and close to the datasheet specs



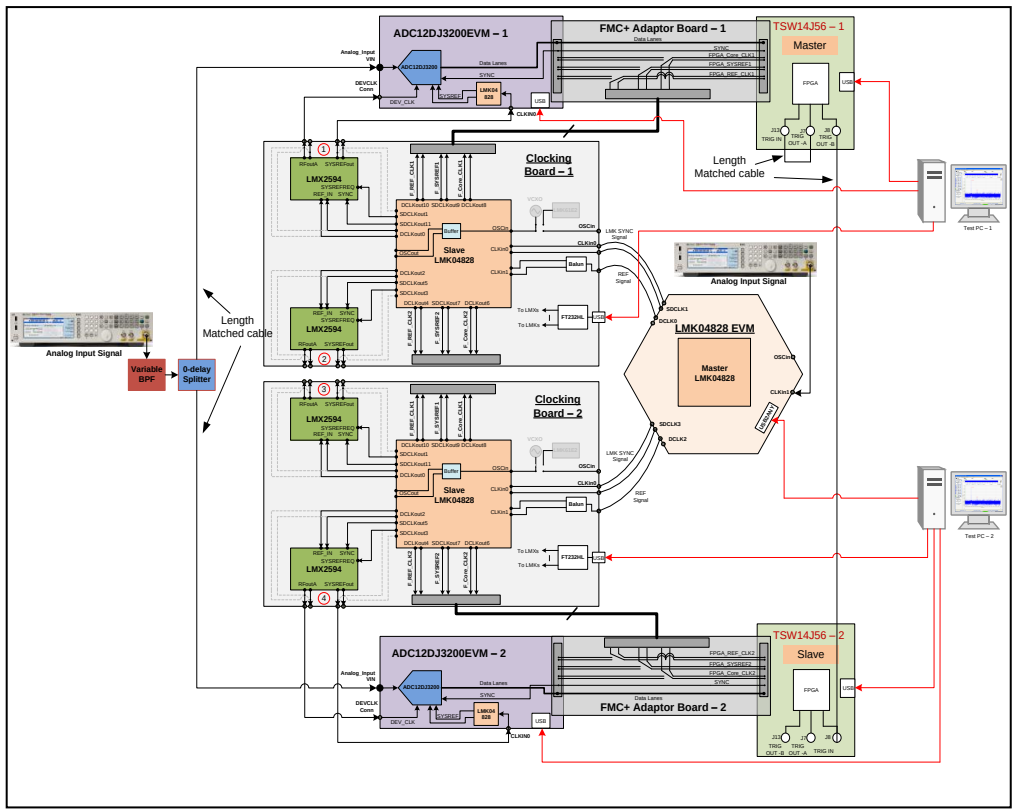


Input Freq (MHz)	ADC Datasheet SNR (dBFS)	Measured SNR on ADC12DJ3200EVM with onboard clocks (dBFS)	Measured SNR on ADC12DJ3200EVM with TIDA-01023 clocks (dBFS)
997	56.3	55.25	55.4
2482	55.2	52.71	53.5

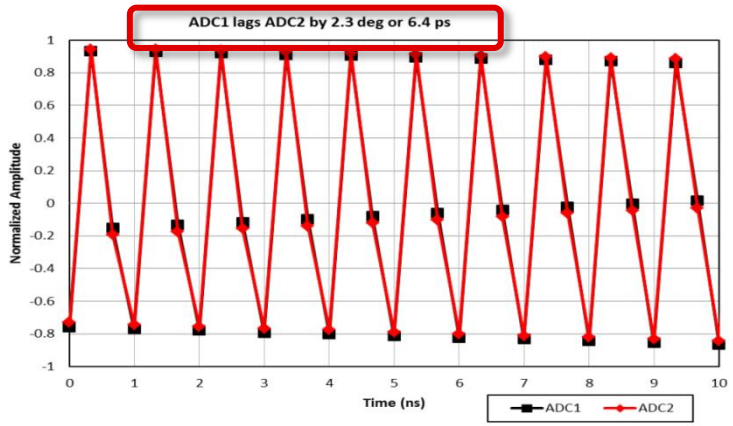
Clock synchronization demonstration with two ADC12DJ3200 channels

High Channel Count JESD204B Clock Generation Reference Design for DSO, Radar and 5G Wireless Testers

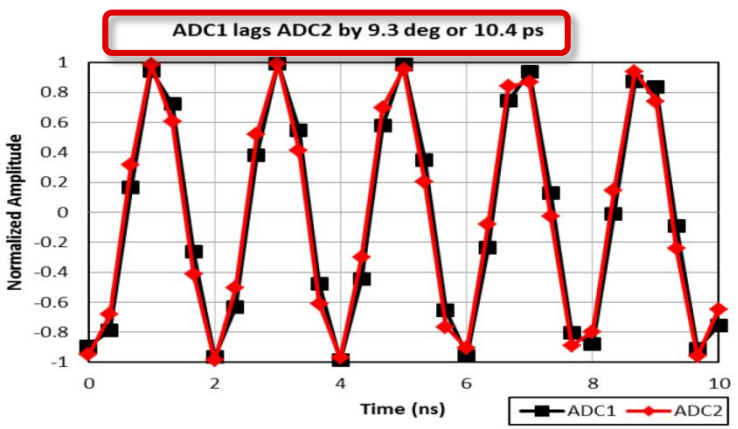
Test setup block diagram



Measured Channel to channel skew



Sampled Signals at 997-MHz Input



Sampled Signals at 2482-MHz Input

Large scale multi-channel daisy chained JESD204B clocking reference design for RADAR, MIMO and 5G systems - TIDA-01024

Features

- Scalable 15 GHz Multi-channel JESD204B complaint clocking solution,
  - Device clock frequency – LMX2594 (max – 15 GHz)
  - SYSREF provided for JESD204B interface – LMX2594
- Scalable clocking solution, which can generate various DEVCLK by LMX2594 / LMK04828
- FMC connector adaptor boards to interface with TI high speed analog front end EVMs
- Low power and highly integrated multi-channel clocking solution with JESD204B complaint

Benefits

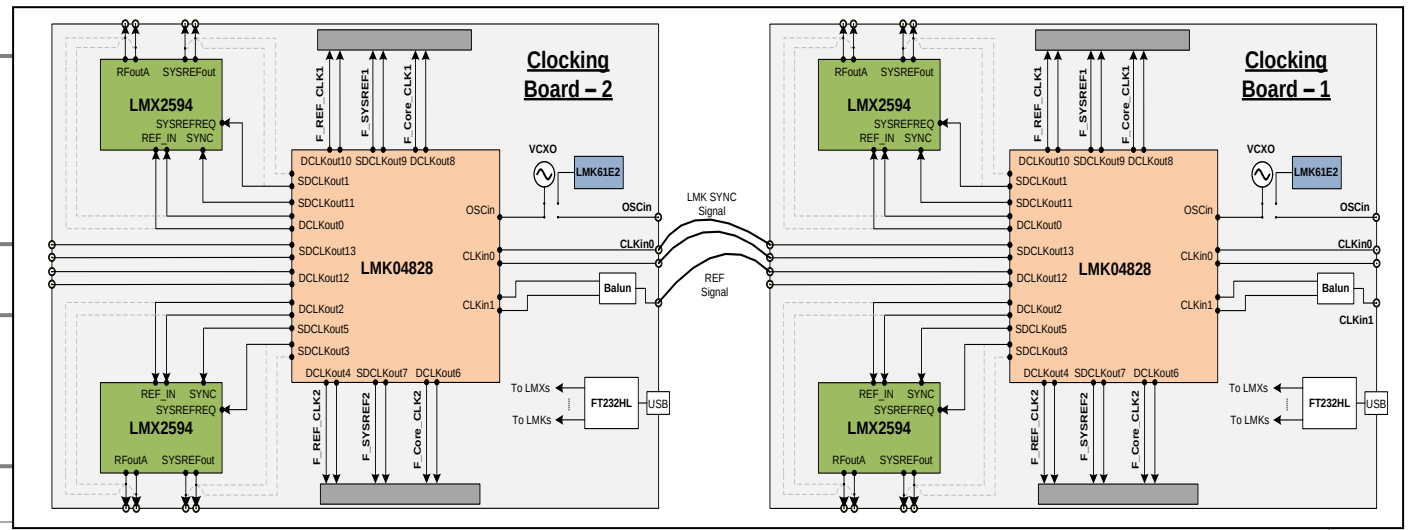
- JESD204B compatible clocking solution for high dynamic range and high SNR multi-channel AFE signal chain
- Configurable phase synchronization to achieve low skew
- Scalable 15 GHz clocking solution can be used in multiple end equipments (DSO, Radar, Wireless Test, etc.)
- Supports low latency signal measurement and signal generation systems

Target Applications

Oscilloscope
Wireless Communication Tester
Software Defined Radio
Phased Array Radar

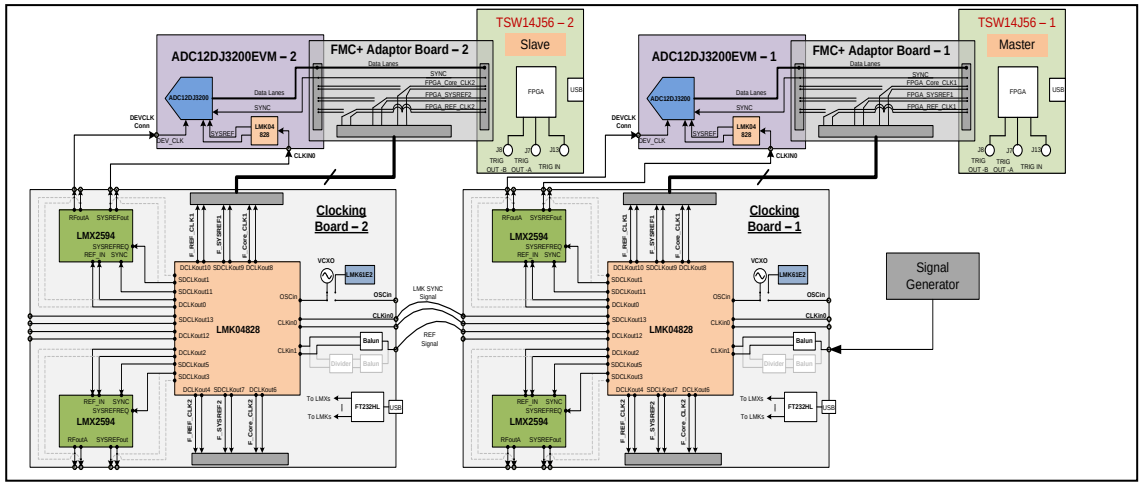
Tools & Resources

- TIDA-01021
- LMK04828EVM
- ADC12DJ3200EVM
- TSW14J56/57



Subsystem block diagram

Large scale multi-channel daisy chained JESD204B clocking reference design for RADAR, MIMO and 5G systems

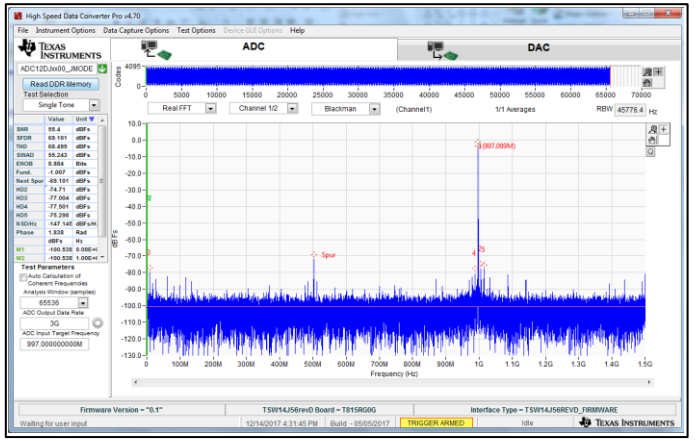


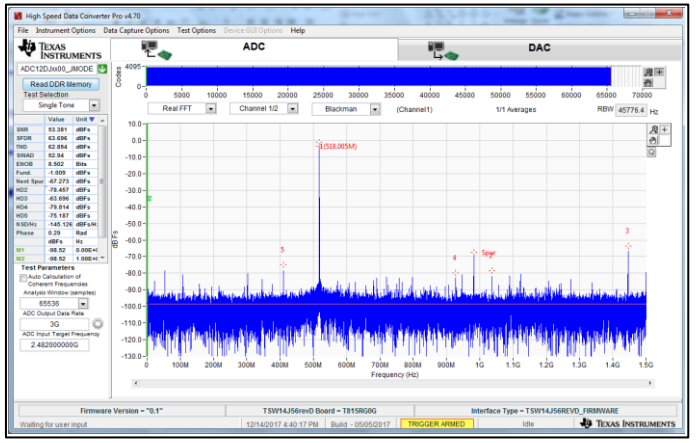
- Designed multi channel clocking board 1 & 2 provides the synchronized JESD204B complained clocks in daisy chain configuration, which get the reference signal and sync signals from the previous board.
- Designed FMC+ adaptor boards provides the interface between TI existing HS ADC EVMs and capture cards
- Multi channel clocking board further scalable without affecting the previous section of the chain
- Scaling up is more easy but it could not be use where temp drift is more which affects the reference signal feeding to each board

Clock demonstration with ADC12DJ3200

Large scale multi-channel daisy chained JESD204B clocking reference design for RADAR, MIMO and 5G systems

- ADC12DJ3200 EVM on-board clocks are replaced with TIDA-01024 clocks
- TIDA-01024 on-board LMX2594 generates DEV_CLK – 3GHz and SYSREF – 37.5MHz
- FPGA Clocks are distributed by TIDA-01024 on-board LMK04828 (Slave)
- LMX2594 PLL Synthesizer settings are:
  - REFin – 37.5MHz
  - PD freq – 37.5MHz
- Measured system SNR is improved by the 0.2 to 0.5 dB to the ADC12DJ3200EVM performance and close to the datasheet specs



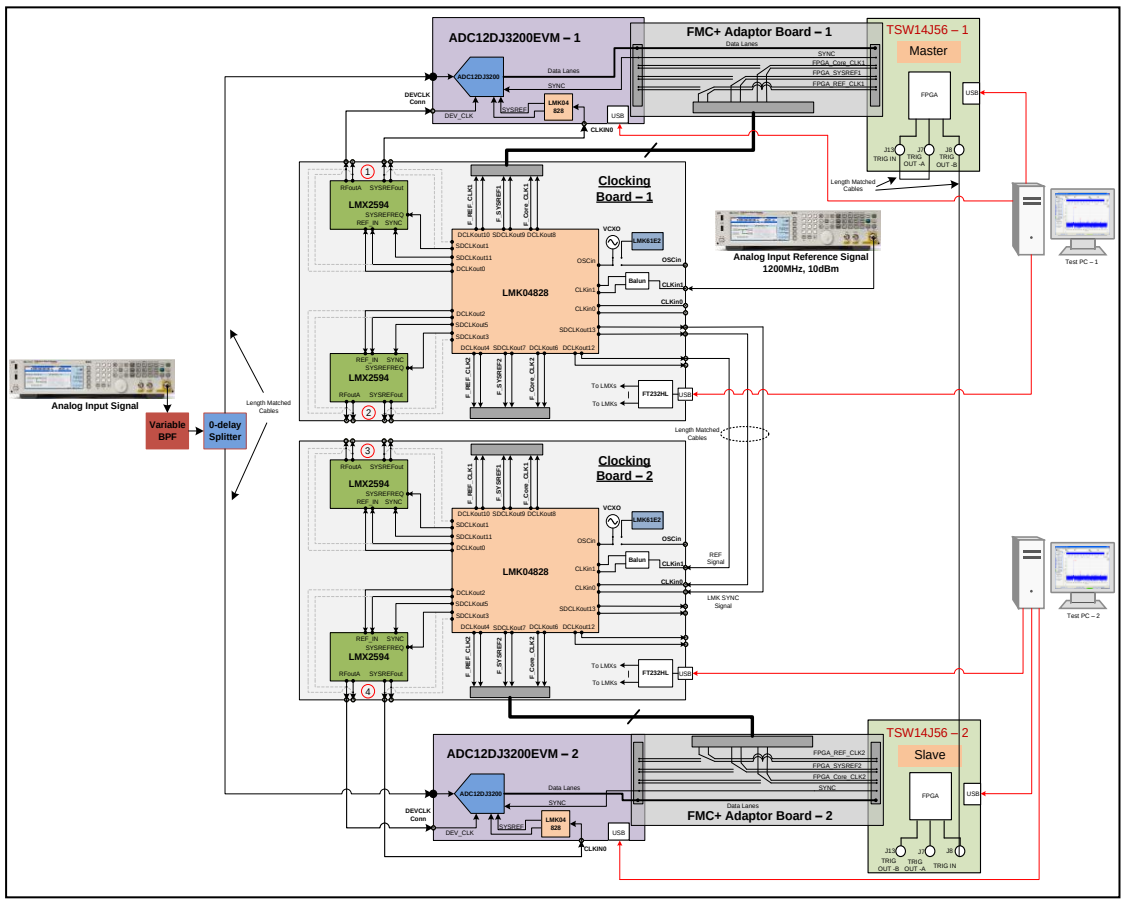


Input Freq (MHz)	ADC Datasheet SNR (dBFS)	Measured SNR on ADC12DJ3200EVM with onboard clocks (dBFS)	Measured SNR on ADC12DJ3200EVM with TIDA-01024 clocks (dBFS)
997	56.3	55.25	55.4
2482	55.2	52.71	53.38

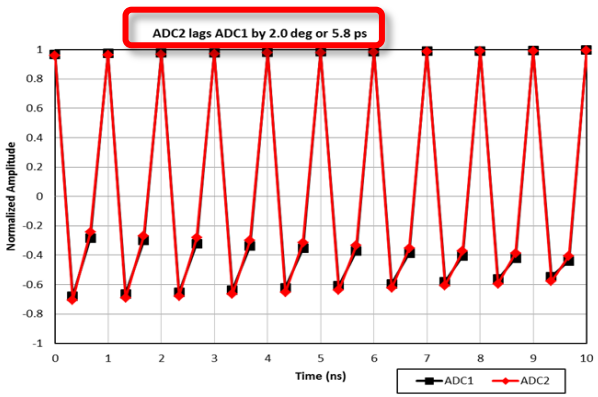
Clock synchronization demonstration with two ADC12DJ3200 channels

Large scale multi-channel daisy chained JESD204B clocking reference design for RADAR, MIMO and 5G systems

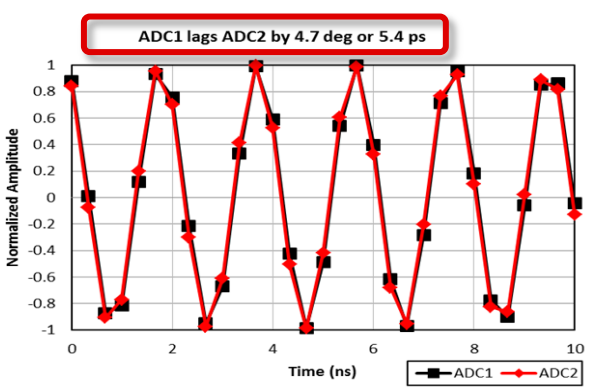
Test Setup Block Diagram



Measured Channel to channel skew



Sampled Signals at 997-MHz Input



Sampled Signals at 2482-MHz Input

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems - TIDA-01022

Features

- Flexible analog input bandwidth and sample rate for multichannel configuration
- Maximum Analog Input Bandwidth – DC to 1.5 GHz
- Analog Front End Sampling Performance
  - 3.2 Gsps (Multi-channel 4 channel)
- Pin compatible ADCs
  - ADC12DJ3200 / ADC12DJ2700 / ADC12DJ1600
- Multi-channel JESD204B complaint clocking solution to generate DEV CLK / SYSREF
  - LMK04828 with LMX2594
- JESD204B Support
  - Connects to Next Generation High Speed ADC capture cards (TSW14J56 / TSW14J57)
  - 8/16/32 lanes options @ 12.5 Gbps

Benefits

- High performance 12 bit analog capture
- Scalable Platform
  - Analog Input Channels (up to 4)
  - Analog input bandwidth (DC to 1.5GHz)
  - Front End Sampling clock (Up to 3.2 Gsps)
  - JESD lane support (up to 32 lanes on board)
- Integrated high speed clocking solution for multichannel synchronization.
- Support HSDC Pro GUI for Advanced system parameter Analysis

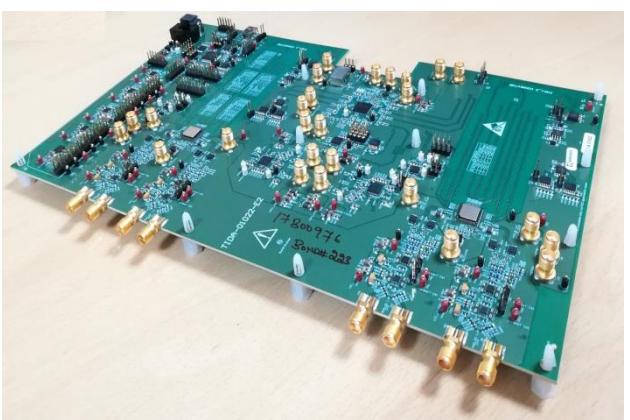
Target Applications

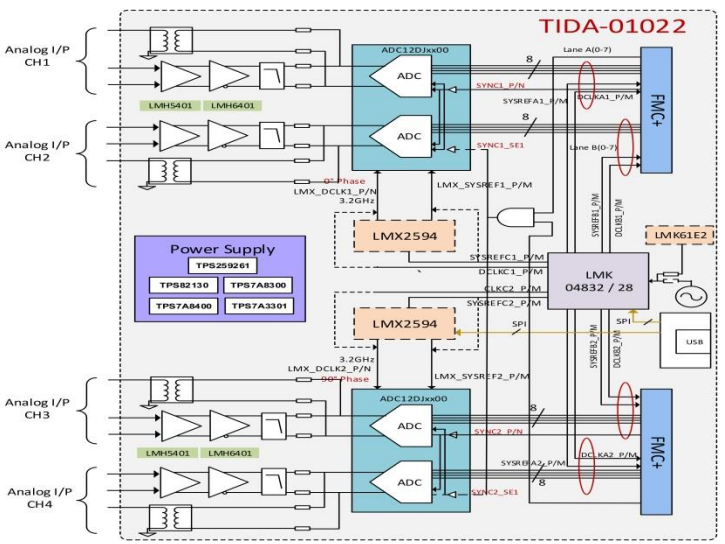
- High Performance Oscilloscopes
- Wireless Communication Test Equipment
- Software Defined Radio
- RADAR

Tools & Resources

TSW14J56EVM
ADC12DJ3200 EVM

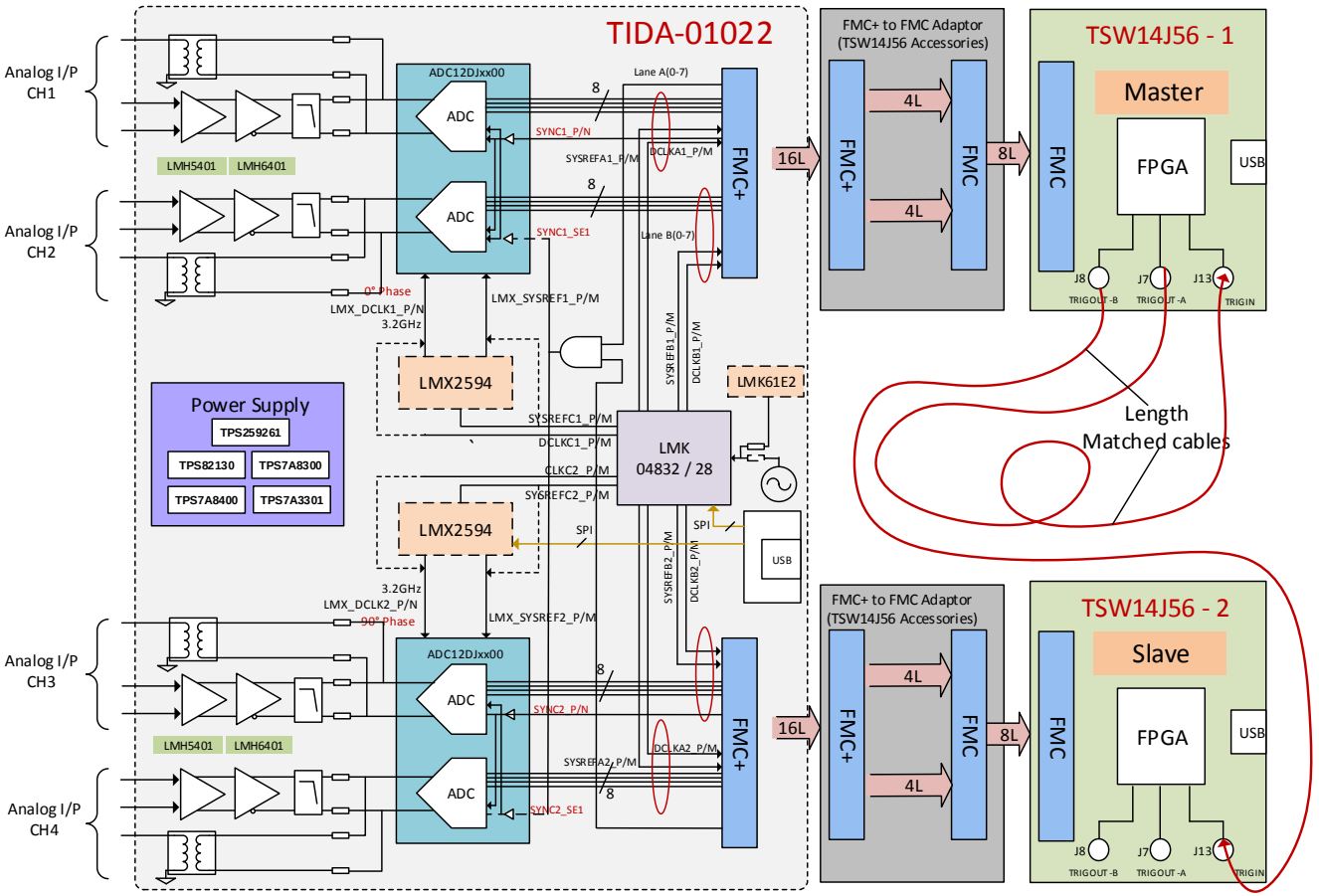
Key parts
ADC12DJ3200, LMK04828, LMX2594, LMH5401, LMH6401





System block diagram/test setup with TSW14J56

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems



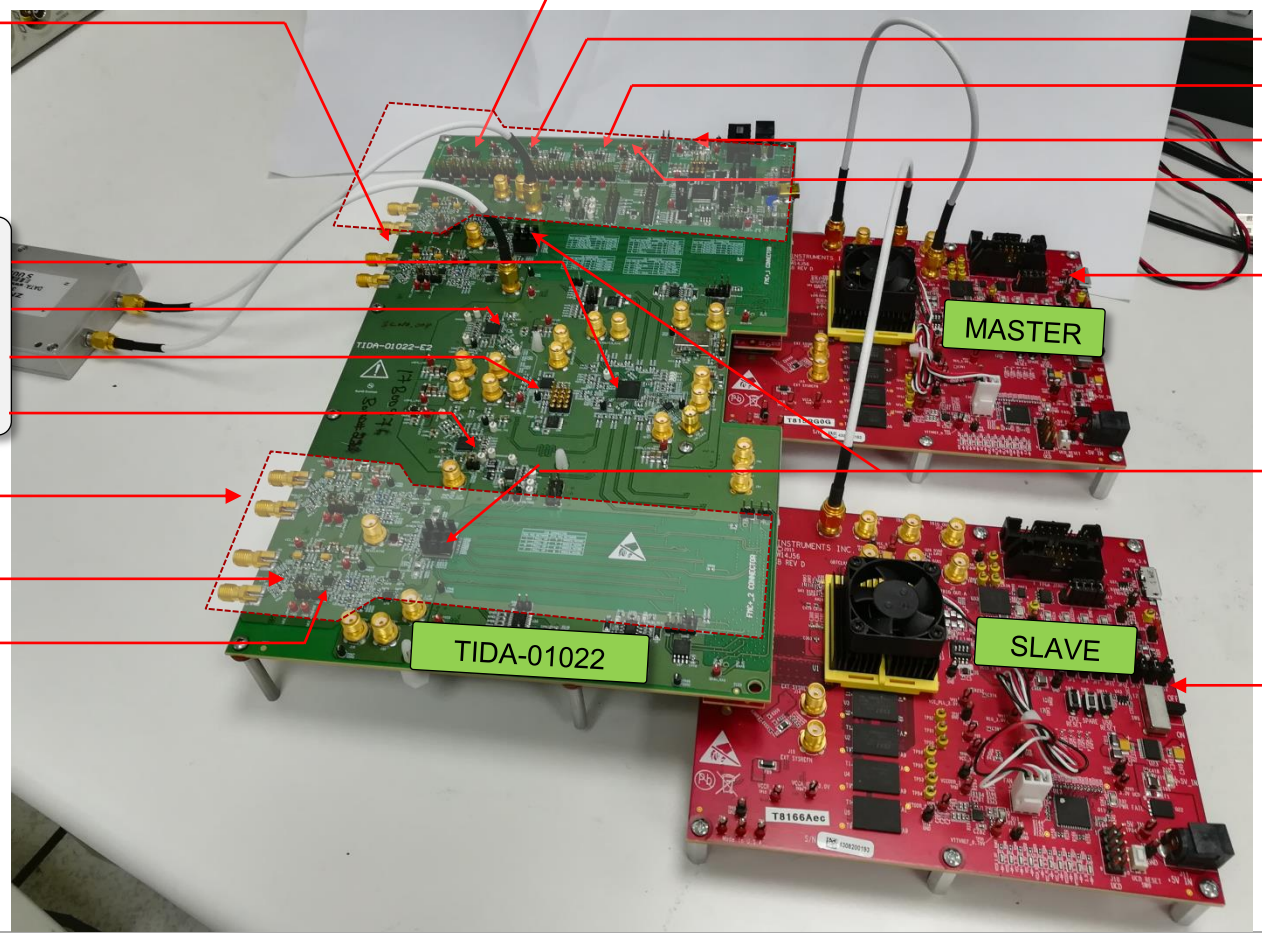
TSW14J56 Master Slave Mode				
Clock Solution : LMK04828 & LMX2594 (up to 15 GHz max) Input Bandwidth : 6 GHz ‡				
Input Channels/ Interleave	**Sampling Speed (Gsps)**	**ADC**	**No of Lane / Per Device**	**Lane rate (Msps)**
4-ch	1.6	2x ADC12DJ1600	8L	6400
	2.7	2x ADC12DJ2700	8L	10800
	3.0	2x ADC12DJ3200	8L	12000
2-ch On chip	3.2	2x ADC12DJ1600	8L	6400
	5.4	2x ADC12DJ2700	8L	10800
	6.1	2x ADC12DJ3200	8L	12800
1-ch On board	6.4	2x ADC12DJ1600	8L	6400
	10.8	2x ADC12DJ2700	8L	10800
	12.8 (12.3 †)	2x ADC12DJ3200	8L	12800
† Clock solution : LMK04832 alone ‡ Amplifier bypassed				

Sample clock option

- 3.2 Gsps (LMK04828 + LMX2594)

Hardware setup

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems



Channels 1 & 2

Clock
LMK04828
LMX2594
LMK00304
LMX2594

Channels 3 & 4

LMH5401
LMH6401
Amplifier

Power
TPS7A3301 (LDO)
TPS7A8300 (LDO)
TPS7A8400 (LDO)
TPS259261
TPS82130 (DC-DC)

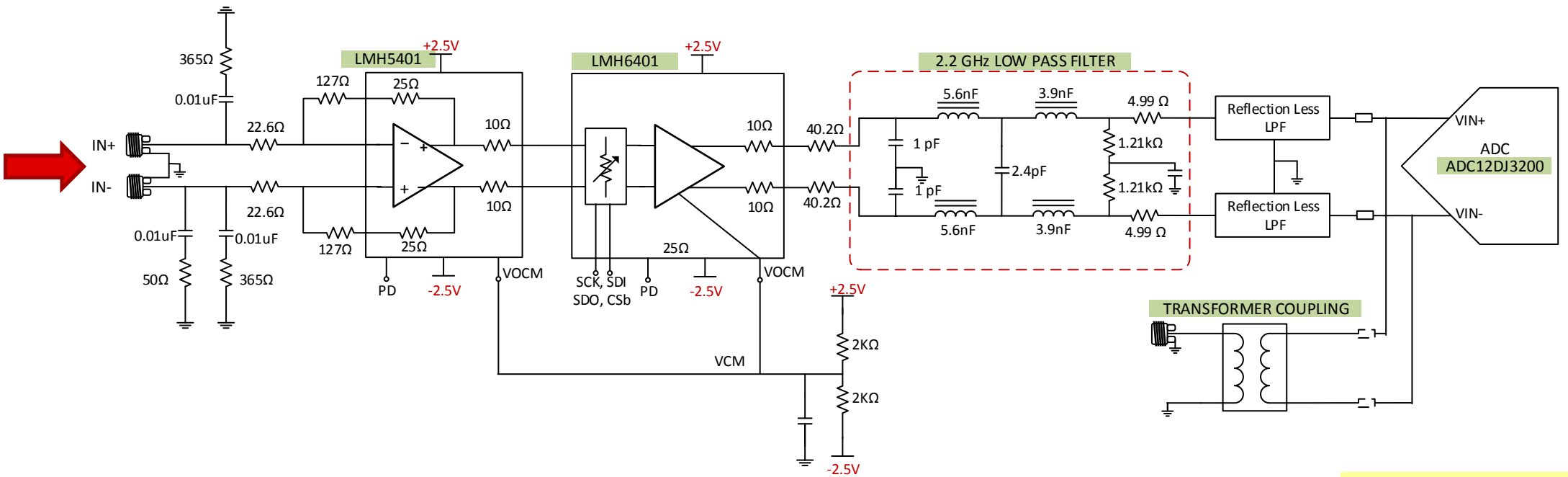
Capture Card
TSW14J56/57

Data Converter
ADC12DJ3200

Capture Card
TSW14J56/57

Analog front end – high performance signal chain

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

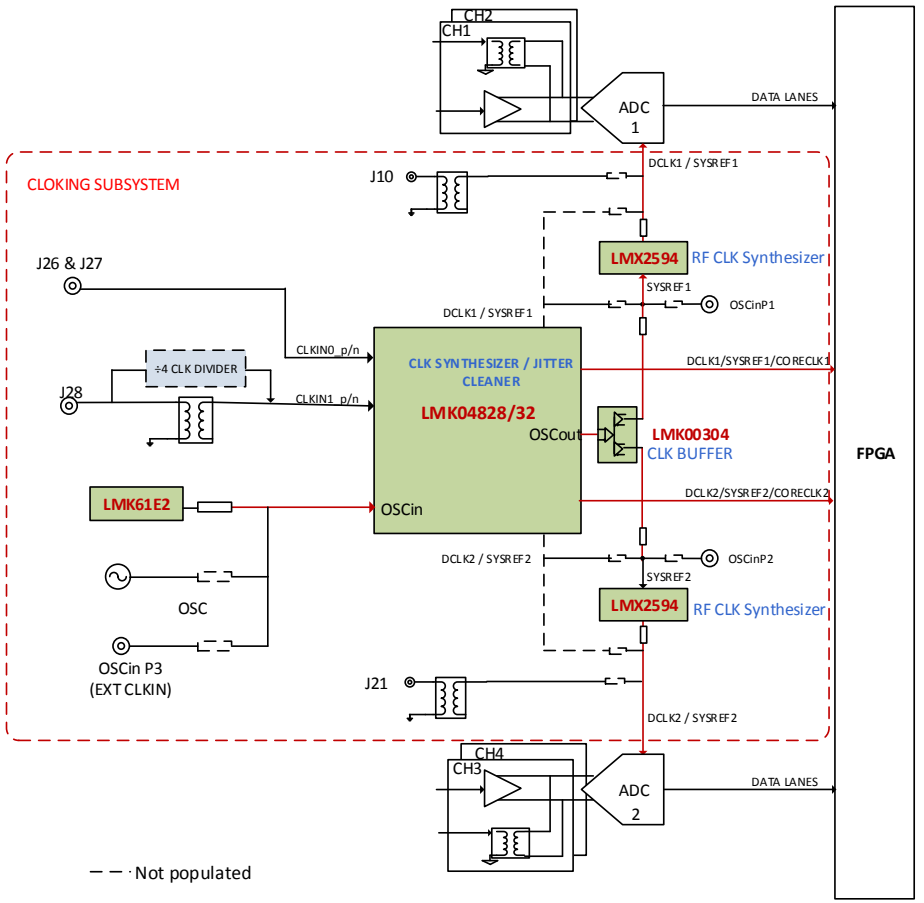


- Support AC and DC input coupling
- Support both single ended and differential Input
- Input Analog Bandwidth DC - 1.5GHz
- Programmable Gain up to 30.4dB (LMH5401+LMH6401)

Key parts
ADC12DJ3200
LMH5401
LMH6401

Clocking options – clock tree

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems



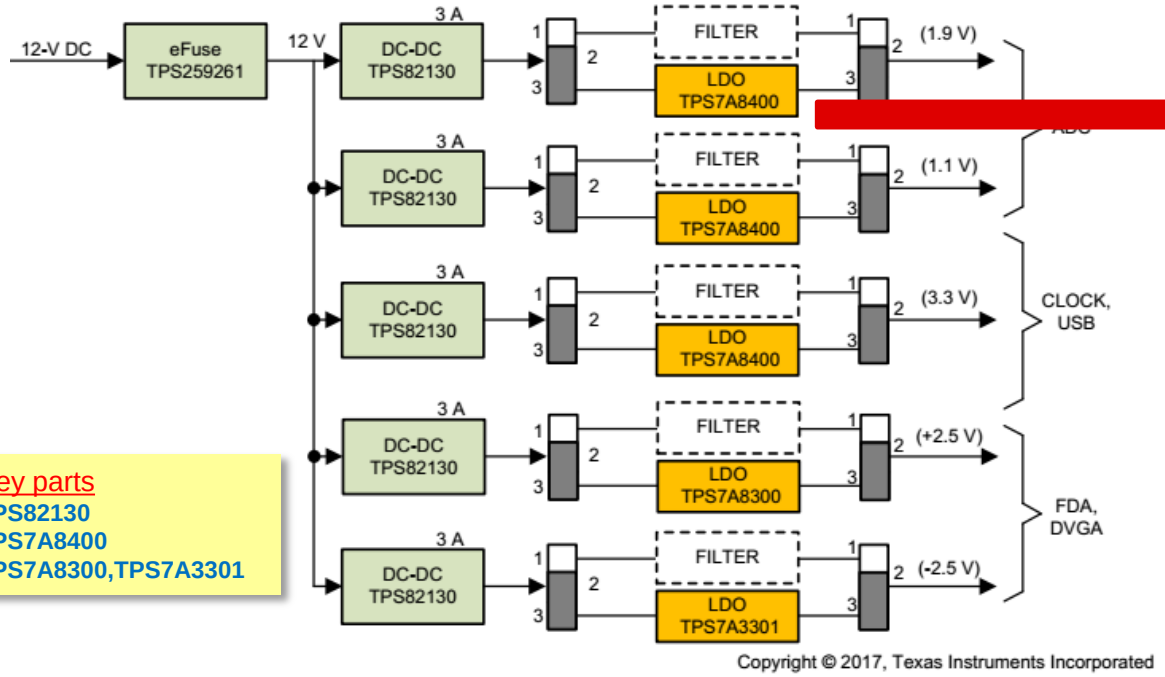
Connector Options

1. OSCin of LMK04828 accepts reference clock input from any one of following
   - LMK61E2 oscillator
   - On board VCXO
   - External clock via OSCin P3 SMA connector
2. CLKIN0 accepts standard 10 MHz or 100 MHz reference from SMA connector (J26,J27)
3. CLKIN1 accepts clocks from SMA connector (J28) through clock divider ,this divide by 4 clock divider useful to divide very high input clock source
4. SMA connector OSCinP1,OSCinP2 used to provide external SYSREF to LMX2594
5. SMA connector J10,J21 used to provide the DCLK to ADC1 & ADC2 directly from external clock source

Key parts
LMK04828
LMX2594
LMK61E2

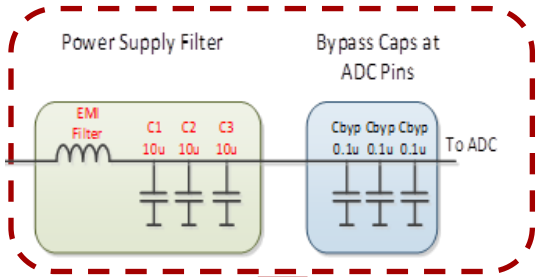
Power supply block diagram

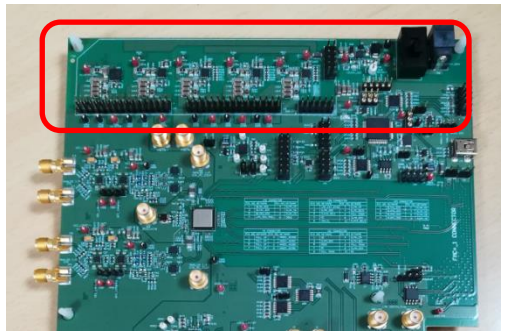
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems



Key parts
TPS82130
TPS7A8400
TPS7A8300,TPS7A3301

TI Design planned for Q1-2018





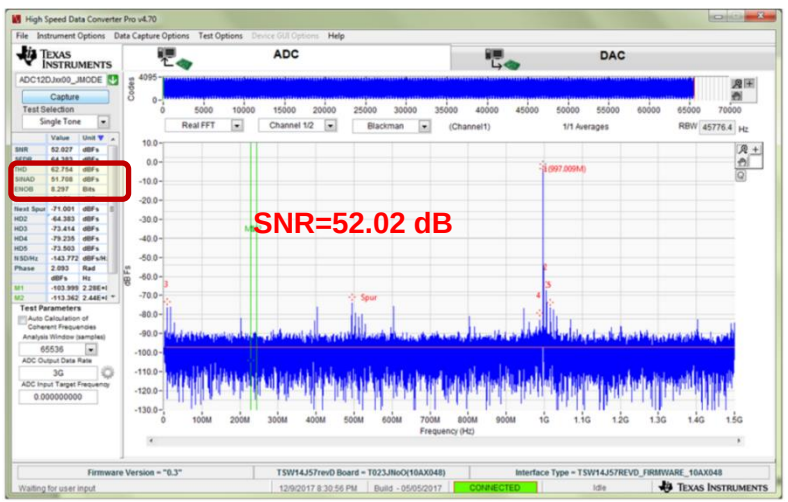
- Provided optimized power solution that minimize SNR and SFDR degradation while using switching regulator.
- Optimized solution for overall system power and PCB board area.

Test results – (LMH5401 + LMH6401) input

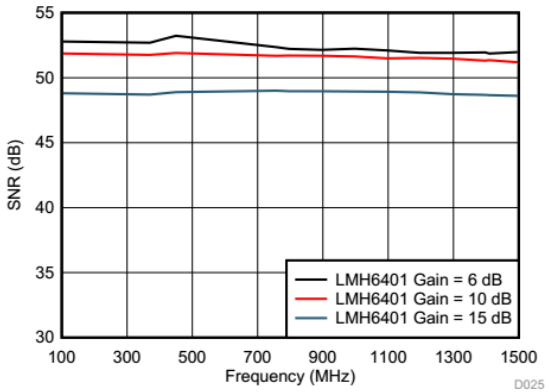
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

Test Condition:

- ADC dual channel mode (JMODE2)
- Single channel measurement
- Sample rate 3GHz
- AIN = -1dBFS
- CH3,4 LMX2594 clock portion off
- Capture card used
  - TSW14J57

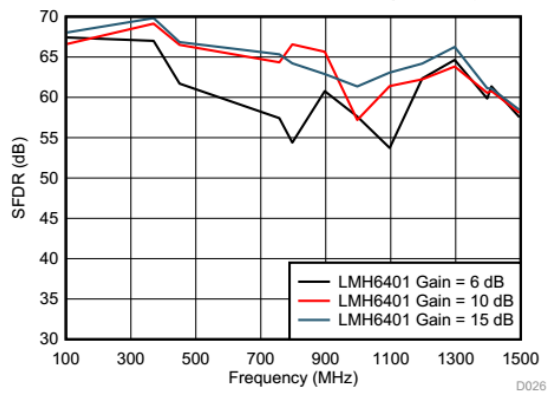


SNR, Gain vs Frequency



LMH5401 Gain = 12 dB

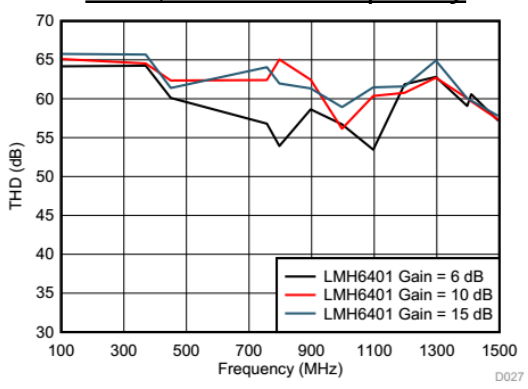
SFDR, Gain vs Frequency



LMH5401 Gain = 12 dB

- Cascaded Amplifier Input (FDA + DVGA)
- front end provides wide dynamic range (-6 to 24.4 dB)
- Programmable gain in 1dB step
- Programmable common mode voltage

THD, Gain vs Frequency



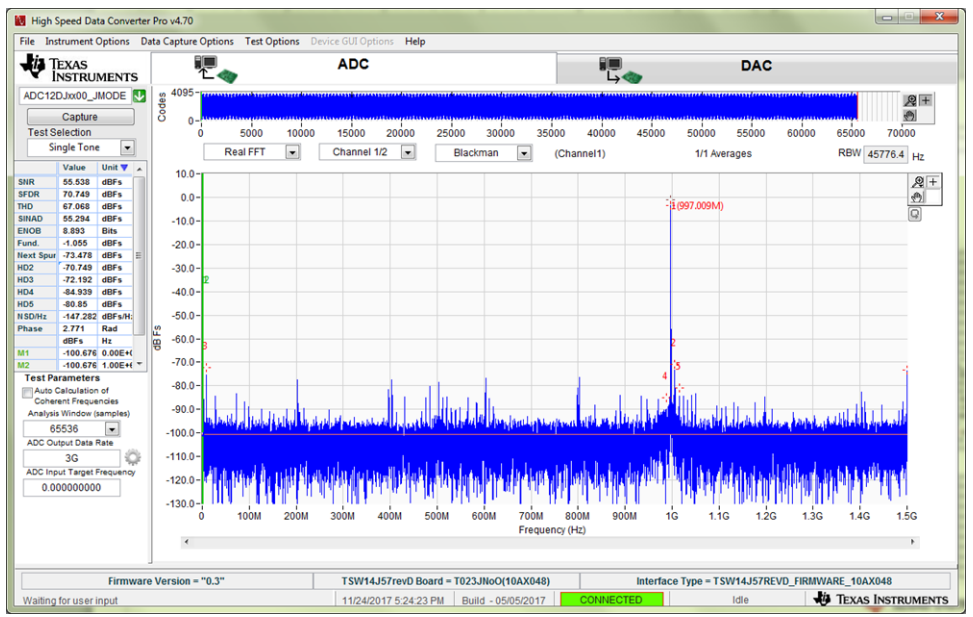
LMH5401 Gain = 12 dB

Test results – transformer input

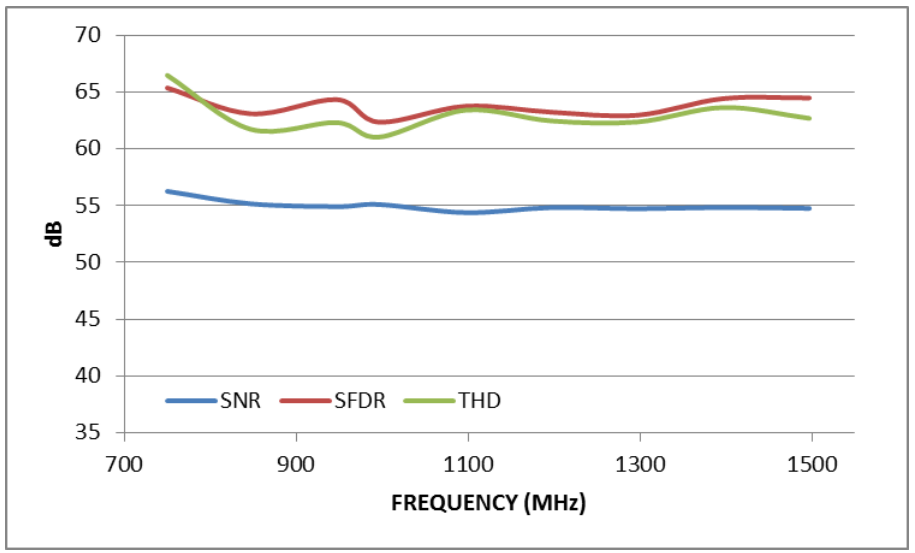
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

Test Condition

- ADC Dual channel mode (JMODE2)
- Sample rate 3GHz
- AIN = -1dBFS



SNR, SFDR and THD vs Frequency



Test results – channel to channel skew

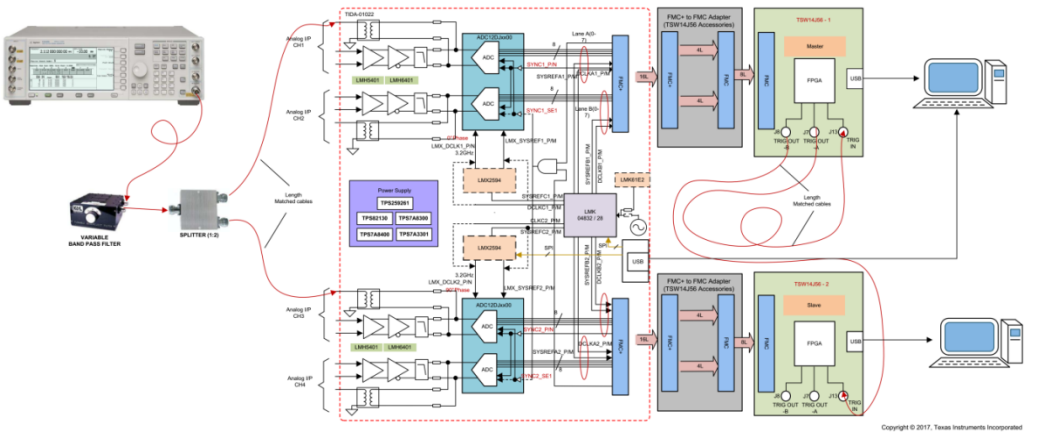
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

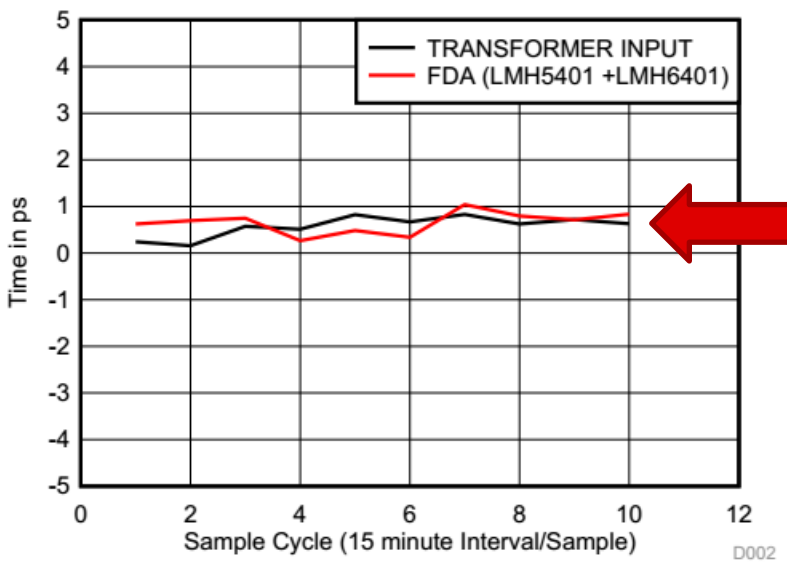
Test Condition

- Input Signal Frequency: 997 MHz
- Sampling Frequency : 2700 MHz

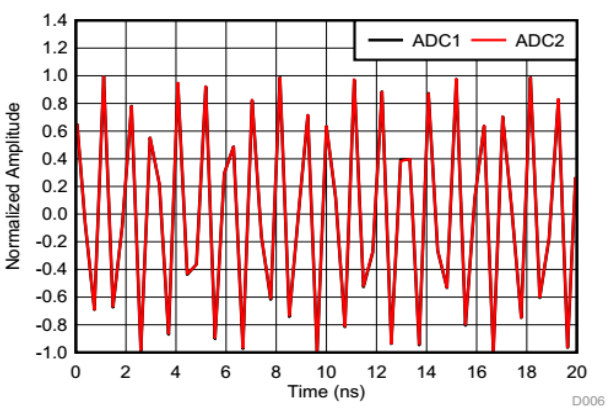
Test Mode

- Master slave with TSW14J56





Less than 5 psec skew

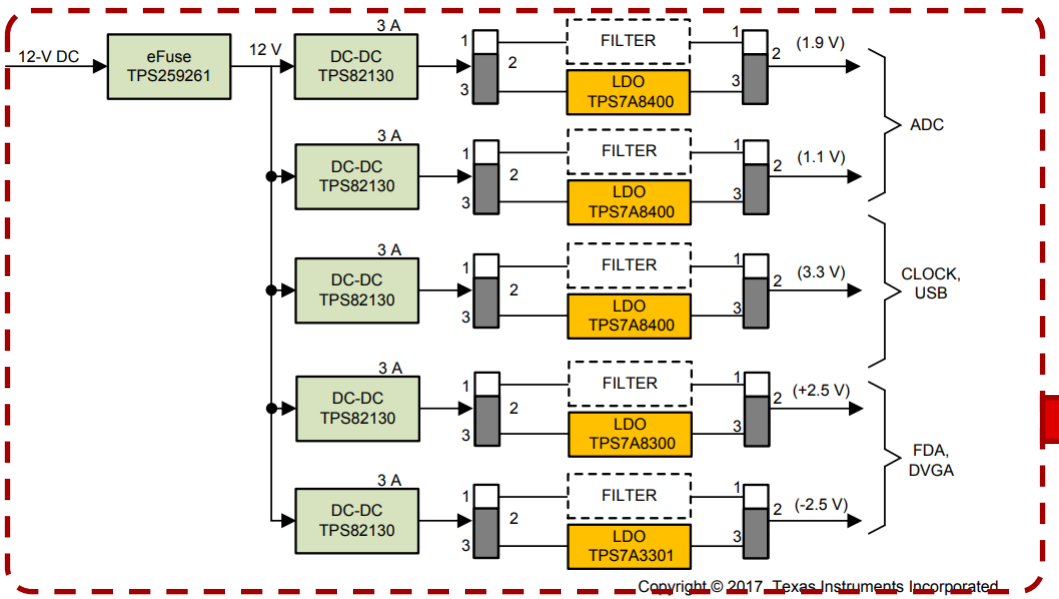


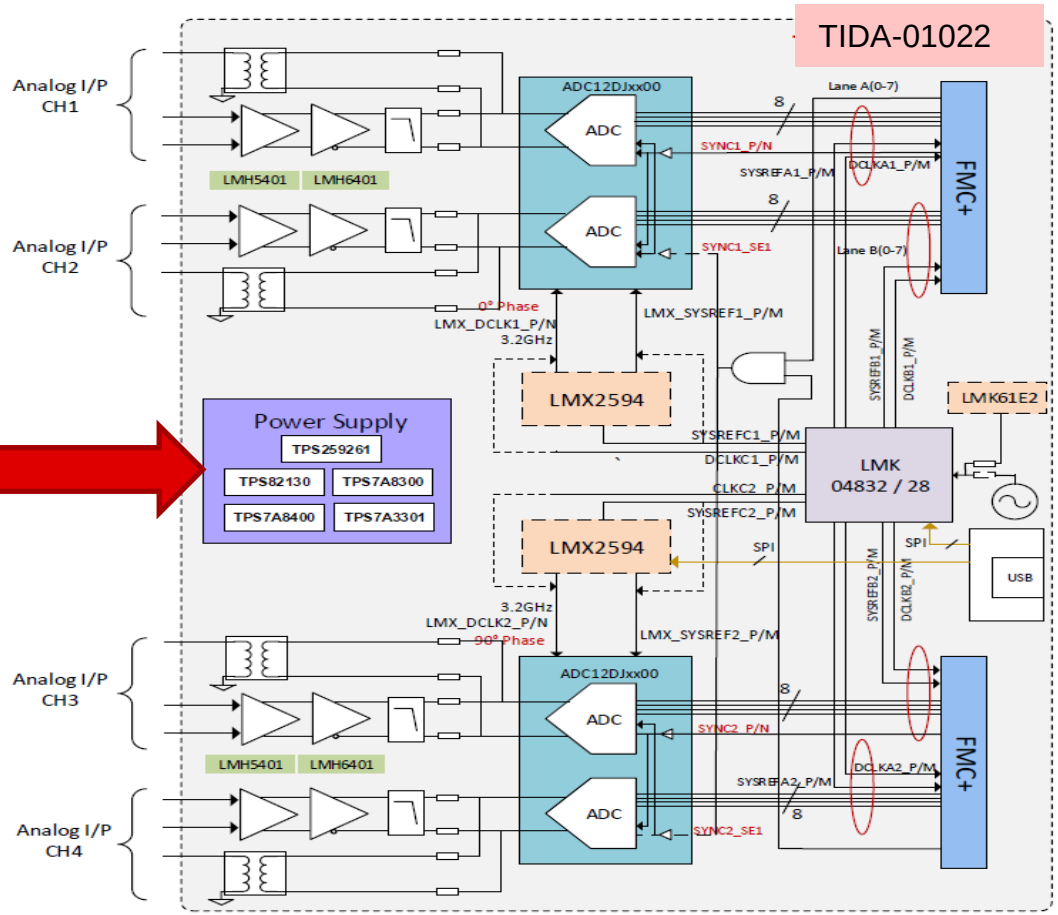
ADC2 lags ADC1 by 0.111 deg or 0.23 ps

Power solution update for ADC12DJ3200

System block diagram on board power

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

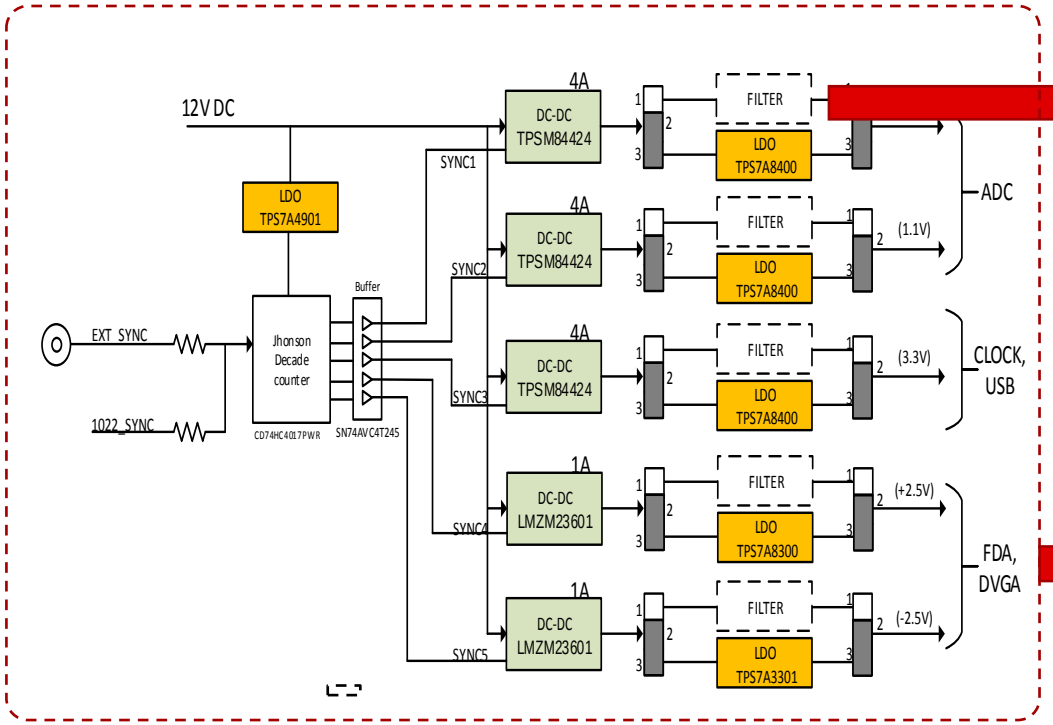


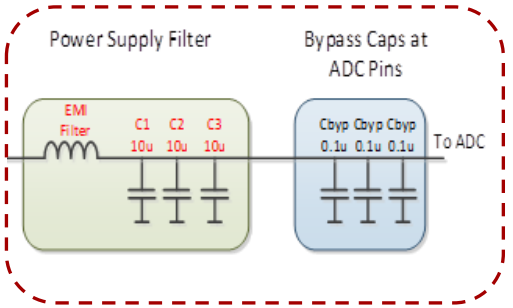


- TPS82130 power module use
- No External Frequency SYNC
- Thermal performance is not good due to very tiny package

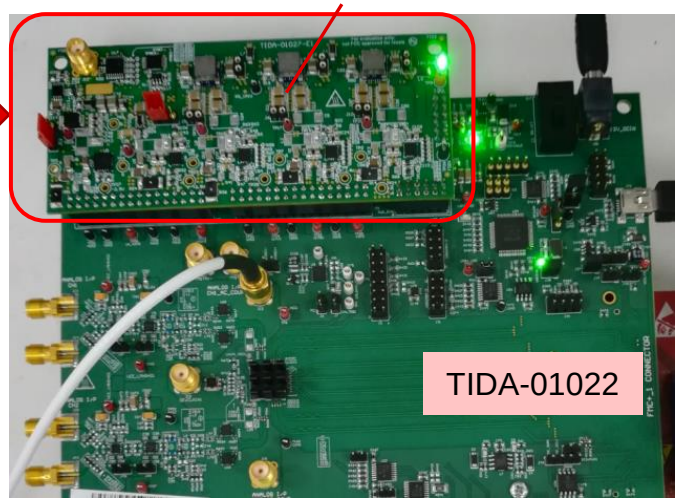
System block diagram with TIDA-01027

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems





TIDA-01027



- TPSM84424 power module used
- External Frequency SYNC with phase shifted clock
- Thermal performance is good
- Hot rod package helps to improve EMI performance

Test results – with TIDA-01027

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

Calculated

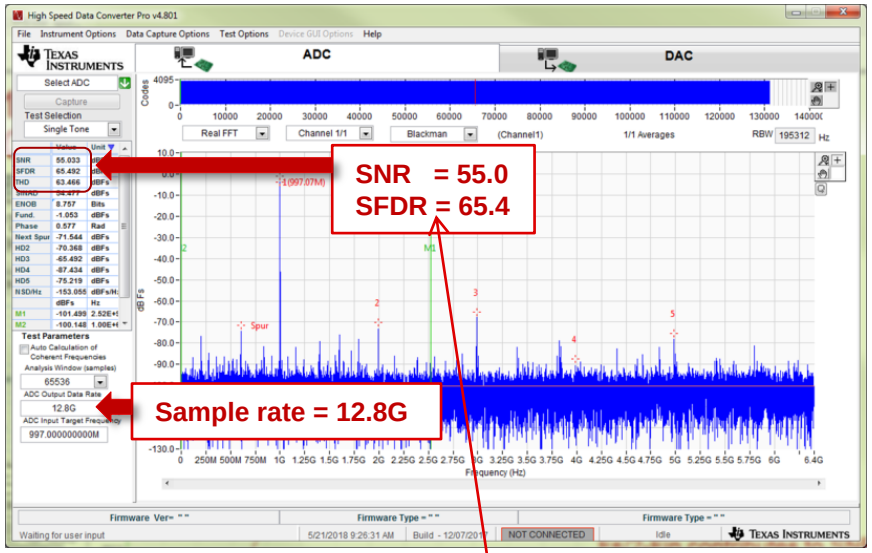
Supply Rail (V)	Calculated	
	Current (A)	Power (W)
1.9	1.9	3.61
1.1	2.7	2.97
3.3	1.874	6.18
2.5	0.56	1.40
-2.5	0.56	1.40
	Total Output Power	**15.56**

Measured

Supply Rail(V)	Current (I)	Power(W)
1.9	2.17	4.12
1.1	2.89	3.18
3.3	1.94	6.4
2.5	0.519	1.30
-2.5	0.506	1.27
Total Output Power		**16.27**

Input Supply: 12V @ 1.65A	
Input Power	19.8 W
Efficiency	82.15 %

Spectrum Performance



ADC performance SNR, SFDR close to datasheet specification

Test Condition

- TIDA-01027 operation mode
  - LDO bypassed , DCDC + Filter Only at output
  - DCDC running free mode(No frequency SYNC across convertors)
- TIDA-01022 operation mode
  - JMODE0, Fs =12.8 Gsps, Fin = 997MHz

Note: We are getting ≈70% efficiency in TIDA-01022 with on board power supply

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- Implementing demanding high current applications using Point of Load devices
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- Get an overview of radiation testing, procedures and requirements needed for radiation qualification
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Thank you!