Designing a Front-End Circuit for Driving a Differential Input ADC

TI Precision Labs – Op Amps

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Topics to review before continuing

- Fully Differential Amplifiers
 - <u>TI Precision Labs Op Amps: Fully Differential Amplifiers Introduction to FDAs and Differential Signaling</u>
- Noise
 - <u>TI Precision Labs Op Amps: Noise 1</u>
 - <u>TI Precision Labs Op Amps: Fully Differential Amplifiers Noise Analysis, Advanced Compensation</u> <u>Techniques, and Variable Gain FDAs</u>
- Stability
 - TI Precision Labs Op Amps: Stability 1
 - <u>TI Precision Labs Op Amps: Fully Differential Amplifiers FDA stability and Simulating Phase Margin</u>
- Total Harmonic Distortion
 - Application Note: Maximizing Signal Chain Distortion Performance Using High Speed Amplifiers
- Settling Time
 - TI Precision Labs ADCs: Building a SAR ADC Model
 - TI Precision Labs ADCs: Refine the Rfilt and Cfilt Values



Converting a single-ended signal to differential





ADC Driver Requirements

Input Signal

- Single ended signal
- + 2 V_{pp} amplitude
- 500 kHz frequency

ADS8910B Specifications

- Differential Input
- ADC input voltage: -V_{REF} to V_{REF}
- 1 MSPS
- \cdot THD f_{in} = 100 kHz is -110 dB
- 18 bit resolution

• Least Significant Bit (LSB) =
$$\frac{\text{Full Scale Range}}{2^{N}} = \frac{2*5V}{2^{18}} = 38.14 \text{ uV}$$

ADC driver requirements

- The differential range is -5V to 5 and the range of each input is 0 to 5gain of 4.6 to allow for dynamic range and for some room
- Amplifier supply voltage of 5.2V
- Bandwidth > 500 kHz
- Better or equal distortion performance to maintain signal fidelity
- · Good noise performance to maintain signal fidelity
- Minimize the power consumption

	PARAMETER	TEST CONDITIONS	MIN T	YP MAX	UNIT
ANALOG	INPUT				
FSR	Full-scale input range (AINP – AINM)		-V _{REF}	V _{REF}	v
VIN	Absolute input voltage (AINP and AINM to REFM)		0	V _{REF}	v



Specifications	Units	OPA625	Comment	THS4551
Number of Channels	#	2		1
Total Supply Voltage min	V	2.7		2.7
Total Supply Voltage max	V	5.5	Ability to maximize dynamic range of the ADC (5V)	5.4
GBW typical MHz 120		120	Sufficient Bandwidth	135
Voltage Noise typical	nV/√Hz	2.5	Low noise to maintain signal fidelity	3.3
THD typical	dBc	-110	Low distortion to maintain signal fidelity	-138
Iq per channel (mA)	mA	2	Low power consumption	1.35

Discrete Solution



Fully Differential Amplifier Solution



Discrete Solution Resistor Values

Amplifier 1 - Gain Resistors

 $V_{in} = 2V_{pp}$

 $V_{out} = 4.6 V_{pp}$

$$G = V_{out}/V_{in} = 2.3$$
$$G_{inverting} = -\frac{R_F}{R_G} = -2.3 \frac{V}{V}$$

RF1 = 246 RF2 = 107 – Analog engineers calculator

Amplifier 1 - V_{SHIFT} Resistors $G_{\text{non inverting}} = 1 + \frac{R_F}{R_G} = 3.3 \frac{V}{V}$ $V_{\text{OCM}} = 2.5 V$ $V_0 = \frac{V_{\text{OCM}}}{G} = \frac{2.5V}{3.3} = 0.7575V$





 $i_1 = i_2$

Discrete Solution Resistor Values

Amplifier 2 - Gain Resistors

$$G_{inverting} = -\frac{R_{F2}}{R_{G2}} = -1 \frac{V}{V}$$

 $R_{F2} \ _ \ RG_2 \ _ \ _{470} \Omega$

Amplifier 2 - V_{OCM} Resistors

 $G_{non inverting} = \frac{1}{R_{F2}} + \frac{R_{F2}}{R_{G2}} = 2$

In a voltage divider, when the resistors are the same value the input voltage will be divided in half.

 $R_3 = R_4 = 470 \,\Omega$





FDA Solution Resistor Values

Output Common Mode Voltage



FDAs have a $V_{\text{OCM}}\,\text{pin}$

Voltage a the V_{OCM} pin sees a G = 1 No resistors are required

To maximize the dynamic range of the input of our ADC:

$$R_F = 493$$

$$R_G = 107$$

$$G = -\frac{RF}{RG} = -\frac{493}{107} = -4.6$$



Both Solutions Resistor Values Charge Bucket Filter



Link for free download of Analog Engineer's Calculator

Math Behind the R-C Component Selection

Refine the Rfilt and Cfilt Values



Noise Theory



TI Precision Labs – Operational Amplifier Noise



1/f Noise is Negligible



If $BW_N > 10^* f_{FLICKER}$ then 1/f noise will be
then 1/f noise will be
then 1/f noise will rIf $BW_N < 10^* f_{FLICKER}$ then 1/f noise will r

$$BWN = k * \frac{1}{2\pi RFIL_{TCFILT}} = 1.57 * \frac{1}{2\pi * 16.25\Omega * 690pF} = 22 MHz$$



Noise Calculations

Discrete Stage 1



	Key Specifications
	GBW = 120 MHz
	R_{F1} = 246 Ω
	$R_{G1} = 150 \Omega$
	$K = 1.38 x 10^{-23} (J/K)$
	k = 1.57
	$T = 25^{\circ}C = 293 K$
— 0	$v_{n(OPA625)} = 2.5 \ nV / \sqrt{Hz}$
	$i_{n(OPA625)} = 2.8 \ pA/\sqrt{Hz}$
	$R_{FILT}/2 = 16.25 \Omega$
	$C_{FILT} = 690 \ pF$
	Key Calculations
	$G_N = (1 + RF_1/RG_1) = 3.3 V/V$
	$Req_{RF} = RF_1 RG_1 = 74.5\Omega$
	$Req_{12} = R1 R2 = 162\Omega$
	$fc = \frac{1}{2\pi PEU} = 14.1 MHz$

Voltage Spectral Noise $e_{vn} = vn = 2.5 \ nV/\sqrt{Hz}$ Current Spectral Noise $e_{in1} = in * ReqR_F = 0.209 \ nV/\sqrt{Hz}$ $e_{in2} = in * Req_{12} = 0.454 \ nV/\sqrt{Hz}$ Resistor Spectral Noise $e_{nagere} = \sqrt{4KTR_{agere}} = 1.1 \ nV\sqrt{Hz}$

$$e_{Req12} = \sqrt{4KTR_{eqRF}} = 1.62 \ nV/\sqrt{Hz}$$

Stage 1 Spectral Noise

$$e_1 = 2 * GN \sqrt{e_{vn}^2 + e_{in1}^2 + e_{in2}^2 + e_{ReqRF}^2 + e_{ReqRF}^2}$$
$$= 21 \text{ nV} / \sqrt{Hz}$$



Noise Calculations

Discrete Stage 2 and V_{RMS}



Key Specifications GBW = 120 MHz R_{F2} _ 246 Ω R_{G2} _ 107 Ω $K = 1.38 \times 10^{-23} (I/K)$ k = 1.57 $T = 25^{\circ}C = 293 K$ $v_{n(0PA625)} = 2.5 \, nV/\sqrt{Hz}$ $i_{n(OPA625)} = 2.8 \, pA/\sqrt{Hz}$ $R_{FILT}/2 = 16.25 \,\Omega$ $C_{FILT} = 690 \ pF$ **Key Calculations** $G_N = (1 + RF/RG) = 2 V/V$

$$Req_{RF} = RF_2 || RG_2 = 235\Omega$$
$$fc = \frac{1}{2\pi RFIL_{TCFILT}} = 14.1 MHz$$

Voltage Spectral Noise $e_{vn} = vn = 2.5 \ uV/\sqrt{Hz}$ Current Spectral Noise $e_{in1} = in * ReqR_F = 0.658 \ nV/\sqrt{Hz}$ $e_{in2} = in * Req_{34} = 0.658 \ nV/\sqrt{Hz}$ Resistor Spectral Noise

 $e_{ReqRF} = \sqrt{4KTReq_{RF}} = 1.95 \ nV\sqrt{Hz}$ $e_{Req34} = \sqrt{4KTReq_{34}} = 1.95 \ nV/\sqrt{Hz}$

Stage 2 Spectral Noise

$$e_{2} = G_{N}\sqrt{e_{vn}^{2} + e_{in1}^{2} + e_{in2}^{2} + e_{ReqRF}^{2} + e_{Req34}^{2}}$$

= 7.67 nV/\sqrt{Hz}

Total RMS Noise

$$e_{TOTAL} = \sqrt{e_1^2 + e_2^2} = 22.5 \text{ nV}/\sqrt{Hz}$$
$$E_{TOTAL} = e_{TOTAL}\sqrt{k * fc} = 106 \text{ }\mu\text{V}_{\text{RMS}}$$

Noise Simulation Discrete Solution





Noise Simulation Discrete Solution with Capacitor





Noise Calculations

Fully Differential Amplifier



	Key Specifications
	$R_F = 493 \ \Omega$
	$R_G = 107 \Omega$
	$K = 1.38 x 10^{-23} (J/K)$
	k = 1.365
	$T=25^{\circ}C=293~K$
	$v_{n(THS4551)} = 3.3 \ nV / \sqrt{Hz}$
г	$i_{n(THS4551)} = 0.5 \ pA/\sqrt{Hz}$
	$R_{FILT}/2 = 16.25 \Omega$
	$C_{FILT} = 690 pF$
	Key Calculations

Key Calculations $G_N = (1 + RF/RG) = 5.6 V/V$ $Req_{RF} = RF ||RG = 87.9\Omega$ $fc = \frac{1}{2\pi RFILTCFILT} = 14 MHz$ $BW_N = \sqrt{k * fc} = 4.4 kHz$

Voltage Spectral Noise $e_{vn} = vn = 3.3 \ nV/\sqrt{Hz}$ Current Spectral Noise $e_{in1} = in * ReqRF = 0.04 \ nV/\sqrt{Hz}$ $e_{in2} = in * Req_{12} = 0.04 \ nV/\sqrt{Hz}$ Resistor Spectral Noise

 $e_{ReqRF} = \sqrt{4KTR_{eqRF}} = 1.19 \ nV\sqrt{Hz}$

$e_{ReqRF} = \sqrt{4KTR_{eqRF}} = 1.19 \ nV/\sqrt{Hz}$

Total Stage 1 Spectral Noise

 $e_{TOTAL} = G_N \sqrt{e_{\nu n}^2 + e_{in1}^2 + e_{in2}^2 + 2eReqR_F^2}$ = 20.7 nV/ \sqrt{Hz} **Total FDA Solution RMS Noise** $E_{TOTAL} = eTOTA_I \sqrt{fc * k} = 92 \, uVrms$

Noise Simulation Fully Differential Amplifier Solution





Noise Results

Solution	Discrete	Discrete with Cap	Fully Differential
Calculation	106 μV _{RMS}	89 μV _{RMS}	92 μV _{RMS}
Simulation	104 μV _{RMS}	87 μV _{RMS}	91 µV _{RMS}



Stability Theory

Stability rule of thumb If phase margin > 45° then amplifier is considered **optimally stable** If phase margin < 45° then the amplifier is considered **marginally stable**



Ana	alysis T&M Tools TI Utiliti	es Help				
	ERC					
	Mode Select Control Object	Ctrl+Alt+M	Γ			
	Set Analysis Parameters	Ctrl+Alt+P				
	DC Analysis					
	AC Analysis			Calculate nodal voltages		
	Transient	Ctrl+Alt+T		Table of AC results		
	Steady State Solver			AC Transfer Characteristic Ctrl+Alt+A		
	Fourier Analysis	•		·····		
	Noise Analysis	Ctrl+Alt+N				
	Options	Ctrl+Alt+O				

TI Precision Labs – Op Amp: Stability



Stability Simulation Discrete Amplifier 1



Marginally Stable!



Stability Simulation Discrete Amplifier 2



Marginally Stable/Potentially Unstable



Stability Simulation Fully Differential Amplifier



STABLE!



Total Harmonic Distortion Theory FDAs Even Order Harmonic Distortion

$$V_{out_{+}} = k_1 Vin + k_2 Vin^2 + k_3 Vin^3 + k_4 Vin^4 \dots$$
(1)
$$V_{out_{-}} = k_1 (-Vin) + k_2 (-Vin)^2 + k_3 (-Vin)^3 + k_4 (-Vin)^4 \dots$$
(2)

Where $k_1, k_2... k_N$ are constants Taking the differential output:

$$V_{o} = VOUT_{+-}V_{OUT}_{-}$$

= $k_{1}V_{in} - (-k_{1}V_{in}) + k_{2}V_{i_{n}^{2}} - k_{2}(-Vi_{n})^{2} + k_{3}V_{in}^{3} - (-k_{3}V_{in}^{3}) \dots$
= $2k_{1}V_{in} + 2k_{3}V_{in}^{3} + 2k_{5}V_{in}^{5}\dots$ (3) No added even-order harmonics



Calculations Total Harmonic Distortion

6.5 Electrical Characteristics: (V_{S+}) – (V_{S-}) = 5 V THS4551

at $T_A \approx 25^{\circ}$ C, VOCM pin = open, $R_F = 1 \text{ k}\Omega$, $R_L = 1 \text{ k}\Omega$, $V_{OUT} = 2 \text{ V}_{PP}$, 50- Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see Figure 61 for a gain of 1-V/V test circuit

	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP} , G = 1, R_L = 1 kΩ –128		dDa	С
HDZ		f = 100 kHz, V_{OUT} = 8 V_{PP} , G = 1, R _L = 1 k Ω	-124	uвс	С
HD3	Third-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP} , G = 1, R _L = 1 k Ω	–139	dDo	С
		f = 100 kHz, V_{OUT} = 8 V_{PP} , G = 1, R_L = 1 k Ω	–131	uвс	С

6.5 Electrical Characteristics High-Drive Mode OPA625

at $T_A = 25^{\circ}$ C, V+ = 5 V, V- = 0 V, MODE pin connected to V- pin, $V_{COM} = V_O = 2.5$ V, gain (G) = 1, $R_F = 1 \text{ k}\Omega$, $C_F = 2.7 \text{ pF}$, $C_{LOAD} = 20 \text{ pF}$, and $R_{LOAD} = 2 \text{ k}\Omega$ connected to 2.5 V (unless otherwise noted)

HD2	Second-order harmonic Distortion	V _O = 2 V _{PP} , G = 2	f = 10 kHz	144		
			f = 100 kHz	122	dBc	
			f = 1 MHz	80		
HD3	Third-order harmonic Distortion	V _O = 2 V _{PP} , G = 2	f = 10 kHz	155		
			f = 100 kHz	140	dBc	
			f = 1 MHz	80		



Settling Time Theory





Transient Analysis				
<u>S</u> tart display	0	[s]	/	ОК
E <u>n</u> d display	1u	[s]	×	Cancel
 Calculate operating point Use initial conditions Zero initial values 			?	<u>H</u> elp
☑ Draw excitation				

TI Precision Labs - ADCs: Building the SAR ADC Model



Settling Time Simulation Discrete Amplifiers – ½ LSB



Settling time = 141 ns Final Error Voltage = 427 nV



Settling Time Simulation Fully Differential Amplifier – ½ LSB



Settling time = 206 ns Final Error Voltage = 1.147 μV



Fully Differential Amplifier vs Discrete Solutions



Specifications	FDA	Discrete (w/Capacitor)		
Noise	91 µV _{RMS}	87 μV _{RMS}		
Stability	Stable	Marginally Stable		
THD (HD2, HD3)	(-128 dBc, -139 dBc)	(-122 dBc, -140 dBc)		
Settling Time	208 ns	141 ns		
Quiescent Current1.35 mA		4 mA		
Components	9	16		



THANKS FOR YOUR TIME!

